Status of CMX and Topology Processor Modules

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Overview

- L1Calo upgrade includes two brand new modules: CMX and Topological Processor

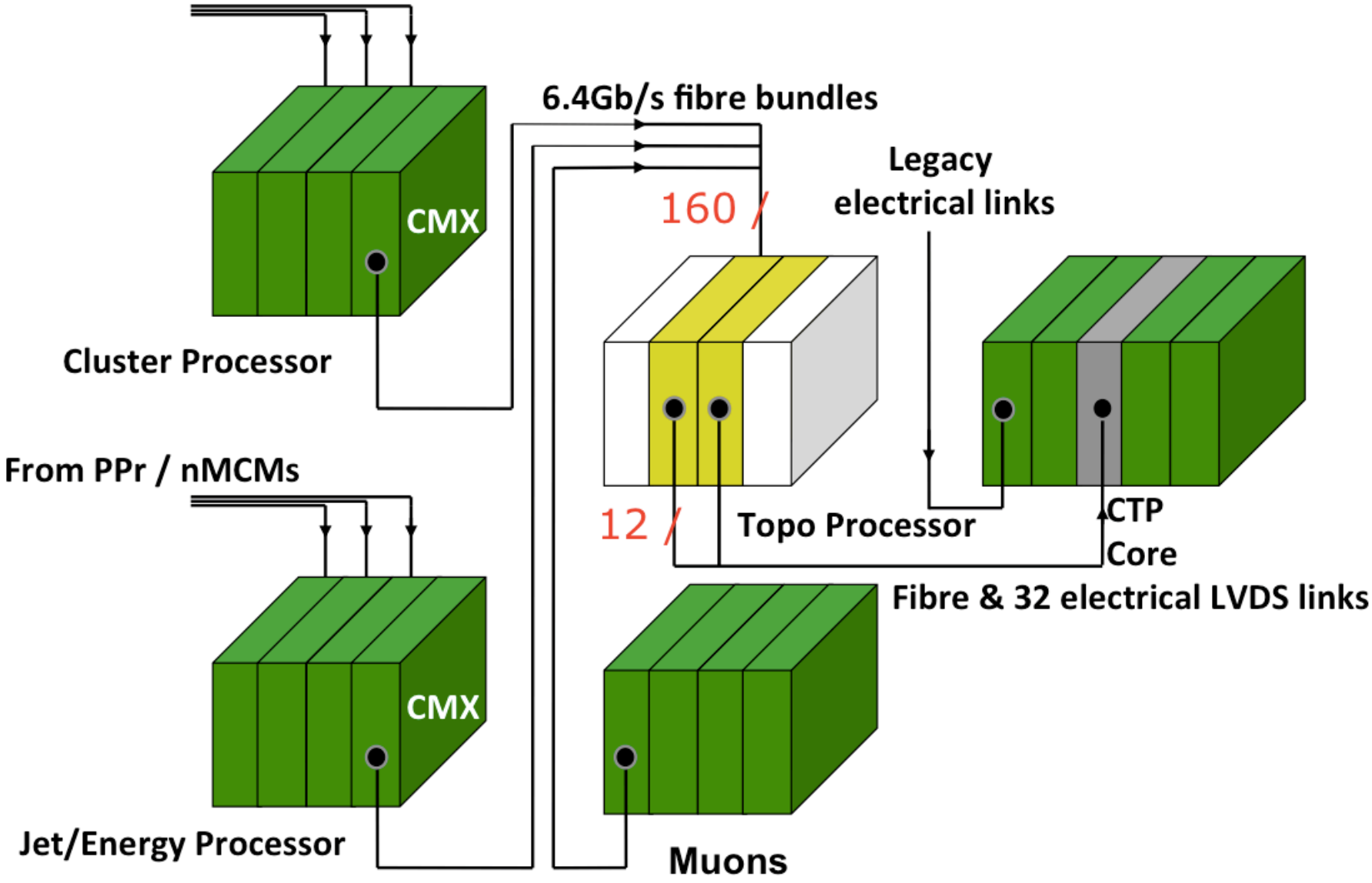
- CMX is upgraded version of the Common Merger Module
  - Will receive data from CPMs and JEMs, format and transmit to Topological Processor

- Topological Processor is completely new
  - Will trigger on event topologies at L1 using e/gamma, jets and muons

- Both modules currently at the ~prototype stage

- Installation at P1 foreseen late 2013 / 2014

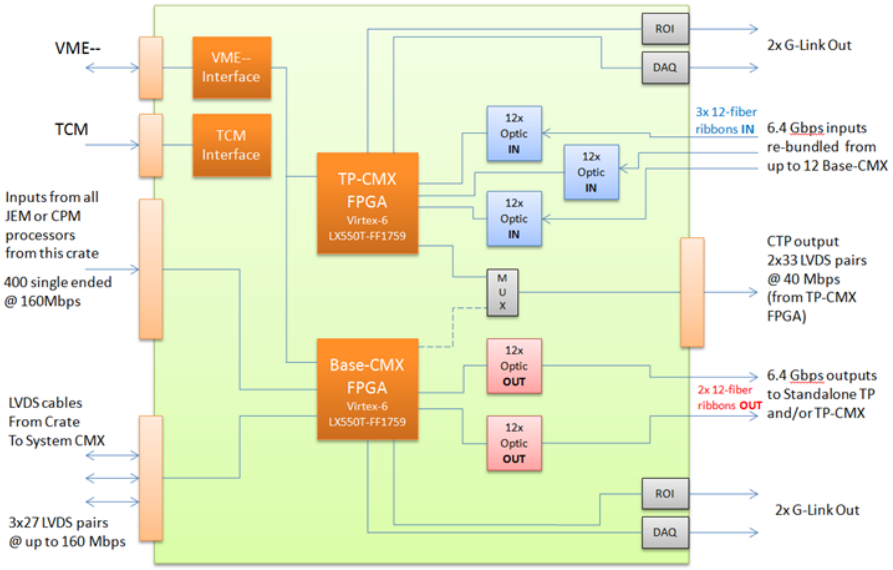
L1 RTDP Overview



CMX Module

- Same crates, slots as current CMM

- Increased data transfer rates
  - From JEMs/CPMs: 40 → 160 Mbps
  - To "system" CMX: 40 → 160 Mbps
  - To CTP: 40 → 80 Mbps



- Newer FPGA (Xilinx Virtex 6) for **increased** functionality (e.g. extra jet thresholds)

- Also **new** functionality
  - (zero-suppressed) cluster info sent to Topo Processor via fiber bundles
  - Optional capability to run as a standalone CMX/TP
    - e.g. if TP is late
    - Separate "TP" FPGA can be optionally installed

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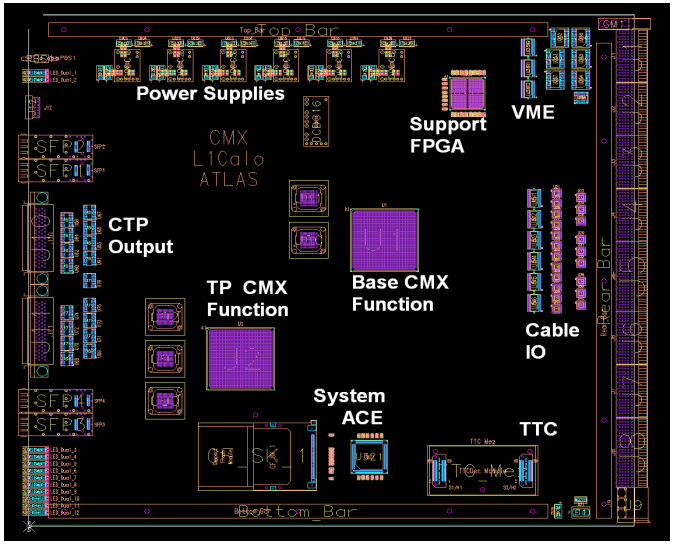
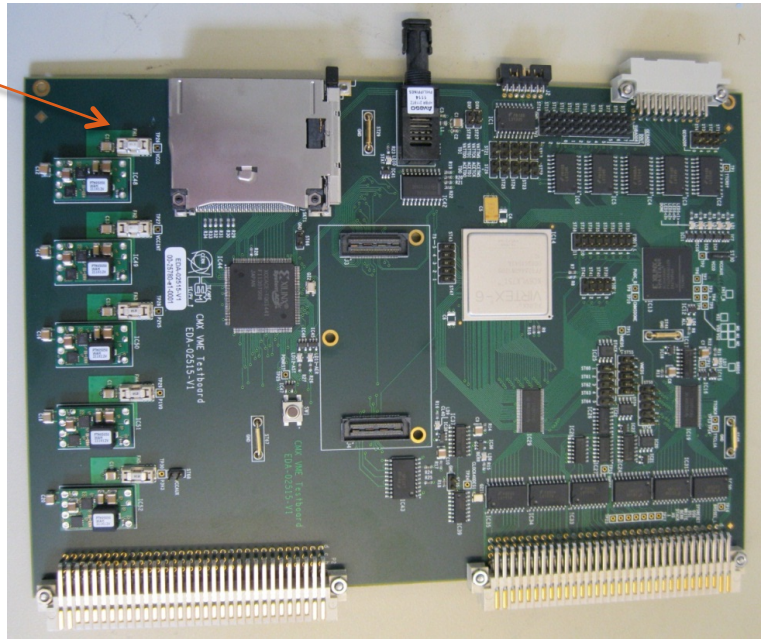
CMX Hardware

- Schematics and PCB layout work ongoing at MSU
  - Backplane inputs, cable I/O, CTP output all understood
  - Maximized signal integrity, critical for 160 Mbps bandwidth
  - Trace layout optimized on 24-layer card
  - Working on details of optical I/O



- VAT (VME/ACE/TTC) test card at CERN
  - Test ancillary functions of CMX
  - Practice VME control, FGPA configuration via SystemACE, TTC signal handling
  - Test bed of CMX operating environment with small FPGA
  - Lessons learned will be applied to production CMX



CMX Firmware

- Firmware efforts have been focused on:
  - Backplane data capture
    - Difficult challenge with 160 Mbps rate, unequal line delays
    - Provide feedback to PCB layout, adjust locations of FPGA input pins to reduce complexity, maintain high signal integrity
  - Power estimation (feedback to hardware design)
    - Sizing power supplies
    - FPGA heat dissipation
    - Estimates made for CMM emulation on Virtex 6 and for data capture

- Current / future work:
  - Defining functionality of and interfaces between the various firmware modules
  - Starting from the current 'jet' version of the CMX firmware

CMX Test Bench

• Have built a stripped-down version of an L1Calo Readout Crate for testing backward compatibility (required!) of CMX prototype when it is ready

Topological Processor

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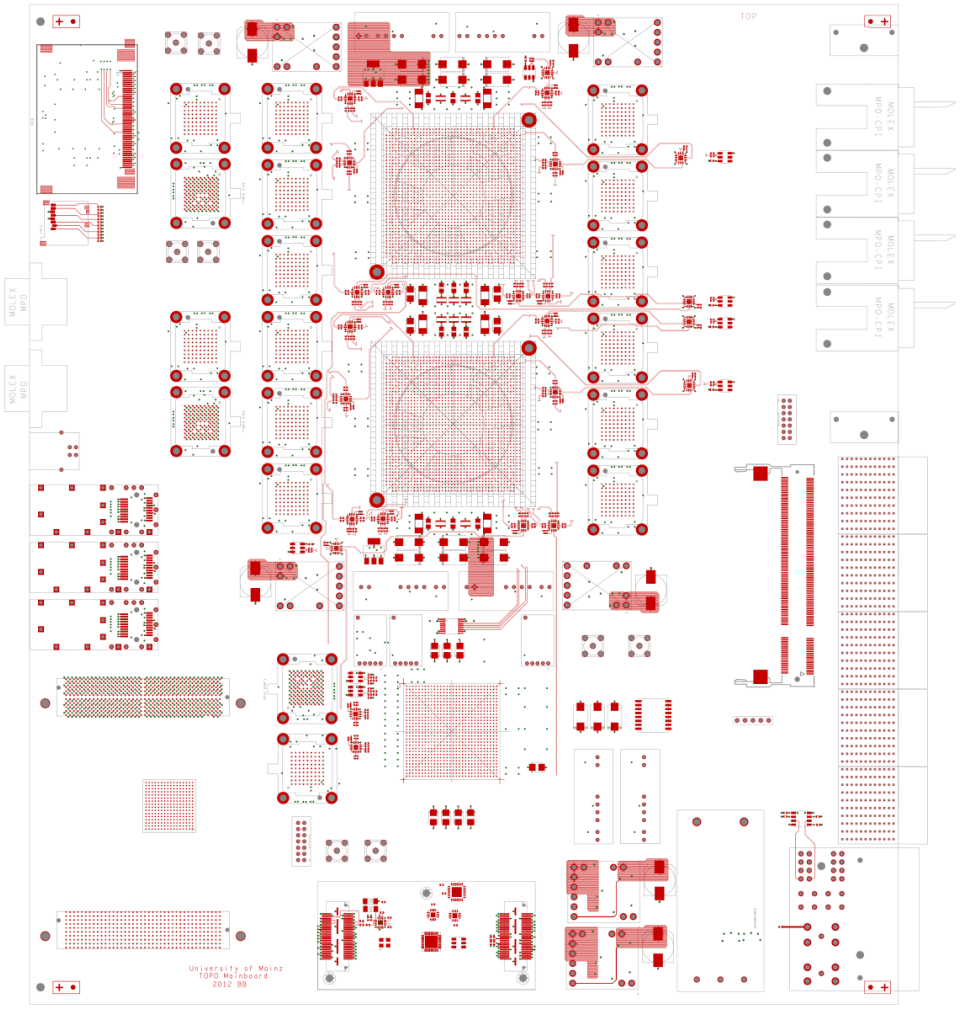
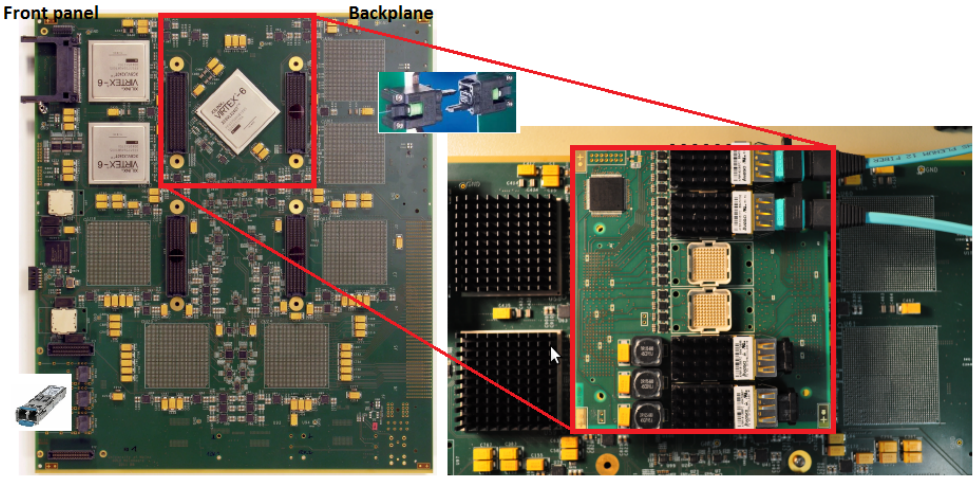
- Goal is maximum flexibility in applying topological trigger criteria
- Two high-end processors (Virtex 7)
- Jets, clusters, muons on single module… can correlate all trigger types within full solid angle
- Option to run separate topology algos on more than one module in parallel
- Fiber bundles from CMX and muons, fiber bundles and LVDS to CTPcore
- Can accept line rates above 6.4 Gb/s from future processors e.g. FEXes

Topological Processor Hardware

- Schematics near final
- Layout done to ~60%
- Module control via Kintex and Zynq processors
- FPGA configuration via SystemACE and module control
- Hardware to support both L1Calo-style ROD interface, and embedded ROD / S-Link interface on opto fibers
- Some circuitry moved to a mezzanine module, to be finalized later



Functional Demonstrator for L1Topo ("GOLD")



- "Generic Opto Link Demonstrator" → test technologies and schemes for TP
- Using mid-range (Virtex 6) FPGAs
- Typical sort/ΔΦ algorithm has already been successfully implemented
- Also used for jitter analysis, signal integrity, eye width, crosstalk, latency measurements
- Will continue to be used as a source / sink for future L1Topo tests…

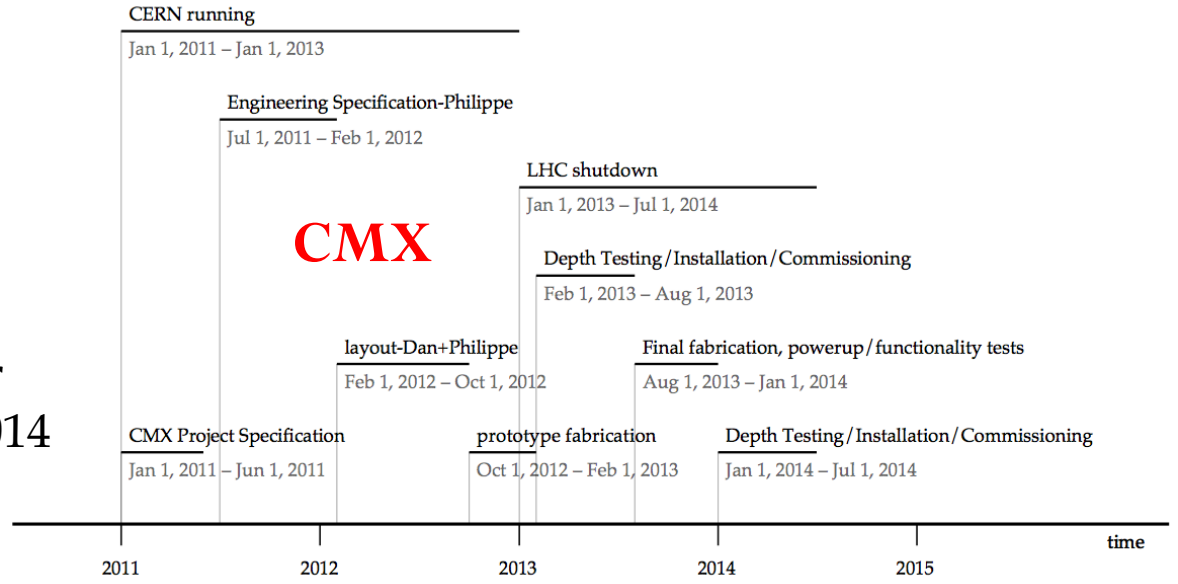
Topological Processor, ongoing work

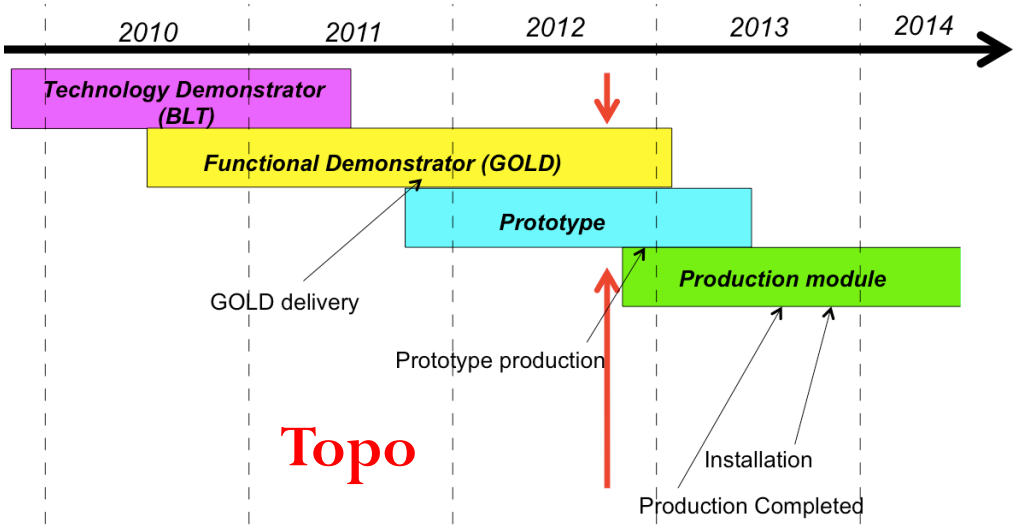
- Development of module control
  - The environment that will eventually be used (Kintex & Zynq) for FPGA configuration and control is somewhat new.
  - Will require significant software development
- Register model (input from software side)
- Firmware will need to be moved to Virtex 7
- Plenty of algorithm firmware still to be updated / developed
- Prototype layout expected to be finished end November

Timeline(s)

- Taken from L1Calo Joint Meeting, 12/10/12

- Coordinated schedules for installation in late 2013 / 2014





Summary

• Prototype modules nearly ready for both CMX and L1Topo.

• In the meantime, both teams are learning valuable lessons from their test cards: VAT (for CMX) and GOLD (for L1Topo).

• Firmware (and software!) efforts proceeding in tandem with and providing feedback to hardware development.

• Test bench ready for backward-compatibility testing of CMX prototype.

• On schedule for production modules in second half of 2013, installation/ commissioning in late 2013 / 2014.