

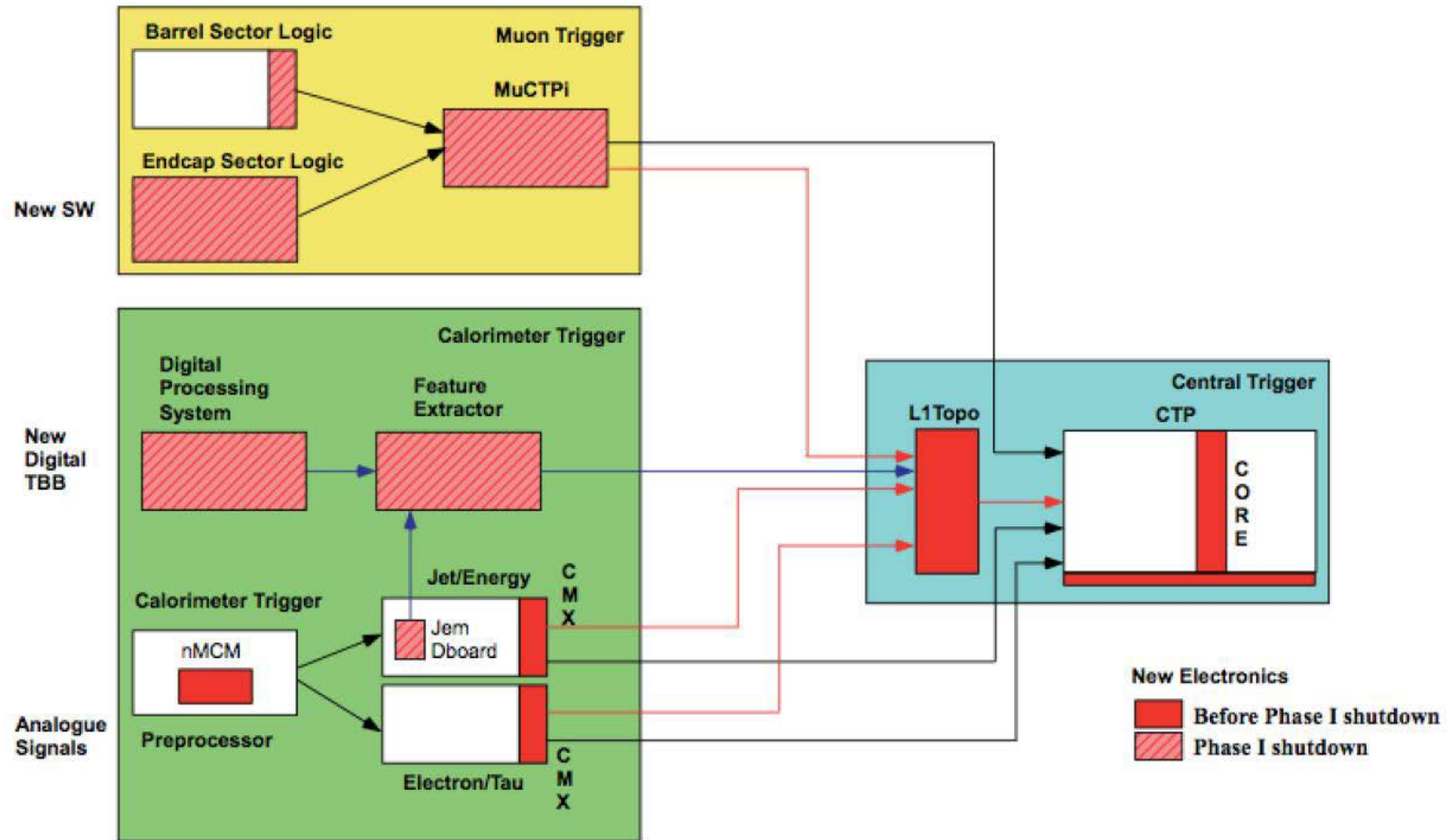
CMX Status and News

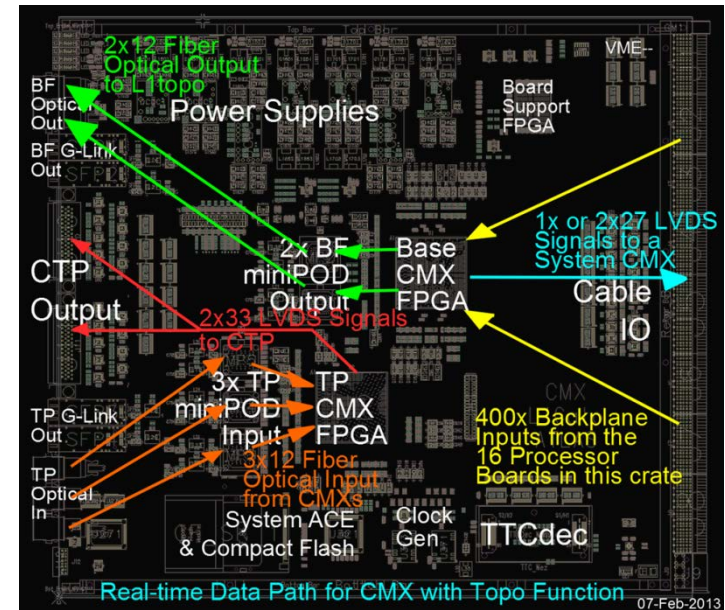
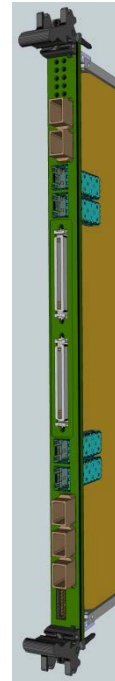
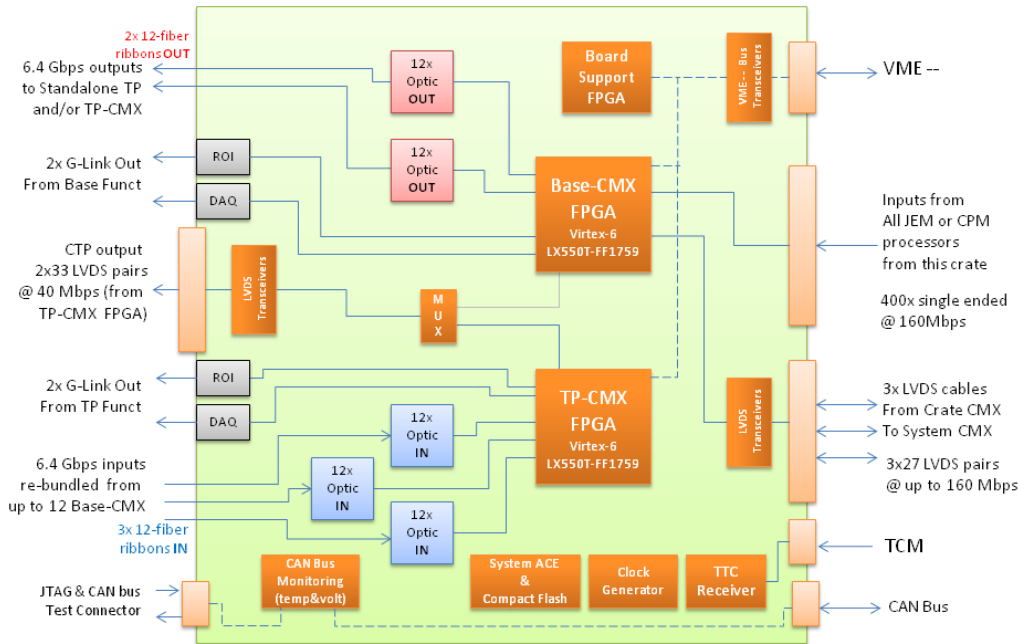
- post PRR -

R. Brock, S. Caughron, D. Edmunds, Y. Ermoline, W. Fedorko, P. Laurens, J. Linnemann,
Pawel Plucinski, Samuel Silverstein

TDAQ Week, CERN
8-12 April 2013,

CMX scope (Phase 0 item)





■ The CMX must:

- Be able to perform all tasks currently handled by any CMM.
- Be able to perform these CMM tasks at higher input and output line rates.
- Provide more computing power to support additional algorithms.
- Provide new functionality to send a raw or processed copy of its inputs out optically.
- Provide optional functionality to perform Topological Processing on CMX data.

- Compatibility with existing L1Calo crate Infrastructure
 - Avago MiniPOD component height
 - ⇒ MiniPOD clearance verified at CERN
 - No front-panel access to the CompactFlash card
 - ⇒ Moving Compact Flash module to the front panel
- Board Functionality
 - Required output from the TTCDec to the BF FPGA
 - ⇒ L1_Accept, BC_Reset, 40.08 MHz clock from an LHC locked crystal PLL.
 - CANbus monitoring should also include currents
 - ⇒ Adding an analog multiplexer to one microprocessor analog input
 - All single-ended signal lines on the backplane have 60 ohms impedance
 - ⇒ 400 backplane processor input traces are now 60 Ohm
 - Front-panel outputs for the deskew1 and deskew2 clocks
 - ⇒ Two pins in the bottom connector on the CMX front panel can be used to supply a copy of clock signal(s) OR to send out S-Link Busy signals

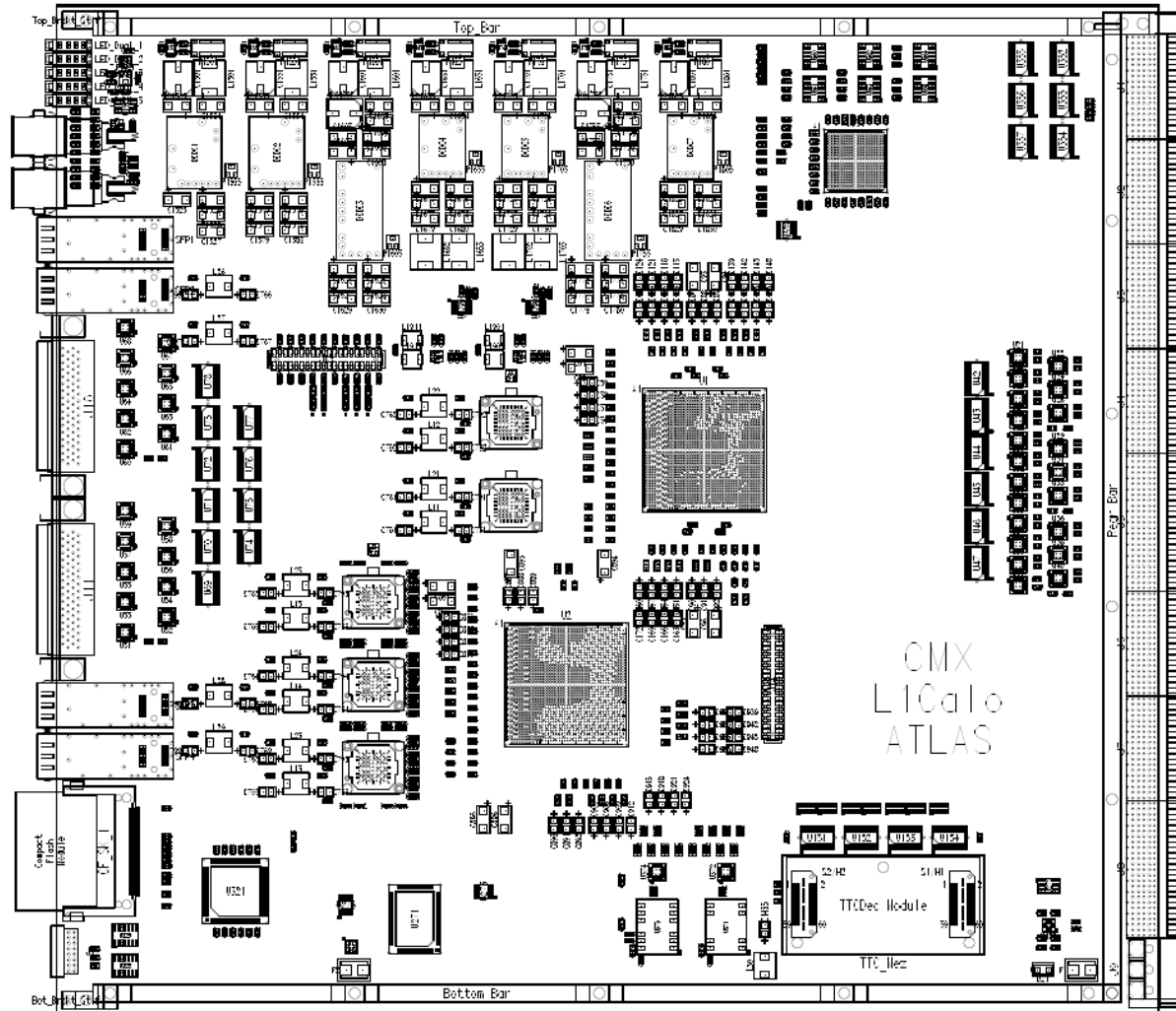
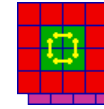
■ Interfaces with connected systems

- **No 40.000 MHz crystal clock for G-Link readout to L1Calo RODs**
 - ⇒ Adding 40.000 MHz crystal oscillator to the CMX design
- **CMX to act as its own ROD, providing readout to DAQ and the ROIB using S-link protocol.**
 - ⇒ Adding hardware support to make possible S-Link readout from the TP FPGA
- **Replacement of 12-fiber MTP feedthrough with 48-fiber**
 - ⇒ Reducing number of front-panel optical feed-throughs from 5 to 2 (Note: Most CMX cards use only the Base Function and thus can still use 1x or 2x simpler 12-fiber ribbons)
- **Recommended to use 3.3V devices that are 5V tolerant**
 - ⇒ CMX design was already using 5V tolerant 3.3V CMOS components for VME-- bus

MiniPOD clearance



CMX → new layout



- Draft report from the review (15.03.13)
- Note in reply to the draft report sent to review committee (03.04.13)
 - All review actions addressed → go-ahead for production?
- Efforts in parallel on 5 fronts:
 - MSU – CMX design
 - ⇒ Raymond Brock, Dan Edmunds, Philippe Laurens
 - CERN – VAT card testing
 - ⇒ Yuri Ermoline
 - CMX software
 - ⇒ Seth Caughron
 - UBC – BF FPGA firmware: IO
 - ⇒ Wojtek Fedorko
 - Stockholm – BF FPGA firmware: zero-suppression, thresholding
 - ⇒ Pawel Plucinski, Samuel Silverstein



- 2013: Prototype fabrication and testing at MSU
 - Mar: Prototype Readiness Review
 - Apr-Jun: Prototype fabrication
 - Jun: Test rig checked out at MSU
 - Jun-Aug: CMM firmware ported on CMX
 - Sep-Dec: Basic tests for backward compatibility at MSU
- 2014: Full prototype testing at CERN / final fabrication
 - Jan-May: Full prototype tests in test rig at CERN
 - Jan-Sep: CMX firmware development and test
 - May-Sep: Fabricate and assemble full set of CMX modules
 - Sep-Dec: Test in the USA15 L1Calo system during shutdown
- 2015: Final commissioning in the L1Calo trigger system in USA15
 - Jan-Mar: Final commissioning