CMX Status and Schedule

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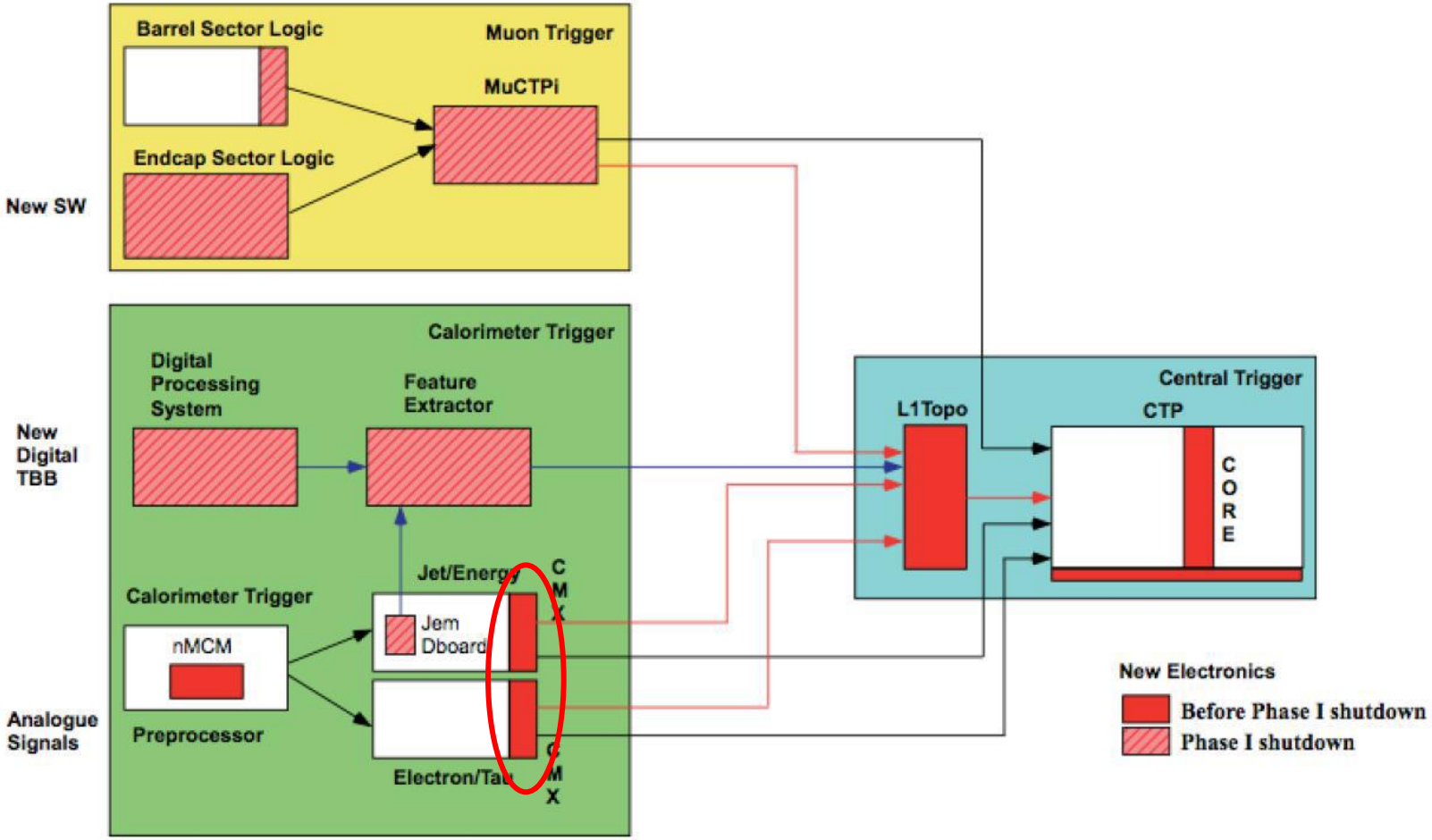
Level-1 Calorimeter Trigger Joint Meeting

CERN, 8 July 2013

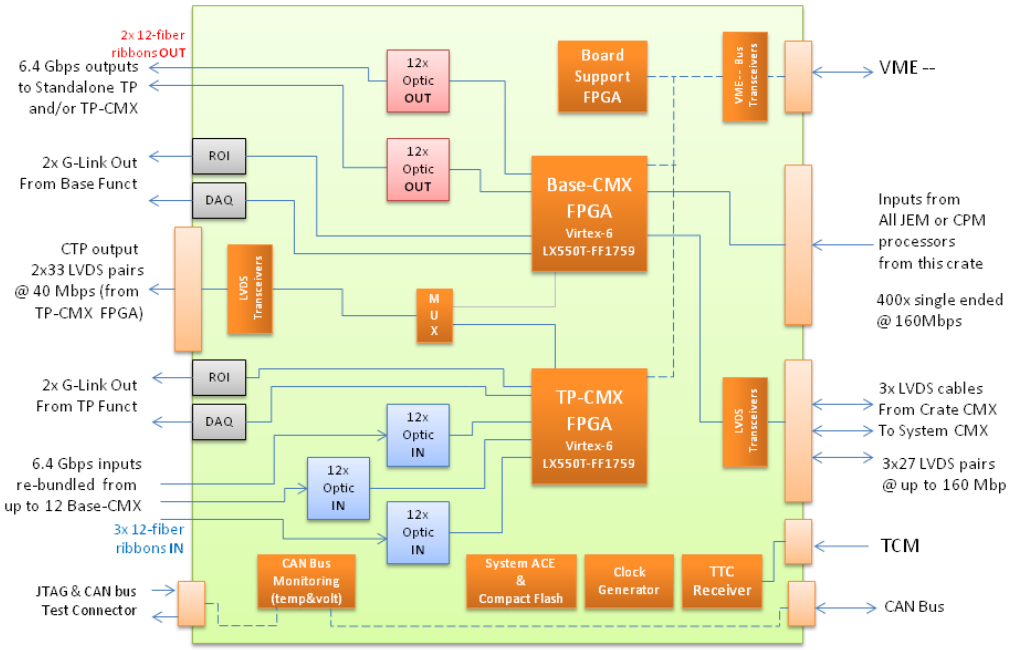
Summary

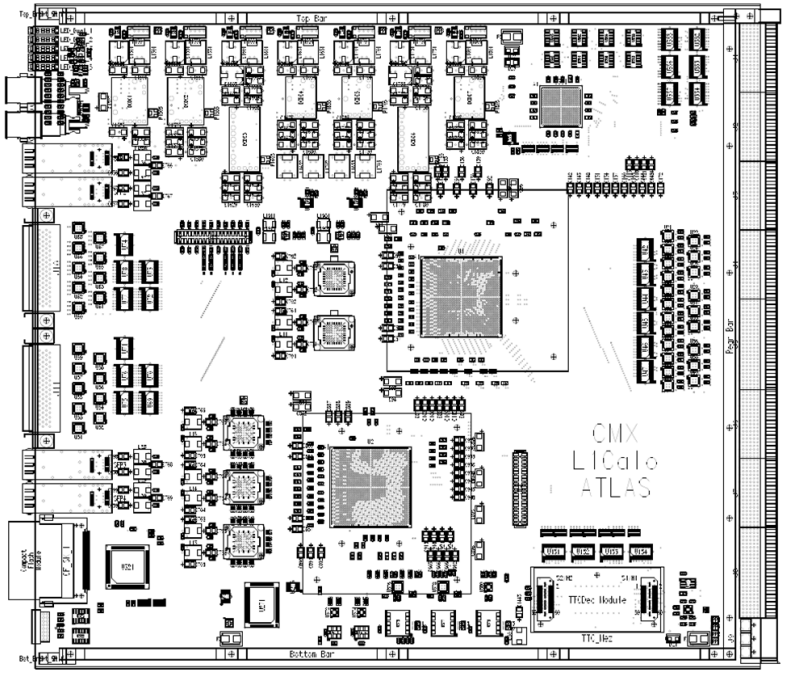
- CMX scope and functionalities
  - Phase-I accelerated item, a.k.a. Phase-0
- CMX Prototype RR (07.03.13) outcome
  - responded to review report, all actions addressed, production go-ahead
- CMX development schedule v2.3
  - Last version from 15.05.2013
- Efforts
  - @MSU – CMX PCB design
    - ⇨ Raymond Brock, Dan Edmunds, Philippe Laurens
  - @CERN – VAT card testing and MSU test rig software
    - ⇨ Yuri Ermoline, Duc Bao Ta
  - @UBC and @Stockholm – CMX FW
    - ⇨ Wojtek Fedorko, Pawel Plucinski, Samuel Silverstein
- Next steps

CMX scope


Barrel Sector Logic
Muon Trigger
MuCTPi
Endcap Sector Logic
New SW
Calorimeter Trigger
Digital Processing System
Feature Extractor
New Digital TBB
Central Trigger
L1Topo
CTP
CORE
Jet/Energy
CMX
Calorimeter Trigger
Jem Dboard
nMCM
Preprocessor
Analogue Signals
Electron/Tau
CMX
New Electronics
Before Phase I shutdown
Phase I shutdown

CMX functionalities





- The CMX functionalities:
  - Be able to perform all tasks currently handled by any CMM.
  - Be able to perform these CMM tasks at higher input and output line rates.
  - Provide more computing power to support additional thresholds.
  - Provide new functionality to send a raw or processed copy of its inputs out optically.

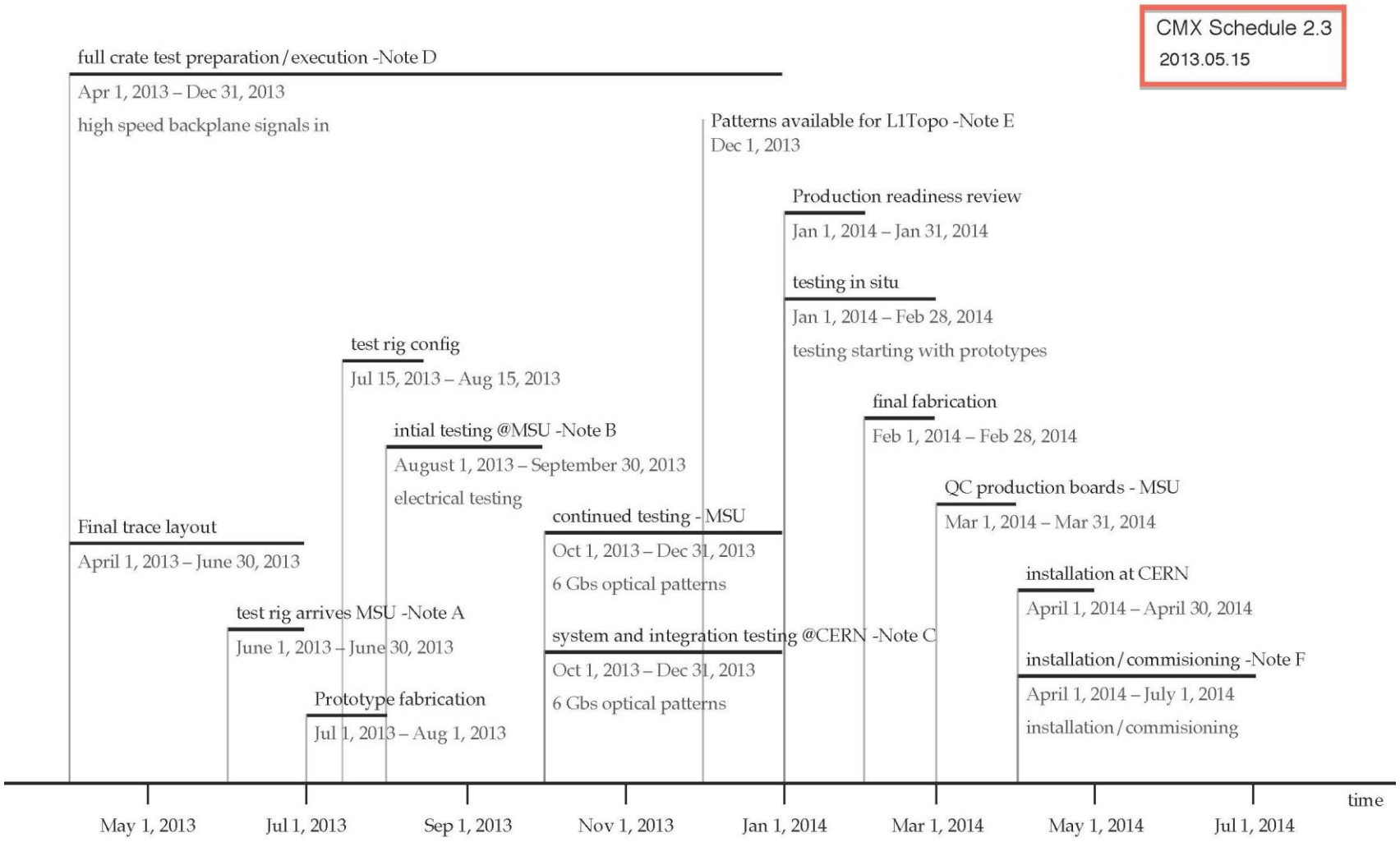
CMX Prototype RR (07.03.13) outcome

- Compatibility with existing L1Calo crate Infrastructure
  - Avago MiniPOD component height clearance verified
  - Front-panel access to the CompactFlash card
- Board Functionality
  - TTCDec outputs required by the BF FPGA were specified by the panel
  - CANbus monitoring includes currents
  - All single-ended processor input signals on CMX use 60 ohms traces
  - Optional Front-panel access to a TTCdec clock
- Interfaces with connected systems
  - Adding 40.000 MHz crystal clock for G-Link readout to L1Calo RODs
  - CMX will provide all necessary hardware support for S-link so that the optional TP could act as its own ROD for DAQ and ROI readout. Note that extensive new FW would be required.
  - CMX now only has 2x MTP feedthroughs instead of 5x
    - ⇨ Nearly always: 2x MPT feedthroughs sufficient for 2x 12-fiber ribbons from the BF function
    - ⇨ Exception: 1x 24-fiber output from the BF function and 1x 36-fiber input to the TP function

CMX development schedule v2.3

- 2013: Prototype fabrication and testing at MSU
  - Apr-Jun: Final trace layout
  - Jul: Prototype fabrication
  - Aug-Sep: Initial testing @MSU
  - Oct-Dec: Testing at MSU and system and integration testing @CERN
  - Dec: Patterns available for L1Topo
- 2014: Full prototype testing at CERN / final fabrication
  - Jan: Full-crate test at 160 MHz operation
  - Jan: Production Readiness Review (PRR)
  - Feb: Final fabrication
  - Mar: QC production boards @MSU
  - Apr-Jun: Installation and commissioning @CERN
  - Sep-Dec: Test in the USA15 L1Calo system during shutdown

CMX development timeline



CMX development timeline notes

- Highest priority critical project paths
  - release of boards at CERN available to provide patterns for L1Topo
  - a full-rack test of backplane signals at 160 MHz before a Production RR
  - Following receipt of prototypes, testing will commence at MSU and then once electrical and power layout is confirmed, testing will then continue in both MSU and CERN test rigs.
- Notes:
  - A. The shipping of test rig components to MSU can happen at any time
  - B. Initial testing @MSU: power, clocks, configuration, VME access, slow speed I/O through front and back LVDS and the 400 backplane inputs
  - C. The system and integration testing will focus on 6 Gbps optical transmission. This is both a hardware and a firmware test and should be focused initially on satisfying the needs of the L1Topo designers.
  - D. Full-crate test at 160 MHz operation is mandatory prior to a PRR
  - F. Final commissioning and in particular, the replacement of CMM cards with CMX and L1Topo cards requires a lot of coordination and planning.

Efforts @MSU – CMX PCB design (1)

- CMX PCB design
  - Trace layout has been underway for the whole CMX board and CMX prototype layout is almost coplete.
  - Following receipt of prototypes, testing will commence at MSU and then once electrical and power layout is confirmed, testing will then continue in both MSU and CERN test rigs
    - ⇨ The goal of the local MSU testing is to see that power supplies and clocks function as expected and that all 3 FPGAs can be configured and that VME read/write to registers works. Finally, once these milestones are accomplished, slow speed I/O through front and back LVDS and the 400 backplane inputs will be confirmed. At that point, boards will be released to CERN for parallel system and integration testing.
- Other news from MSU (next page):
  - Snapshot of the CAD screen (traces)
  - Snapshot of the top side view

Efforts @MSU – CMX PCB design (2)

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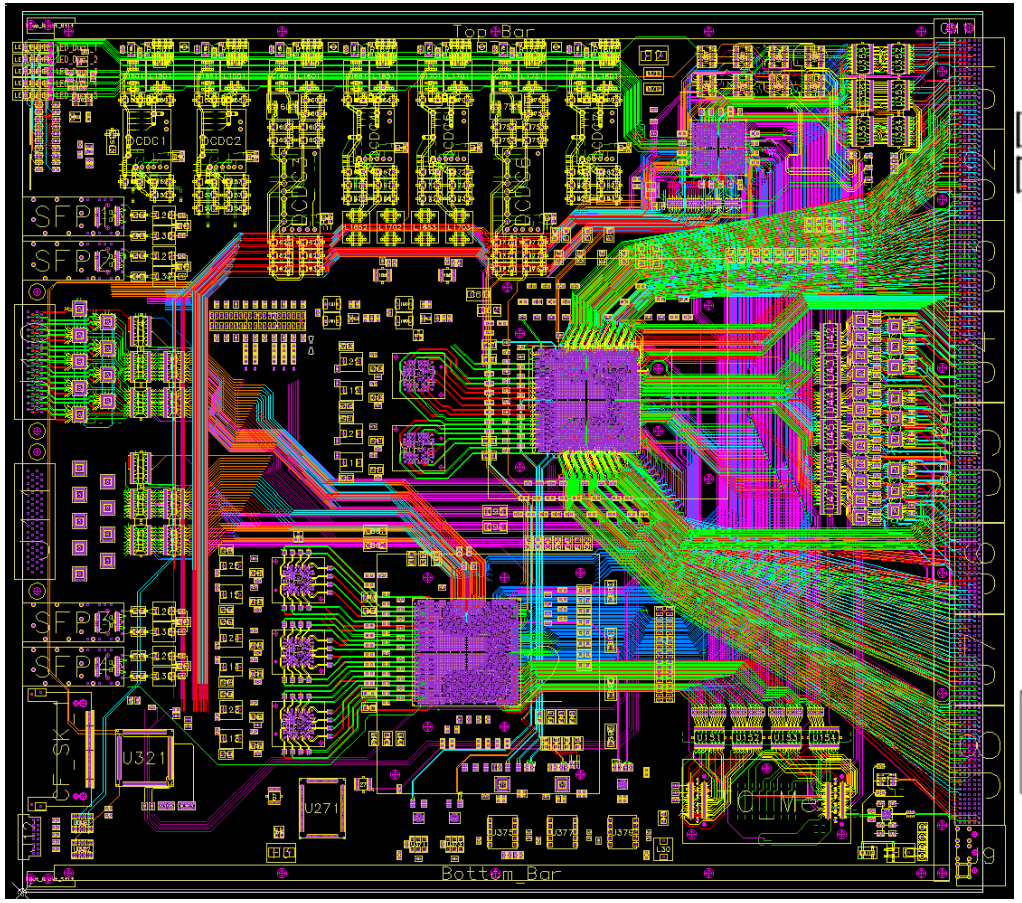
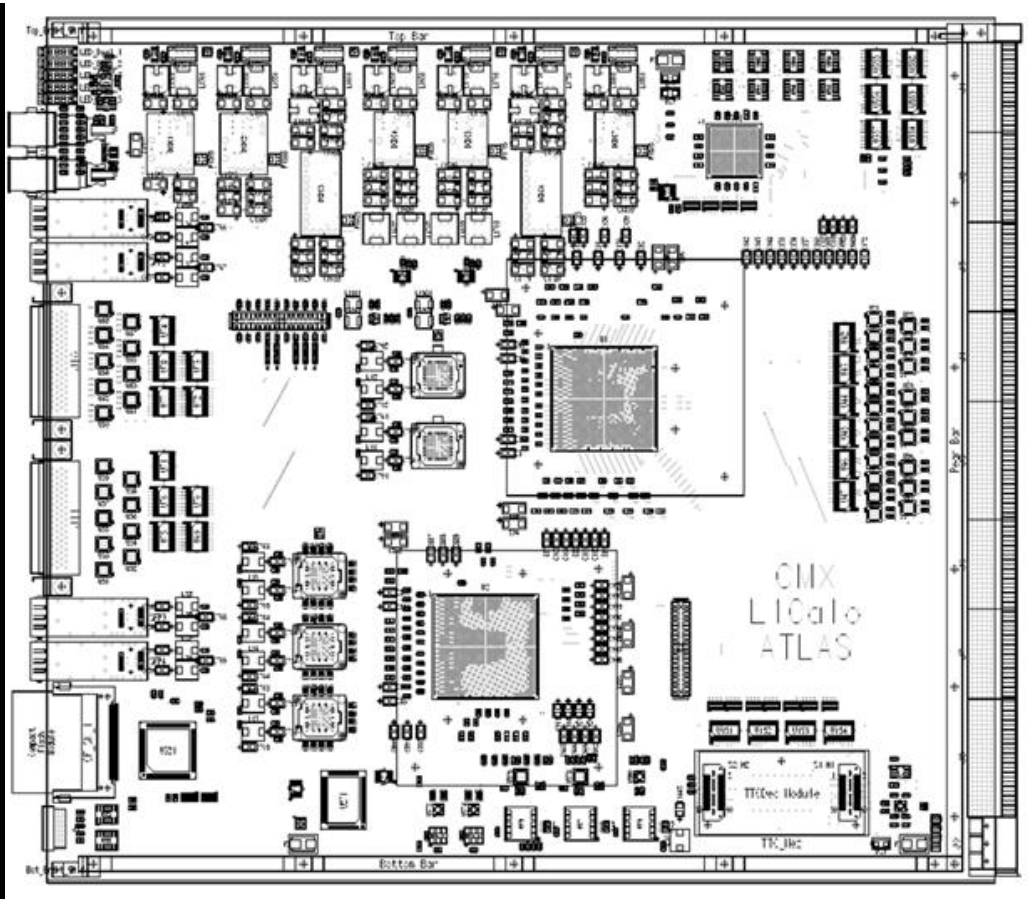
Snapshot of the CAD screen (traces)



Snapshot of the top side view



Efforts @MSU – CMX PCB design: DCS issue

- DCS CANbus interface to CMX
  - Based on obsolete Fujitsu MB90F594 microcontroller
    - ⇨ Proprietary micro-controller that was basically sold only to the automotive industry, was no "second source“, was never a commodity part
    - ⇨ Parts available from resellers for 20-50 times higher price, are often old, have not been stored properly, failed an incoming inspection at the OEM…
  - Deployment of a new Fujitsu microcontroller
    - ⇨ Absence of a backward compatible devices for F2MC-16LX family
    - ⇨ New-generation family of 16-bit processors 16FX exists with CAN interfaces
    - ⇨ 16FX CPU uses all 16LX machine instructions
    - ⇨ Need both HW and microcontroller FW modifications
  - Backup option that may be considered
    - ⇨ Factorize DCS functionalities on CMX (analog IO, digital IO, CANbus IO)
    - ⇨ Route DCS functionalities on CMX with current microcontroller and all IO’s via connectors for a (possible) daughter card
  - Issue currently being investigated

Efforts @CERN – VAT card and test rig software

- Vat card testing
  - VME/ACE/TTC (VAT) test card for CMX
    - ⇨ Parallel effort and study platform
    - ⇨ Lessons and details are merged into CMX
  - Redesign of CMM with new components
    - ⇨ Re-use of Ian and Uli VHDL code
    - ⇨ Ancillary functions fit in single Support FPGA
    - ⇨ FPGA configuration using JTAG connector and
    - ⇨ configuration from CF card via System ACE
    - ⇨ VME access to FPGA registers
    - ⇨ VAT card operated from TTC clock
    - ⇨ Access to TTCrx chip (TTCDec) via VME/I2C
    - ⇨ Access to System ACE from VME
- MSU test rig – HW and SW
  - CPM replaced by JEM as a data source
  - Duc take over Seth on test rig SW activities

Efforts @CERN – MSU test rig software (1)

- CMM software model cloned to CMX (Seth thanks to Murrough)
- MSU test rig is up at CERN
- VME read/writes from registers
- Basic tests of loading data and reading data into/from playback memories tried with CPM:
  - Available CPM has FW incompatible with L1Calo SW
  - Will be replaced by JEM
- Duc Bao Ta take over Seth on MSU test rig SW
  - Supplied with documentation left over by Seth
  - Will continue interaction with Murrough
  - First study on the L1Calo test rig in Bld.104

Efforts @CERN – MSU test rig software (2)

- Online SW tasks for CMX (Murrough talk on 06.06.2013)

Online Software Tasks (4)

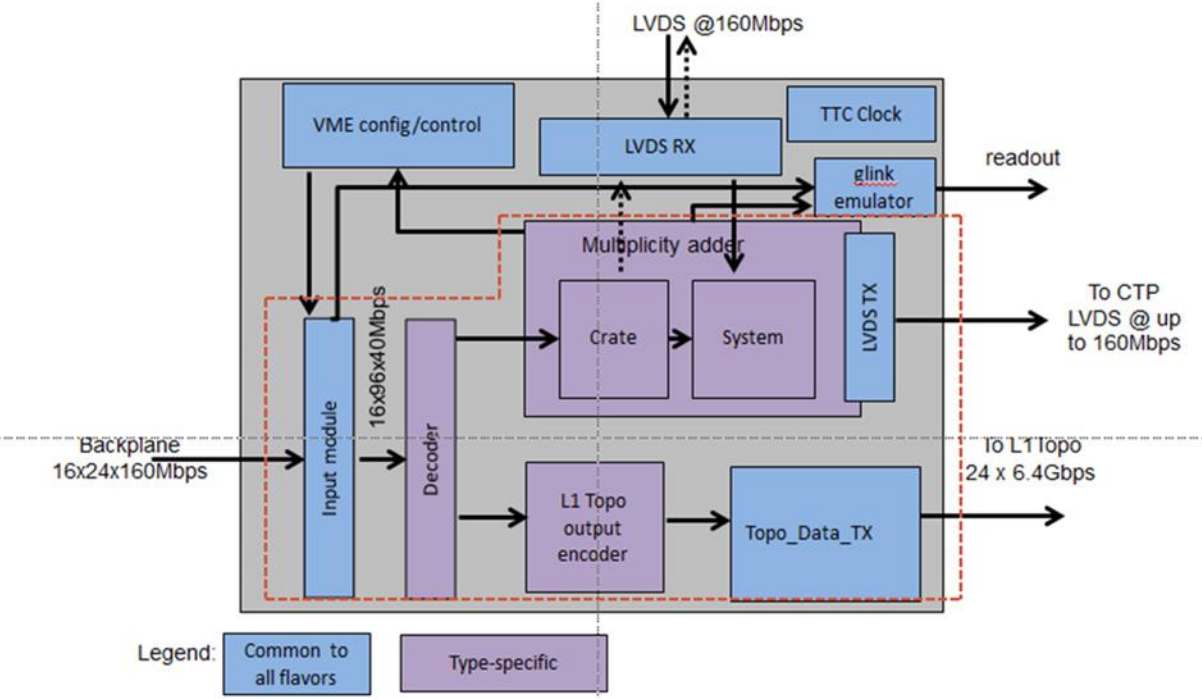
- CMX: Module Services
  - Update HDMC register map
    - New EM/Tau/Jet thresholds handled by CMX [DONE]
    - Doubling of energy thresholds?
    - Larger playback/spy memories for higher speeds [DONE]
    - Configuration of optics
    - Configuration of system ACE (change from present scheme?)
  - Changes for different FPGA setup (base/topo)
    - Reset, loading, version handling?
  - Updates for different setup of the module
    - Usually needs to be developed along with hardware tests
  - Anything for the Topo FPGA...

Online Software Tasks (5)

- CMX: Simulation
  - Change interpretation of backplane signals to new format
  - Use extended trigger menu API
  - Implement thresholding of EM/Tau/Jet objects
    - Port or adapt code from CPM/JEM simulation?
  - Adapt current multiplicity counting
  - Expand playback/spy memories to new sizes
  - Update test vectors to match new functionality
    - Add new test vector patterns as required
  - Implement outputs to L1Topo
- CMX: Calibration & Tests
  - Develop calibration program for backplane/cable delays
  - Any other standalone test programs?

Efforts @UBC and @Stockholm – CMX FW (1)

Firmware development status: Base Function FPGA



- Approach: Develop the common modules for the TOPO and CTP RT path and Jet CMX (system) specific components first
  - W. Fedorko (UBC) : physical interfaces, formatting/CRC, infrastructure
  - P. Plucinski (Stockholm): Decoder (0-suppression), adder (using Ian's CMM as a starting point), readout

8 July 2013 W. Fedorko, P. Plucinski CMX firmware 1

Efforts @UBC and @Stockholm – CMX FW (2)

Firmware development status

- Both real time paths (TOPO and CTP) are implemented
  - Jet (system) version of the type-specific modules
  - Timing closure has been achieved
  - Topo data transmission format and protocol (including 12-bit CRC) implemented according to: *circulated proposal*
    - Tests using ML605 ongoing
  - Some code cleanup needed
- Work in the immediate future
  - Incorporate VME control (already developed by Yuri for VAT) (July)
  - Include glink readout (glink firmware previously tested by Pawel) (August)
  - Incorporate 'spy' memories and control into the RT modules (July)
- Test plans:
  - Re-use firmware components for initial prototype tests at MSU
    - (backplane data capture, MGT IO, LVDS IO, g-link)
  - Detailed list of tests and firmware support being made for initial tests
  - Jet type firmware will be available for tests in CERN rig in September

Efforts @UBC and @Stockholm – CMX FW (3)

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CMX firmware summary

- Resource usage:
  - Occupied Slices: 5.7k (6%)
  - Slice LUTs: 11.5k (3%)
  - Slice Registers: 11.4k (1%)
  - RAMB18E1s: 58 (4%)
  - BUFGs: 5/32
  - BUFRs: 16/72
  - MMCMs: 3/18
- Current preliminary latency estimate:
  - Topo path: ~4 BC
    - Counted from appearance of event's first word on backplane (~1BC)
    - Includes serialization budget (½ time CMX parallel GTX interface → Topo parallel GTX interface (no fiber delay included))
  - CTP: ~7 BC
    - Counted from appearance of event's first word on backplane (~1BC)
    - Preliminary multiplicity adder latency estimate is 6BC

Next steps

- @MSU :
  - CMX prototype PCB layout and production
  - DCS issue investigation
- @CERN :
  - L1Calo DCS study
  - CMX test procedure description
  - VME interfaces for CMX FPGAs and VME registers map
  - MSU test rig SW for (test data generation JEM-CMX)
- @UBC and @Stockholm :
  - More work to be done…