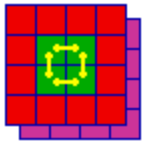

CMX Hardware Status

Chip Brock, Dan Edmunds, Philippe Laurens@MSU
Yuri Ermoline, Duc Bao Ta @CERN
Wojciech Fedorko @ UBC

Michigan State University
25-Oct-2013

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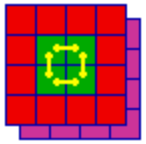
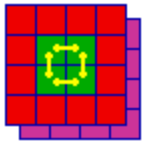


Outline

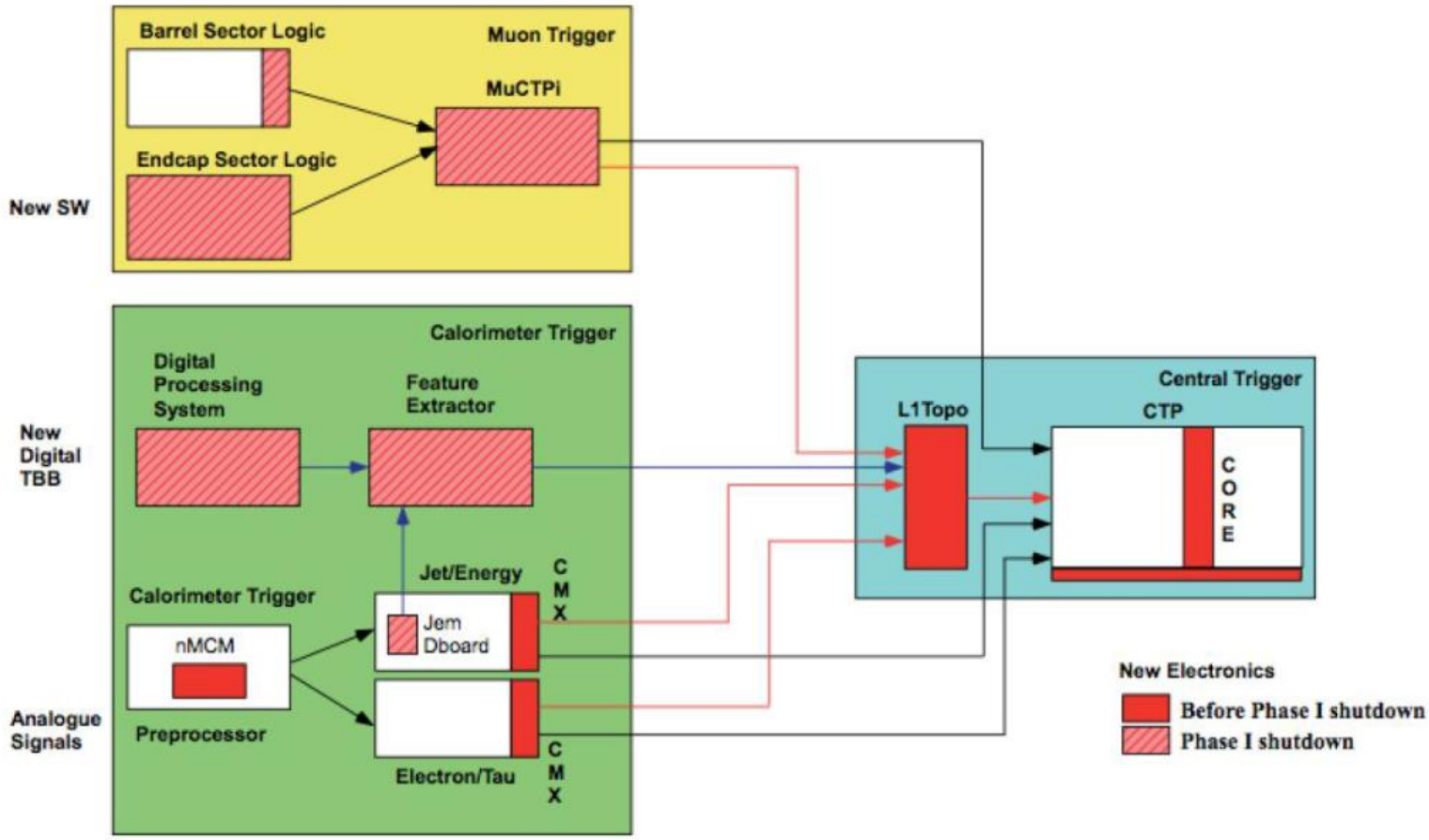
- Review of CMX hardware project
- (Some) CMX hardware design features
- Current hardware status



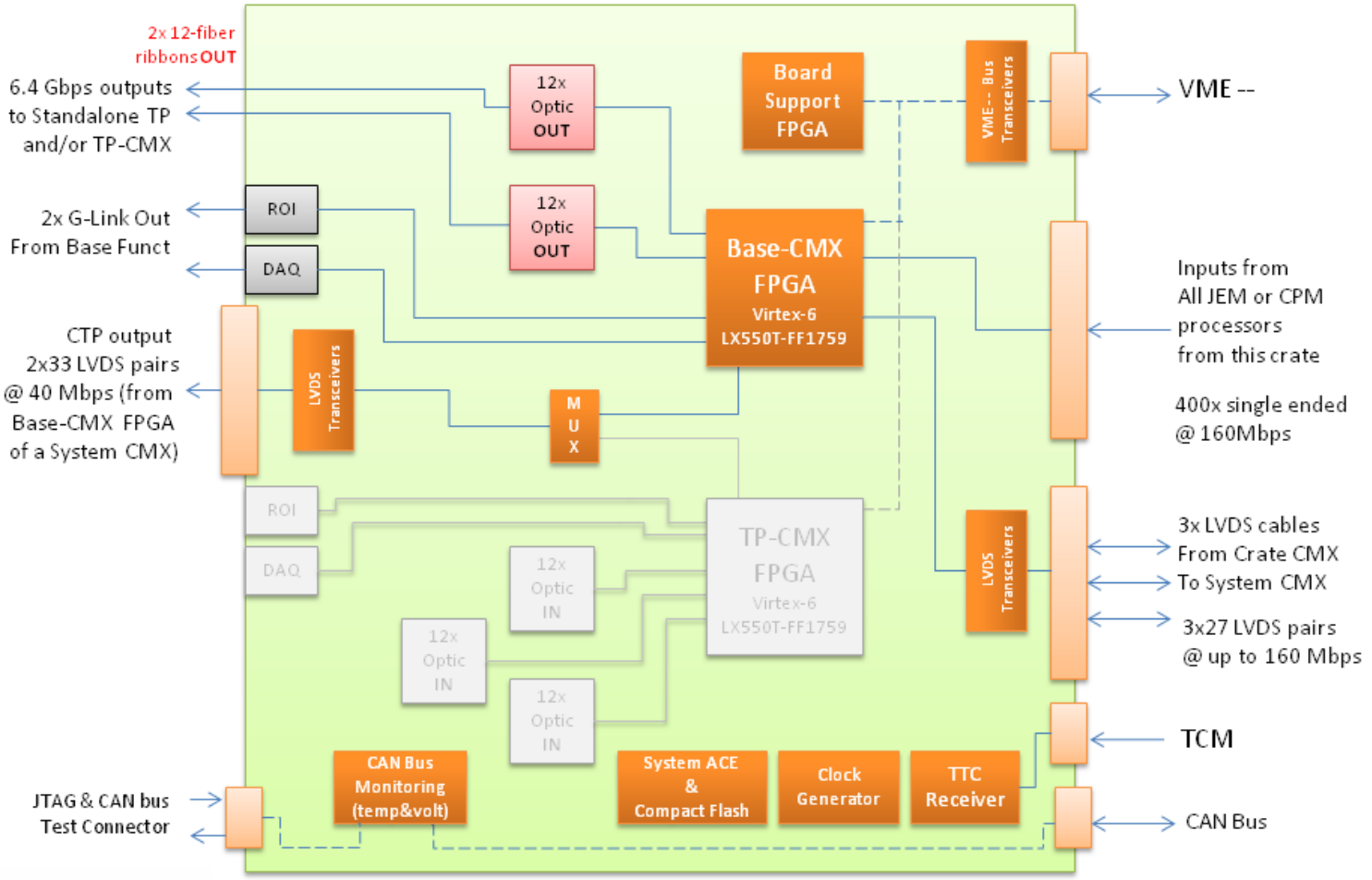
Overall project CMX HW/FW/SW

- Efforts in parallel on 5 fronts:
  - MSU – CMX design
    - Raymond Brock, Dan Edmunds, Philippe Laurens
  - CERN – VAT card, BSPT FPGA firmware, CANbus tests
    - Yuri Ermoline
  - CERN – CMX software
    - Duc Bao Ta (previously Seth Caughron)
  - UBC – BF FPGA firmware (I/O)
    - Wojtek Fedorko
  - Stockholm – BF FPGA firmware (zero-suppression, thresholding, etc)
    - Pawel Plucinski, Samuel Silverstein

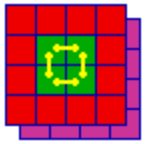
CMX is part of L1calo Phase 0 upgrade



- CMX == L1Calo Trigger replacement for current Common Merger Module (CMM)
  - Phase-I accelerated item a.k.a. Phase-0



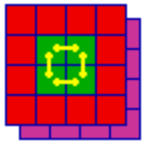
- The CMX was designed to:
  1. Be able to perform all tasks currently handled by any CMM.
  2. Extend these CMM tasks to higher input and output line rates.
  3. Offer more computing power for additional thresholds or algorithms using the extended input
  4. Provide an output to L1topo and send a raw or processed copy of its inputs optically at 6.4Gb.
  5. Provide optional functionality to perform Topological Processing on CMX platform if needed.



Definition: **Base-CMX** functionality

- **Extended CMM functionality** (Crate CMMs and System CMMs)
  - Receive and process 400 JEM/CPM input signals (@4x CMM rate)
  - All Crate CMXs send local summary to their System CMX through backplane connectors over LVDS cables (plan is @2x CMM rate)
  - System CMXs form and send triggering information to CTP over LVDS cables (plan is no change from CMM rate)
  - all CMXs send ROI and DAQ information over G-links (same as CMM)

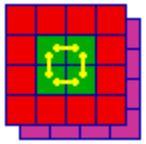
- **Source of data for L1topo: send CMX inputs** from JEMs or CPMs
  - Using 2x Avago miniPOD optical transmitters and 12-fiber ribbons
  - Some level of duplication is required (at least 2x copies)
  - **One** 12-fiber ribbon @6.4Gbps sufficient for all raw input data
  - But plan is to send zero-suppressed data on 6x fibers per CMX
    → optical patch panel required



Definition: **TP-CMX** functionality

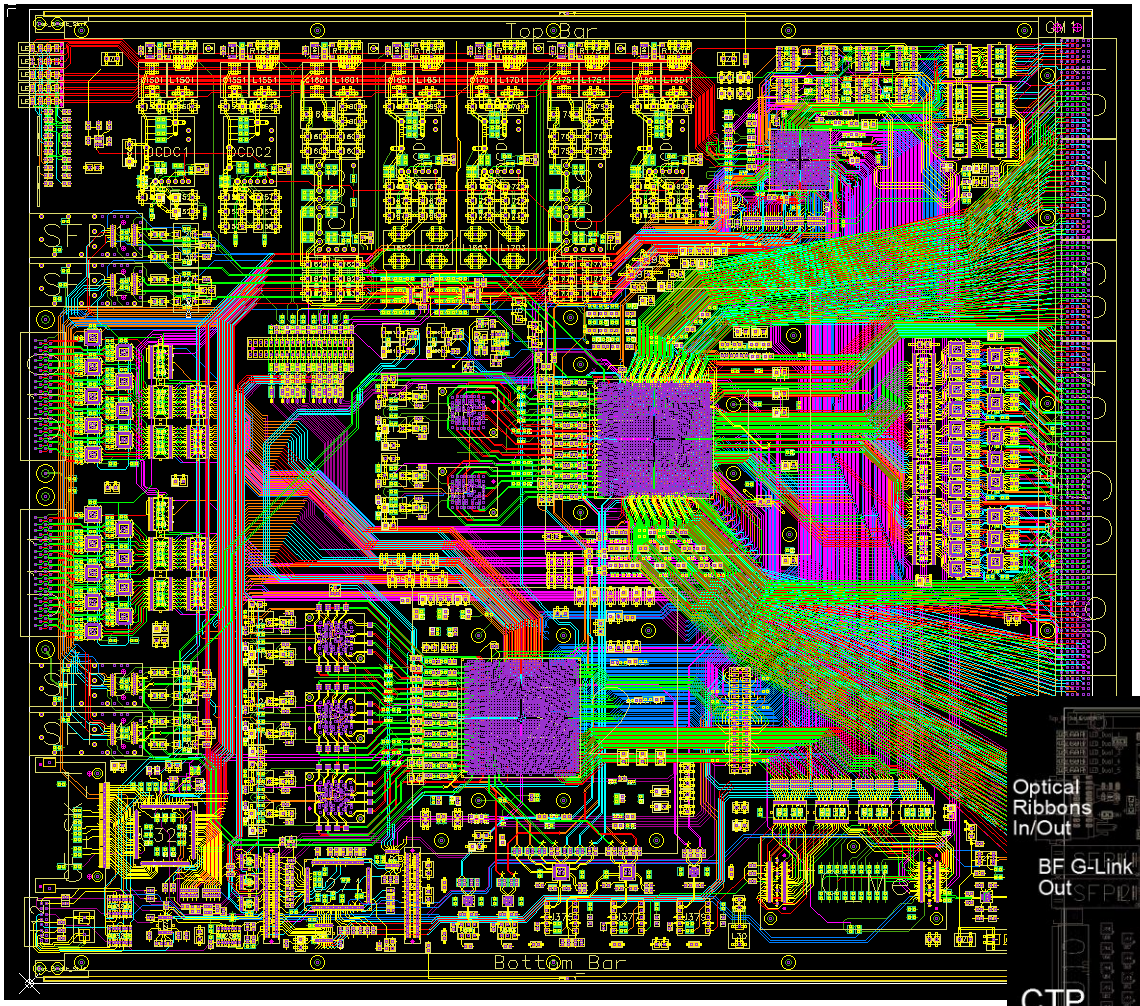
- Limited **Topological Processing** capability **on CMX** platform
  - Receive optical inputs from some/all of the 12x CMXs using 3x Avago receivers for up to 36x input fibers
  - Run multiple Topological Algorithms
  - Send Topological Triggering Information to CTP
  - Able to act as its own ROD for DAQ and ROI readout → support both G-link and S-link

- TP-CMX functionality was a backup plan requested in case L1topo would not be built, or availability was delayed.
- The TP-CMX feature now unlikely to be used past the prototypes.

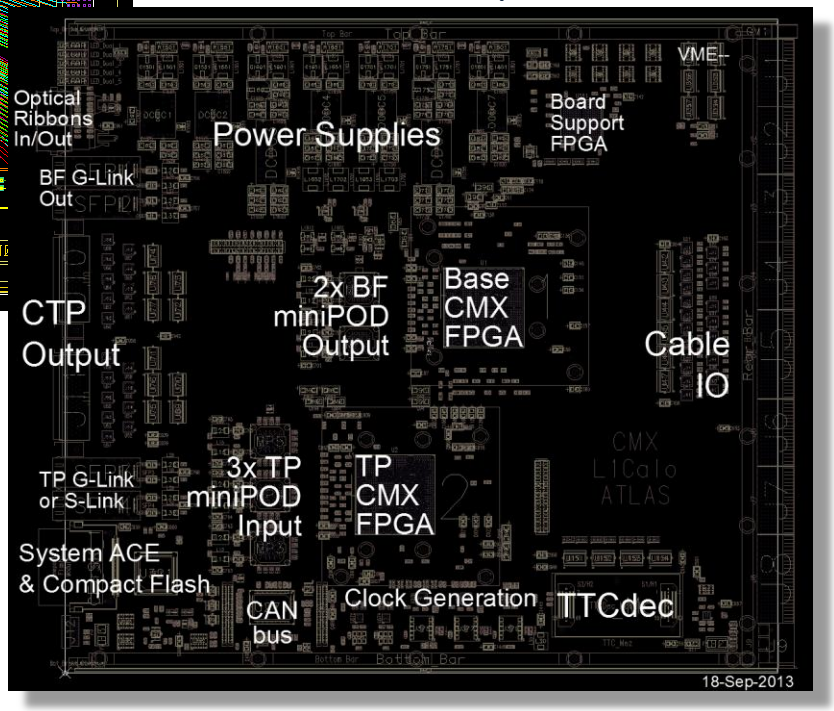


CMX Project Evolution

- Preliminary Design Review Stockholm (June 2011)
  - **Initial Specification**
- **Design Study** → Technical Workshop @RAL (Feb 2012) with decisions:
  - Use 2x separate FPGAs: Base-CMX and TP-CMX
  - Use Virtex 6 XC6VLX550T for both
  - 2x 12-fiber outputs from Base-CMX to l1topo
  - 3x 12-fiber inputs for TP-CMX functionality
- **Prototype Design Review** (March 2013) corrected assumptions, added requirements:
  - Use higher density MTP connectors
    - 5x MTP connectors were taking too much front panel → 2x MTP connectors
    - Higher density if/where needed; production CMXs with only Base Function only need 2x 12-fiber outputs
    - now CF card accessed through front-panel
  - CANbus now required to also monitor power supply currents
  - Both LHC derived Deskew-1 and Deskew-2 clocks from TTCdec sent to both FPGAs
  - Separate fixed 40MHz clock required for for G-link readout (probably better is 120 MHz)
  - TP function needs to be able to act as its own ROD
    - Provide an additional 100MHz clock to FPGA serial links for S-link outputs
    - Instrument the receiver port of the SFP bays (need to use Base-CMX serial inputs)
    - Provide all TTCdec signals to TP-CMX FPGA
- Final Informal Prototype Review (Oct 2013) verified all needed functionality has been included



- Two Virtex 6 LX550T
  - Base Function FPGA
  - Topo Processing FPGA (not installed)
- One Spartan 3a
  - Board Support FPGA
- 10x power supplies
  - 7x DC-DC supplies
  - 2x fixed reference
  - 1x variable reference
- 5x clock distribution networks
  - 2x 40.08 MHz from TTCdec
  - 1x 320.64 MHz (for 6.4Gb I/O)
  - 2x fixed freq (for G-link or S-link)



- 22x layer circuit board
  - 9x signal layers (5x with 60 Ohm traces)
  - 3x power fill layers
  - 10x ground plane layers
  - blind vias through top L1-L6 for Gb traces

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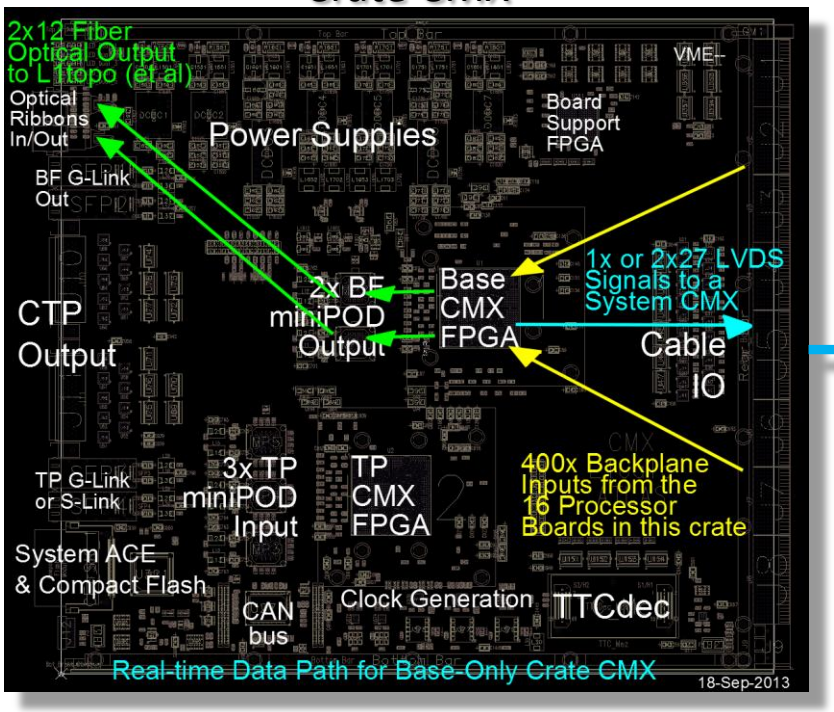
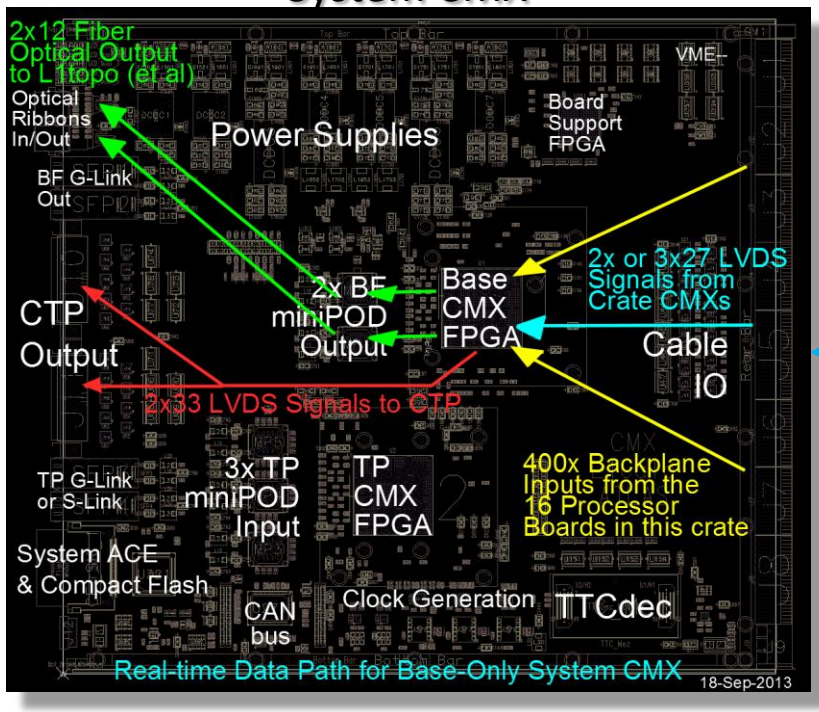
CMX connectivity

❑applies to electron, Tau, Energy or Jet data types

Crate CMX



System CMX



❑ Merger Cables

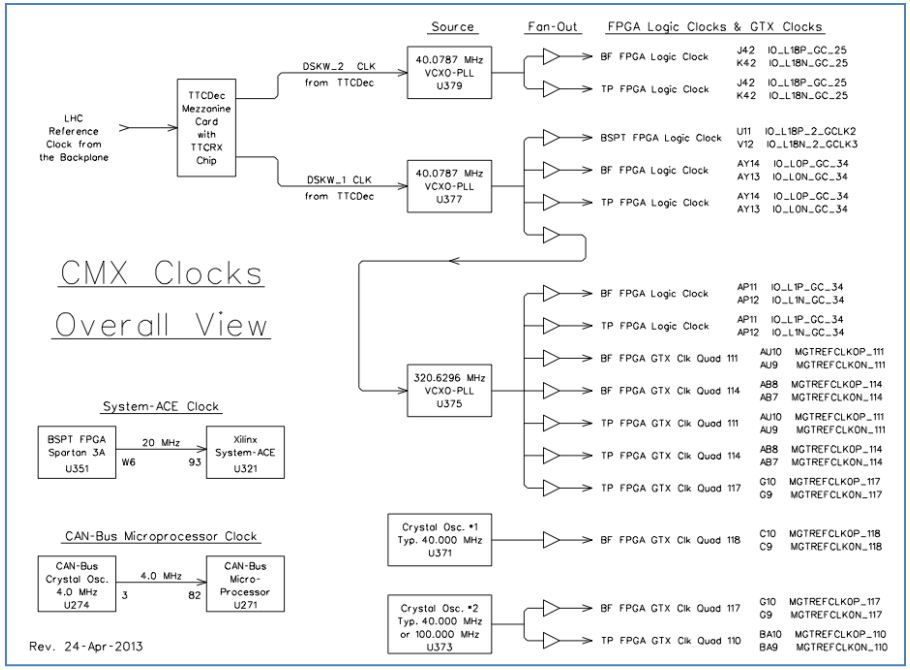
➢from one of more Crate CMX

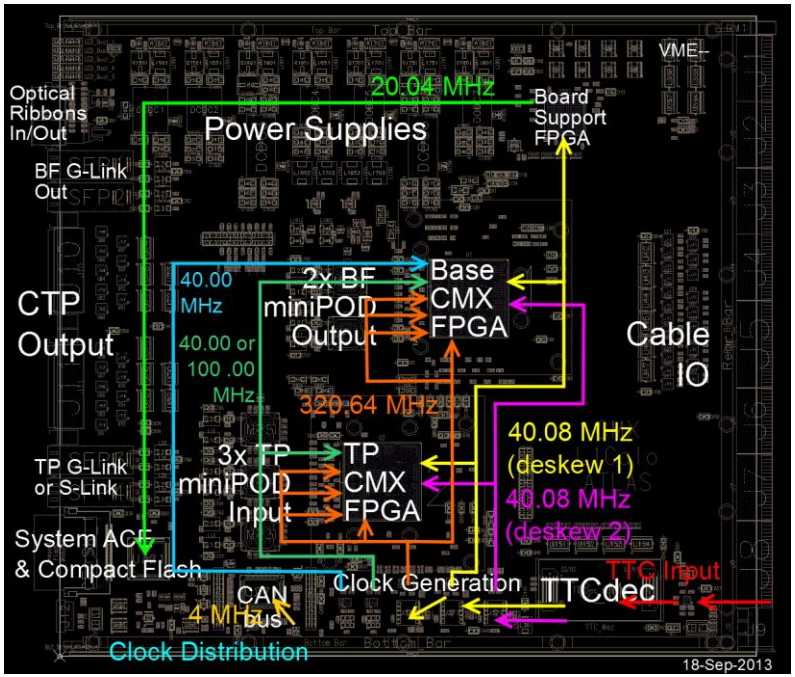
➢ To its System CMX

❑ All 12x CMXs in L1calo forward their inputs to L1topo

❑ Only the 4x System CMXs send info to CTP

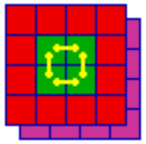
Circuit Diagrams and design details available on the CMX website





http://www.pa.msu.edu/hep/atlas/l1calo/

http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/block_diagrams/
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/



Challenge: backplane inputs

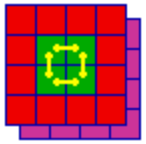
- 400x inputs, 60Ω Single-ended, @160 MBps
  - Limited tests done with BLT card
- Initial protocol requirement used a merged forwarded Clock/Parity
  - Now abandoned, but CMX remains compatible
  - implied complications for I/O pin assignment (MMCM usage)
- Initial goal was to route all 400 inputs straight under their FPGA pin with no extra via
  - Doable but not practical. Too many signal layers needed (12)
  - Board too thick, especially because of 9x 60 Ω layers required.
- Compromise: a fraction of the 400 inputs have to switch layer
  - For their last < 2 cm and to ~50Ω. Simulation says ok.
  - Now fewer trace layers (9), especially fewer 60Ω layers (5).
- Make use of Virtex 6 Select IO block features
  - IODELAY to help with relative skews among 25 signals from each input source
  - Provide external reference impedance (if 60 Ω termination needed)
  - Provide external VREF (if default VCCO/2 turns out not to be optimal)

LVDS I/O

- 2.5V to 3.3V translator components and LVDS transceiver components used on CMX are specified well in excess of 160Mbps; used for Merger cables and for CTP output

- The 3x Merger cable ports can be independently controlled as Input or Output to help testing of a single CMX

- The 2x CTP cable ports can be independently controlled as Input or Output to help testing of a single CMX

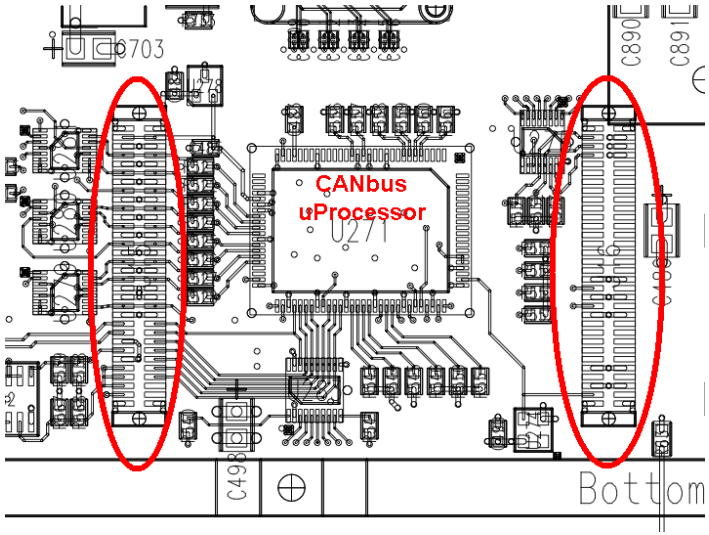


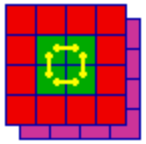
Misc Safety, Backup, Testing Features

- Hardware Oversight Logic
  - Help prevent CMX from hanging VME– bus
  - Help prevent CMX from harming itself until configured
- Spare signals from BF and TP FPGA to BSPT FPGA
- Spare debug connector
  - 10 signals from each FPGA
- Front panel access to 2x signals, from any FPGA
- Separate crystals for DAQ&ROI output BF FPGA vs TP FPGA to support any combination of G-link or S-link protocol

CANbus Backup Feature

- CMX would like to use same CANbus uProcessor (and the same firmware) as CMM but MB90F594 is obsolete
  - Yuri found a promising source and is testing one sample
  - CMX Prototype will use these parts
  - Also added spare connectors to CMX layout as backup plan for a mezzanine





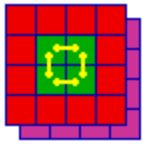
CMX Schedule

- 2013: Prototype fabrication and testing
  - Mar: CMX Prototype Readiness Review
  - Apr-Oct: PCB design and layout
  - Oct-Nov: Prototype fabrication (2x boards with TP, 1x without, 1x with none)

    now:
    - ❖Bidding phase complete, Assembly house visited and selected.
    - ❖MSU PO about to be issued, some final technical details being worked out with board manufacturing house

  - Nov-Dec: Testing first only at MSU, continue in parallel at MSU and CERN
- 2014: System testing and integration / final fabrication
  - Jan-Feb: Full-crate test (USA15), patterns for L1Topo (bldg 104)

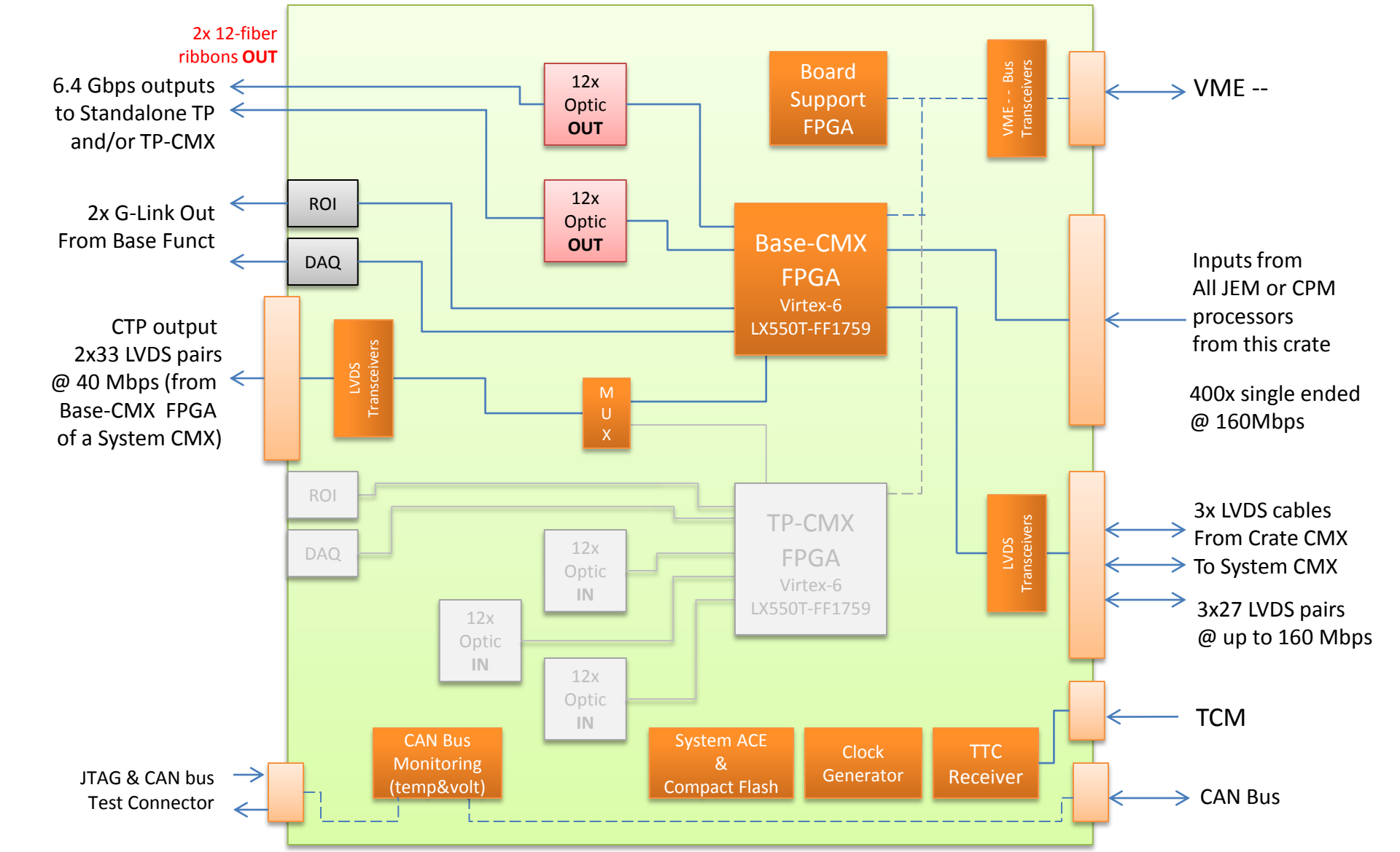
    Production Readiness Review
  - Feb-Mar: Final fabrication (20 production boards, no TP) & QC @MSU
  - Apr-Jul: Installation and commissioning @CERN (**M4**: July 7-11)
  - Aug-Sep: Test in the USA15 L1Calo system (**M5**: Sept 8-12)
  - Oct-Dec: Integration with L1Topo (**M6**: Oct 13-17)



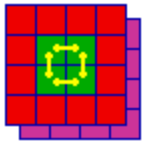
Thank you

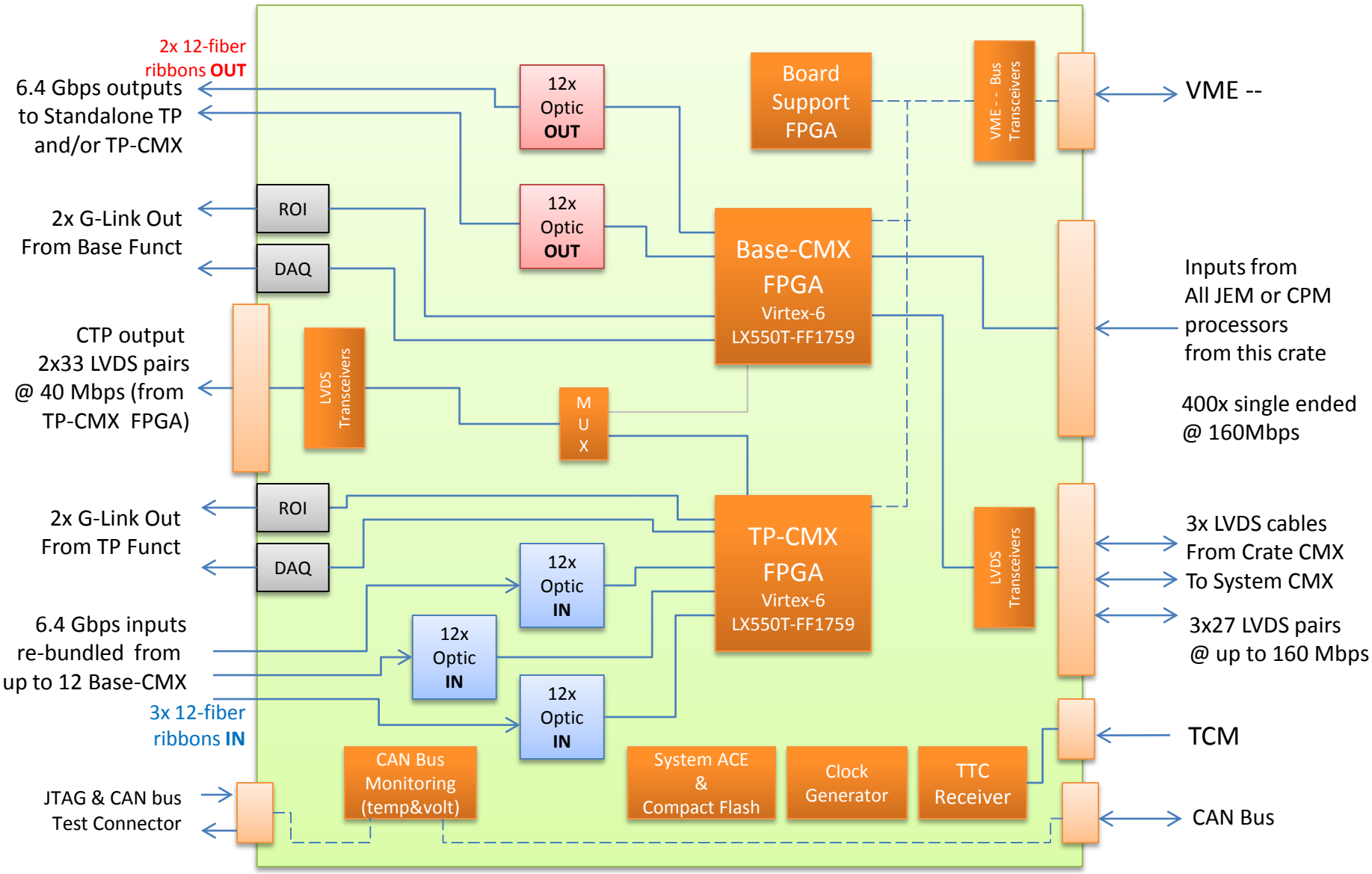
(Extra slides)

CMX Card with Base-CMX functionality only

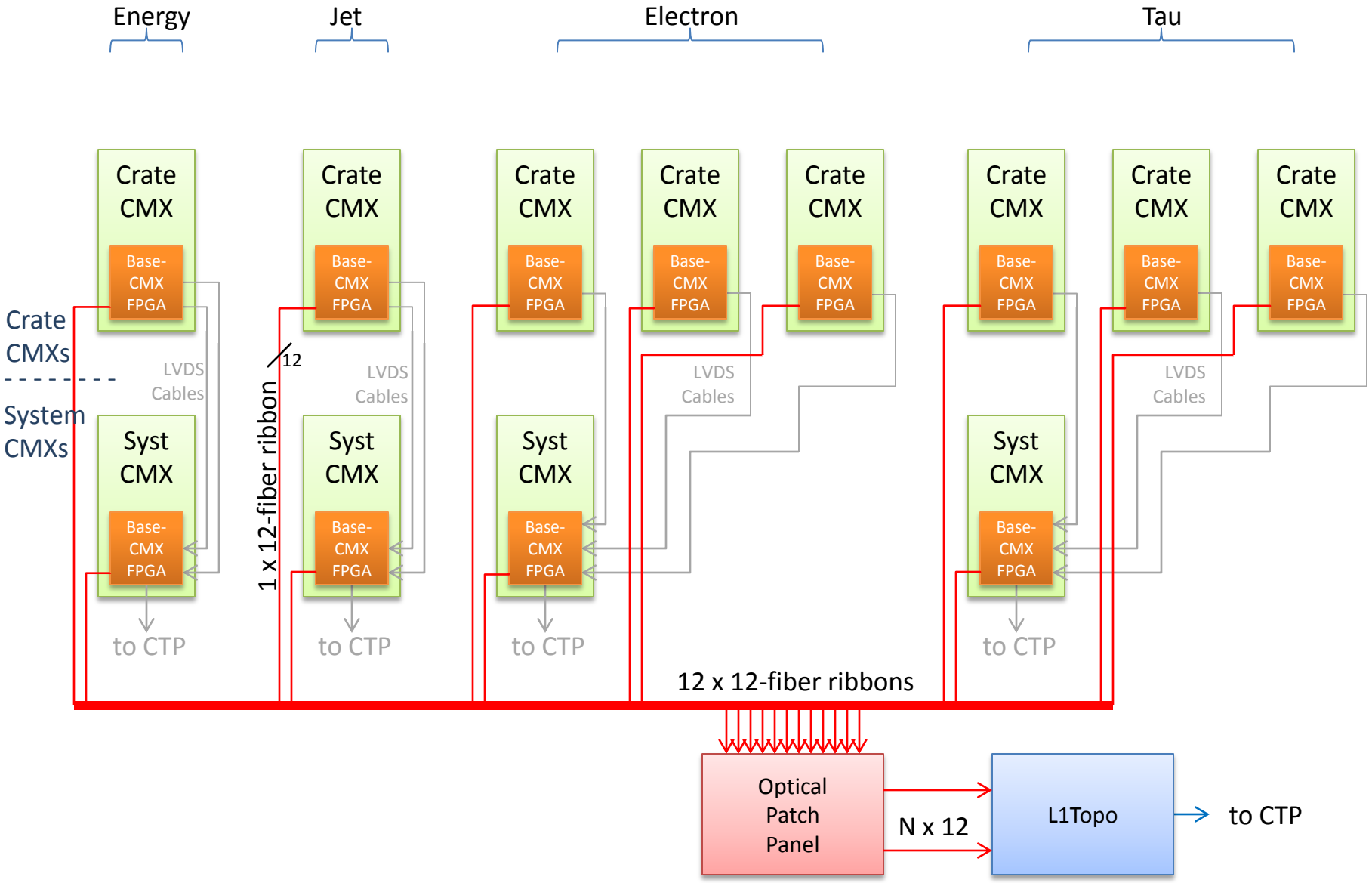


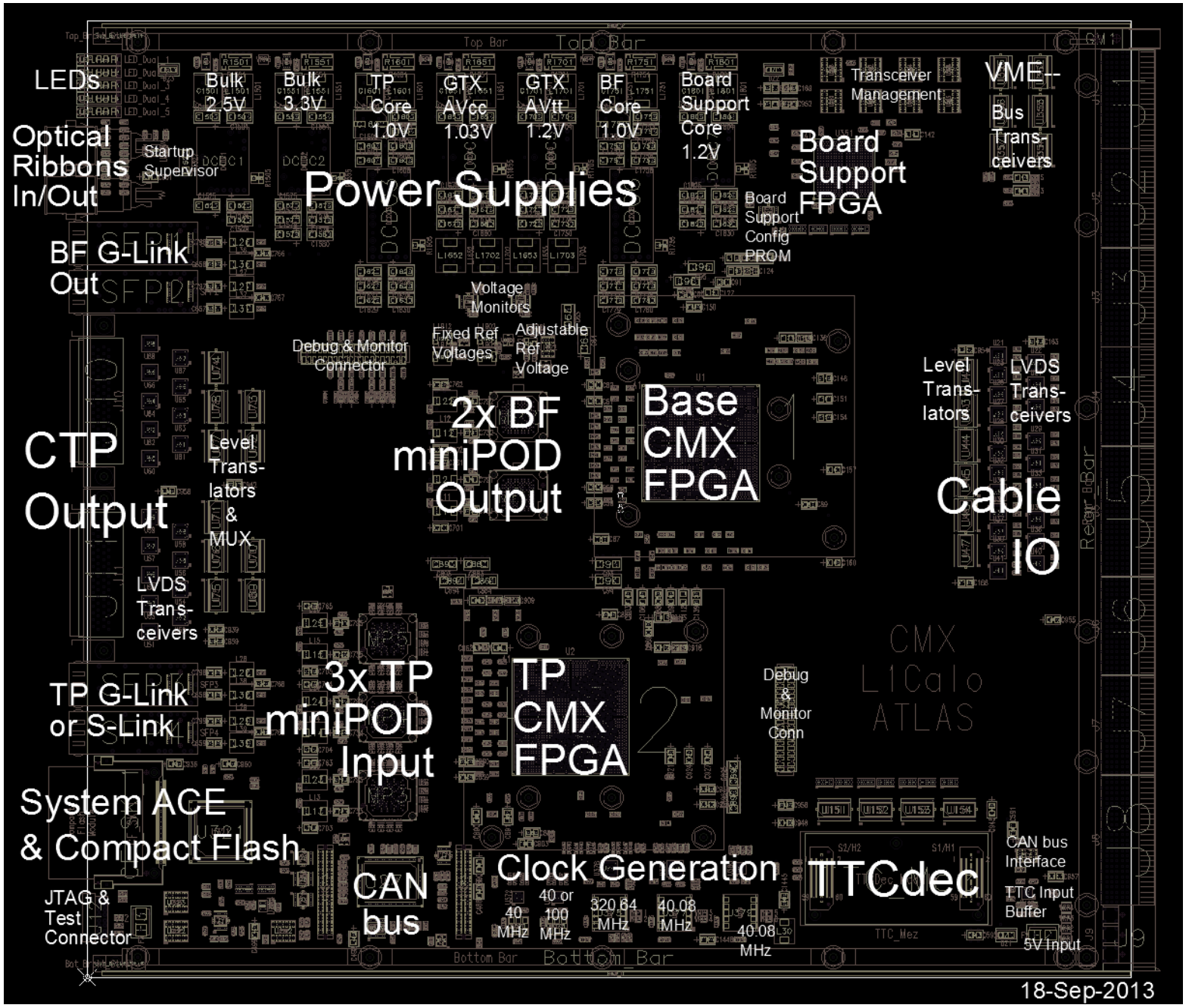
CMX Card with Base-CMX functionality and TP-CMX capability

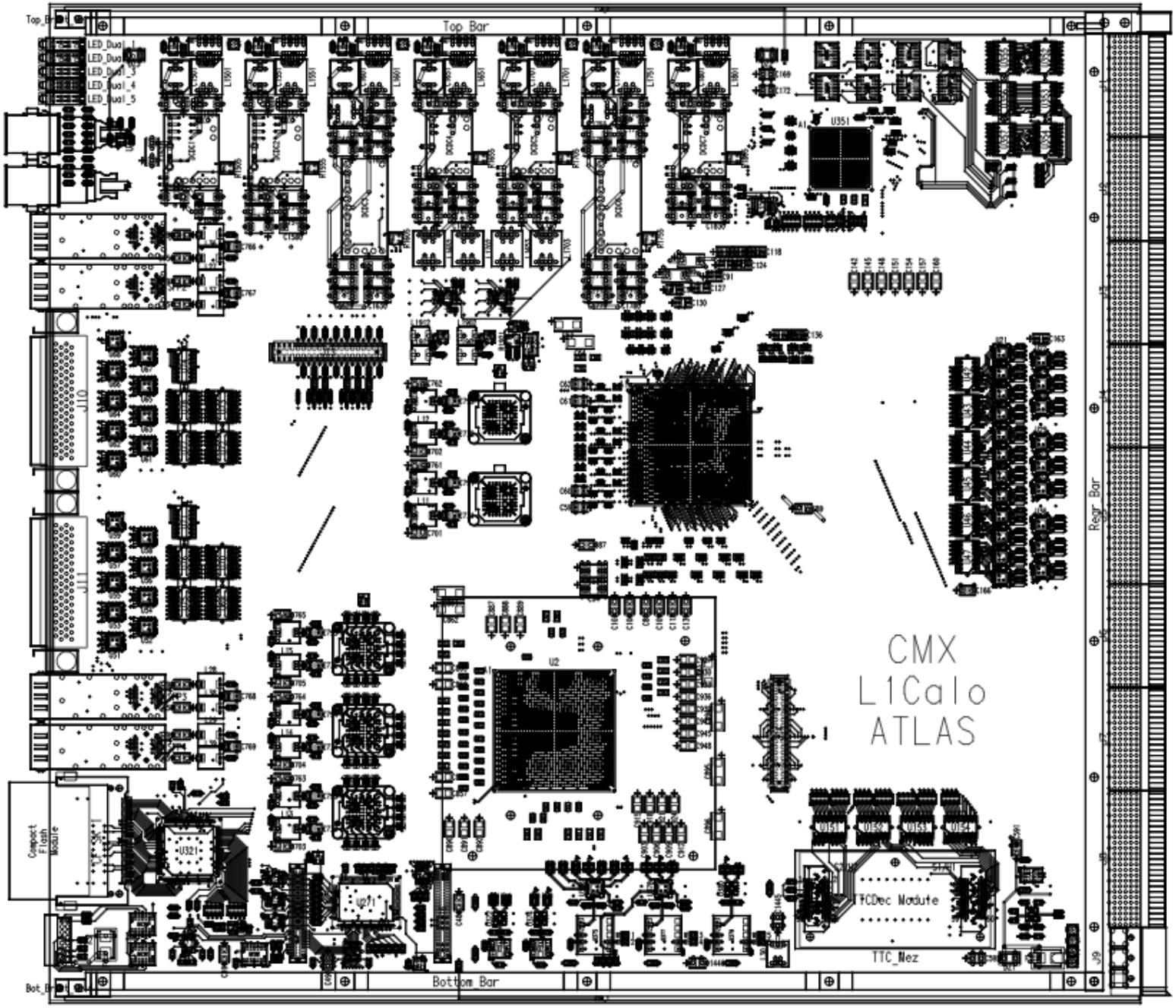




L1topo will receive Zero-Suppressed data from all CMXs




LEDs
Optical Ribbons In/Out
Startup Supervisor
Bulk 2.5V
Bulk 3.3V
TP Core 1.0V
GTX AVcc 1.03V
GTX AVtt 1.2V
BF Core 1.0V
Board Support Core 1.2V
Power Supplies
Transceiver Management
Board Support FPGA
Board Support Config PROM
VME-- Bus Trans-ceivers
BF G-Link Out
Voltage Monitors
Debug & Monitor Connector
Fixed Ref Voltages
Adjustable Ref Voltage
2x BF miniPOD Output
Base CMX FPGA
Level Trans-lators
LVDS Trans-ceivers
Cable IO
CTP Output
Level Trans-lators & MUX
LVDS Trans-ceivers
TP G-Link or S-Link
3x TP miniPOD Input
TP CMX FPGA
Debug & Monitor Conn
CMX L1Calo ATLAS
System ACE & Compact Flash
JTAG & Test Connector
CAN bus
Clock Generation
40 MHz
40 or 100 MHz
320.64 MHz
40.08 MHz
40.08 MHz
TTCdec
CAN bus Interface
TTC Input Buffer
5V Input
Top Bar
Bottom Bar
Rear Bar
18-Sep-2013


Top_Bar
Bottom_Bar
Regr_Bar
CMX
L1Calo
ATLAS
TTCDec Module
TTC_Mez
Compact Flash Module