CMX: installation, integration and commissioning plans

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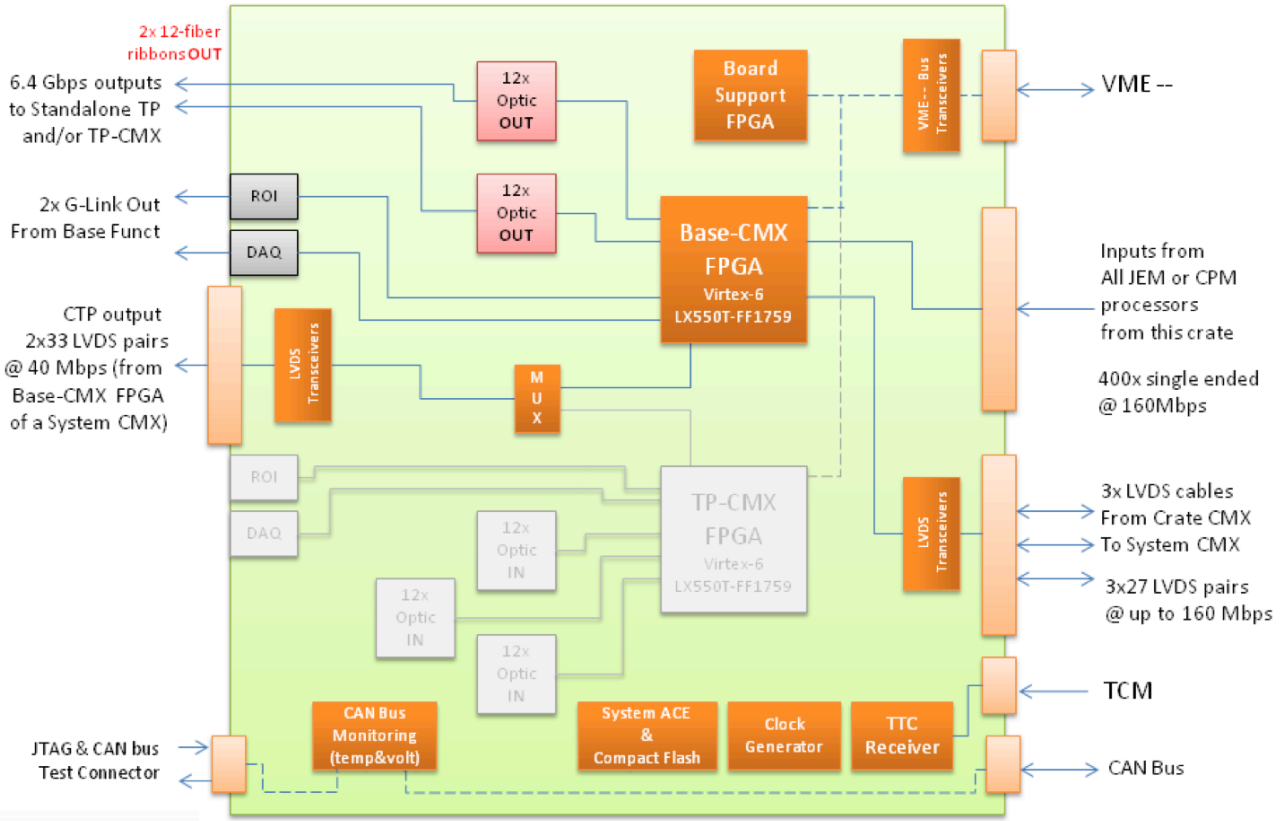
Overview



Three functional CMX prototypes expected end of December

Overview

I. Initial testing

- Initial board checkout @ MSU
- Board interface tests @ MSU/CERN
- *Wojciech covered the details in last L1calo week*

II. System tests with goal of a successful PRR

- At CERN starting February in Lab 104, high speed backplane testing
- In USA15, full rack testing, mid-end of February
- *We were asked to provide details about time scales and resources needed*

III. Post PRR focus on system integration and commissioning

- Continue tests in Lab 104, focusing on logic and algorithms

I. Initial testing

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Initial board checkout to be done @ MSU

- Board inspection and final assembly and installation of components
- Grounding and power verification
- Clock testing and characterization
- FPGA programming via JTAG/CF

I. Initial testing

Interface tests to be done @ MSU

- Test data interfaces standalone in loopback
  - CTP outputs, merger cable I/O, SFP optical output, L1topo optical output
- Using the MSU rig (later in parallel with test @ CERN)
- Find parameters to successfully receive 160 Mbps backplane input from single JEM in MSU test rig
  - Special test firmware versions for BF and Topo FPGA, with components from target FW (Wojtek, Pawel)
  - Special FW for JEM for sending direct test patterns at the output to test data integrity (Pawel)
- Embed Chipscope cores for control and monitoring to minimizing SW support
  - At the same time CMX/JEM software is being adapted, possibly use already in interface tests (Duc)

I. Initial testing

Close to target FW for Board Support FPGA (Yuri)

- Control of the AVAGO TXRXs
- LVDS buffer control
- TTC control

Timescale

- Initial board checkout will start end of December/beginning of January
- Pawel and Wojciech perform interface tests @MSU beginning of January, planned for two weeks
- Shipping of initially one CMX to CERN (for full crate test will have two), continue with tests in parallel at MSU with remaining CMX

II. System tests towards PRR

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Backplane data transmission tests in Lab 104

- Determine and manage the parameters for test rack in lab 104 before full crate tests in USA15
  - Use and continue to develop special CMX and JEM FW that was used in the initial test phase (Pawel, Wojciech)
  - Test data integrity with FW and software elements for the timing procedure (under development) via the backplane line/clock delays (SW: Savanna, Duc, FW: Wojciech)
    - Parity error counters for each input module data
    - Data error flag/counters for each backplane line

II. System tests towards PRR

Backplane data transmission tests in Lab 104, cont.

- Development of software needed prior to the tests (support of new JEP/SumEt capabilities, partially based on software used in initial test phase) and availability of software experts maybe beneficial
- Not testing any algorithms or logic

Further tests in Lab 104, but not needed before USA15 full crate test

- DCS tests
- Full tests of proper electrical/optical operation of all inputs and outputs

II. System tests towards PRR

System tests in USA15 with full crate and two CMX prototypes

- Tests will be done with JEMs only
- Test of full high-speed backplane performance with full crate of at least JEMs for long periods of time
- Redo data integrity test as in CERN test rig
- Power and power quality tests

II. System tests towards PRR

System tests in USA15 with full crate and two CMX prototypes, cont.

- Re-use special FWs used in previous tests
- L1calo standalone partition for one (JEM) crate would be sufficient, no CTP needed
- No other detector systems needed
- Operations experts would be needed to facilitate partition building and running tests concurrently with other sub-systems
  - Would want to have separate partition for CMX test from partition for other L1Calo test or ATLAS subsystems

Timescale

- Earliest start by beginning of February with CERN test rig, continued interface tests in parallel @ MSU
- Full crate test in USA15, middle of February for 1-2 weeks

II. System tests towards PRR

Remarks on full-crate system test

- Tests are planned with JEM (Jet) modules and CMX alone
  - Expertise and support on JEM at hand
  - Looking into having JEM energy sum as well for electrical tests
- Might also require full-crate CPM testing
  - Do not have fully working CPM at hand and cannot test if problems occur which are related to CMX design
  - Would need updated CPM firmware and software, if test with CPM is required for PRR

III. Post PRR testing

III. Post PRR testing and commissioning

Tests @CERN after PRR

- Continue with system tests
- Test algorithms and data content
- Working towards final firmware
- Shift focus to CPM, if it was not fully included before

Installation of CMX production cards for M-runs as soon as…

- PRR successful
- Production of CMX card completed
- Tests of production CMX cards @MSU finished
- Firmware and software ready

Summary

I. Initial testing

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- Board interface tests

II. System tests with goal of a successful PRR

- At CERN Lab 104, high speed backplane testing
- In USA15, full rack testing

III. Post PRR focus on system integration and commissioning

- Continue tests in Lab 104, focusing on logic and algorithms

CMX prototypes arrive end of **December**

Initial tests **December/January** @MSU

System tests **beginning of February** @CERN Lab 104

Full rack test @USA15 **mid-February**

Backplane tests for PRR finished by **end of February**

Post PRR test @MSU and @CERN