CMX Status, installation and integration plans

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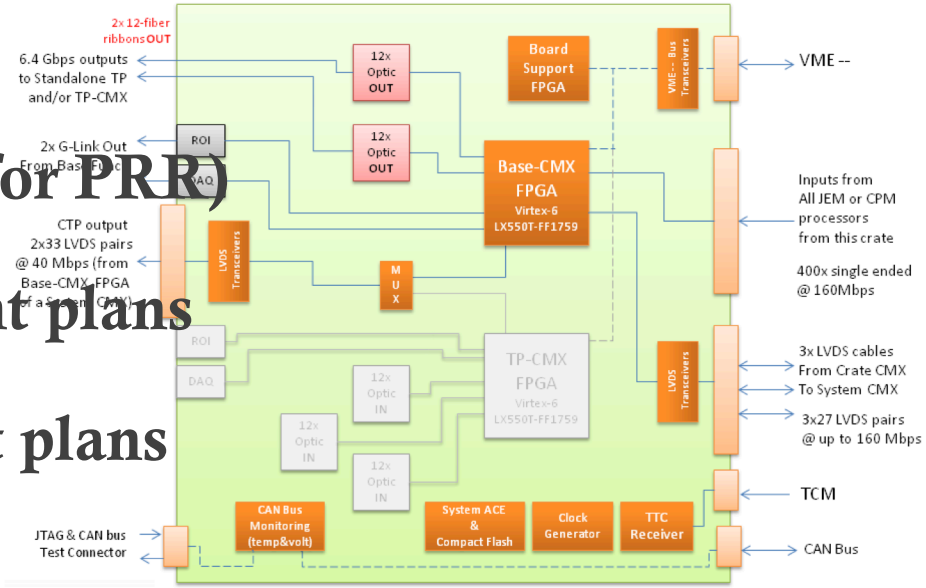
Overview

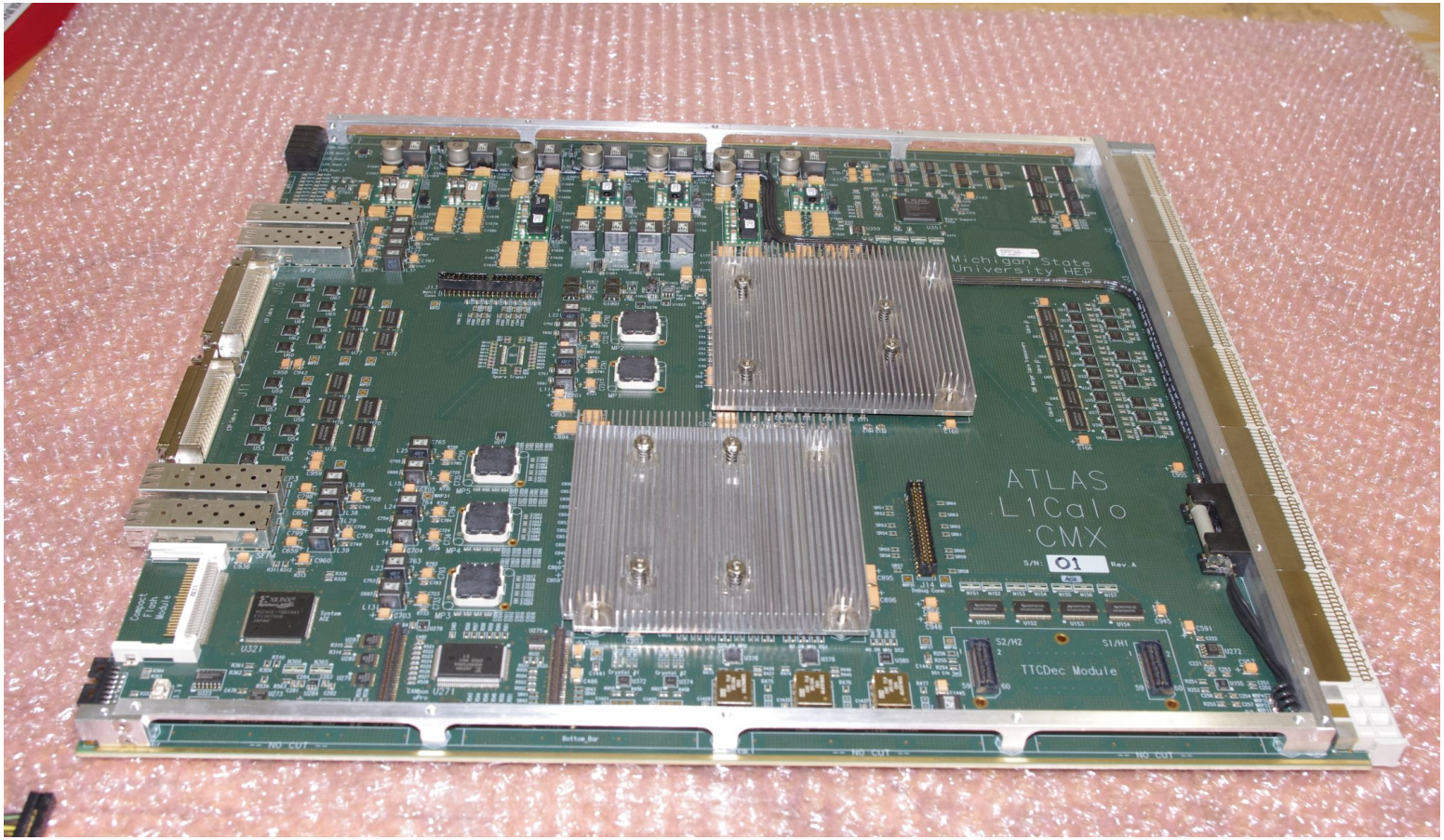
- Status of the CMX
- Hardware test plans (for PRR)
- Firmware development plans
- Software development plans
- Integration plans



Status of CMX

- **Arrival of three prototype CMX**
  - One empty board
  - One only with board support FPGA
  - Two will be fully loaded
  - First tests performed, today achieve pattern capture on CMX from JEM

Status of CMX



Hardware test plans

- **Test plans for successful PRR**
  - Initial bare tests @ MSU, then with MSU test rig and JEM
  - System tests @ CERN test rig, system test in one crate in USA15
  - Concentrate on basic interface tests, esp. backplane transmission
- **Initial board checkout@ MSU (Dan, Philippe)**
  - Board inspection and final assembly and installation of components
  - Board support FPGA configuration via JTAG and VME IO
  - Base and top FPGA configuration via JTAG/CF

Hardware test plans

- **Interface tests to using the MSU test rig (Dan, Philippe, Wojciech, Pawel)**
  - Establish the system clocking for Base and Topo FPGAs
  - Backplane connectivity and timing measurement
  - Test data interfaces standalone in loopback
  - Embed Chipscope cores for control and monitoring to minimizing SW support
  - Possibly use updated CMX software and CMX timing software already in interface tests

2 weeks @ MSU, continue @ MSU&CERN for ~4 weeks

Hardware test plans

- **Backplane data transmission tests in Lab 104 (Wojciech, Pawel, Duc, Savanna, Yuri)**
  - Preparation for USA15 tests
  - Operation parameters for 160 Mbps backplane input from single JEM using timing procedure/software
  - Long term data stability test with stress data patterns in test crate
- **System tests with full crate and two CMX prototypes in USA15 (Wojciech, Pawel, Duc, Savanna, Yuri)**
  - Test of full high-speed backplane performance with full crate of at least JEMs for long periods of time
    - Looking into having JEM energy sum as well for electrical tests
  - Redo data integrity test as in CERN test rig
  - Power and power quality tests
  - L1calo standalone partition for one (JEM) crate would be sufficient, no CTP needed, no other detector systems needed

1+1 week

Hardware test plans

Continued interface testing in Lab 104

- CPM testing
  - In contact with Jurai about CPM firmware and software
  - Would need same/similar capability as the JEM

Installation of CMX production cards for M-runs as soon as…

- PRR successful
- Production of CMX card completed
- Tests of production CMX cards @MSU finished

2 weeks

FW development plans

- **Development of firmware along with the hardware tests (Wojciech, Pawel)**
  - Prototype firmware for initial test
  - Focus on jet firmware first, re-use building blocks for other parts of the firmware
- **Development of Board Support FPGA (Yuri)**
  - Control of the AVAGO TXRXs
  - LVDS buffer control
  - TTC control

FW development plans

- **JET System**
  - ROI, DAQ readout
  - LVDS IO module adaptation Spy memory integration
  - RT path thresholding
  - FW integration and verification with simulation software and comparing to software model on test vectors
- **Jet Crate:**
  - Adaptation of thresholding logic from system
  - FW integration and verification
- **Following the Jet System/Jet Crate firmware**
  - Sum ET Crate/System, CPM
    - Decoder, Encoder, Sum logic
    - FW integration and verification

in sync with simulation development

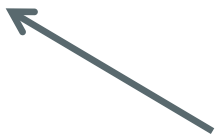
in sync with simulation development

SW development timescale

- **Development along with hardware tests and firmware development (Duc, Savanna)**
  - Prototype software in hardware tests, especially timing software
  - Simulation needs to be completed for firmware verification
  - Basic structure available via copy of CMM simulation
  - Creation of test vectors, but no sensible patterns defined, yet

SW development timescale

- **Online software development, finished tasks**
  - Various data formats implemented
  - Thresholding of jets implemented
  - JEM System and crate merger updated/implemented
- **Online software development, on-going**
  - CMX timing procedure and software
    - Documentation in development
    - Abstract version of procedure in code
    - Implementation of interfaces to actual CMX registers
  - Update of other CMM parts in the software
  - CMX test vector generation
  - CMX to Topo development
  - CMX stand-alone test environment



in sync with hardware tests

Integration plans

- **Hardware level integration (data sending receiving)**
  - During hardware tests initial integration with
    - JEM (single), CPM (single), ROD (DAQ/ROIB)
  - Integration at later stage
    - Complete integration with above
    - Crate-System CTP (CMX as sink) LVDS
    - Topo (CMX as sink)
- **Online software development and system integration**
  - DB interface available
  - Software interfaces to other simulations via agreed data formats and data ports
    - JEM, CP, TOPO, CTP, ROS

Summary

- **Hardware tests**
  - Initial hardware tests @ MSU have started
  - Interface tests @ MSU will start soon
  - Backplane transmission tests and system tests planned @ CERN in Lab 104 and USA15
- **Development of firmware and software**
  - Prototype firmware and software used for first tests
  - Continued firmware and software development
  - Firmware verification needs completed simulation software
- **Integration plans**
  - Hardware/firmware integration will start in hardware test
  - Software integration hopefully easier via agreed-on data formats

Hardware test plans

- **Test plans for successful PRR**
  - Initial bare tests @ MSU, then with MSU test rig and JEM
  - System tests @ CERN test rig, system test in one crate in USA15
  - Concentrate on basic interface tests, esp. backplane transmission
- **Initial board checkout@ MSU (Dan, Philippe)**
  - Board inspection and final assembly and installation of components
  - Grounding and power verification
  - Clock testing and characterization
  - Board support FPGA configuration via JTAG and VME IO
  - Base and top FPGA configuration via JTAG/CF

Hardware test plans

- **Interface tests to using the MSU test rig (Dan, Philippe, Wojciech, Pawel)**
  - Establish the system clocking for Base and Topo FPGAs
  - Backplane connectivity and timing measurement
  - Test data interfaces standalone in loopback
    - Low speed serial TX connectivity test
    - High speed serial Base RX/ Topo TX connectivity
    - LVDS RTM (crate to system) communication at 80 Mbps
    - LVDS front panel (CTP) communication at 40 Mbps
    - BASE to TOPO GPIO link
    - Operation parameters for 160 Mbps backplane input from single JEM using timing procedure/software
    - Development of stress test data patterns
  - Embed Chipscope cores for control and monitoring to minimizing SW support
  - Possibly use updated CMX software and CMX timing software already in interface tests

2 weeks @ MSU, continue @ MSU&CERN for ~4 weeks

Hardware test plans

- **Backplane data transmission tests in Lab 104 (Wojciech, Pawel, Duc, Savanna, Yuri)**
  - Preparation for USA15 tests
  - Operation parameters for 160 Mbps backplane input from single JEM using timing procedure/software
  - Long term data stability test with stress data patterns in test crate
  - Further data interface tests on-going @ MSU
- **Further tests in Lab 104, but not needed before USA15 full crate test**
  - DCS tests
  - Continuing data interface test, possibly with other hardware components (e.g. CPMs)

1 week

Hardware test plans

- **System tests with full crate and two CMX prototypes in USA15 (Wojciech, Pawel, Duc, Savanna, Yuri)**
  - Test of full high-speed backplane performance with full crate of at least JEMs for long periods of time
    - Expertise and support on JEM at hand
    - Looking into having JEM energy sum as well for electrical tests
  - Redo data integrity test as in CERN test rig
  - Power and power quality tests

1 week

Hardware test plans

System tests with full crate and two CMX prototypes in USA15, cont.

- Re-use prototype FWs used in previous tests
- L1calo standalone partition for one (JEM) crate would be sufficient, no CTP needed, no other detector systems needed
- Operations experts would be needed to facilitate partition building and running tests concurrently with other sub-systems
  - Would want to have separate partition for CMX test from partition for other L1Calo test or ATLAS subsystems

Hardware test plans

Continued interface testing in Lab 104

- CPM testing
  - In contact with Yurai about CPM firmware and software
  - Would need same/similar capability as the JEM

Installation of CMX production cards for M-runs as soon as…

- PRR successful
- Production of CMX card completed
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2 weeks

FW development plans

- **Development of firmware along with the hardware tests (Wojciech, Pawel)**
  - Prototype firmware for initial test
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- **Development of Board Support FPGA (Yuri)**
  - Control of the AVAGO TXRXs
  - LVDS buffer control
  - TTC control

FW development plans

- **JET System**
  - ROI, DAQ readout
  - LVDS output module adaptation (CP, CRATE->SYSTEM) (80 Mbps), LVDS input module adaptation (CRATE->SYSTEM) (80 Mbps)
  - Spy memory integration
  - RT path thresholding
  - FW integration

FW development plans

- **Jet System FW verification**
  - 'FPGA' level TB developed
  - generation of stimulus file based on
    - physics simulation
    - case-based
  - Verification with simulation software and comparing to software model on pre-loaded data

in sync with simulation development

- **Jet Crate:**
  - adaptation of thresholding logic from system
  - FW integration and verification

in sync with simulation development

FW development plans

- **Following the Jet System/Jet Crate firmware**
  - Sum ET Crate/System, CPM
    - Decoder
    - Encoder
    - Sum logic
    - FW integration
    - Verification

in sync with simulation development

SW development timescale

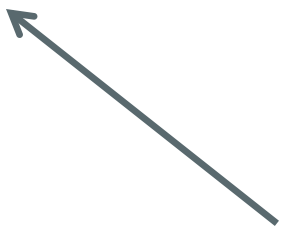
- **Development along with hardware tests and firmware development (Duc, Savanna)**
  - Prototype software in hardware tests, especially timing software
  - Simulation needs to be completed for firmware verification
- **Online software development**
  - Services = register map update along the development of firmware
    - On-going effort
  - Copy of CMM simulation
    - Basic structure available
    - Reading test vectors
    - Creation of test vectors, but no sensible patterns defined, yet

SW development timescale

- **Online software development, finished tasks**
  - Data formats implemented
    - JEM (jet and energy sum), CP -> CMX
    - crate CMX -> system CMX created
    - CMX -> ROS, CTP
  - Thresholding of jets implemented
  - JEM System and crate merger implemented

SW development timescale

- **Online software development, on-going**
  - CMX timing procedure and software
    - Procedure agreed on, documentation in development
    - Abstract version of procedure in code
    - Implementation of interfaces to actual CMX registers
    - Merge code to read/write timing test patterns
    - Integration into TDAQ system



in sync with hardware tests

SW development timescale

- **Online software development, on-going**
  - Update of CMM parts in the software
    - JET Daq merger
    - Energy sum merger, similar to CMM
    - Eg merger, similar to CMM
  - CMX test vector generation
  - CMX to Topo development
  - CMX stand-alone test environment

in sync with firmware verification

Integration plans

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