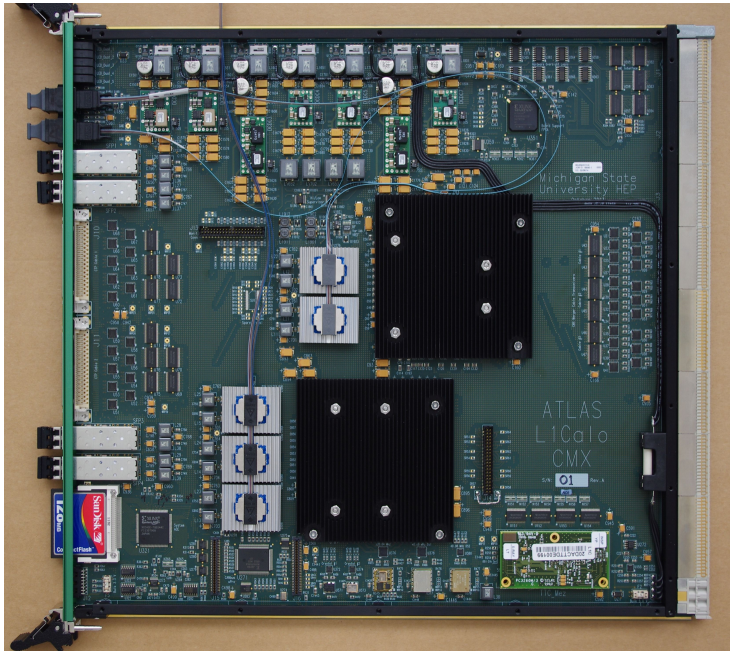
CMX – status

W. Fedorko, P. Plucinski, D.B. Ta, P. Laurens,
D. Edmunds, Y. Ermoline, R. Brock, J. Linnemann

Hardware!

- Prototypes are here:
  - 1 without Virtex 6 parts: SN0
    - Final assembly and checkout complete (power supply, PLL tracking)
  - 2 with both Virtex 6 parts on: SN1, SN2
    - SN1:
      - Final assembly complete
        - 120 MHz reference clock to be mounted
      - 'RT' Interfaces tested at MSU (see below)
      - On the way to CERN
    - SN2:
      - Final assembly complete
      - Initial interfaces tests ongoing at MSU
  - 1 with only 'Base Function' (standard configuration): SN3
    - Final assembly >50% complete



RT data path tests

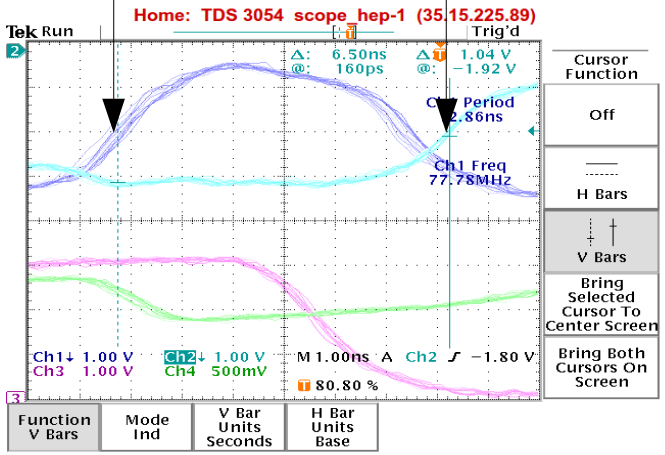
- Tests performed at MSU Feb 17-28
- SN1 used
- Will continue in parallel at MSU and CERN

RT data path tests: backplane static pattern test

- Pre-defined static pattern generated by JEM.
  - (1 slot tested)
- Monitored on the CMX via chipscope.
- Checked for no xtalk and no dead bits
- 160 Mbps pattern generated on JEM.
  - Basic timing measurements

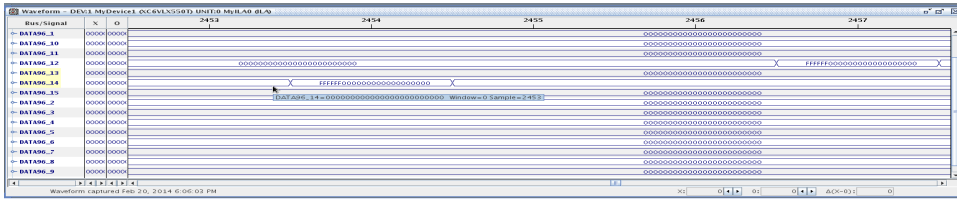
80 MHz forwarded clock

40 MHz dskw1 clock



RT data path tests: backplane 160 Mbps test

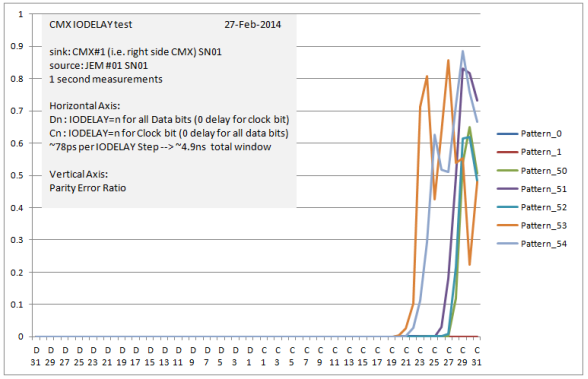
- Pre-defined 160 Mbps pattern sent from JEM (Jet FPGA)
  - 3 patterns used routinely:
  - Pulse
  - Switching in phase
  - Switching out of phase

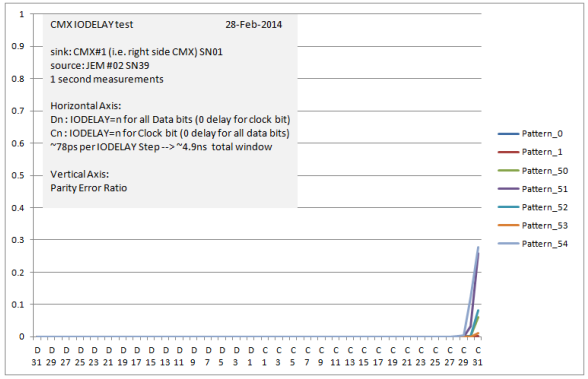


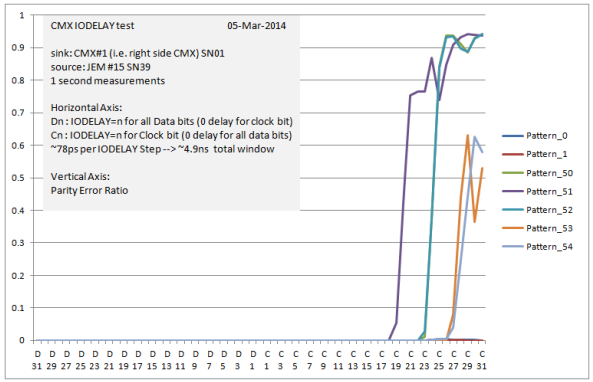
- 2 JEMs used at a time
- Chipscope error triggering and counters for parity errors
- All slots tested
- 50+hrs running with 2 JEMS without a single error

RT data path : backplane IDELAY scans

- Preliminary IDELAY scanning:
  - Relies on parity error monitoring
  - Delay forwarded clock by up to 31 'taps'; next delay all data signals by up to 31 taps simultaneously while clock delay set to 0
  - Tap ~78 ps → 4.9 ns total dynamic range



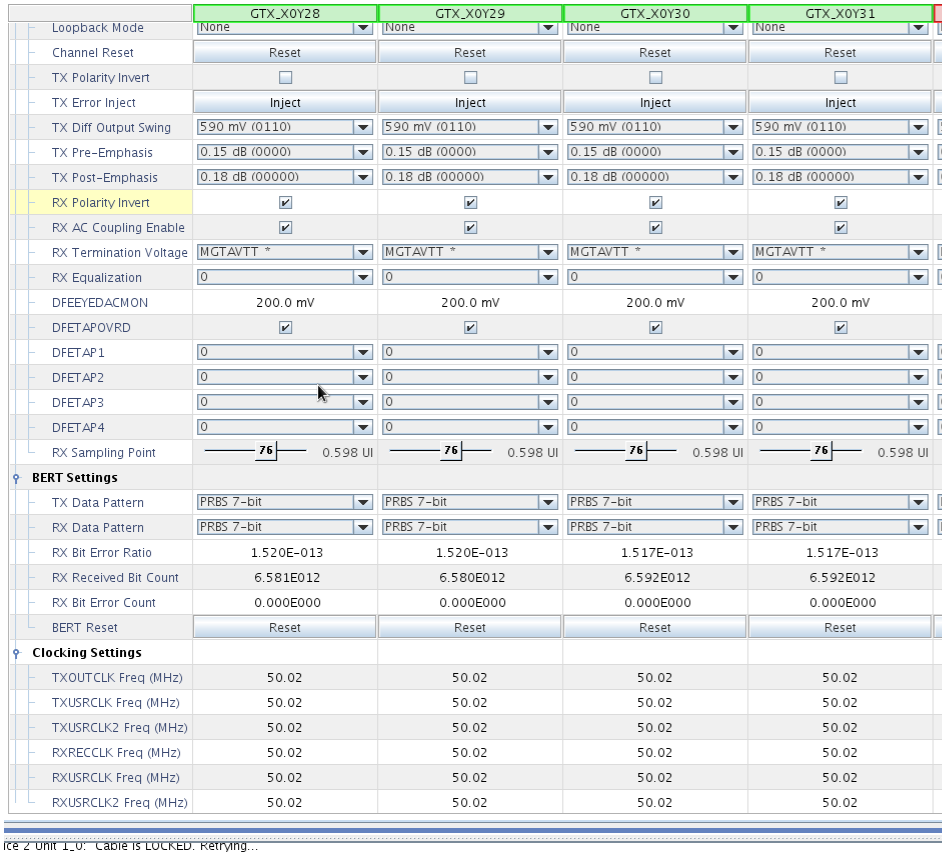




  - Differences in behavior between different JEMs in nearby slots
  - Differences for same JEM in different slots
  - Stability of behavior over few days
  - 'window' seems open
  - Needs calibration and bitwise tests

Data path tests: SFP

- Loopback set up Base TX → Base RX and Topo TX → Base RX.
- IBERT cores used to generate PRBS 7-bit pattern
- 100 MHz reference, 1 Gbps line rate
- No errors found in >1hr run with default GTX/SFP settings

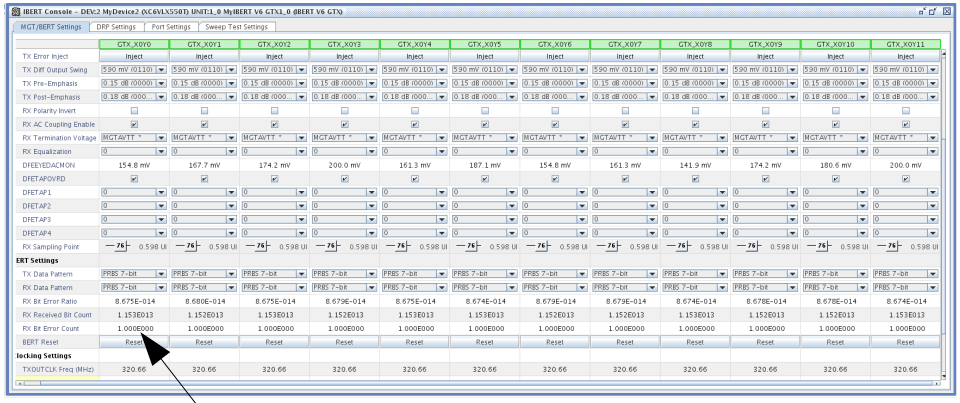


	GTX_X0Y28	GTX_X0Y29	GTX_X0Y30	GTX_X0Y31
Loopback Mode	None	None	None	None
Channel Reset	Reset	Reset	Reset	Reset
TX Polarity Invert	☐	☐	☐	☐
TX Error Inject	Inject	Inject	Inject	Inject
TX Diff Output Swing	590 mV (0110)	590 mV (0110)	590 mV (0110)	590 mV (0110)
TX Pre-Emphasis	0.15 dB (0000)	0.15 dB (0000)	0.15 dB (0000)	0.15 dB (0000)
TX Post-Emphasis	0.18 dB (00000)	0.18 dB (00000)	0.18 dB (00000)	0.18 dB (00000)
RX Polarity Invert	☑	☑	☑	☑
RX AC Coupling Enable	☑	☑	☑	☑
RX Termination Voltage	MGTAVTT *	MGTAVTT *	MGTAVTT *	MGTAVTT *
RX Equalization	0	0	0	0
DFEEYEDACMON	200.0 mV	200.0 mV	200.0 mV	200.0 mV
DFETAPOVRD	☑	☑	☑	☑
DFETAP1	0	0	0	0
DFETAP2	0	0	0	0
DFETAP3	0	0	0	0
DFETAP4	0	0	0	0
RX Sampling Point	76 0.598 UI	76 0.598 UI	76 0.598 UI	76 0.598 UI
BERT Settings				
TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Bit Error Ratio	1.520E-013	1.520E-013	1.517E-013	1.517E-013
RX Received Bit Count	6.581E012	6.580E012	6.592E012	6.592E012
RX Bit Error Count	0.000E000	0.000E000	0.000E000	0.000E000
BERT Reset	Reset	Reset	Reset	Reset
Clocking Settings				
TXOUTCLK Freq (MHz)	50.02	50.02	50.02	50.02
TXUSRCLK Freq (MHz)	50.02	50.02	50.02	50.02
TXUSRCLK2 Freq (MHz)	50.02	50.02	50.02	50.02
RXRECCLK Freq (MHz)	50.02	50.02	50.02	50.02
RXUSRCLK Freq (MHz)	50.02	50.02	50.02	50.02
RXUSRCLK2 Freq (MHz)	50.02	50.02	50.02	50.02

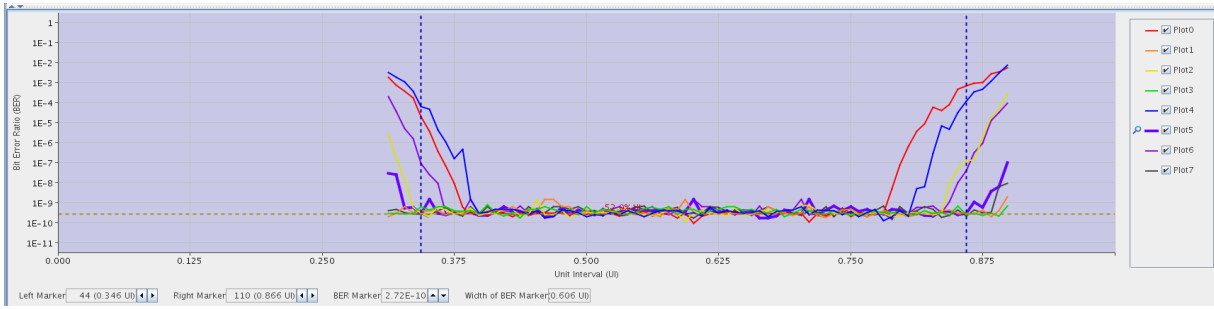
ice 2 Unit 1_0: Cable is LOCKED. Retrying...

RT Data path tests: MGT TX/RX

- Loopback tests set up one MiniPod at the time on TX (Base function) and RX (Topo function).
- Tested MP1 → MP3 and MP2 → MP5 transmission with minimal adjustment to GTX and default MP settings
- Initial parameter scan 'bathtub curves'



Error inserted on purpose



RT Data path tests: LVDS

- Test set up in parallel to Backplane data transmission.
- Pre-defined 80 Mbps DDR source-synchroneous stress patterns sent
  - RTM 1,2 → 3
  - CTP1 (driven by BF) → CTP2
    - received on both BF and TP FPGA's
- 2.5m cable RTM
- 9.5m cable CTP
- Parity monitored using chipscope ~1hr no errors

FPGA configuration, VME R-W tests, TTC timing adjustment

- Initial problems with JTAG configuration solved – able to reliably configure FPGAs and BSPT PROM
- CF configuration not yet achieved
- Registers implemented on BSPT stress tested
  - Random writes and reads at ~10 Hz rate.
- Registers implemented on BF tested but need a stress test
- Registers on TP failed initial test (suspect FW implementation, timing etc)
- TTC Dskw1 adjustment control via VME

Major TODO's: RT

- MP4 gigabit data reception
- LVDS in other directionalities
- Base-Topo communication
- Timing delay calibration
- TTC signal reception (BC reset, L1A...)

Major TODO's: 'Services'

- MP, SFP monitoring and control
- CAN

Immediate next steps

- Backplane full crate test preparation 6-14 Mar.
- Anticipating CMX SN 01 arrival early next week.
- Hope for SN 02 arrival following week.
- Work in B104 next week.

Lookout for next few weeks

- Propose and agree on complete list of tests for the PRR
- Work with respective experts to schedule 'pairwise' tests:
  - Topo
  - Glink
  - CTP