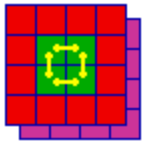
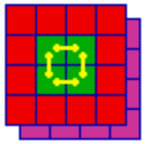


CMX Hardware Overview

Chip Brock, Dan Edmunds, Philippe Laurens@MSU
Yuri Ermoline @CERN
Wojciech Fedorko @UBC

Michigan State University
19-May-2014

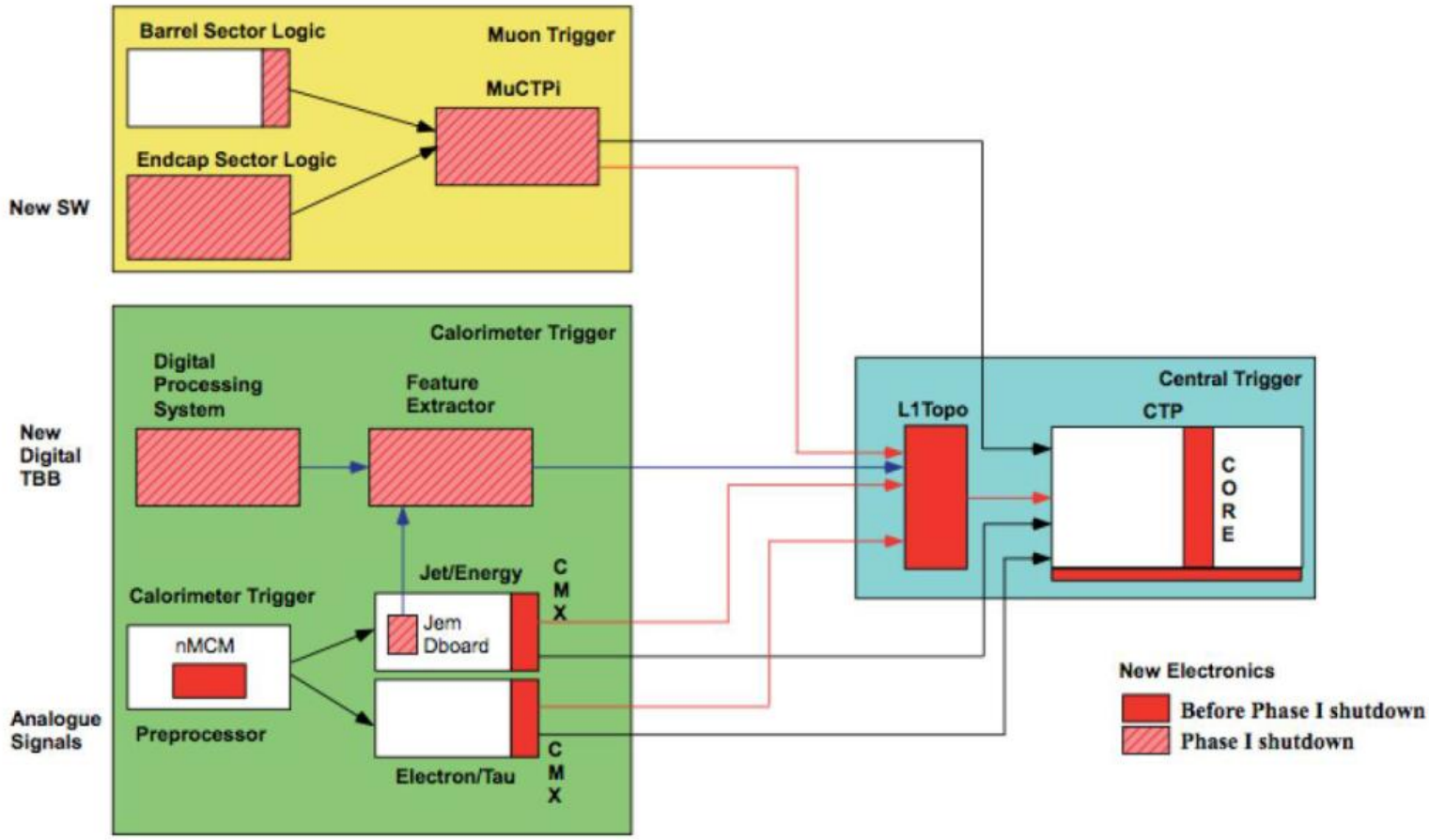
MICHIGAN STATE
UNIVERSITY



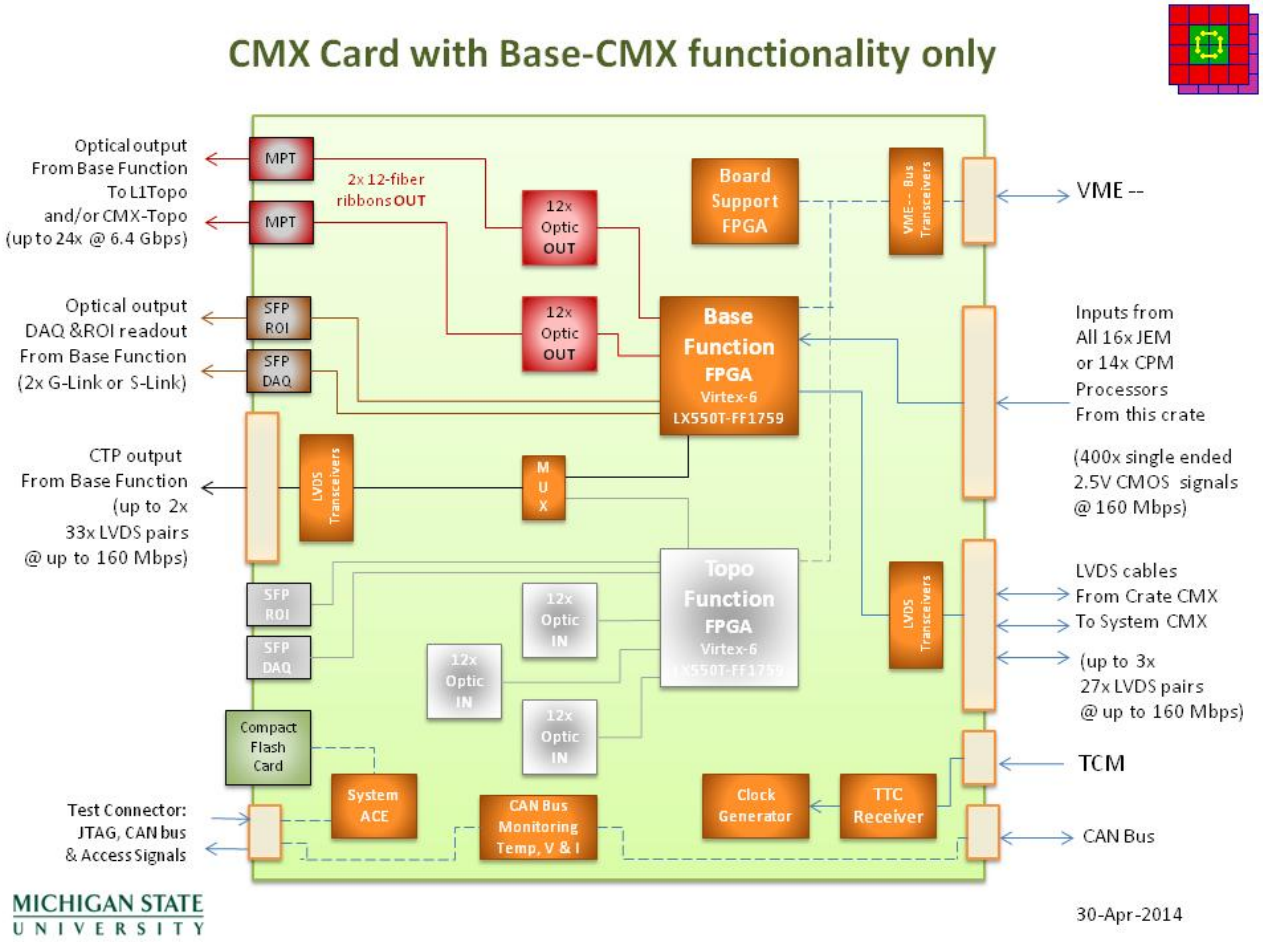
Overall project CMX HW/FW/SW

- Design Efforts in parallel on 5 fronts:
  - MSU : CMX hardware
    - Raymond Brock, Dan Edmunds, Philippe Laurens
  - CERN : VAT card, BSPT FPGA firmware, CANbus tests
    - Yuri Ermoline
  - CERN : CMX software
    - Duc Bao Ta
  - UBC : BF FPGA firmware
    - Wojtek Fedorko
  - Stockholm : BF FPGA firmware, TP FPGA test firmware, JEM test firmware
    - Pawel Plucinski

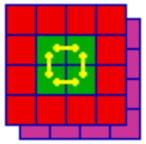
CMX is part of L1calo Phase 0 upgrade



- CMX == L1Calo Trigger replacement for current Common Merger Module (CMM)
  - Phase-I accelerated item a.k.a. Phase-0



- The **CMX was designed to**:
  1. Perform all tasks currently handled by any CMM in L1calo (Electron, Tau, Jet, Energy)
  2. Extend these CMM tasks to higher input and output line rates
  3. Offer more computing power for additional thresholds or algorithms using this extended input
  4. Become an input to L1topo, sending raw or processed copies of its own inputs optically at 6.4Gb
  5. Provide optional functionality to perform Topological Processing on the CMX platform, if needed



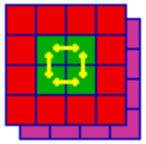
Definition: **CMX Base Function**

- **Extended CMM functionality** (Crate CMXs and System CMXs)
  - Receive and process 400 JEM/CPM input signals **(@4x CMM rate)**
  - All **Crate CMXs** send local summary to their **System CMX** through backplane connectors over LVDS cables (plan is @2x CMM rate)
  - System CMXs form and **send triggering information to CTP** over LVDS cables (plan is no change from CMM rate)
  - all CMXs send **ROI and DAQ** information over **G-links** (same as CMM)

- **Source of data for L1topo: send CMX inputs** from JEMs or CPMs
  - Using 2x Avago miniPOD optical transmitters and **2x 12-fiber ribbons**
  - Some level of **duplication** is required (originally **2x copies, now 4x**)
  - One 12-fiber ribbon **@6.4Gbps** sufficient to send all raw input data

    But plan is to send zero-suppressed data on **2,6 or 8x fibers** per copy

    → **optical patch panel** is required between 12x CMXs and L1topo



Definition: **CMX-Topo Function**

- Limited **Topological Processing** capability **on CMX** platform
  - Receive optical inputs from some/all of the 12x CMXs using 3x Avago receivers for up to 36x input fibers
  - Run multiple Topological Algorithms
  - Send Topological Triggering Information to CTP
  - Able to act as its own ROD for DAQ and ROI readout → support both G-link and S-link

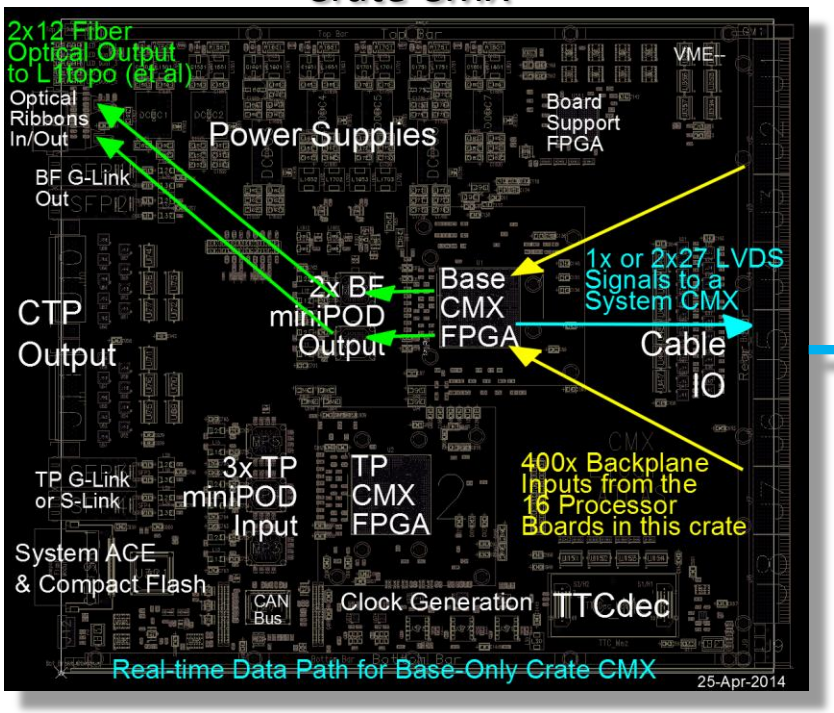
- The CMX-Topo function was requested as a **backup plan** in case L1topo could not be built, or if its availability had been delayed.
- A CMX-Topo system will **most likely not be used in L1calo**
- Somebody may devise an **alternate and creative usage** for the TP FPGA, or its role may remain limited to testing BF optical outputs in the test stand.

- CMX-Topo input used to **test Base Function optical output**

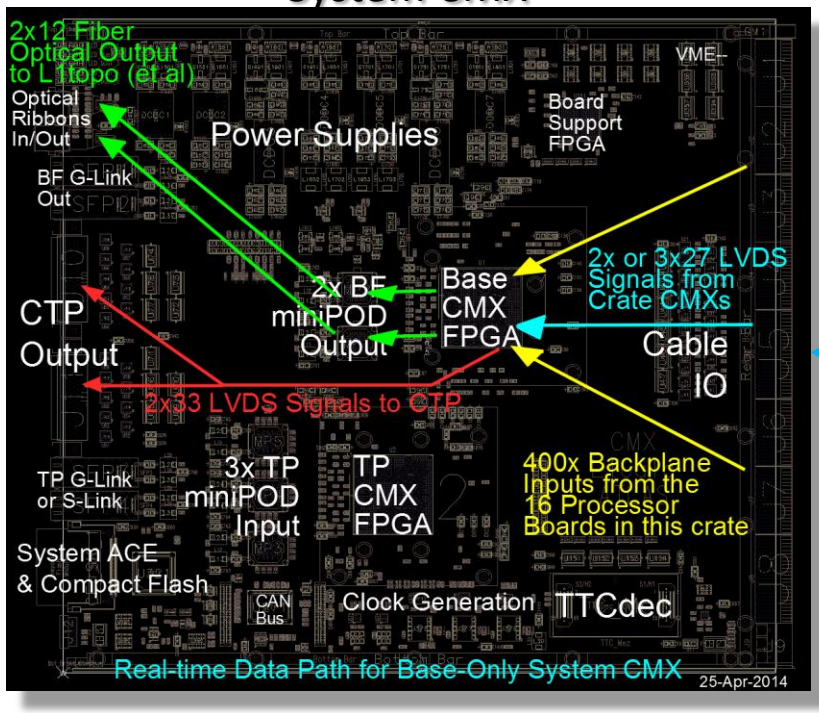
CMX connectivity

❑applies to electron, Tau, Energy or Jet data types

Crate CMX



System CMX



❑ Merger Cables

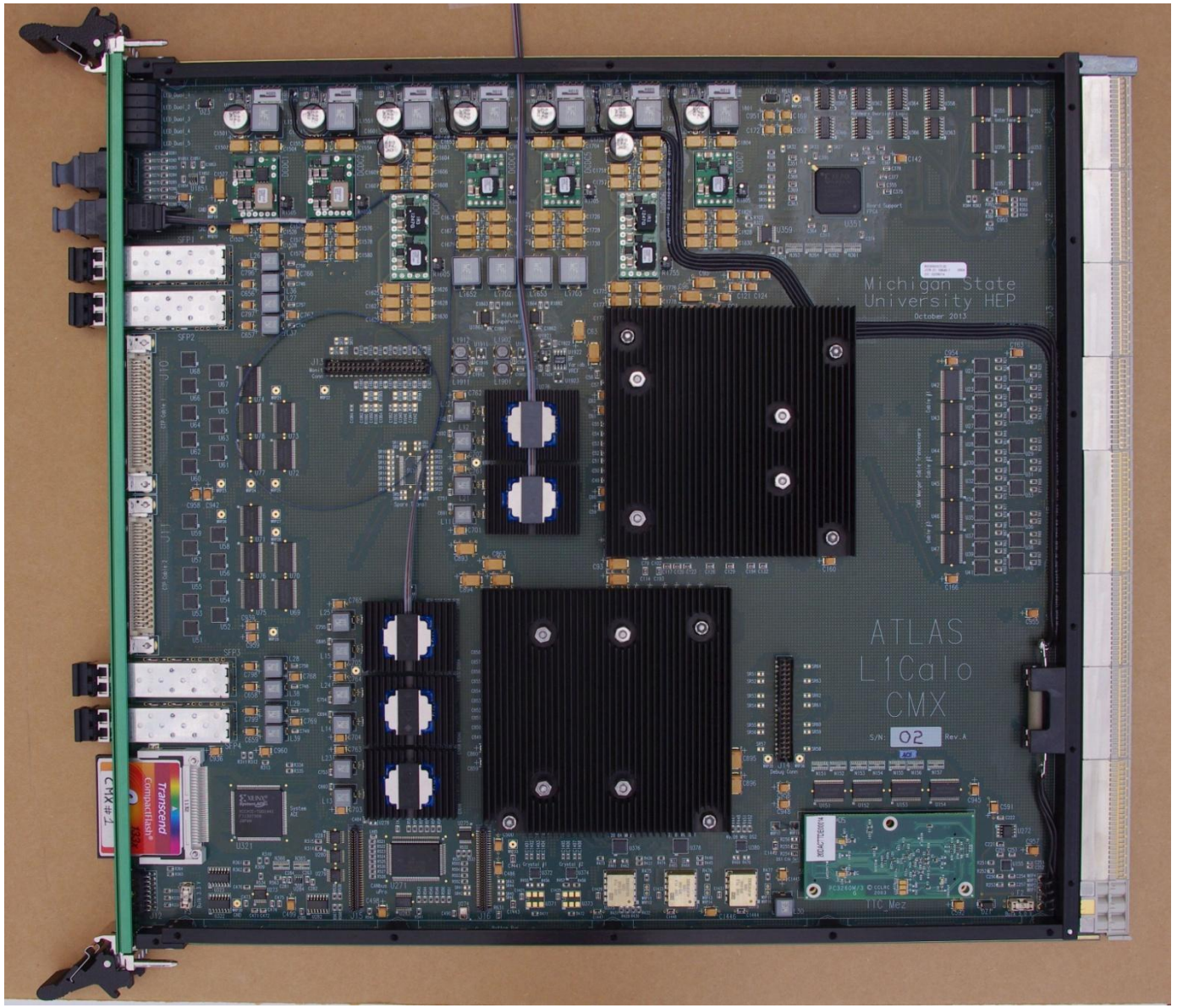
➢from one of more Crate CMX

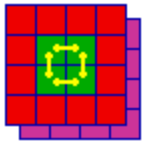
➢ To its System CMX

❑ All 12x CMXs in L1calo forward their inputs to L1topo

❑ Only the 4x System CMXs send info to CTP

Common Merger eXtended module (CMX)

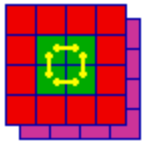




CMX Project Evolution

- **Preliminary Design Review** Stockholm (June 2011)
  - Initial Specification
- **Design Study** → **Technical Workshop** @RAL (Feb 2012) :
  - Additional decisions:
    - Use 2x separate FPGAs: Base Function in BF FPGA and Topo Function in TP FPGA
    - 2x 12-fiber outputs from BF FPGA to L1topo
    - 3x 12-fiber inputs to TP FPGA
- **Prototype Design Review** (March 2013)
  - Some corrections
  - Some added requirements
- Final Informal Prototype **Mini Review** (Oct 2013):
  - Final check: all needed functionality has been included

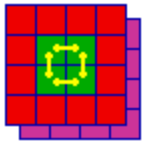
➢ **Production Design Review** **(12-May-2014):**
  - **One last test requested**: all 24x 6.4 Gbps optical outputs simultaneously



CMX Hardware Schedule

- 2013: **Prototype fabrication**
  - March: CMX Prototype Readiness Review
  - Apr-Nov: PCB design and layout
  - October: Final Mini-Review
  - Dec-Jan 2014: Fabrication of **4x CMX prototypes**

- 2x prototypes with TP FPGA
- 1x prototype without TP FPGA
- 1x prototype with no TP and no BF FPGA



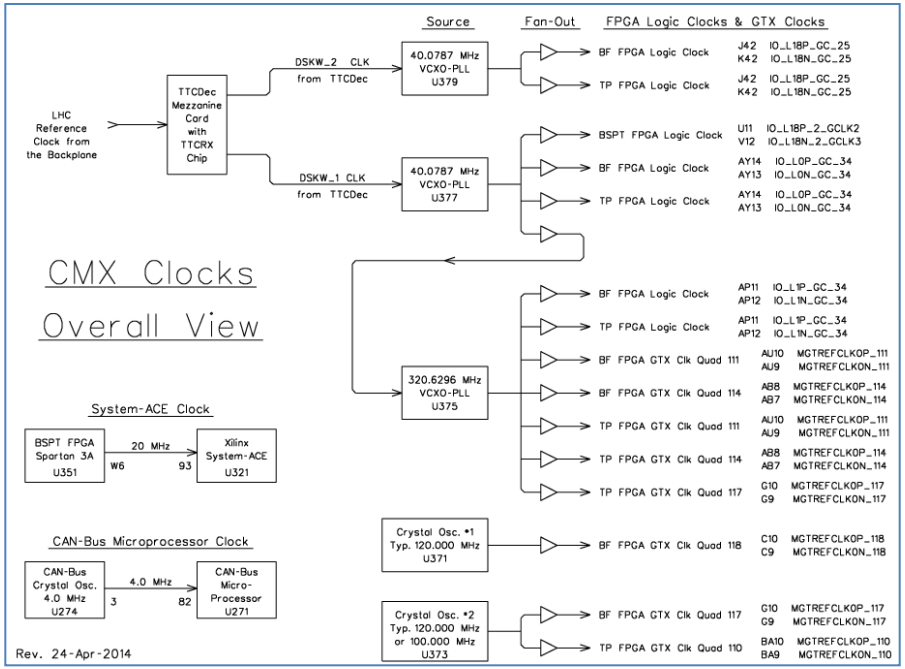
CMX Hardware Schedule

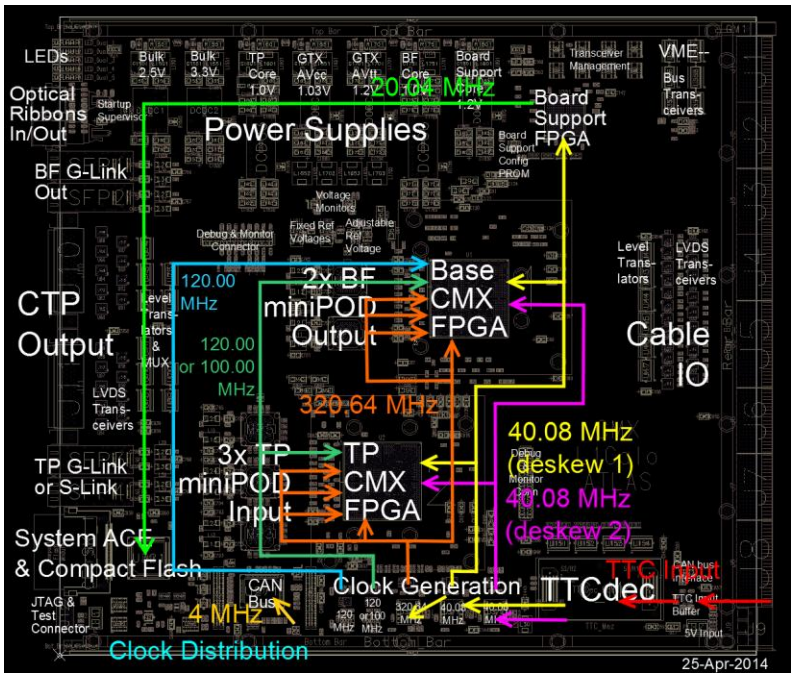
- 2014: Prototype Tests / Production Boards / System & Integration Testing
  - February: **First tests at MSU:**
    - Power Supplies, clocks, FPGA configuration, VME-- bus access.
    - Backplane Input Tests using 2 JEMs in MSU L1calo test crate.
    - **Loopback Tests: LVDS** Merger Cables & CTP output, **Optical** SFP & MiniPOD outputs.
  - Mar-Apr: Testing continues **in parallel at MSU and CERN** (bldg 104, USA15)
    - JEP and CP **Full-crate backplane tests** (USA15)
    - Integration tests to CTP, ROD, and L1Topo

❖ **No hardware problem found** with prototype CMX boards
→ **no changes needed** for production CMX boards
→ 20x Bare circuit boards being manufactured now (4 weeks)
❖12-May-2014: **Production Readiness Review**
→ Start assembly right after the panel's "go ahead"
❖ **3 weeks later: 20x production CMX** boards (2x with TP)

  - June: Final Assembly and Tests at MSU of **first 4 production CMX**
    - Sent to CERN in time for participation in **M4** (July 7-11)
  - Jun-July: Final Assembly and test of rest of CMX production boards
    - Sent to CERN in time for participation in **M5** (Sept 8-12)

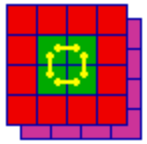
Documentation available on the CMX website



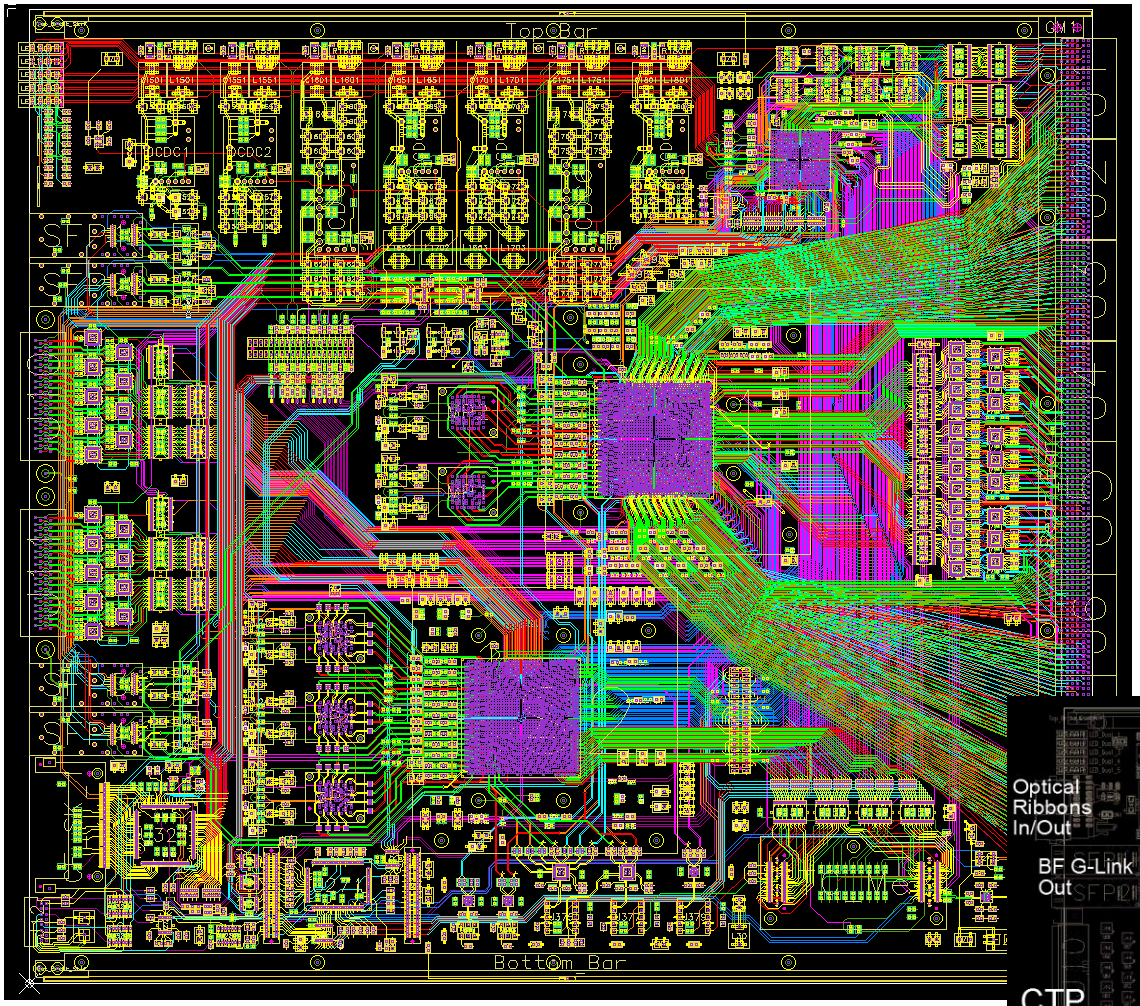


http://www.pa.msu.edu/hep/atlas/l1calo/

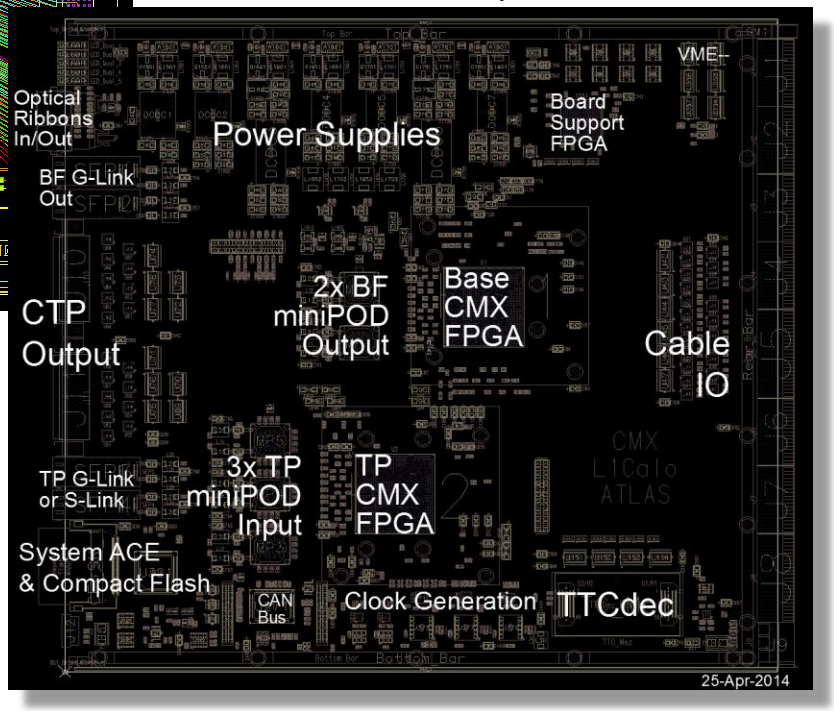
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/block_diagrams/
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/specification/4_production_design_review/



(Extra Slides)



- Two Virtex 6 LX550T
  - Base Function FPGA
  - Topo Processing FPGA (not installed)
- One Spartan 3a
  - Board Support FPGA
- 10x power supplies
  - 7x DC-DC supplies
  - 2x fixed reference
  - 1x variable reference
- 5x clock distribution networks
  - 2x 40.08 MHz from TTCdec
  - 1x 320.64 MHz (for 6.4Gb I/O)
  - 2x fixed freq (for G-link or S-link)



- 22x layer circuit board
  - 9x signal layers (5x with 60 Ohm traces)
  - 3x power fill layers
  - 10x ground plane layers
  - blind vias through top L1-L6 for Gb traces

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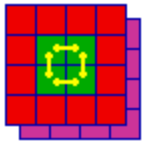


Production CMX Testing Plans

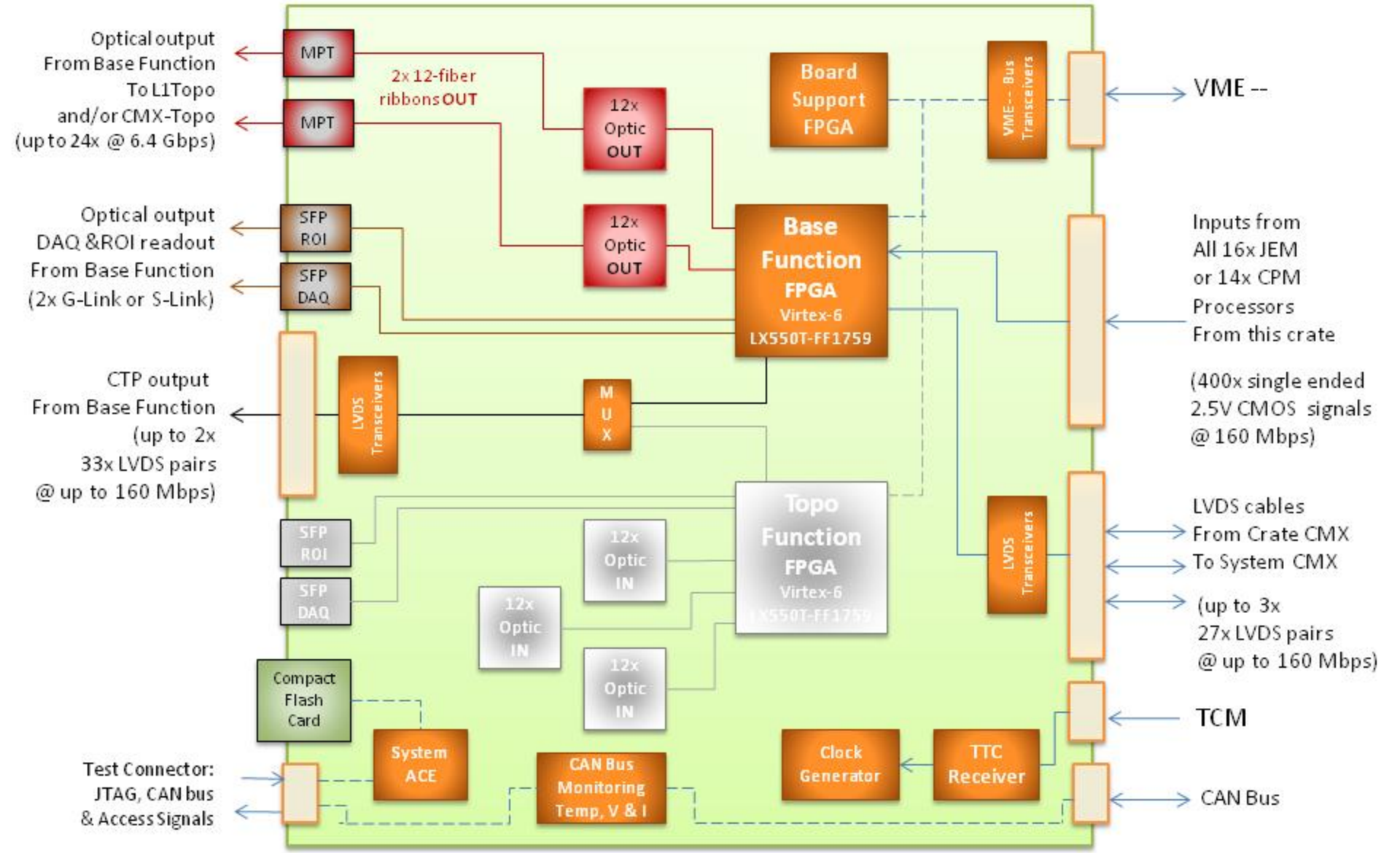
- At MSU: Test Physical paths before shipping to CERN
  - Final Assembly

    Resistors & jumpers , stiffener bars & front-panel, power wiring & fuses, miniPODs & fibers, Heat sinks, …
  - Check Power Supplies, Clocks
  - Check FPGA configuration, VME-- bus access to BSPT
  - Loopback Tests and Production-CMX to Reference-CMX Tests
    - Merger Cables, CTP output
    - Optical outputs from Base Function: SFP and MiniPOD (IBERT tests)

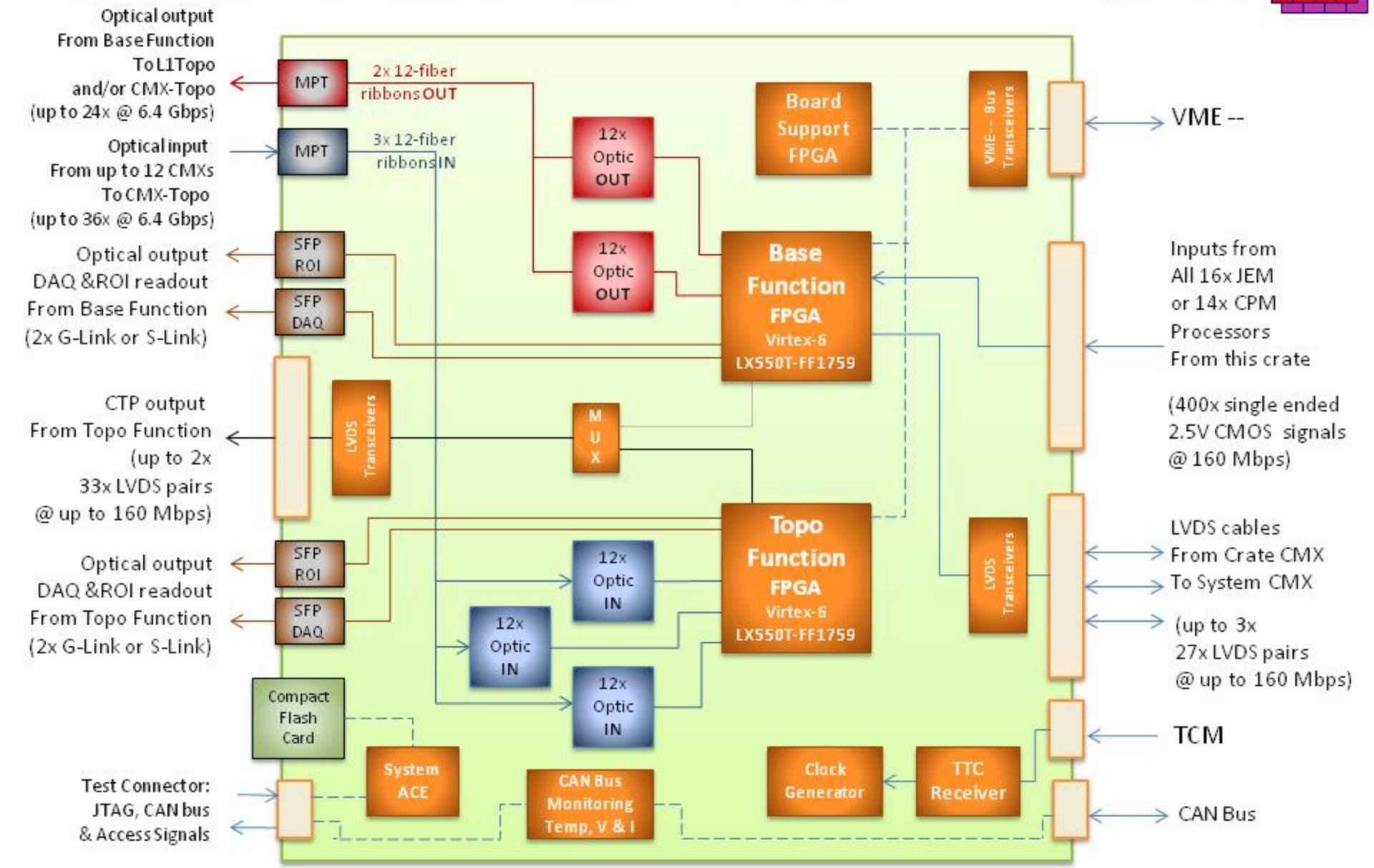
      Record MiniPODs optical power output (self-reported & received)
  - 400x Backplane inputs: test using 2x JEMs currently at MSU
- At CERN (Bldg 104) : System Level Tests
  - Final tests before installation in USA15 (or test stands)

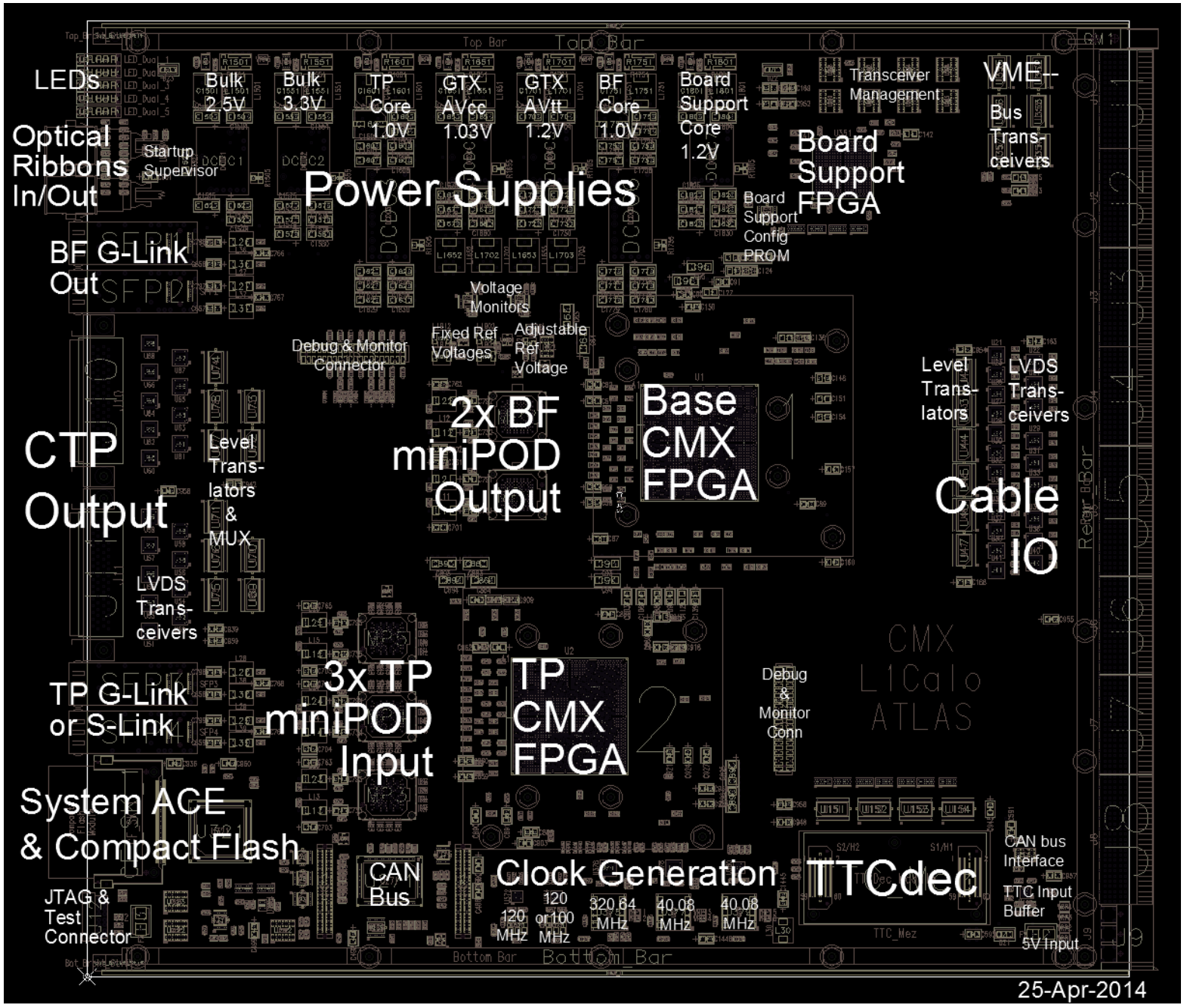
    or before storage as known good spares

CMX Card with Base-CMX functionality only



CMX Card with Base-CMX functionality and TP-CMX capability




LEDs
Optical Ribbons In/Out
Startup Supervisor
Bulk 2.5V
Bulk 3.3V
TP Core 1.0V
GTX AVcc 1.03V
GTX AVtt 1.2V
BF Core 1.0V
Board Support Core 1.2V
Power Supplies
Transceiver Management
VME--
Bus Trans-ceivers
Board Support FPGA
Board Support Config PROM
BF G-Link Out
Voltage Monitors
Debug & Monitor Connector
Fixed Ref Voltages
Adjustable Ref Voltage
2x BF miniPOD Output
Base CMX FPGA
Level Trans-lators
LVDS Trans-ceivers
Cable IO
CTP Output
Level Trans-lators & MUX
LVDS Trans-ceivers
TP G-Link or S-Link
3x TP miniPOD Input
TP CMX FPGA
Debug & Monitor Conn
CMX LICalo ATLAS
System ACE & Compact Flash
CAN Bus
Clock Generation
120 MHz
120 or100 MHz
320.64 MHz
40.08 MHz
40.08 MHz
TTCdec
CAN bus Interface
TTC Input Buffer
5V Input
JTAG & Test Connector
25-Apr-2014

L1topo will receive Zero-Suppressed data from all CMXs