CMX – prototype testing

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Outline of CMX tests

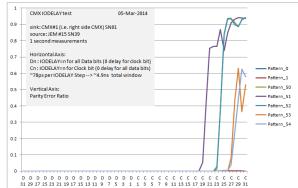
- 4 Prototypes produced:
 - 1 without Virtex 6 parts: SN0 (@CERN)
 - 2 with both Virtex 6 parts on: SN1 (@CERN), SN2 (@MSU)
 - 1 with only 'Base Function' (standard configuration): SN3 (@CERN, USA 15)
- Prototypes arrived early Feb
- RT and readout path testing commenced after final assembly and checkout.
 - MSU 2nd half of Feb
 - CERN b. 104 most of March
 - CERN USA 15 last week of March-mid April.
 - Back to CERN b.104 till now. One CMX left installed at USA15

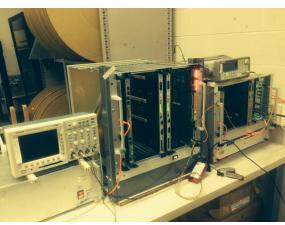
Accomplished during Feb MSU testing:

- All RT/readout interfaces tested to some level, some tests superseded/extended:
 - Backplane tests:
 - 2 JEMs
 - Static patterns
 - Pre-defined patterns
 - First IO-delay scans



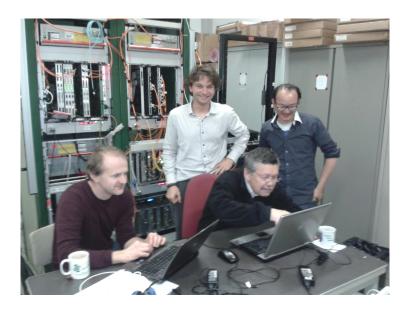
- 'Slow' optical link tests using IBERT \rightarrow Pawel's talk
- 'Fast' optical link tests using IBERT
 → later in this talk
- LVDS link tests \rightarrow later in this talk





March: preparation for full crate tests

- B 104 test rig.
- Debugging FW with on-the fly data checking
- Testing/debugging JEM FW (mostly SumET)
 - Extension of functionality: PRBS
- Testing the CPM FW
- Final preparation and debugging of the software tools





RT Data path tests: LVDS, MSU

- Pre-defined 80 Mbps DDR source-synchroneous stress patterns sent
 - Coherent pulses '1' and '0', switching data.
 - RTM 1,2 → 3
 - CTP1 (driven by BF) \rightarrow CTP2
 - received on both BF and TP FPGA's
- 2.5m cable RTM
- 9.5m cable CTP
- IO pins configured for 6 mA drive strength
- Parity monitored using chipscope ~1hr no errors (~10 min RTM 1 \rightarrow 3)

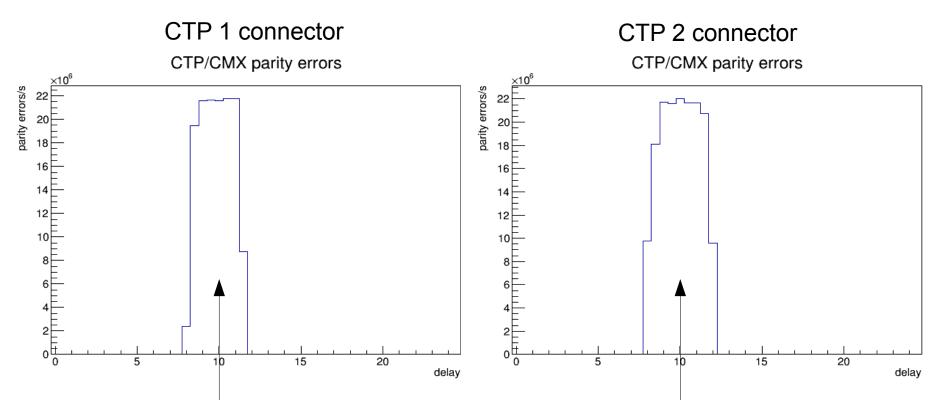
RT Data path tests: LVDS CMX \rightarrow CTP, USA 15

- CMX configured to provide on both CTP output connectors selectable data at 40 Mbps:
 - Stress pattern, 1 orbit long:
 - Walking 1's, walking 0's
 - Coherent pulses '1', and '0'
 - Pulses on selected bits,
 - Switching data (F's and 0's, A's and 5's)
 - Pseudorandom data
 - Array of LFSRs
 - Odd parity preserved

RT Data path tests: LVDS CMX \rightarrow CTP, USA 15

- CTP:
 - Can compare incoming data bit-by-bit against a known sequence (at low frequency)
 - Flag parity errors
 - Adjust timing of incoming signals
- No errors observed in stress pattern running in:
 - 121M events in data from CTP 2
 - 48M events from CTP1
- No parity errors in half hour of pseudo-random data runs
- Logic inverted on all bits

LVDS CMX \rightarrow CTP Link characterisation: 'bathtub'



Invalidity range explained by transition timing differences signal jitter very low <0.2 ns

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RT Data path tests: High Speed Links MSU, CERN, loopback configuration

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- 'IBERT' cores
 - Test a single Minipod (12 channels) pair at a time
 - Tests up to several days (shortest MP2 \rightarrow MP5 30 min)
 - BER 3E-16 reached
 - Two pigtails and 6 ft fibre bundle optical path
 - Standard termination coupling, default TX/RX parameters

	GTX_X0Y12	GTX_X0Y13		GTX_X0Y14	т	GTX_X0Y15		GTX_X0Y16		GTX_X0Y17		GTX_X0Y18		GTX_X0Y19		GTX_X0Y20		GTX_X0Y21		GTX_X0Y22		GTX_X0Y23
MGT Settings																			T			
MGT Alias	GTX0_113	GTX1_113		GTX2_113		GTX3_113		GTX0_114		GTX1_114		GTX2_114		GTX3_114		GTX0_115		GTX1,115	T	GTX2_115		GTX3_115
Tile Location	GTX_X0Y12	GTX_X0Y13		GTX_X0Y14		GTX_X0Y15		GTX_X0Y16		GTX_X0Y17		GTX_X0Y18		GTX_X0Y19		GTX_X0Y20		GTX_X0Y21		GTX_X0Y22		GTX_X0Y23
MGT Link Status	6.413 Gbps	6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbp
MGT Edit Line Rate	6.413 Gbps	6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbps		6.413 Gbp
TX PLL Status	LOCKED	LOCKED		LOCKED		LOCKED		LOCKED		LOCKED		LOCKED		LOCKED		LOCKED		LOCKED		LOCKED		LOCKED
RX PLL Status	LOCKED	LOCKED		LOCKED		LOCKED		LOCKED		LOCKED		LOCKED		LOCKED		LOCKED		LOCKED		LOCKED		LOCKED
Loopback Mode	None	None	-	lone	- 1	None	-	None	-	None	-	None	-	None	-	None	-	None		lone	 No 	one
Channel Reset	Reset	Reset		Reset		Reset		Reset		Reset		Reset		Reset		Reset		Reset		Reset		Reset
TX Polarity Invert																						
TX Error Inject	Inject	Inject		Inject		Inject		Inject		Inject		Inject		Inject		Inject		Inject		Inject		Inject
TX Diff Output Swing	590 mV (0110)	590 mV (0110)	v 5	90 mV (0110)	- 1	590 mV (0110)	-	590 mV (0110)	-	590 mV (0110)	-	590 mV (0110)	-	590 mV (0110)	-	590 mV (0110)	-	590 mV (0110)	. 59	90 mV (0110)	- 59	0 mV (0110)
TX Pre-Emphasis	0.15 dB (0000)	0.15 dB (0000)	- 0	15 dB (0000)	-	0.15 dB (0000)	-	0.15 dB (0000)	-	0.15 dB (0000)	-	0.15 dB (0000)	-	0.15 dB (0000)	-	0.15 dB (0000)	-	0.15 dB (0000)	. 0.	.15 dB (0000)		15 dB (0000)
TX Post-Emphasis	0.18 dB (00000)	0.18 dB (00000)	-	18 dB (00000)	- 0	0.18 dB (00000)	¥	0.18 dB (00000)		0.18 dB (00000)	-	0.18 dB (00000)	-	0.18 dB (00000)	-	0.18 dB (00000)	-	0.18 dB (00000)		.18 dB (00000)	• 0.	18 dB (00000)
RX Polarity Invert																						
RX AC Coupling Enable	×	×		2		×		R		×		2		¥		V		¥		P		×
RX Termination Voltage	MGTAVTT *	MGTAVTT *	- h	IGTAVTT *	- 1	NGTAVTT *	-	NGTAVTT *	-	MGTAVTT *	-	MGTAVTT *	-	MGTAVTT *	-	MGTAVTT *	-	MGTAVTT *	• M	IGTAVTT *	M	STAVTT *
RX Equalization	0	0	-		-	0	¥	0		0	v	0	v	0	-	0	-	0	0		- 0	
DFEEYEDACMON	154.8 mV	148.4 mV		180.6 mV		200.0 mV		148.4 mV		148.4 mV		193.5 mV		161.3 mV		187.1 mV		167.7 mV		187.1 mV		167.7 m
DFETAPOVRD	R							R		×				¥		×		V		P		×.
DFET AP 1	0	0	- 0		- [0	-	0	-	0	-	0	-	0	-	0	-	0	- 0		- 0	
DFET AP2	0	0	-		- 0	0	¥	0	-	0	v	0	-	0	-	0	-	0	0		- 0	
DFET AP3	0	0	-		- 0	0	-	0	Ŧ	0	V	0	V	0	-	0	-	0	0	2	• 0	
DFETAP4	0	0	-		-	0	-	0	-	0	-	0	-	0	-	0	-	0	. 0		- 0	
RX Sampling Point	0.598 UI	0.5	98 UI ·	76 0.598	UI		8 UI	760.	598 UI		98 UI	0.5	98 UI		8 UI		3 UI	0.598 U	JI -	76 0.598	ui –	- 76
BERT Settings																						
TX Data Pattern	PRBS 7-bit	PRBS 7-bit	▼ P	RBS 7-bit	•	PRBS 7-bit	¥	PRBS 7-bit		PRBS 7-bit	v	PRBS 7-bit	v	PRBS 7-bit	-	PRBS 7-bit	•	PRBS 7-bit	· F	RBS 7-bit	 PR 	BS 7-bit
RX Data Pattern	PRBS 7-bit	PRBS 7-bit	- P	RBS 7-bit	-	PR8S 7-bit	-	PR8S 7-bit	-	PR8S 7-bit	-	PRBS 7-bit	-	PR8S 7-bit	-	PRBS 7-bit	-	PRBS 7-bit	· PF	RBS 7-bit	PR	185 7-bit
RX Bit Error Ratio	2.893E-016	2.893E-016		2.893E-016		2.893E-016		2.896E-016		2.893E-016		2.893E-016		2.896E-016		2.893E-016		2.893E-016		2.893E-016		2.893E-0
RX Received Bit Count	3.456E015	3.456E015		3.456E015		3.456E015		3.453E015		3.456E015		3.456E015		3.454E015		3.456E015		3.456E015		3.456E015		3.456E0
RX Bit Error Count	1.000E000	1.000E000		1.000E000		1.000E000		1.000E000		1.000E000		1.000E000		1.000E000		1.000E000		1.000E000		1.000E000		1.000E00
BERT Reset	Reset	Reset		Reset		Reset		Reset		Reset		Reset		Reset		Reset		Reset		Reset		Reset
Clocking Settings																						
TXOUTCLK Freq (MHz)	321.42	321.42		321.42		321.42		321.42		321.42		321.42		321.42		321.42		321.42		321.42		320.66

RT Data path tests: High Speed Links CERN, CMX \rightarrow L1Topo

- 'IBERT' cores again
- First tests with simple optical path from both CMX's MPs
 - ~ ~30 minutes BER 3E-14
- Transmission from one MP tested via optical path:
 - Pigtail → barrel → breakout → barrel → **splitter** → rebundler → barrel → 10m bundle → barrel → pigtail
 - No errors; BER measured to 1E-14
 - Bathtub > 50% open
- Tests pending:
 - Realistic formatted data



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RT Data path tests: High Speed Links

CMX Base \rightarrow CMX Topo function 24 links

Realistically formatted data (before 8b/10b encoding):

$\langle \text{ctr} \rangle \langle \text{ctr} \rangle \langle \text{ctr} \rangle$	ctr / ctr	∕ ctr ∕	ctr	ctr 15:12 CRC
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- ctr is a 40 Mhz, 16-bit counter
- Alignment event including K28.5 sent every ~4k events
- Same data sent over all 24 channels
- ctr repeated on 7 words but recall data is encoded; disparity
- No TX buffer; RX elastic buffer on
- Noise generation:
 - 80 Mbps stress pattern sent on RTM 1,2,3 (drive 12 mA)f
 - 40 Mbps stress pattern sent on CTP 1,2 (drive 6 mA)
- Errors monitored: not in table, disparity, crc, byte and event alignment
- Error flag sent back to BF; Chipscope core triggered on BF
- Chipscope monitoring on all 24 channels on TP (but clumsy)
- 8 errors in >12 hrs all on the same channel.
- Startup procedure FW needs debugging

So far so good:

- All tests so far satisfactory!
- Up next:
 - Duc: Backplane test
 - Pawel 'Slow' optical interfaces

Backup

LVDS CMX \rightarrow CTP Link characterisation: transition timing

CTP 1 connector

signal number	signal name	TDC phase (ns)	TDC phase RMS (ns)	signal number	signal name
0	SIG 00	11.43	0.14	0	SIG00
1	SIG01	13.10	0.13	1	SIG01
2	SIG02	11.87	0.16	2	SIG02
3	SIG03	12.26	0.15	3	SIG03
4	SIG04	11.54	0.16	4	SIG04
5	SIG05	11.13	0.18	5	SIG05
6	SIG06	11.62	0.19	6	SIG06
7	SIG07	11.16	0.15	7	SIG07
8	SIG08	12.67	0.15	8	SIG08
9	SIG09	12.11	0.13	9	SIG09
10	SIG10	11.23	0.13	10	SIG10
11	SIG11	12.46	0.15	11	SIG11
12	SIG12	12.05	0.18	12	SIG12
13	SIG13	12.92	0.19	13	SIG13
14	SIG14	12.82	0.18	14	SIG14
15	SIG15	12.77	0.19	15	SIG15
16	SIG16	11.47	0.14	16	SIG16
17	SIG17	11.83	0.22	17	SIG17
18	SIG18	12.13	0.17	18	SIG18
19	SIG19	12.72	0.12	19	SIG19
20	SIG20	12.12	0.17	20	SIG20
21	SIG21	10.90	0.17	21	SIG21
22	SIG22	12.67	0.12	22	SIG22
23	SIG23	11.87	0.14	23	SIG23
24	SIG24	11.14	0.17	23	SIG23
25	SIG25	12.09	0.13	25	SIG25
26	SIG26	11.03	0.16	25	SIG25 SIG26
27	SIG27	10.55	0.15	20	SIG20 SIG27
28	SIG28	10.54	0.17	28	SIG27 SIG28
29	SIG29	10.61	0.19	28 29	SIG28 SIG29
30	SIG30	13.43	0.26	30	SIG29 SIG30
31	CLK	3.13	0.05	31	CLK
32	PAR	13.63	0.11		
		10100	~	32	PAR

CTP 2 connector

gnal number	signal name	TDC phase (ns)	TDC phase RMS (ns)
0	SIG00	12.74	0.15
1	SIG01	12.40	0.20
2	SIG02	13.15	0.17
3	SIG03	12.27	0.17
4	SIG04	12.79	0.15
5	SIG05	12.75	0.16
6	SIG06	13.00	0.17
7	SIG07	11.22	0.12
8	SIG08	12.34	0.16
9	SIG09	11.42	0.15
10	SIG10	12.12	0.16
11	SIG11	12.01	0.18
12	SIG12	13.39	0.16
13	SIG13	12.36	0.17
14	SIG14	11.68	0.18
15	SIG15	12.44	0.16
16	SIG16	11.76	0.14
17	SIG17	12.49	0.18
18	SIG18	12.99	0.15
19	SIG19	12.21	0.17
20	SIG20	11.80	0.14
21	SIG21	10.72	0.14
22	SIG22	11.91	0.17
23	SIG23	12.86	0.11
24	SIG24	12.36	0.10
25	SIG25	11.80	0.12
26	SIG26	10.85	0.13
27	SIG27	9.89	0.14
28	SIG28	10.82	0.17
29	SIG29	10.99	0.16
30	SIG30	13.57	0.20
31	CLK	3.21	0.10

14.12

0.13

RT Data path tests: High Speed Links $CMX \rightarrow L1Topo$, bathtubs w/splitter

