CMX status

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Hardware Status

- Four production + two fully functional prototype CMX's delivered to CERN
- Four CMX installed in JEP0 and JEP1 crates
- Further boards assembly and production testing on-going.



Firmware Status

- Firmware provided for 'M4'
 - BSPT close to final
 - Jet:
 - Thresholding in ½ of the system
 - Basic DAQ readout
 - No Crate-System integration.
 - Dark fibers to topo.
 - SumET:
 - Basic DAQ readout (backplane)

Software Status

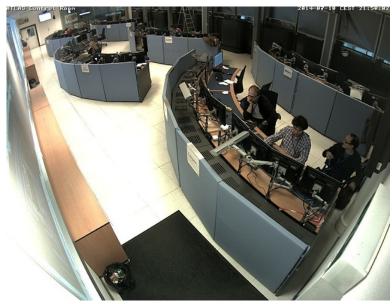
- Simulation
 - CMX Jet:
 - Jet thresholding and summing complete (CTP output)
 - Tested together with HW/FW in the lab
 - CMX ET Sum:
 - Summing done
 - Thresholding nearly complete.
- Services
 - Configuration and control
 - BSPT FPGA control done
 - Base function FPGA control reflects current FW status
 - Backplane timing
 - Standalone version done (supports specialised test FW)
 - Integrated version in-progress
 - DSKW1 timing
 - In progress
 - Offsets, BCID timing support
 - In developement

M4 activities

- Basic thresholding/summing:
 - Tested with playback form JEMs, readout from the CTP
 - 3 bit sums correct
 - 2 bit sums incorrect
 - Triggerring in cosmics not understood (very high rates)
 - Tile pulser triggering not understood (triggers in all BCs)
- Readout:
 - Tests in lab with RODs
 - Format correct (backplane data dump, parity, BCID)
 - Offset settings not tuned
 - Achieved 105 kHz L1A rate random trigger in a combined partition (complex dt limited)
 - Single slice

M4 post-mortem and plans: FW/SW

- M4 postmortem:
 - Understand 2-bit summing discrepancies
 - Understand different behavior with playback data and cosmics/ laser pulser
 - Readout/BCID offset setting procedure to be deployed
- Additional Jet FW to support debugging to be developed soon
 - Spy memories on CTP output
- Finish development of the Jet System and Crate FW:
 - System crate IO pipelines and spy memories
 - Full eta-dependent thresholding
 - System spy memories for DSKW1 timing support



Conclusions

- Big progress during M4
 - CMX functionality exercised in combined ATLAS run:
 - Backplane capture and decoding
 - Thresholding, summing, CTP output
 - Readout to RODs
 - Seven functional CMXs, Four in USA 15
 - EM CMXs installation expected by M5
 - FW debugging and development underway
 - SW and operational procedures in good shape reflecting the FW status.