EDMS Number: ATL-DA-ER-0030

EDMS Id: **1150213**

ATLAS Level-1 Calorimeter Trigger

CMX module

Project Specification

Document Version:	0.8
Document Date:	23 June 2011
Prepared by:	L1Calo CMX collaboration

Document Change Record

Version	Issue	Date	Comment
0	0	11 February 2011	Initial draft by Yuri Ermoline
0	1	25 February 2011	Comments from Jim Linnemann
0	2	26 April 2011	VME addresses, data formats
0	3	27 May 2011	Comments from Ulrich Schäfer and Ian Brawn, CMX
0	4	08 June 2011	Comments and corrections from Samuel Silverstein
0	5	14 June 2011	Comments from Dan Edmunds and Ulrich Schäfer
0	6	15 June 2011	Comments from Philippe Laurens
0	7	22 June 2011	Comments from Hal Evans
0	8	23 June 2011	Comments from Richard Staley, Raymond Brock and Jim Linnemann

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1 SCOPE OF THE PROJECT

The CMX module is part of the Phase-1 upgrade [1] to the ATLAS Level-1 Calorimeter trigger system (L1Calo [2]) – as well as a replacement of the Common Merger Module [3]. This document specifies the CMX functional requirements, differences between the CMM and CMX, and technical aspects of the CMX implementation. The specific engineering solutions and firmware specifications will be described in more detailed documentation for the final design review of this module. The structure of this document is as follows:

- section 2 lists related projects and references,
- section 3 describes functional requirements to the module,
- section 4 describes technical aspects,
- section 5 describes modes of operation,
- section 6 describes project organization.

The CMX module will be designed to fit in the CMM positions in the L1Calo digital algorithm processor crates, and will inherit all main logical components of the current CMM. In addition to the current CMM functionalities, CMX will be designed to receive higher data volumes from the processor modules via the backplane, and send data to the Topological Processor (TP) via multi-fiber optical ribbon links. The module will also have higher data processing capabilities and the ability to operate as a data sink for high speed optical links, allowing additional functionality to be implemented.

2 RELATED PROJECTS AND REFERENCES

The Phase-1 topological upgrade of L1Calo provides a useful enhancement to the current system, adding significant flexibility for a modest hardware change. In addition to the CMX, several coupled sub-projects are included:

- firmware upgrade in the processor modules in order to collect the RoI information, generated in the modules, and to send it to the CMX over the crate backplane,
- Backplane and Link Tester (BLT [4]) module to test data transfer over backplane,
- Generic Opto Link Demonstrator (GOLD [5]) project - a demonstrator for the TP,
- Modifications to the current L1Calo trigger Read-Out Drivers to receive extra data from the processor modules and the CMX module,
- Modifications to the ATLAS Level-1 Central Trigger Processor (CTP) functionality.

[1] [Upgrade project document]
[2] R. Achenbach et al., *The ATLAS Level-1 Calorimeter Trigger*, 2008_JINST_3_P03001. (ATL-DAQ-PUB-2008-001). http://iopscience.iop.org/1748-0221/3/03/P03001/pdf/1748-0221_3_03_P03001.pdf
[3] I.P. Brawn, C.N.P. Gee, *Specification of the Common Merger Module*, v1.8, 18 July 2008. (ATL-DA-ES-0021). https://edms.cern.ch/file/321069/1.8/CMM_V1_8.pdf
[4] B. Bauss, U. Schäfer, C. Schröder, *Backplane Tester Module*, v0.3, 11 December 2008. http://www.staff.uni-mainz.de/baussh/Backplanetester/Sheets_Vers1.0.pdf
[5] B. Bauss, U. Schäfer et al, *GOLD Module*, v0.1, 10 January 2011. http://www.staff.uni-mainz.de/uschaefe/browsable/L1Calo/GOLD/GoldReview.htm
[6] C.N.P. Gee, *VME-- specification*, v1.2, 9 January 2006. (ATL-DA-ES-0043). http://hepwww.rl.ac.uk/Atlas-L1/TIN/Reduced_vme_spec_v1_2.pdf
[7] W. QIAN, *VME Mount Module*, v2.4, 25 November 2005. http://hepwww.rl.ac.uk/Atlas-L1/Modules/VMM/VMM_ProductionVersion2.4.pdf
[8] C.N.P. Gee, *Timing Control Module*, v1.0.5, 12 September 2006. http://hepwww.rl.ac.uk/Atlas-L1/Modules/TCM/TCM_V1_0_5.pdf
[9] S. Silverstein, A. Marmbrant, *High-Speed Links Study.*

[10] S. Hillier, *Overview of the Simulation Framework*, SN 011, Version Draft 0.99, 1 Feb 2002. http://atlas-l1calo.web.cern.ch/atlas-l1calo/doc/out/Simulation.pdf

3 FUNCTIONAL REQUIREMENTS

L1Calo must continue to provide the current multiplicity-based triggers throughout the Phase-1 development and commissioning periods. As a consequence, it is desirable that the CMX module can be tested in parallel with the currently running system before deployment of the Topological Processor. The CMX development scenario assumes that the module can be a drop-in replacement for the CMMs, with the ability to perform additional logic in parallel with all necessary backward-compatible CMM functionality. The basic requirements are that this module should:

- Provide all necessary functionality to replace a current CMM (including electrical interfaces, programming model, and data formats)
- Be able to format and transmit data received via the backplane from upgraded algorithm processor modules to the TP
- Transmit additional information to the Read-Out Drivers (RODs)
- Allow sufficient extra connectivity between CMX modules and extra processing capability to perform some topological trigger tasks in standalone mode in the absence of a dedicated TP

3.1 BACKWARD COMPATIBILITY

The current CMM [3] modules produce system-wide results in two steps. All CMMs gather and process the results from the processor modules in their crates to produce crate-level results. One CMM of each type, designated as "system" CMMs receive the crate-level results from the other modules via cables in order to produce system-wide results. These final results are sent on cables to the CTP. All CMM modules (12 in total in the current L1Calo system) are physically identical; each hardware module carries all FPGA firmware configurations needed to perform both crate and system-level processing in any L1Calo subsystem crate, automatically loading the appropriate FPGA logic according to its position in the system.

The CMX shall provide all the necessary functionality and satisfy the latency requirements to replace a current CMM when running in backward compatible ("CMM emulation") mode. It shall:

- *be designed to fit in the CMM positions in the processor crates ,*
- *inherit all main logical components, electrical interfaces, programming model and data formats of the current CMM,*
- *be able to implement all different CMM versions, adapted to new FPGA hardware.*

No online software or data format changes are foreseen for this mode of operation. From the L1Cal trigger system point of view, CMX will be a pure drop-in replacement for the CMM with no need for any system changes. As for the current CMM, the appropriate FPGA logic will selected and loaded automatically on power-up, based on the geographic address pin configuration encoded on the backplane (see chapter 4).

3.2 DATA SOURCE FOR TOPOLOGICAL PROCESSOR

In the fully implemented topological upgrade of L1Calo, the CMX will provide the interface between the processor crates and the Topological Processor. To achieve this, extra functionality shall be added in order to receive higher data bandwidth from the processor modules and send topology information to the TP.

The CMX shall provide the following extra functionalities for running with the TP:

- *receive data from upgraded processor modules over the crate backplane at higher data transfer rates (160Mb/s),*
- *transmit data to the TP via multi-fiber optical ribbon link(s),*
- *Read out the higher input and output data volumes the L1Calo Read-Out Drivers.*

In providing these additional functionalities the CMX shall satisfy the latency limits of the L1Calo and CTP systems.

For transitioning to the final TP interface functionality there are several possible modes of operation, defined by the firmware in the processor modules and in the CMX module, e.g.:

- "Test mode": The CMX receives data from the processor modules in a new data format, permitting the backward compatible mode of operation (e.g. - current data plus new data, see 5.2) and splits data into two data streams – one for the legacy CMM operation and second for the TP operation. The CMX works in the backward compatible ("CMM emulation") mode supplying data to the CTP and in parallel sending data to the TP for test purposes (with or without internal processing). The TP is not connected to the CTP in this mode.
- "Upgrade mode": The CMX receives data from the processor modules in a new data format (not necessarily backward compatible with the legacy operation), performs data processing, and feeds the data onwards to the TP (as well as possible results to the CTP. Both the CMX and the TP may supply data for the CTP in this mode.

The CMX programming model and online software will require modifications to handle extra data from the processor modules. More data has to be sent to the RODs. Internal data processing in the CMX may results in a smaller number of optical links, required to transfer data to the TP.

3.3 STANDALONE MODE (OPTIONAL)

It is possible that the CMX may be required to provide some limited topological processing functionality in the absence of the final TP. In this mode of operation CMX modules would be interconnected via multi-fiber optical ribbon links (and optionally via legacy electrical links at the rear of the module). Topological trigger results would be reported by the CMX directly to the upgraded CTP.

To operate in this mode, the CMX shall (in addition to the functionalities in 3.2):

- *receive input data via additional multi-fiber optical ribbon links,*
- *provide a compatible interface to the upgraded CTP.*

The CMX programming model and online software will require modifications to new CMX functionalities. As in the data source modes (see 3.2), the CMX will send more data to the RODs and therefore additional optical links to RODs shall be implemented.

To interconnect all CMX cards to the system CMX may require a (relatively simple) interconnect board designed to regroup and distribute a subset of the fiber outputs to the appropriate system CMX inputs.

4 TECHNICAL ASPECTS

The CMX module is a 9Ux400mm module designed to fit in the CMM positions in the CP and JEP processor crates with all present interfaces and connectors preserved. Many parts of the CMM (e.g. – CPLD VME interface, TCM interface, Xilinx System ACE) – both schematics and firmware – may be reused to speed development.

A block diagram of the CMM is shown below. The main functionality is implemented in two Virtex-E FPGAs XCV1000E-6FG860. All CMMs include a System-ACE chipset and a standard Compact Flash card loaded with all current sets of FPGA configuration files. The appropriate FPGA configurations are selected and loaded automatically on power-up, based on the unique geographical address encoded in the backplane.

Like all modules in the digital algorithm processor crates, the CMM uses a subset of the VME standard, referred to as "VME--" and defined in [6]. A VME single-board computer is interfaced with the bus through a VME Mount Module (VMM [7]).

Module timing, trigger and control signals are derived from the TTC signals distributed across the backplane by the Timing and Control Module (TCM [8]) and decoded locally by a TTCrx chip mounted on a TTCdec daughter card. The backplane also includes a local CANbus for crate level slow control and monitoring. The CMM uses a Fujitsu MB90F591 microcontroller as an interface to the CANbus to pass voltage and temperature information via the TCM to the ATLAS Detector Control System (DCS).

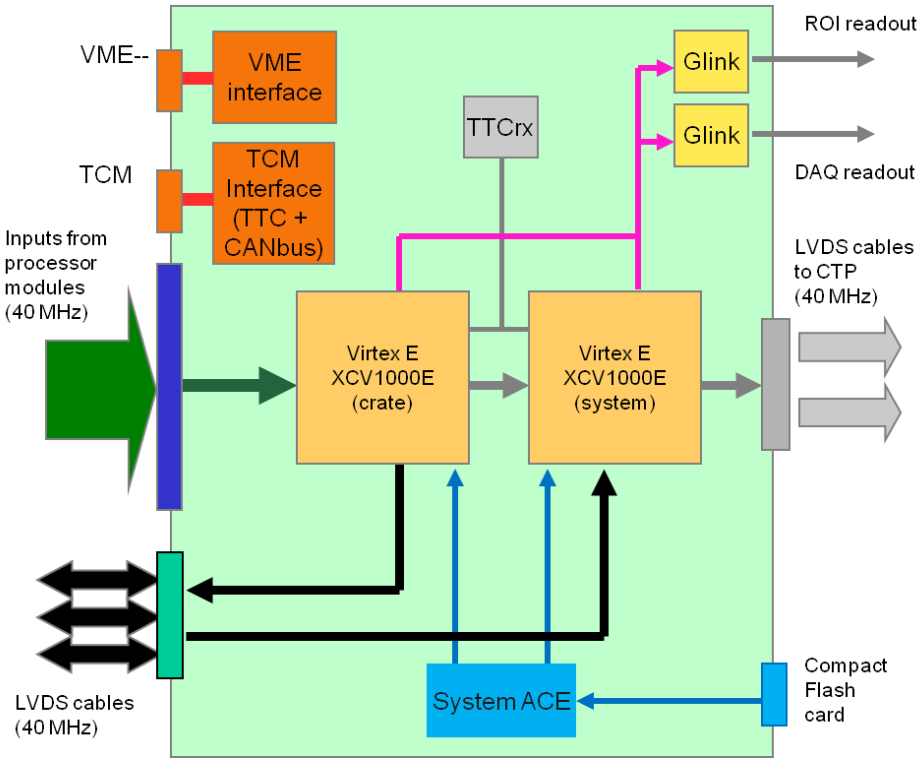


Figure 1: Overview of Common Merger Module (CMM)

Two G-link serializers in 20-bit mode provide the readout interface to the L1Calo readout drivers (RODs) When an L1A is issued, the CMM responds by reading out input and output data readout to the data acquisition system ROD (DAQ ROD)., while the “system” CMMs also read out relevant results, to the RoI Builder ROD (ROI ROD).

A block diagram of the CMX is shown in Figure 2. For the CMX module, the main modifications to the CMM design will include:

- *replacement of the obsolete crate and system FPGA devices by a single, large modern FPGA that can receive data at 160Mb/s from the backplane, transmit and receive data via multi-fiber optical ribbon link using multi-gigabit transceivers*
- *implementation of the G-link protocol in FPGA firmware and high-speed serializers (the original G-Link chips are no longer in production),*
- *implementation of multi-fiber optical ribbon links, interfaced with the FPGA transceivers*
- *selection of FPGA(s) configuration according to the mode of operation, described in 3.1-3.3*

The front panel of the CMM module is already almost entirely occupied with connectors, so it may be necessary to place the parallel optical links on the board away from the front panel.

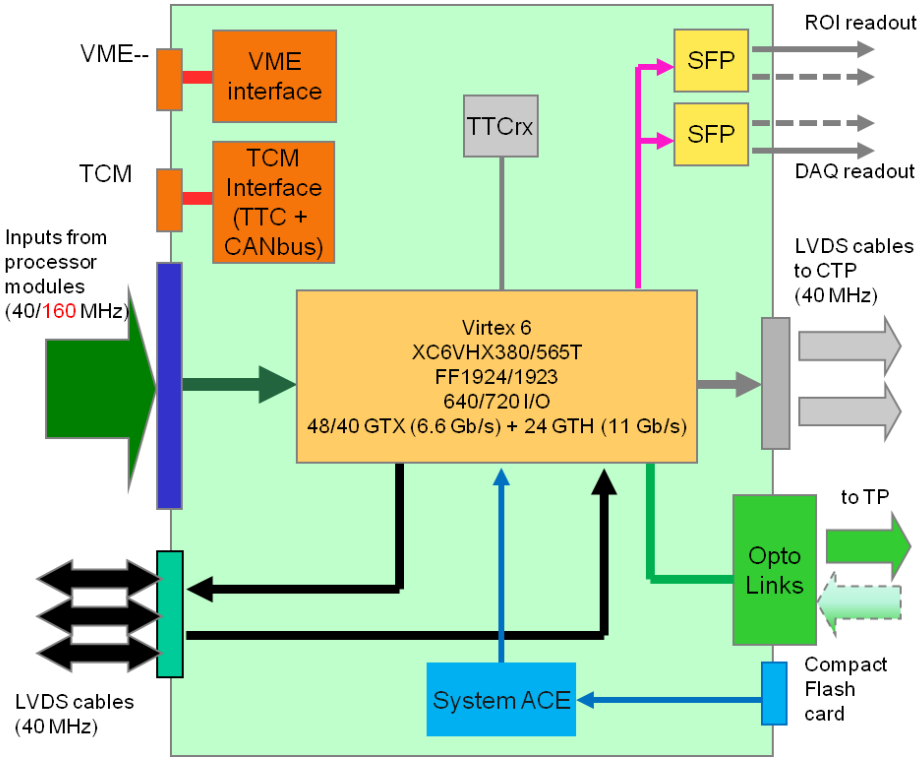


Figure 2: Overview of CMX

Main modifications to the CMM firmware consist of porting the existing CMM firmware to the new hardware, implementation of different CMX modes, and modifications to the programming model.

The main functional parts of the CMX modules are listed below:

- Processing FPGA,
- G-Link (implemented in FPGA) with optical transmitters,
- LVDS cables and rear transition module,
- CTP interface,
- Optical links,
- System ACE (FPGA configuration).

They are described below in more detail.

4.1 PROCESSING FPGA

In the baseline design the two FPGAs in the CMM would be replaced by a single large modern FPGA. The choice of FPGA is driven by the need for large numbers of both low-speed parallel I/O for the legacy CMM connectivity and high-speed serial transceivers for G-Link emulation and topological

processing. The Xilinx Virtex 6 HXT family of FPGAs include up to 720 parallel I/O pins or 72 multi-gigabit transceivers, depending on the package chosen. This makes it almost certainly suitable for a single-FPGA CMX. However, if I/O limitations prove to be a problem, it may be necessary to implement the CMX with two main FPGAs. This will be decided during engineering studies.

The new FPGA or FPGAs for the CMX board shall provide sufficient:

- *IO pins, compatible with the L1Calo system backplane signal levels,*
- *high speed serial transceivers for data transmission and reception,*
- *internal logical resources (logical blocks and memories).*

Backplane data

The backplane data from processor module are transmitted over 25 signal lines using single-ended back-terminated 2.5V CMOS levels. The CMX receives backplane data from up to 16 processor modules, for a total of 400 signal lines.

The backplane input to the CMX will be either in backward compatible or test/upgrade/standalone formats. In the backward compatible mode the backplane data consists of 24 data bits plus one odd parity bit on each 40 MHz clock cycle.

In the test/upgrade/standalone modes the CMX will receive data at 160 Mb/s. Data shall be clocked onto the module separately for each processor using decoded forwarded clock from this processor. Therefore, the FPGA chip shall provide 16 groups of input pins with individual data clocks.

Here 24 lines would be used to transfer the data while the 25th line carries a 80 MHz forwarded clock encoded with an odd parity bit.

I/O pins

The new FPGA on the CMX shall replace two old ones used on CMM. This means that the single device must provide all of the external interfaces originally divided between the two CMM FPGAs A rough estimate of the I/Os needed to replicate the CMM connectivity (after removing spare TTL and test ports) is shown here:

Real-time data path:		
Backplane inputs from processors (16 x 25):	400	
LVDS cables (3 x 25):	75	
CTP outputs (2 x 33):	66	
	Sub-total:	541
Control and timing:		
VME-- from CPLD	35	
TTC (L1A, BCR, deskew 1 and 2)	4	
Crystal clock	1	
clr_pe,rst,rst_dll,pbk_en,can_mc,en_cblout	6	
	Sub-total:	46
Readout:		
Glink data outputs 2 x 20	40	
DAV pins	2	
	Sub-total:	42
Indicator LEDs :	8	
	Sub-total:	8
	Total:	**637**

This pin count is very close to the 640 I/O count of the Virtex-6 FPGA with the most LVDS transceivers. One way to reduce this count is by emulating the readout G-links in the FPGA (see 4.3). Another approach would be to choose a device with 720 parallel I/O pins at the cost of eight transceivers.

High speed transceivers

The total data volume received by the CMX from 16 processor modules is 384 bits at 160 MHz, or 61.44 GBit/s. The 8/10 encoding will increase the data volume up to 76.8 GBit/s. Transmission of this full data volume over 12 optical links is possible using 6.4 GBit/s serial transmitters in the FPGA. Instead of sending the full backplane contents out of the CMX, it is possible to reduce the data volume and the number of required optical links by a factor of 2 to 3 by pre-processing the backplane data in the CMX and sending a zero-suppressed list of topological features to the TP.

For data reception in standalone mode, the FPGA shall provide a sufficient number of high speed serial receivers. Early estimates, presented in chapter 5, suggest that on the order of 60 receivers per CMX module would suffice.

Implementation of the G-link protocol in firmware requires some of the serial transmitters in the FPGA chip to be reserved for this purpose. The number of transmitters depends on the data volume sent to the L1Calo Read-Out Drivers.

The transmitter and receiver in each FPGA transceiver can be used independently, making it possible to use the transmitters to send data from the CMX and at the same time use their receivers to receive data from other sources.

FPGA

The most recent and advanced families of XILINX FPGAs are Virtex-6 (HXT) and Virtex-7. The first samples of the Virtex-7 chips may be available for selected customers beginning of 2012 (information from XILINX seminar at CERN on 17.02.11). The Virtex-6 HXT devices shall be available this year.

Examples of suitable FPGA devices are Virtex-6 XC6VHX380T and XC6VHX565T:

- IO pins organized in 16 or 18 banks with 40 pins per bank; all inputs and outputs support Double Data Rate (DDR),
- supports 1.2 to 2.5V I/O operation and Digitally-Controlled Impedance (DCI) active termination (optional series or parallel termination) on every pin,
- 18 Mixed-Mode Clock Managers (MMCM) blocks provide zero-delay buffering, frequency synthesis, clock-phase shifting, input jitter filtering, and phase-matched clock division,
- any input or output can be individually delayed; the number of delay steps can be set by configuration and can also be incremented or decremented while in use,
- GTX transceivers (6.6 GBit/s) and GTH transceivers (11.18 GBit/s).

The two devices differ in the amount of internal logical resources (logic cells and memory). They are available in two types of packages (http://www.xilinx.com/products/virtex6/index.htm):
FFG1924 package: 640 IO pins organized in 16 banks; 48 GTX transceivers and 24 GTH transceivers.
FFG1923 package: 720 IO pins organized in 18 banks; 40 GTX transceivers and 24 GTH transceivers.

Backplane receivers

The deployment of the CMX module requires firmware modifications in the processor modules in order to collect the RoI information generated in the modules, and to send it to the CMX over the crate backplane. Due to the VirtexE FPGA used in the Cluster processor module, the 40MHz clock can only be multiplied by x2 or by x4 (80MHz or 160MHz) due to nature of the DLLs inside the FPGA. Therefore the maximum clock frequency is limited to 160MHz; otherwise some serious modification to the clock circuitry would be required.

In order to quadruple data transfer rate over backplane (from 40 Mb/s to 160 Mb/s), it is proposed to use Double Data Rate (DDR) technique (new data sent at each edge of clock) and 80MHz forwarded clock. In this case, for each 40 MHz clock cycle 96 bits of data (24x4) can be transferred from each processor module to CMX module over 24 lines. The 25^{th} signal line on the backplane will be used to forward an 80 MHz clock encoded with parity bit as follows: the rising edge provides the clock timing and the duty cycle value encodes the parity bit (see below).

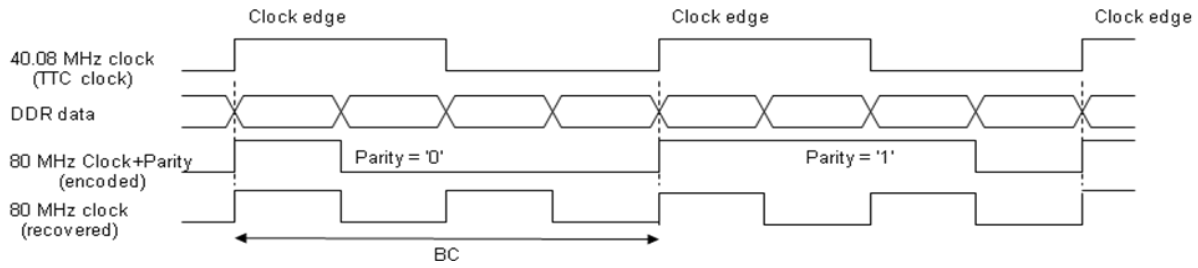


Figure 3: Clock/parity encoding

The 80 MHz clock recovery is implemented in the FPGA's Mixed-Mode Clock Managers (MMCM). DDR data are clocked onto the CMX separately for each processor using the recovered clock from this processor. The data path delay for the individual data inputs will be measured and adjusted using software based delay scan. The data transmission will be implemented with the serial termination in the transmitters (processing modules) and no termination in the CMX.

4.2 G-LINK IMPLEMENTATION

The G-Link transmitter chips (HDMP 1022) used on the CMM are obsolete, and not produced any more. While distributors still have them in stock, it will be preferable to implement the G-Link chip protocol in the FPGA and use GTX serial transmitters in the FPGA chip. This can also lower the number of pins needed in the FPGA (emulating G-Links in the FPGA saves about 40 pins). As in the current CMM, the 40 MHz low-jitter crystal clock will be used. G-Link protocol emulation has been already implemented in FPGAs - Altera provided code for Stratix GL. It has been ported to Xilinx Virtex-4 and Virtex-5 FPGAs (both simple and enhanced modes) and simulated on Virtex-5 FPGA using GTX transmitter at 960 Mbit/s by Samuel Silverstein.

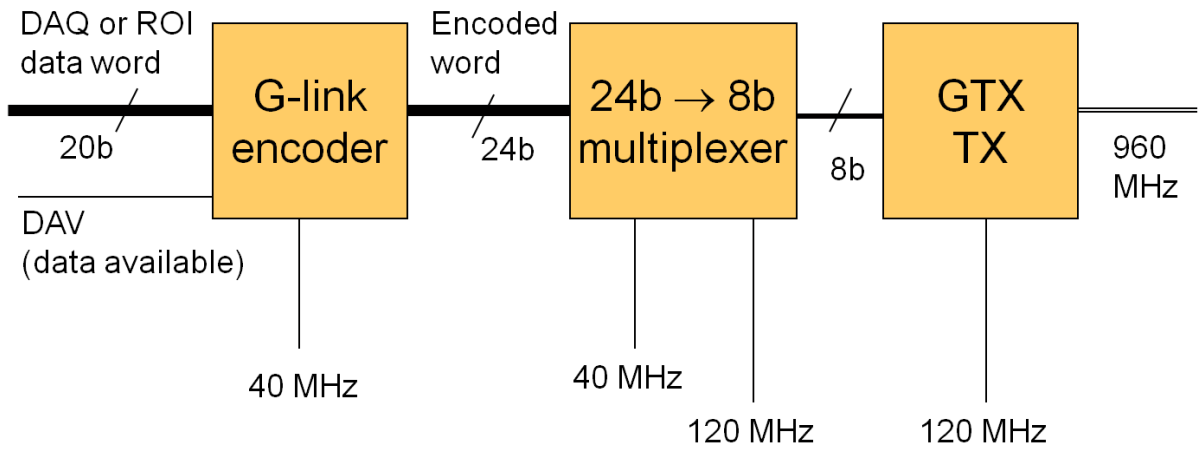


Figure 4: G-link emulation in Virtex 6

For backward compatibility, the optical transceivers shall be the same as on the CMM module - Small Form-factor Pluggable (SFP) Multimode 850 nm optical transceivers with LC connectors. The Infineon V23818-M305-B57 is no longer available; an equivalent Avago part is AFBR-57M5APZ. These devices are economical and their active parts are plug-in and therefore replaceable. Only the transmitting half of the transceiver is used. Another possibility would be to use optical transmitters for the multi-fiber optical ribbon links, but this solution would require an adaptor.

The number of transmitters depends on the data volume sent to the L1Calo Read-Out Drivers, so extra transmitters may be needed.

4.3 LVDS CABLES AND REAR TRANSITION MODULE

A passive transition module is required at the rear of the backplane for connection to up to three cables, each carrying 25 LVDS parallel signals at 40 MHz between Crate and System-CMMs in the backward compatible mode. Identical transition modules are used at both ends of cable links. The cables are the same type as for the CMM-CTP cables in the current system.

These transition modules will be required in both TP and standalone modes if the CMX performs both crate and system-level trigger data processing. The modules and the cables may be able to transmit information between CMX modules at higher than 40 MHz (this has to be tested). In this case additional information can be transferred between CMX modules.

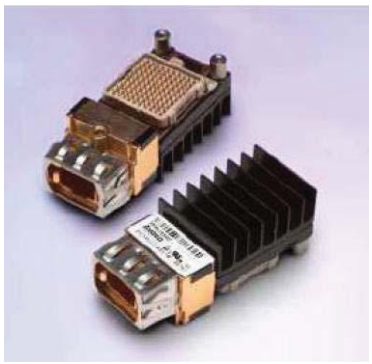
4.4 CTP INTERFACE

For the CMX backward compatible mode of operation no changes to the 40 MHz CTP interface are foreseen.

In both TP and standalone modes, the CMX module may still transmit trigger results to the CTP. The CTP input module (CTPIN) may be upgraded to 80 MHz operation during the lifetime of the CMX module (the mechanical interface to the CTP will remain unchanged). This CTP modification would in turn require the CMX CTP output to be upgraded to 80 MHz.

4.5 OPTICAL LINKS TO TP / FROM OTHER CMX

The CMX optical links will be implemented using Virtex-6 FPGA transceivers - GTX (6.6 GBit/s) and GTH (11.18 GBit/s). Transmitters and receivers in these transceivers can be used concurrently.



Optical transceivers will be parallel fiber modules that use fiber ribbon cables which commonly contain either 12 or 24 individual fibers terminated by an MTP (or MPO) connector. Today, parallel optics modules are available in variety of configurations and form factors which are specified in a number of multi-source agreements (MSA), e.g. - SNAP-12 which specifies separate 12-channel transmit and receive Z-axis pluggable modules. Avago Technologies offers a multimode parallel optic solution based upon internally developed 850 nm based VCSELs, PINs and driver ICs with a maximum aggregate bandwidth of up to 72 Gb/s (12 channels @ 6 Gb/s). The 10Gb/s capable transceivers are also available

The maximum number of transceivers for the XILINX XC6VHX380T and XC6VHX565T devices in FFG1924 package is 72. Therefore up to 12 parallel fiber modules (6 transmitters and 6 receivers) can be routed on the CMX PCB and soldered upon need. In the initial backward compatible mode of CMX operation, no optical links to the TP will be exploited. In the subsequent “test” and “upgrade modes (see chapter 3), when CMX will be operated with TP, only transmitters need be used. In the “standalone” mode both transmitters and receivers will be utilized.

4.6 VME INTERFACE

The current VME-- address ranges [6] allocate 0x80000 bytes for each CMM (512k), of which about half is currently used:

- CMM0 (slot 3): 0x00700000-77FFFE
- CMM1 (slot 20): 0x00780000-7FFFFE

The CMX in the “backward compatible” (5.1) mode of operation will use the same VME-- address range as current CMM.

The additional functionality for the CMX in the “data source for TP” (5.2) mode of operation (test or upgrades modes) should easily fit within the same register space.

In the “standalone” (5.3) mode of operation (CMX/TP) to implement topological processing CMX may need to fill large lookup tables or CAMs, spy and playback memories. Therefore, the CMX would not fit in the same register space. However, CMX needs to have sufficient addresses space for this mode of operation in order to be configured and read out in the crate.

From a software point of view it is preferable to allocate a contiguous address range for CMX (in any mode of operation) and to create a new software class(es) for the CMX in “data source for TP” and “standalone” modes rather than extending the current CMM software with extra functionality. With a new module class, the address map for the CMX in “data source for TP” and “standalone” modes doesn’t need to be strictly backwards compatible with CMM - though it will be easier to port the old software to the new module if it is.

In the VME-- specification, the address space used by existing modules, including CMMs, goes from 0x0600000 to 0xFFFFFE. The lower address space is currently reserved for any module in slot 2 (the second SBC slot) which gives nearly 6 megabytes of unused address space.

The Virtex 6 FPGAs have up to 38 Mbits of block RAM, or 4.75 megabytes. This fits easily within the extra 6 megabytes of VME-- space as long as no more than one CMX per crate can act as a CMX/TP. Alternatively, instead of direct mapping of the CMX to the VME-- space, an indirect addressing might be used - a moveable window, where a register on the CMX defines the base address of this window. This would allow the many megabytes of CMX to be accessed through a smaller VME-- address space. Provided the window is big enough to encompass any of the single blocks of RAM this solution would not be expected to slow access significantly.

4.7 TCM INTERFACE (TTC + CANBUS INTERFACES)

The CMX module will receive timing from the ATLAS TTC 40.08 MHz system as in the current system. The optical receiver is located in the TCM module and then TTC signals are electrically distributed on the backplane to the modules in the processing crate. They are decoded in the CMM by TTCrx chip, controlled from VME interface via small FPGA which provides various control and status pins of the TTCrx (I2C, Brcst, etc). The CMX will keep this functionality.

The CMM uses a Fujitsu MB90F591 microcontroller as an interface to the CANbus in the processing crate to pass voltage and temperature information via the TCM module in the crate to the ATLAS Detector Control System (DCS). CANbus based monitoring might be required on TP as well. A CANbus daughter module might in this case be a common item using the Fujitsu microcontroller basically as a CAN to I2C bridge only, with all monitoring done via I2C sensors. This scheme requires just a very small number of lines to be routed between a daughter card and the main board.

4.8 FPGA CONFIGURATION

In the current L1Calo trigger system the CMM module has several configuration versions of hit- and energy-summing functions (for different CMM position in the L1Calo system). The XILINX System ACE contains configuration files on the Compact Flash card for all possible CMM positions; the appropriate FPGA configuration file is selected and loaded automatically on power-up, based on backplane pin configuration - geographical VME Address. The CMM functionality doesn’t change during module operation apart from settings in internal configuration registers.

For the CMX configuration this model will be also used, but in addition to several configuration versions for different CMX position in the L1Calo system the CMX has several modes of operation with different functionalities (see chapter 3). A practical solution will be to have individual files for different CMX modes of operation. It may require either physically changing the Compact Flash card in the System ACE device or updating it in-situ via VME.

4.9 CLOCK

The CMX module will run at 40.08 MHz clock delivered by TTC system or local crystal clock.

For full backward compatibility the DAQ and ROI G-Links are going to run at 40.00 MHz.

5 MODES OF OPERATION

During its lifetime the CMX will be operated in different modes. The CMX modules will replace the current CMM modules (12 in total) in the L1Calo crates. They will be designated as “em CMX”, “tau CMX”, “jet CMX” and “energy CMX” like current CMMs.

5.1 BACKWARD COMPATIBLE (CMM EMULATION, CMMe) MODE

The backward compatible mode of CMX operation (CMM emulation mode) will be the initial one. It requires that the different firmware versions of the CMM can be adapted to the new hardware (new FPGA, G-Link protocol implementation in firmware) and that the CMX provides all the necessary functionality and satisfies the latency requirements. No online software or data format changes are foreseen for this mode of operation. Processor modules use current firmware and supply data at 40MHz. All data formats and internal programming model of the CMX will be the same as for the CMM. No online software changes are foreseen for this mode of operation. The CMX connectivity in the L1Calo trigger system will reproduce the current one (Fig.27 from [2]), shown below (G-Link connections to RODs are not shown):

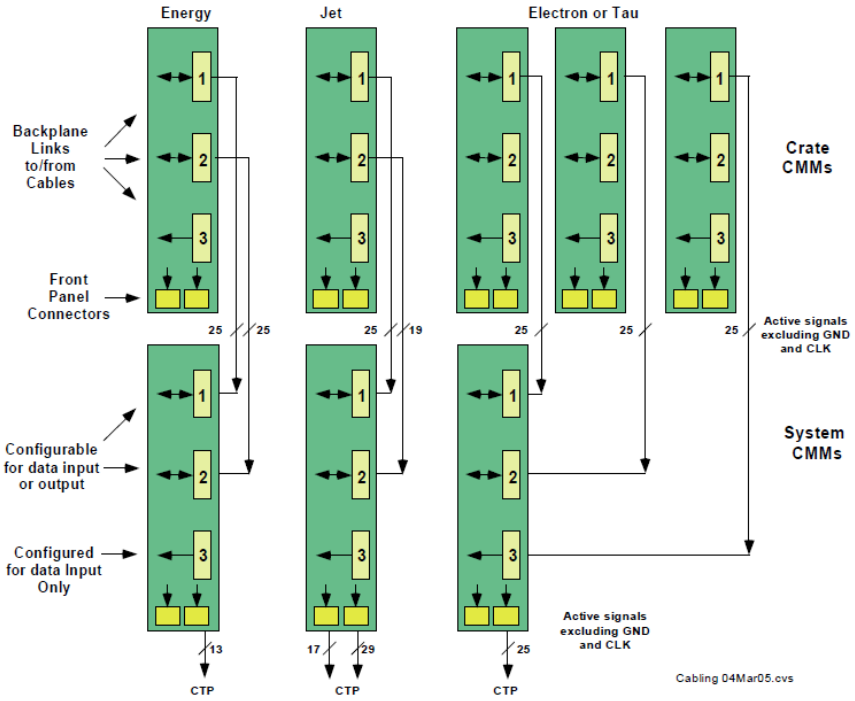


Figure 5: Interconnection scheme for CMMs (only half of electron/tau CMMs is shown).

In this mode of operation no optical links to the TP or from other CMX modules will be used.

5.2 DATA SOURCE FOR TP

This is a main mode of CMX operation in fully implemented topological upgrade program. The CMX acts as the interface from the processor modules to the TP. There are several possible sub-modes of operation, defined by the firmware in the processor modules and in the CMX module.

Test sub-mode

In the initial phase of CMX and TP commissioning and testing, it may be advantageous to keep CMX running in the backward compatible mode supplying data to the CTP and in parallel sending the data to the TP for test purposes. The CMX interconnections will be the same, as in Fig. 4 and connection to the CTP is still maintained. The TP is not connected to the CTP. The incoming data from L1Calo processors shall have, however, a new format, in order to operate CMX in test mode:

- current L1Calo data (current 24 bits per bunch crossing) plus new data in remaining 72 bits,
- a new data format which allows recovery of the information to run CMX in the backward compatible mode.

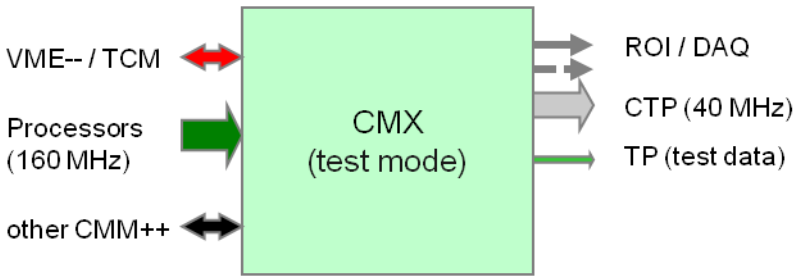


Figure 6: CMX in test mode.

Implementation of these modes requires extra firmware development efforts for both – processors and CMX and shall be looked carefully in order to balance between efforts and benefits.

Upgrade sub-mode with or without internal processing

This is a main mode of CMX operation. It requires firmware updates in the processor modules and new firmware development for the CMX. The CMX receives data from the processor modules in a new (not backward compatible) format which is still under discussion and development. It performs data processing, feeds the data onwards to the TP (and supplies some information to the CTP?). Both, the CMX and the TP may supply data for the CTP in this mode. There are two possibilities:

- all data, received by CMX from the processor modules are immediately sent to the TP over twelve parallel fibers running at 6.4 Gbit/s without any data processing. This implies about 12 optical ribbon cables coming into the TP from 12 CMX. The data from "energy CMX" may require fewer (1-4?) fibres per ribbon. The total amount of fibres would be ~128-144.
- data from processor modules undergo reduction in CMX, so that the TP receives a more manageable data volume. It can be done by sending to the TP only a list of non-zero ROIs, with coordinates and results in fewer optical links to the TP (assume half for this discussion).

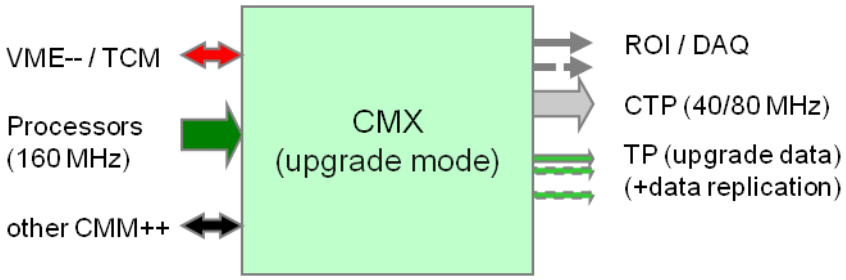


Figure 7: CMX in upgrade mode.

The maximum number of transceivers per CMX (see 4.6) is 72. As only 12 transmitters (or 6 with the data processing) are used to send data to the TP, remaining transmitters can be used for data replication and distribution to multiple TP "processing slices" working in parallel on the same data.

Data processing (reduction) in CMX sub-mode (Sam Silverstein)

Send only a list of non-zero ROIs, with coordinates. The absolute coordinates for a jet ROI can be encoded in 9 bits, and em/tau clusters would have 13 bit coordinates. But since the TP still "knows" which crate each fiber comes from, these can be reduced to these to 8 and 11 bits, respectively.

For ROI content, each CMX reports 8 threshold bits per ROI, respectively. An additional 8-12 bits of additional information per ROI (energy, etc) should also be budgeted. So a total budget of ~31 bits (coordinates plus content) per ROI can be easily allocated. A 32nd bit per RoI should be reserved as a flag for error or overflow detection. In summary, each ROI would look something like this:

- absolute coordinates: 9 bits for jets, 13 bits for clusters (8 and 11 bits, respectively, if crate number implicit),
- thresholds: 8 bits per ROI,
- additional information (energy, etc): 10-12 bits per ROI,
- flag: 1 bit

Total: 32 bits per ROI

5.3 STANDALONE MODE (OPTIONAL)

In this mode CMX modules are used without TP (in case TP delayed, for instance). The role of the topological processor can be executed by one CMX module in the system (CMX/TP).

In this scenario, like in the upgrade mode with internal data processing, all CMX modules (but CMX/TP) send data to the CMX/TP over six parallel fibers running at 6.4 Gbit/s.

The total number of fibers from 11 CMX after data processing is about 64-72 which can be accepted by the number of receivers, available in the XILINX XC6VHX380T and XC6VHX565T devices (see 4.6). Therefore one CMX/TP can receive all the data (like the TP) and use its internal processing capabilities to provide some limited topological trigger functionality.

One shall profit from the fact, that there are many transmitters on the CMX modules, which can be used for data replication (see 5.2). In this case, event data can be sent to multiple CMX modules acting as CMX/TP – up to the maximum number of CMX modules. They can run different topological algorithms in parallel. Additional information (e.g. – muon RoIs) can be sent to the CMX/TP modules via the rear transition modules. A partial data processing results from individual CMX/TP modules will be sent via front panel CTP connectors to the "global" CTP interface, performing the final merging of results.

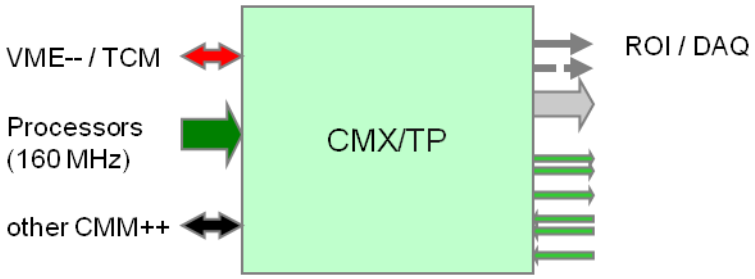


Figure 8: CMX in standalone mode.

To implement such a scheme, an additional passive interconnect card regrouping the output fibers form the CMX modules into fiber ribbons for the inputs of the CMX/TP modules.

5.4 NUMBER OF OPTICAL LINKS IN DIFFERENT MODES OF OPERATION

Backward compatible mode

The number of high-speed fibers in the backward compatible mode of operation is zero.

Data source for TP mode

In this mode the number of transmitters is 12 (one optical 12-fibers ribbon link) in a case all backplane data are sent to the TP without internal CMX processing. If there is an internal data processing in CMX, data volume can be reduces by a factor of 2-3 - but we probably will still need one 12-links optical transmitter. The remaining transmitters can be used to duplicate (fan-out) the data to multiple destinations (multiple TP slices).

Standalone mode

In the standalone mode, internal data processing in CMX will be used and the number of transmitters is 4-6. Remaining transmitters can be used to duplicate (fan-out) the data to multiple destinations - in

this case CMX modules. In addition, in this mode we have to implement in CMX module optical receivers for incoming data. With internal data processing in CMX we may need, let say, 6 x 11 fibers to send data from one CMX to other 11 CMX modules. An additional passive interconnect card regrouping the output fibers form the CMX modules into fiber ribbons for the inputs of the CMX/TP modules.

Summary table: number of fibers in different modes

The maximum number of transceivers is 72. They are used for the optical links to the TP (or to/from CMX/TP) and for the DAQ and ROI G-Links.

Tx: number of required transmitters without internal data processing

Tx proc: number of required transmitters with internal data processing

Tx GL: number of required transmitters for the DAQ and ROI G-Links

Tx repl: number of available transmitters for data replication (fan-out)

Rx: number of required receivers

	Tx	Tx proc	Tx GL	Tx repl	Rx
Backward compatible	0	0	2	0	0
Data source for TP	12	4-6	4-6	54-64	0
Standalone *	0	0	4-6	66-68	66

* Assumption is, that in the standalone mode all CMX are used as the CMX/TP, therefore CMX doesn't send the data to itself, but only to other 11 CMXs. Each CMX receives processed data from 11 CMX. (In 4.6 it is stated that no more than one CMX per crate can act as a CMX/TP in a case of direct VME addressing scheme – 6 CMX/TP in total. In a case of an indirect addressing, all CMX can act as CMX/TP).

5.5 LATENCY

Backward compatible mode

The latency in this mode will not exceed the current latency of the CMM, estimated as 8 BCs (Bunch-Crossings, 25 ns) and possible will be smaller due to the faster FPGA used.

Data source for TP mode

In this mode data will be reformatted in the CMX module before transmission to the TP, which may take up to 2-3 BCs. In a case of some data processing in the CMX, the added latency will be defined by the executed algorithm. The serialization latency in CMX for the data transmitted to TP is estimated as 2 BCs.

Standalone mode

In this mode, the maximum available latency in the L1 trigger system will define the possible set of algorithms to be executed in the CMX.

6 PROJECT ORGANISATION

The design of CMX will take into account experience gained during the design of the current CMM module and prototyping of the technology demonstrators in the L1Calo collaboration:

- CMX hardware design and testing will be a MSU responsibility and will require interaction with the designers of the current CMM module,
- modifications to the L1Calo processor modules' firmware will be done by the processor designers with the help from MSU as concerns the interface to the new module,
- adaptation of the several versions of the current CMM firmware to the new hardware will be done by MSU with a help from the developers of the current CMM module,
- firmware modification to RODs for both algorithm processors and CMX will be done by the ROD designers with the help from MSU as concerns the interface to the new module,
- design of the firmware framework for the topological algorithms development will be a MSU responsibility with possible involvement of other interested groups,
- MSU test rig development will be a joint responsibility, but led by MSU.

6.1 CMX ENGINEERING SCHEDULE V0.9 (JAN 2011)

- 1/11 - 6/11 : 6 months….CMX Project Specification.
  - target CMX project specification review
- 7/11 - 1/12 : 7 months….Engineering Specification.
  - Test rig installed, checked out at MSU
  - Simulation and some preliminary routed design studies with constrained pins and timing
  - Preliminary: FPGA resource allocation - memory blocks, serial I/O facilities, global clock nets, clock management.
  - preliminary: FPGA pin out
  - coding standards, version control established
- 2/12 - 9/12 : 8 months….Detailed layout.
  - PCB trace layout...requires pin out understanding
  - some preliminary parts ordering
  - identify potentially long-lead time parts
  - pre-production review
- 10/12 - 1/13 : 4 months….Prototype fabrication, power up/functionality tests
  - Release PCB to vendor - month to fabricate
  - Procure all parts
  - Outside assemble boards - month to fabricate few boards
  - Leave at least 2 months for power up/functionality tests in basic test stand @MSU
  - Specialized firmware and software required for testing
- 2/13 - 7/13 : 6 months….Depth Testing/Installation/Commissioning.
  - First real need of a fully-functioning test stand @CERN as prototypes will be sent.
  - run all inputs and outputs simultaneously @ CERN test stand
  - test that algorithms all function as planned
  - Installation into L1Calo trigger as appropriate (since in shutdown)
  - Commissioning in situ if prototypes sufficiently useful
- 8/13 - 12/13 : 5 months….Final fabrication, powerup/functionality tests
  - Fabricate and assemble full set cards - ~2 months
  - Power up/functionality tests on all final cards - 2 months @ MSU
  - QC procedures established
- 1/14 - 6/14 : 6 months….Depth Testing/Installation/Commissioning.
  - run all inputs and outputs simultaneously@ CERN test stand
  - test that algorithms all function as planned
  - Installation into L1Calo trigger
  - Commissioning in situ and then with data

6.2 HARDWARE DEVELOPMENT

Engineering design

Detailed design of the CMX is based on the current CMM design, adapted to the new available components and on the results of the BLT [4], GOLD [5] and High-Speed Links [9] study and prototyping.

The outcome of this detailed design phase is the engineering implementation of individual parts of the CMX and appropriate components selection as the input to the complete CMX schematic capture.

Schematic capture

The CMX schematic capture is done on (Cadence, Mentor?) system.

PCB layout

The CMX PCB layout is done on (Cadence, Mentor?) system.

6.3 FIRMWARE DEVELOPMENT

Firmware development framework

The CMX project includes a number of firmware sub-projects:

- Porting the existing CMM firmware to the new CMX hardware,
- Creating the new firmware necessary to contend with new interfaces of CMX and FPGA,
- Creating the new algorithms necessary to receive new data formats, transmit data on high-speed links and add the topological functionality.

The overall infrastructure (VHDL firmware framework) will be created in order to achieve these goals and give the possibilities to work by several participants on different firmware sub-projects:

- Based on Xilinx ISE design tool for the FPGA used in the CMX module,
- Project settings, I/O configuration and placement, clock distribution and timing constraints,
- Test-bench with set of models for CMX external systems.

Legacy CMM firmware porting to new hardware

For the backward compatible mode of CMX operation (CMM emulation mode) different firmware versions of the current CMM have to be adapted to the new CMX hardware (new FPGA, G-Link protocol implementation in firmware) in a way that the CMX provides all the necessary functionality and satisfies the latency requirements. This task will be accomplished with the help from designers of the current CMM firmware:

- CMM e/tau firmware contact: Ian Brawn (RAL),
- CMM e/tau firmware contact: Ian Brawn (RAL),
- CMM Energy firmware contact: Ian Brawn (RAL),
- CMM jet firmware contact: Sam Silverstein (Stockholm).

Firmware for CMX interfaces

In the test and upgrade modes of CMX operation new interfaces and data formats are exploited.

The CMX receives data from processor modules in the crate at 160 Mb/s with a new data format. The backplane interface is implemented with FPGA DDR IO blocks. Data are clocked onto the CMX using encoded forwarded 80 MHz clock recovered in MMCM. The data path delay for the individual data inputs is measured using software based delay scan and adjusted using IODELAY.

The G-Link protocol is implemented using FPGA internal logic and GTX serial transmitter of FPGA. A new data format for the ROI/DAQ ROD(s) shall accommodate extra data received from the processor modules.

The optical links are implemented using FPGA internal logic and FPGA high-speed serial transmitters (GTX and GTH). They have to provide a possibility to replicate outgoing data and receive data.

Firmware for topological algorithms

The different topological algorithms for the TP and the CMX/TP will be developed inside the VHDL firmware framework follow the VHDL guidelines. Possible list of tasks/activities:

- detailed algorithm discussion and specification based on MC study and offline simulation,
- definition of necessary input data and data format,
- implementation of the algorithm simulation in C,
- implementation of the algorithm in VHDL for Virtex-6 FPGA,
- implementation of the test bed for the algorithm,
- generation of input test vectors and output results check,
- integration in the VHDL firmware framework,
- upload to the firmware repository.

The topological algorithms shall fit into latency budget.

6.4 SOFTWARE DEVELOPMENT

Offline rigger simulation

TBD

Online software and databases

TBD

Simulation software

There is a detailed software simulation framework for the L1Calo system [10]. The intention is to provide a functional description of the L1Calo trigger system at the level of data that can be recorded by the standard DAQ or in test memories throughout the system. When data are recorded at various points along the real-time path, the simulation can be used to verify the correct operation of the algorithms used. This procedure can also be used when known test data is being injected at one point of the system.

This software provides a way to model the modules and connections (as well as their settings) directly and can be integrated with the configuration database to automatically pick up the current situation. However, it does not go into the detail needed for a full hardware simulation, which would be too slow to run on a large integrated system.

Test software

At different phases of the CMX development and tests (see 6.5) test software will be needed, e.g.:

- data transfer from processors to CMX,
- new G-Link implementation (CMX /ROD) test,
- optical links tests,
- new CTP interface test…

The test software may be integrated in the online software or implemented as a standalone.

6.5 TEST AND INTEGRATION

The CMX will be initially tested at MSU at the test rig established for this purposes, then in the test rig at CERN and finally in the current L1Calo trigger system.

Test at MSU test rig

The MSU test rig (see appendix A) will provide limited possibility for the initial tests of the CMX. Limitation comes from the limited number of processor modules available as data sources (only 2 currently foreseen), simplified emulation of the CTP and the TP data receivers, and absence of the ROD emulator.

Initially the data transfer from original (backward compatible mode) and upgraded (upgrade modes) processor modules will be tested. The CTP interface, the rear module and the optical links can be tested just using the CMX itself or a second CMX in the crate (in order to test the optical link, the second CMX shall be equipped with the receiver). The ROD interface will be tested in the CERN test rig.

Test at CERN test rig

Next tests will be performed at CERN L1Calo test rig in a complete L1Calo environment. In this case more data sources are available and CMX will be connected to the real RODs and CTP emulator. Initially the backward compatible node of CMX operation (CMM emulation mode) can be tested. In order to perform realistic test of CMX in other modes, the GOLD can be used.

Test in the L1Calo system

Final test will be done in the L1Calo trigger system during the LHC shutdown. After complete test of the backward compatible node of CMX, all CMM modules in the L1Calo trigger system will be replaced with CMX modules.

Nest steps will depend on availability of the TP prototype (or GOLD) and test mode can be checked. In parallel, the preparation for the tests of upgrade/standalone modes will be done and the operation of the CMX will be defined.

APPENDIX A: MSU TEST RIG

The test rig will be required to acquire the initial knowledge on the L1Calo CMM module operation and develop and test the CMX. It will be assembled at CERN, tested and sent to MSU. The overall layout of the MSU test rig is shown in the figure below:

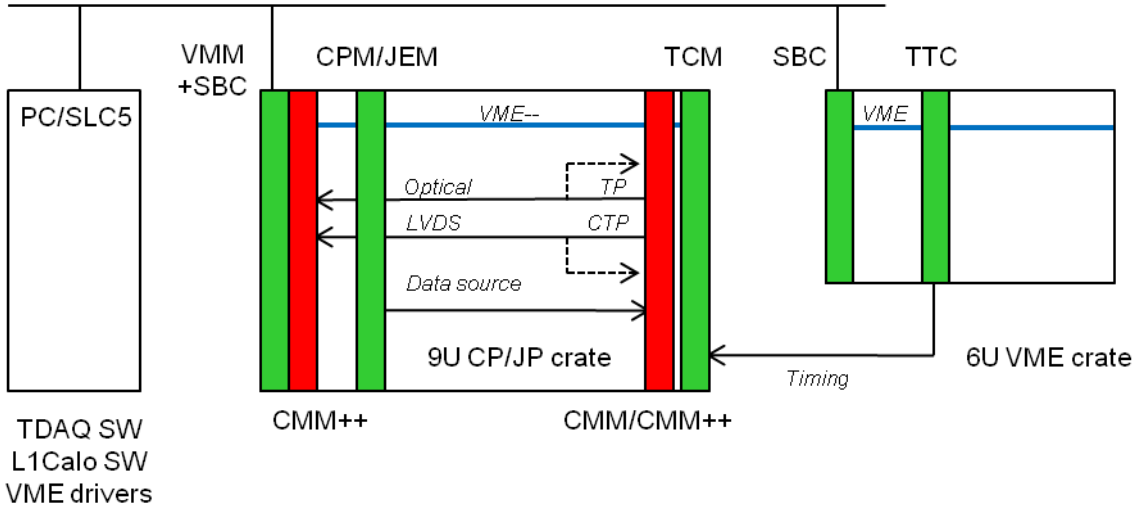


Figure 9: The overall layout of the MSU test rig

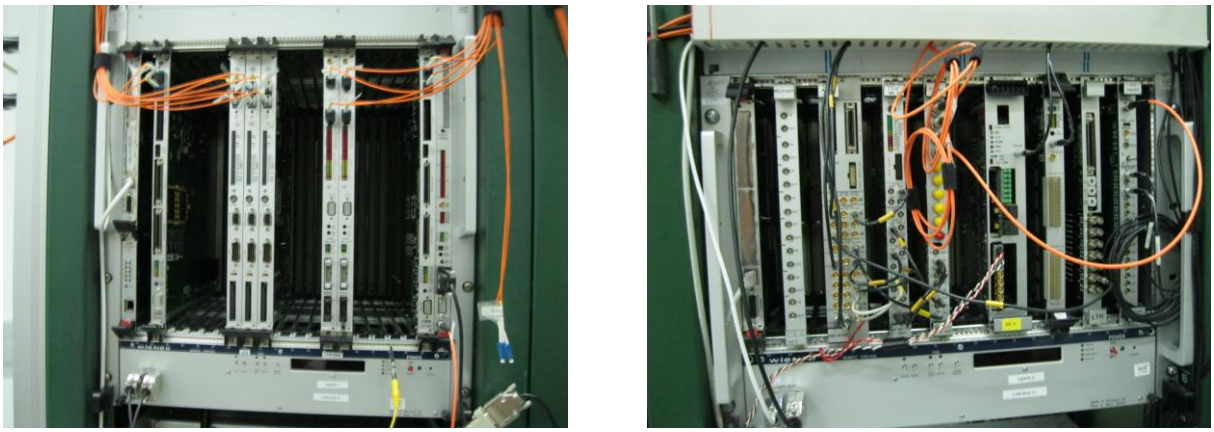


Figure 10: The 9U Cluster Pocessor (CP)/Jet Energy Processor (JEP) crate and the 6U VME crate of the L1Calo CERN test rig

The hardware, needed for the MSU test rig is listed below. It will be housed in two crates:

1. 9U L1Calo custom CP/JEP processor crate with custom processor backplane and power supply. This crate will house the CMX module under the test and extra modules needed to run and test it:
   - The VME Mount Module (VMM), which accommodates a 6U VME Single Board Computer (SBC - Concurrent Technologies VP315) in 9U VME mechanics and bridges the standard VME bus on the 6U SBC to a reduced VME bus (named VME--) on the processor backplane. The VMM is used to control other modules in the crate from the test rig software. http://hepwww.rl.ac.uk/Atlas-L1/Modules/VMM/VMM_ProductionVersion2.4.pdf
   - The Timing Control Module (TCM) which provides for the final stage of the clock distribution from the ATLAS Timing, Trigger and Control (TTC) system; provides an

interface to the ATLAS Detector Control System (DCS) - temperature and voltage information from all modules in a crate; provides a diagnostic VME bus display, which is particularly necessary for the custom backplane in CP and JEP crates.
http://hepwww.rl.ac.uk/Atlas-L1/Modules/TCM/TCM_V1_0_5.pdf

- The Common Merger Module (CMM) – for the initial tests in order to acquire initial experience with the 40 MHz data transfer in the L1Calo system. This module will be later replaced by the CMX module.
  http://hepwww.rl.ac.uk/Atlas-L1/Modules/CMM/CMM_V1_8.pdf
- The Cluster Processor Module (CPM) and Jet Energy Module (JEM) as data sources with original firmware (for initial 40 MHz data transfer tests with the CMM module) and modified firmware (for the 160 MHz data transfer in the upgraded L1Calo system). In order to test fully populated crate of the L1Calo system (14 slots of CPM modules or 16 slots of JEM modules), these modules may be substituted by the emulators (to be discussed).
  http://hepwww.rl.ac.uk/Atlas-L1/Modules/CPM/CPM_Specification_2_03.pdf
  http://hepwww.rl.ac.uk/Atlas-L1/Modules/JEM/JEMspec12d.pdf

2. Ordinary 6U VME crate with extra modules to run the system:
   - 6U SBC (Single Board Computer , Concurrent Technologies VP315) to control the modules in the 6U VME crate from the test rig software.
     http://www.cct.co.uk/sheets/VP/vp31502xu.htm
   - TTC modules (TTCvi, TTCex and LTP) to emulate the CTP (L1Accept) and the TTC system.
     TTCvi: https://edms.cern.ch/file/110746/2/writeup_mk2.pdf
     TTCex: https://edms.cern.ch/file/305816/1/TTCexManual.pdf (can be replaced by TTCvx: https://edms.cern.ch/file/292649/1/manual.pdf)
     LTP: https://edms.cern.ch/document/374560

The list of the modules, needed for the MSU test rig and status of their acquisition/commissioning:

Module	Source	Comments
9U CP/JEP crate	R. Staley	Available, assembled
Power supply	R. Staley	Available
VMM	I. P. Brawn	Available, SN11
TCM	I. P. Brawn	Available, SNxx
CMM	I. P. Brawn	Available, SNxx
JEM	U. Schäfer	Pre-production (fully functional spare)
CPM	R. Staley	Available, SN06
6U VME crate	Y. Ermoline	Available
TTCvi	Y. Ermoline	Available, SNxx
TTCvx	Y. Ermoline	Available, SNxx
LTP	Ph. Farthouat	Available, SNxx
VP 315/022-96U (3pc)	M. Joos	Available
Online SW PC (SLC5)	MSU	Available
Rack for VME crates	CERN scrap yard	Available

As specified in 6.5, initially the data transfer from original (backward compatible mode) and upgraded (upgrade modes) processor modules will be tested. The CTP interface, the rear module and the optical links can be tested just using the CMX itself or a second CMX in the crate (in order to test the optical link, the second CMX shall be equipped with the receiver). The ROD interface will be tested in the CERN test rig.

APPENDIX B: DATA FORMATS

No data format changes are foreseen for the "Backward compatible" (see 5.1) mode of CMX operation (CMM emulation mode).

Data formats for the "Data source for TP" mode / "Test" sub-mode are not defined yet as the deployment of this sub-mode is not yet clear.

The following data formats are proposed for the other sub-modes of the "Data source for TP" mode and "Standalone" mode.

CPM

Cluster Processing to Hit Merger

In the CPM module data can be transferred from CP to HM FPGAs at 80 MHz – 2x current rate, 8 extra bits in addition to 8-bit hit map (0.2 x 0.2 precision). These 8 extra bits can be used to transfer either:

- 8 bits RoI transverse energy (E_T) or
- 6 bits E_T + 2 bits fine RoI location (0.1 x 0.1 precision).

Cluster Processor Module to CMX over backplane

Therefore, there are two proposed backplane data formats from CPM to CMX:

- 0.2 x 0.2 RoI precision, 8 bits cluster E_T for 5 RoIs:

P 1L	P 1R	P 2L	P 2R	P 3L	P 3R	P 4L	P 4R	P 5L	P 5R	P 6L	P 6R	P 7L	P 7R	P 8L	P 8R	
Cluster ET ROI 1 (8b)								Cluster ET ROI 2 (8b)								Threshold bits ROI 2 (8B)
Cluster ET ROI 3 (8b)								Cluster ET ROI 4 (8b)								Threshold bits ROI 3 (8B)
Cluster ET ROI 5 (8b)								Threshold bits ROI 4 (8B)								Threshold bits ROI 5 (8B)

- 0.1 x 0.1 RoI precision, 6 bits cluster E_T for 5 RoIs:

P 1L	P 1R	P 2L	P 2R	P 3L	P 3R	P 4L	P 4R	P 5L	P 5R	P 6L	P 6R	P 7L	P 7R	P 8L	P 8R	
Cluster ET ROI 1 (6b)						FP 1(2b)		Cluster ET ROI 2 (6b)						FP 2(2b)		Threshold bits ROI 2 (8B)
Cluster ET ROI 3 (6b)						FP 3(2b)		Cluster ET ROI 4 (6b)						FP 4(2b)		Threshold bits ROI 3 (8B)
Cluster ET ROI 5 (6b)						FP 5(2b)		Threshold bits ROI 4 (8B)								Threshold bits ROI 5 (8B)

JEM

Jet Energy Module to CMX over backplane

0.2 x 0.2 RoI precision, up to 12 bits Jet E_T (and/or other info) for 4 RoIs:

P1	P2	P3	P4	P5	P6	P7	P8	Fine Pos ROI 1	Fine Pos ROI 2	Fine pos ROI 3	Fine Pos ROI 4	
												Threshold bits ROI 1 (8b)
												Threshold bits ROI 2 (8b)
Jet ET ROI 1 (12b)				Jet ET ROI 2 (12b)				Jet ET ROI 3 (12 b)		Jet ET ROI 4 (12b)		Threshold bits ROI 3 (8b)
												Threshold bits ROI 4 (8b)

The above data formats are not exactly backward compatible. The hit count multiplicities saturate at 4/5 per JEM/CPM instead of 7, so the CTP results are in theory not quite EXACTLY the same as in the "Backward compatible" mode of CMX operation.