CMX
(Common Merger eXtension module)

Y. Ermoline for CMX collaboration

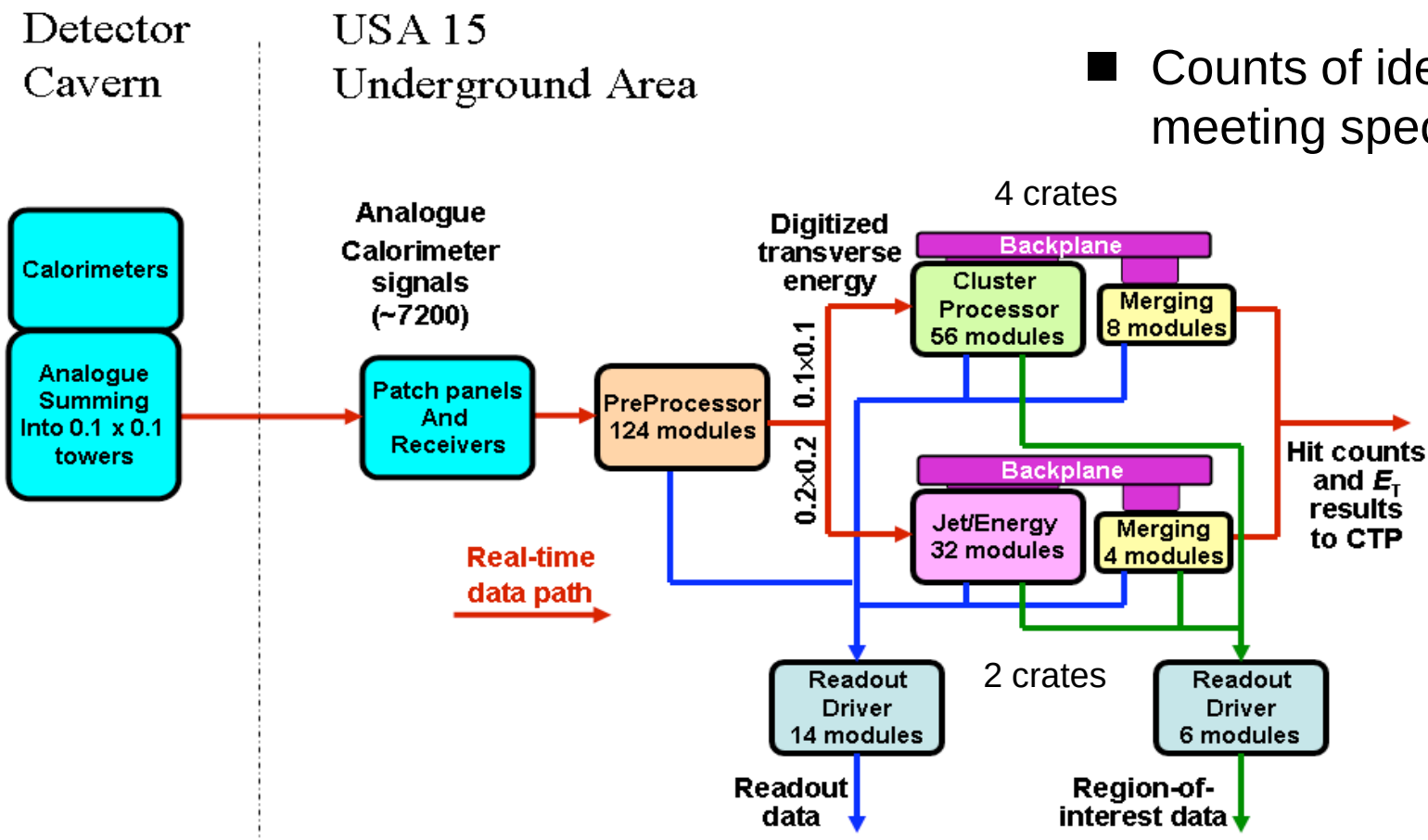
Preliminary Design Review,

Stockholm , 29 June 2011

Outline

- Current L1 Calorimeter trigger system
  - Possible improvement to maintain trigger quality
- Topology information in real-time data path
  - Functional requirements
  - Project specification overview
  - Development schedule
- Technical aspects
  - CMM/CMX differences
  - FPGA & Links
- CMX modes of operation
- CMX firmware development
- MSU test stand

Current L1 Calorimeter trigger system

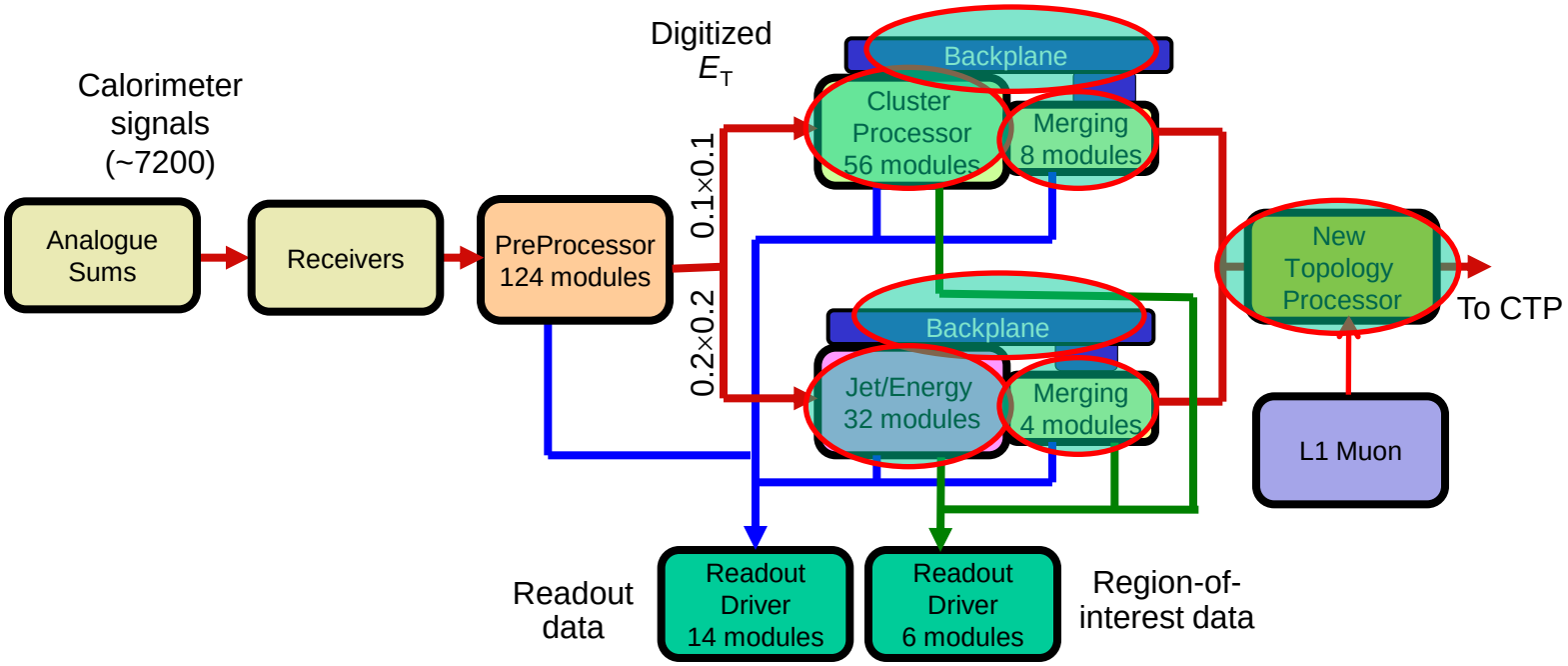


- Counts of identified objects meeting specified thresholds.
- Jets and em/tau clusters identified in different subsystems
- Region of Interest (ROI) topology information read-out only on L1Accept.

Possible improvement to maintain trigger quality

- Add topology information to the real-time data path
- Examples using local topology information (single calo quadrant)
  - Identify spatial overlap between e/tau clusters and jets
  - Use local jet Et sum to estimate energy of overlapping e/tau object
    - ⇨ Requires jet energies to be added to real time data path
- Examples using global topology
  - Non back-to-back jets
  - Rapidity gaps
  - Invariant or transverse mass calculations
  - Jet sphericity
- Required **upgraded CMM and Topology Processor**
- Simulation study
  - In progress (see talk on Monday)

Topology information in real-time data path



- Add ROI positions to the real-time data path, enabling new algorithms based on event topology (in new Topological Processor)
- Modify firmware in processor modules to increase data transfer rate over crate backplane (40 Mbit/s -> 160 Mbit/s)
- Replace merging modules (CMM) with upgraded hardware (CMX)
- Add new Topological Processor (TP)

CMX functional requirements

- Backward compatibility :
  - be designed to fit in the CMM positions in the processor crates ,
  - inherit all main logical components, electrical interfaces, programming model and data formats of the current CMM,
  - be able to implement all different versions of CMM FPGA logic, adapted to new hardware.
- Data source for topological processor:
  - receive extra data from upgraded processor modules over the crate backplane at higher data transfer rate (160Mb/s),
  - transmit data to the TP via multi-fiber optical ribbon link(s),
    - ⇨ optionally – electro-optical data replication using available spare transmitters
  - transmit extra data from upgraded processor modules to the L1Calo DAQ and RoI Read-Out Drivers (RODs).
- “Insurance policy" option against unforeseen
  - Optional standalone mode - may require (unnecessary) extra complexity
    - ⇨ have to be weighted against benefits

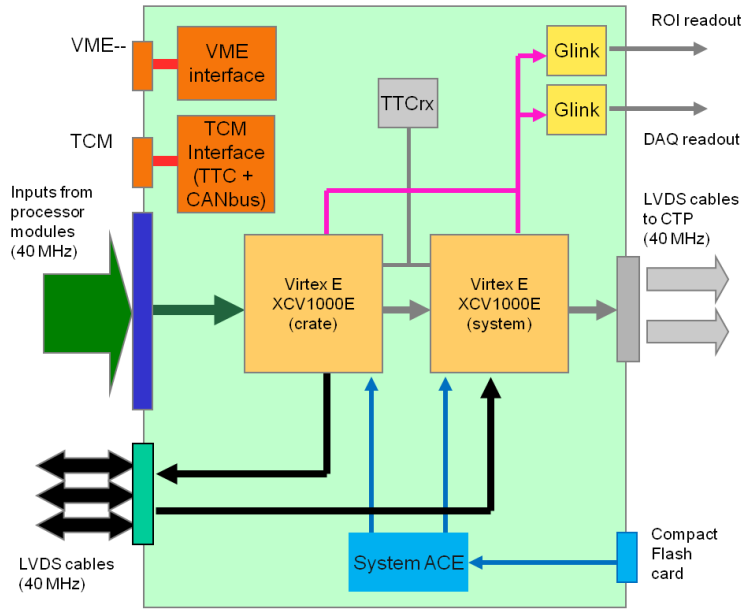
CMX project specification overview

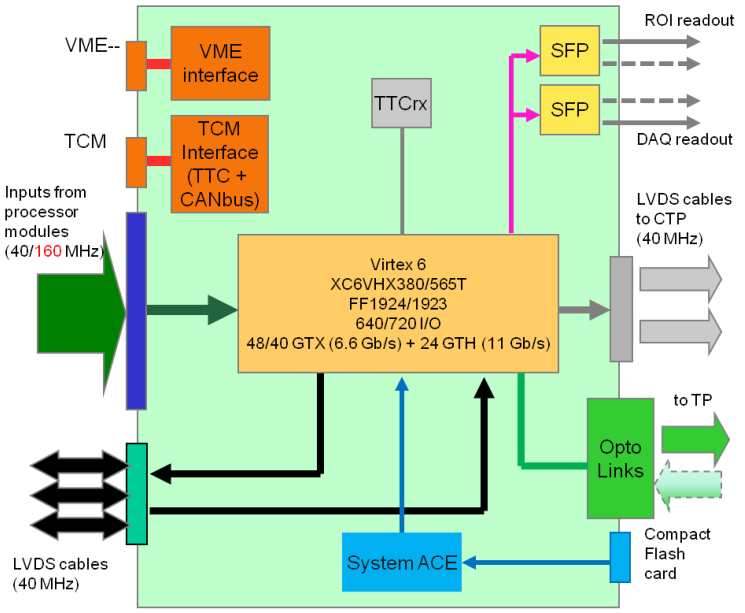
- The version 0.7 of the CMX project specification available:
  - http://ermoline.web.cern.ch/ermoline/CMX/
- This document specify:
  - CMX functional requirements,
  - CMM/CMX differences,
  - technical aspects of the CMX implementation.
    - ⇨ The engineering solutions will be reflected in the following detailed hardware and firmware specifications
- Comments from Jim, Uli, Ian, Sam, Dan, Philippe, Hal, Chip
  - Added into document
- Next steps:
  - Jul 2011 - Jan 2012: Preliminary design study, engineering specification, design documentation, test rig checked out at MSU
  - Feb 2012 - Sep 2012: Prototype design and test
    - ⇨ Sep 2012: Production Readiness Review

CMX development schedule

- 2011: Project and engineering specifications
  - CMX project Preliminary Design Review (this week)
  - Preliminary design studies
  - Test rig installed, checked out at MSU
- 2012: Prototype design and fabrication
  - CMX schematics and PCB layout
  - Production Readiness Review
  - Prototype fabrication, CMM firmware ported on CMX
  - Basic tests for backward compatibility in test rig at MSU
- 2013: Prototype testing/installation/commissioning, final fabrication
  - Full prototype tests in test rig at CERN
  - CMX firmware development and test
  - Test in the L1Calo system during shutdown
  - Fabricate and assemble full set of CMX modules
- 2014: Final commissioning in the L1Calo trigger system in USA15

Technical aspects (1): CMM/CMX differences



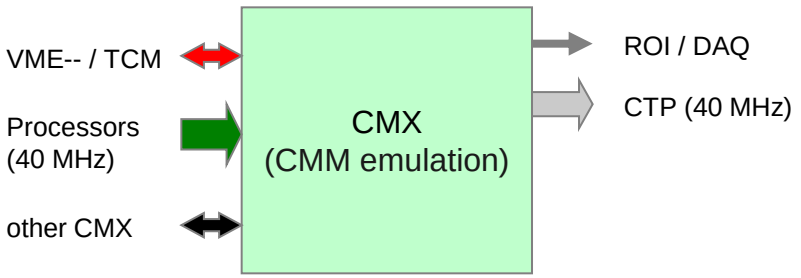


- Main modifications to the CMM hardware:
  - replacement of the obsolete FPGA devices by new parts to receive data at 160Mb/s from the backplane, transmit and receive data via multi-fiber optical ribbon link using transceivers in FPGA,
  - implementation of the G-link protocol in firmware,
  - implementation of multi-fiber optical ribbon links.

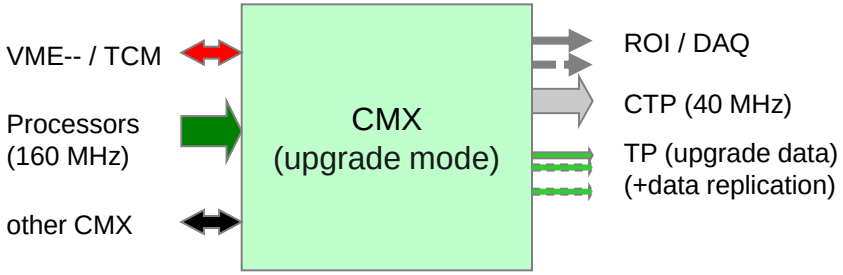
Technical aspects (2): FPGA & Links

- The new FPGA or FPGAs for the CMX board shall provide sufficient:
  - IO pins, compatible with the L1Calo system backplane signal levels,
    - ⇨ pins (~640) for all external interfaces of two original CMM FPGAs
  - high speed serial transceivers for data transmission and reception,
    - ⇨ Minimum: 8 to 18 transmitters (TP, RODs); optionally - fan-out and reception
  - internal logical resources (logical blocks and memories).
    - ⇨ Virtex 6 / Virtex E: ~ x2 LUTs, x4 FFs, x10 RAM, x2.5 faster
- G-Link implementation
  - Original part obsolete:
    - ⇨ G-Link transmitter chips (HDMP 1022) -> G-Link protocol emulation in FPGA
    - ⇨ FPGA GTX transmitter at 960 Mbit/s
    - ⇨ Transceiver Infineon V23818-M305-B57 -> Avago AFBR-57M5APZ
- Multi-fiber (12 fibers) optical ribbon links
  - GTX and GTH Virtex 6 FPGA transceivers
  - parallel fiber modules: SNAP12 or Avago (-> compatible with TP)

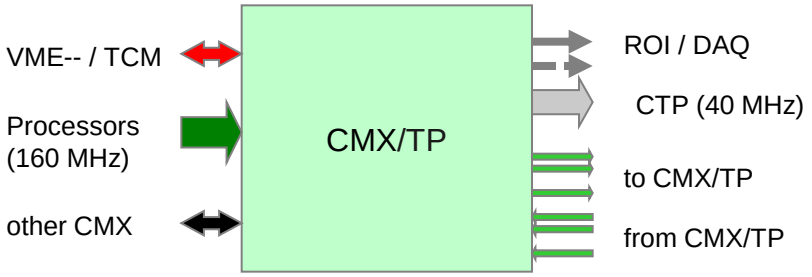
CMX modes of operation overview



- Backward compatible mode:
  - CMM firmware ported to CMX h/w
  - Looks like CMM in current system
  - No optical links to TP



- Upgrade mode:
  - new data format
  - data processing/reduction
    - ⇨ to fit links in a single TP module
  - data replication to multiple TPs



- Standalone mode (optional) :
  - “Insurance policy" option
  - data reception from other CMX

Backward compatible mode

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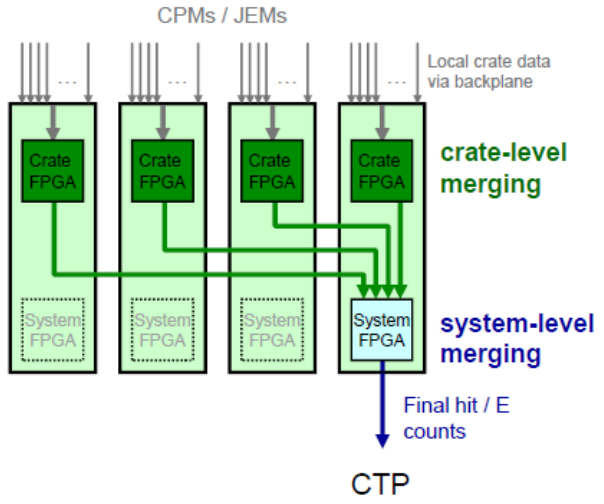
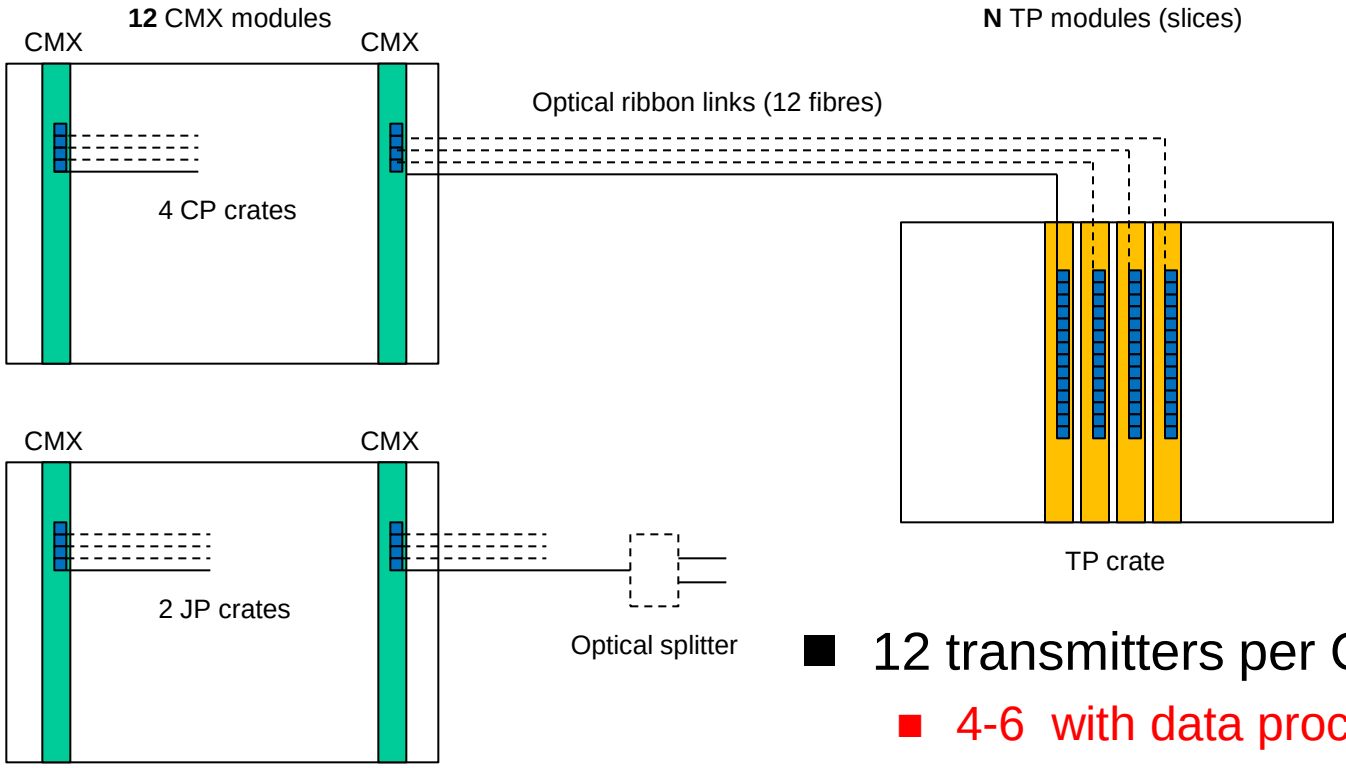
The Common Merger Module (CMM)

- CP (e/γ) / Tau hits:
  - 3-bit multiplicity x 16 threshold sets x 56 CPMs (4 crates) → 3 bits x 16 threshold sets
- Jet hits:
  - 3-bit multiplicity x 8 thresholds x 32 JEMs (2 crates) → 3 bits x 8 thresholds
  - 2-bit multiplicity x 8 thresholds x 4 JEMs (2 crates) → 2 bits x 8 thresholds (forward jets)
- Total E_T:
  - Sum E_T over 32 JEMs (2 crates) & compare with 4 thresholds → 4 bits
- Missing E_T:
  - Vector sum $E_X \oplus E_Y$ over 32 JEMs (2 crates) & compare with 8 thresholds → 8 bits
- Organised in tree structure:
  - all CMMs receive CPM/JEM data over backplane & perform crate-level merging
  - 1 CMM / tree also receives crate-level results via cable & performs system-level merging
  - CP / Tau system: 4 CMMs x 2
  - Jet hits: 2 CMMs
  - Energy: 2 CMMs



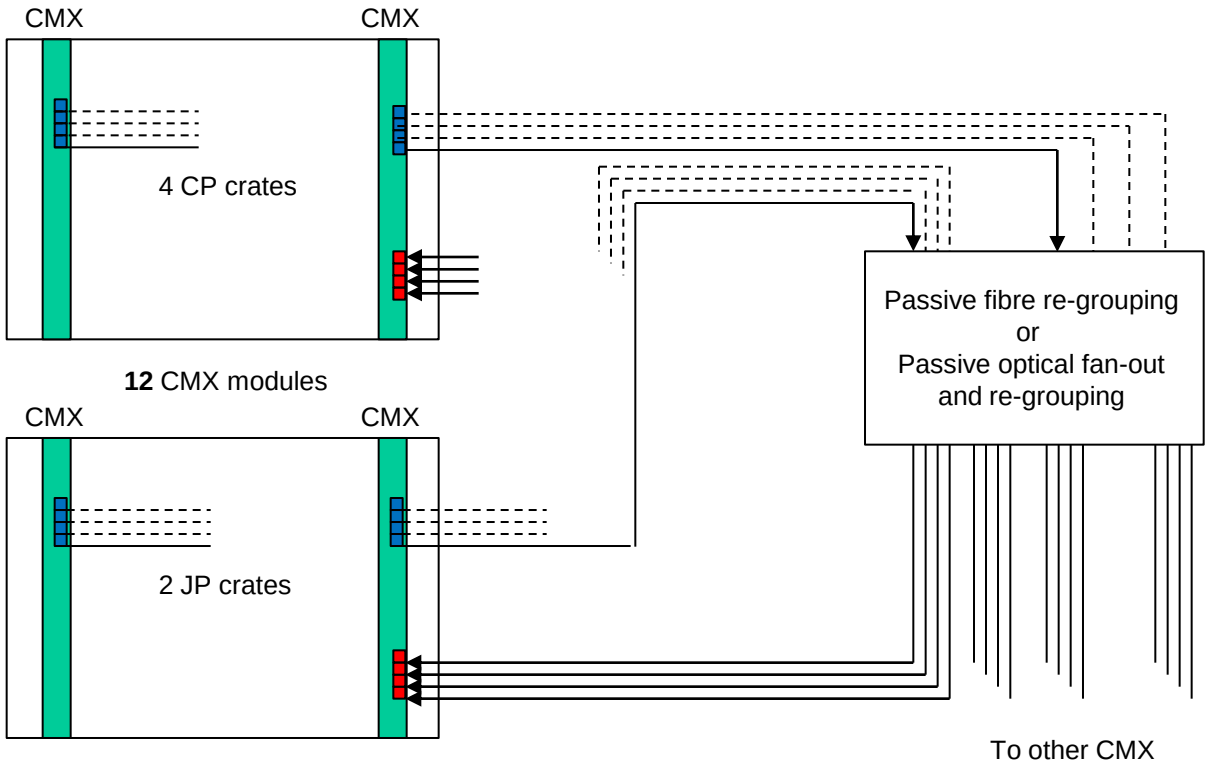
- 2 FPGA transmitters for the DAQ and ROI G-Links

Upgrade mode with data replication / fan-out



- 12 transmitters per CMX
  - 4-6 with data processing
- 4-6 transmitters for the DAQ and ROI G-Links (not shown)
- Spare transmitters (out of 72) - for data replication / fan-out to N TPs
  - 54-64 with data processing

Standalone mode (optional)



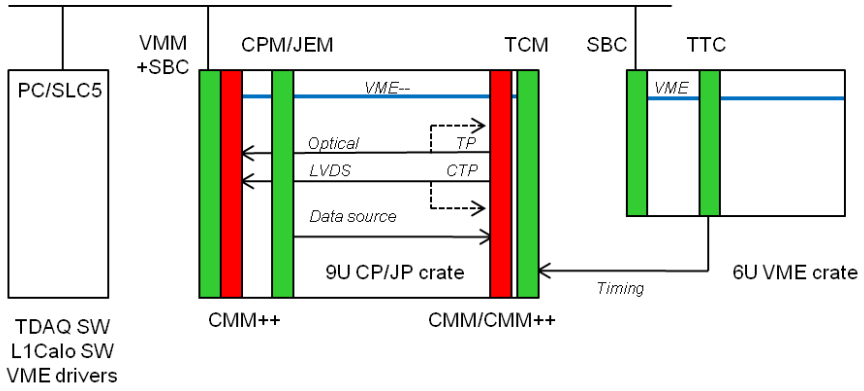
- CMX modules may be used without TP
  - The role of the topological processor can be executed by one (or several) CMX module(s) in the system.
- Require inter CMX communication - data fan-out and re-grouping

CMX firmware development

- Two little-overlapping activities with different sub-sets of people
- Porting the existing CMM firmware to the new CMX hardware
  - MSU (CMX), RAL/Stockholm (CMM) + ?
  - new FPGA selection, I/O pin allocation, signal levels, clock distribution
  - new G-Link implementation in FPGA will be used in upgrade modes
  - test firmware in the test rig hardware, no VHDL test-benches
- New firmware for the upgrade modes of CMX operation
  - MSU (CMX), Mainz (TP, JEM), Birmingham (CPM), RAL (ROD) + ?
  - new CMX interfaces development, data transfer CMX->TP (MSU)
  - algorithm development for the TP (Mainz),
    - ⇨ Optionally - applicability for CMX (MSU)
  - test-benches:
    - ⇨ data source for CMX from upgraded CPM (Birmingham) and JEM (Mainz)
    - ⇨ data source for TP from CMX (MSU) [also for ROD and CTP ?]
  - Data files for the test-benches:
    - ⇨ from simulation software and MC

MSU test stand

Proposed MSU test stand



CPM/Jem and TTC crates at CERN

- The test rig will be required:
  - To acquire initial knowledge on CMM module operation
  - To develop and test the CMX
- Initially assembled at CERN, tested and then sent to MSU
  - Hardware (without DCS)
  - Online software
  - Online simulation
- Hardware available
  - -> focus on software
- Testing procedure:
  - Backplane data transfer
  - Optical & LVDS links (2nd CMX)
  - ROD connection -> at CERN

Back-up slides

CMM++ installation