MICHIGAN STATE UNIVERSITY

Status of CMX design studies

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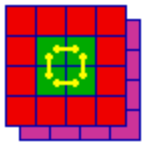
8-Feb-2012

@RAL



CMX development work on 3 fronts

1. VME/ACE/TTC interface “daughter card” @CERN
   - Yuri
2. CMX input module firmware @CERN
   - Wojciech and Yuri
3. Engineering @MSU
   - Philippe and Dan

Only focusing on #3 today

CMX Project's Goals for this meeting

We would like a short term outcome of this meeting to be:

1. "Yes/No" on continue designing for CMX-TP
   - and agreement on approach
2. Agreement on FPGA choice
3. Agreement on 10Gb output option

Initial CMX design studies phase

- Trying to address **two main questions**
  1) FPGA choice for implementing the Base-CMX functionality
  2) Strategies, costs and risks for adding Topological Processing capability to the CMX platform
- Guidance from **Stockholm review**
  - Use Virtex 6
  - Evaluate FF1924 & FF1923 packages
  - Design for 6.4Gb optical outputs
  - Implement G-link encoding on FGPA
  - → **be conservative** to deliver on time

Definition: **Base-CMX** functionality

1. **All of CMM functionality** (both Crate CMM and System CMM)
   - Receive and process 400 JEM/CPM input signals (4x higher rate)
   - Crate CMXs send local summary to System CMX through backplane connector over LVDS cables (2x higher rate probably desirable)
   - System CMXs form and send triggering information to CTP over LVDS cables (same as CMM)
   - all CMXs send ROI and DAQ information over G-links (same as CMM)

2. **Send JEM/CPM info out to a TP** optically
   - using 12-fiber bundles
   - with some level of duplication (at least 2x copies sent)
   - 6.4Gbps nominally sufficient for all raw data on **one** 12-fiber bundle
   - also possible to send zero-suppressed data on less fibers
   - SNAP12 (modified) or miniPOD available from Avago up to 10Gbps

Definition: **TP-CMX** functionality

Topological Processing capability **on CMX platform**

1. Receive optical inputs from each of 12x CMXs
2. Run multiple Topological Algorithms
3. Send Topological triggering information to CTP

- TP-CMX functionality is needed if dedicated TP not built, or availability delayed, or as additional safety/backup
- The CMX platform would then be asked to provide as much generic TP functionality as possible.
- When all final TP decisions can be made is not clear.

Nota Bene

Distinction between **locally** and **globally derived** triggering information

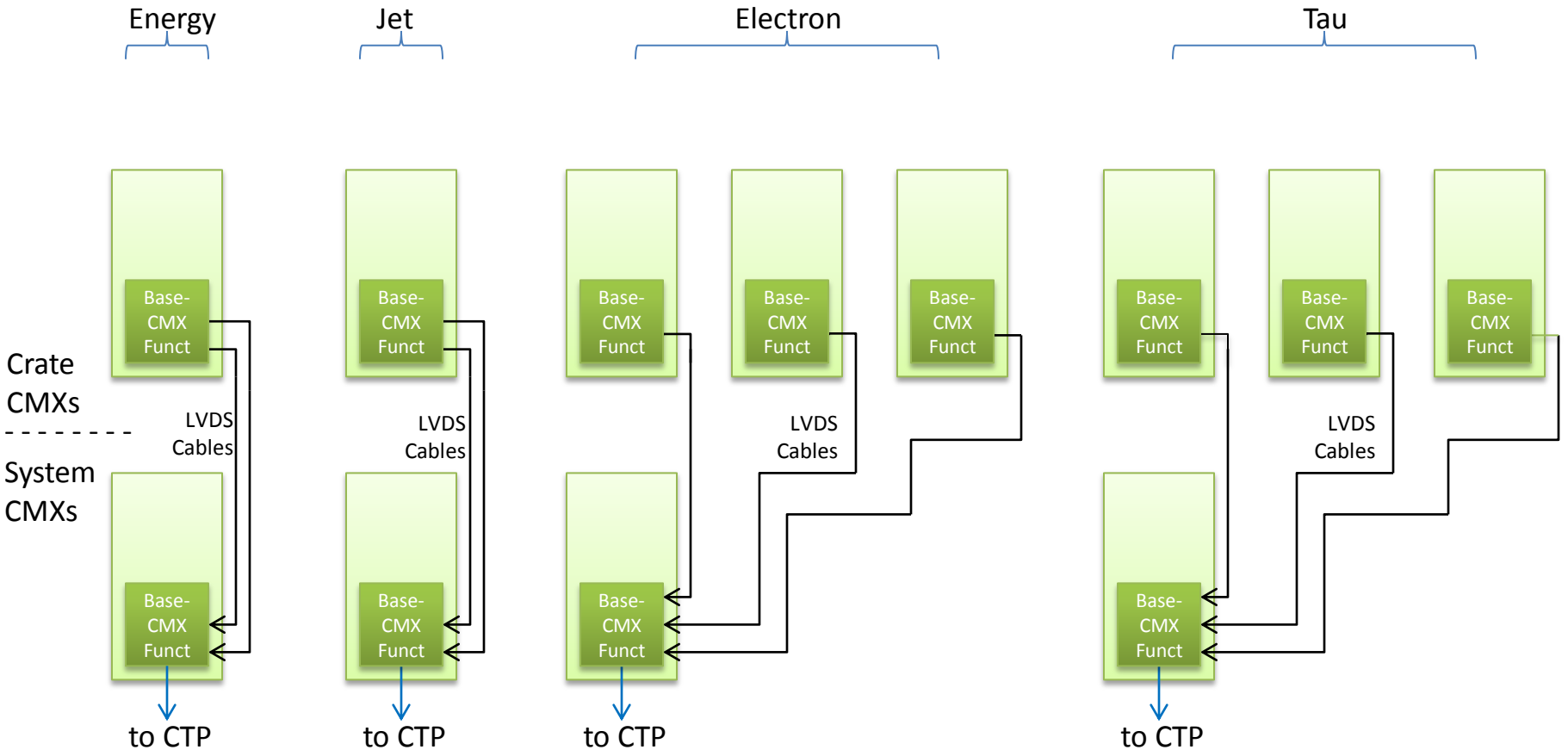
- Any Trigger Information that can be derived locally and then gathered/summed into an overall summary
  - can use the Crate->System path
  - e.g. implementing additional thresholds
- An Algorithm that correlates geographically separated or different types (e.g. electron vs jet) of information
  - needs TP architecture

Overview/Review of possible use cases

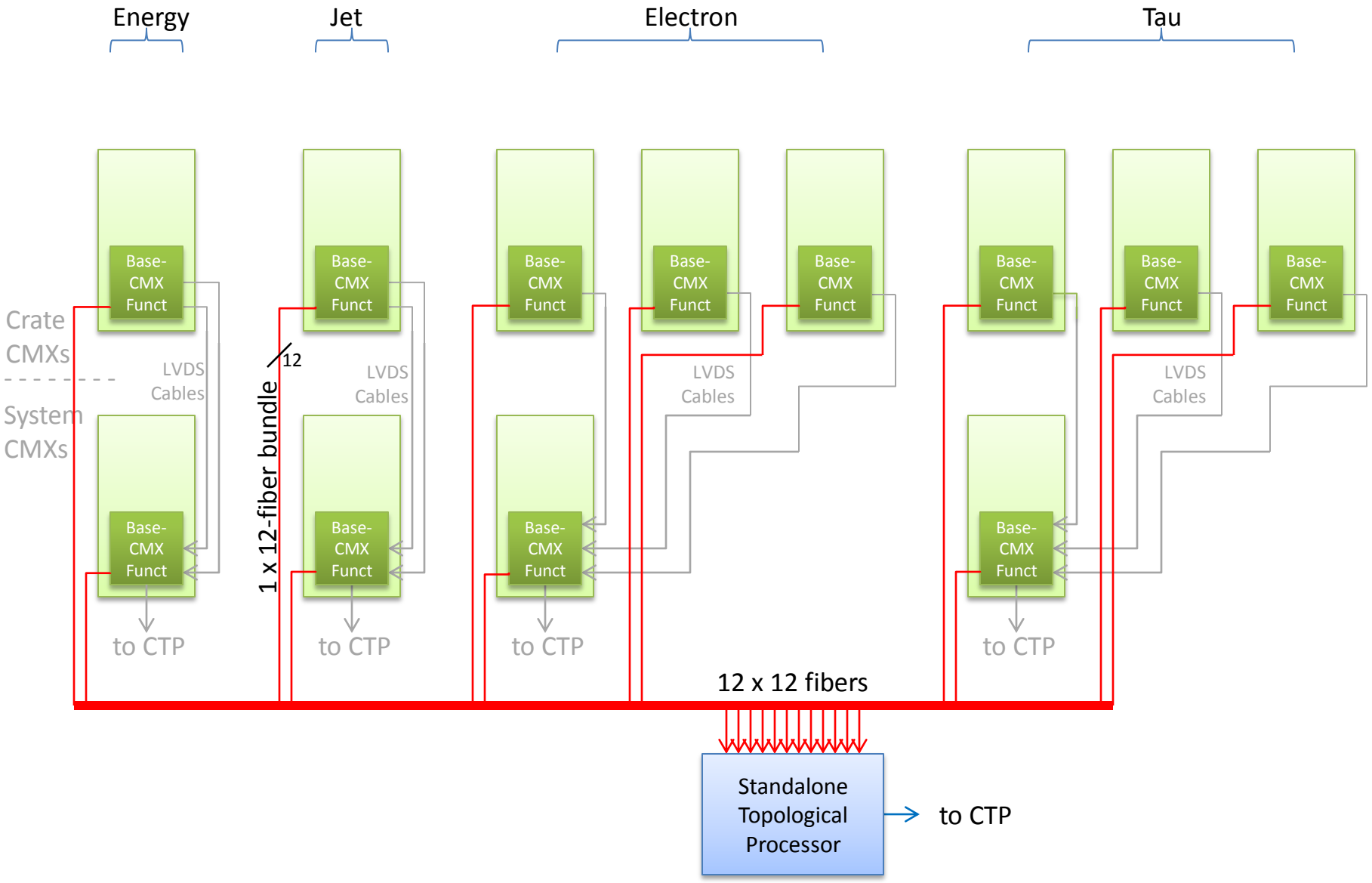
Illustrated in following diagrams…

- CMM emulation only
- Base-CMX functionality only
  - Send data to Standalone TP
- TP-CMX functionality used
  - Only CMX-TP
  - Both CMX-TP and Standalone TP

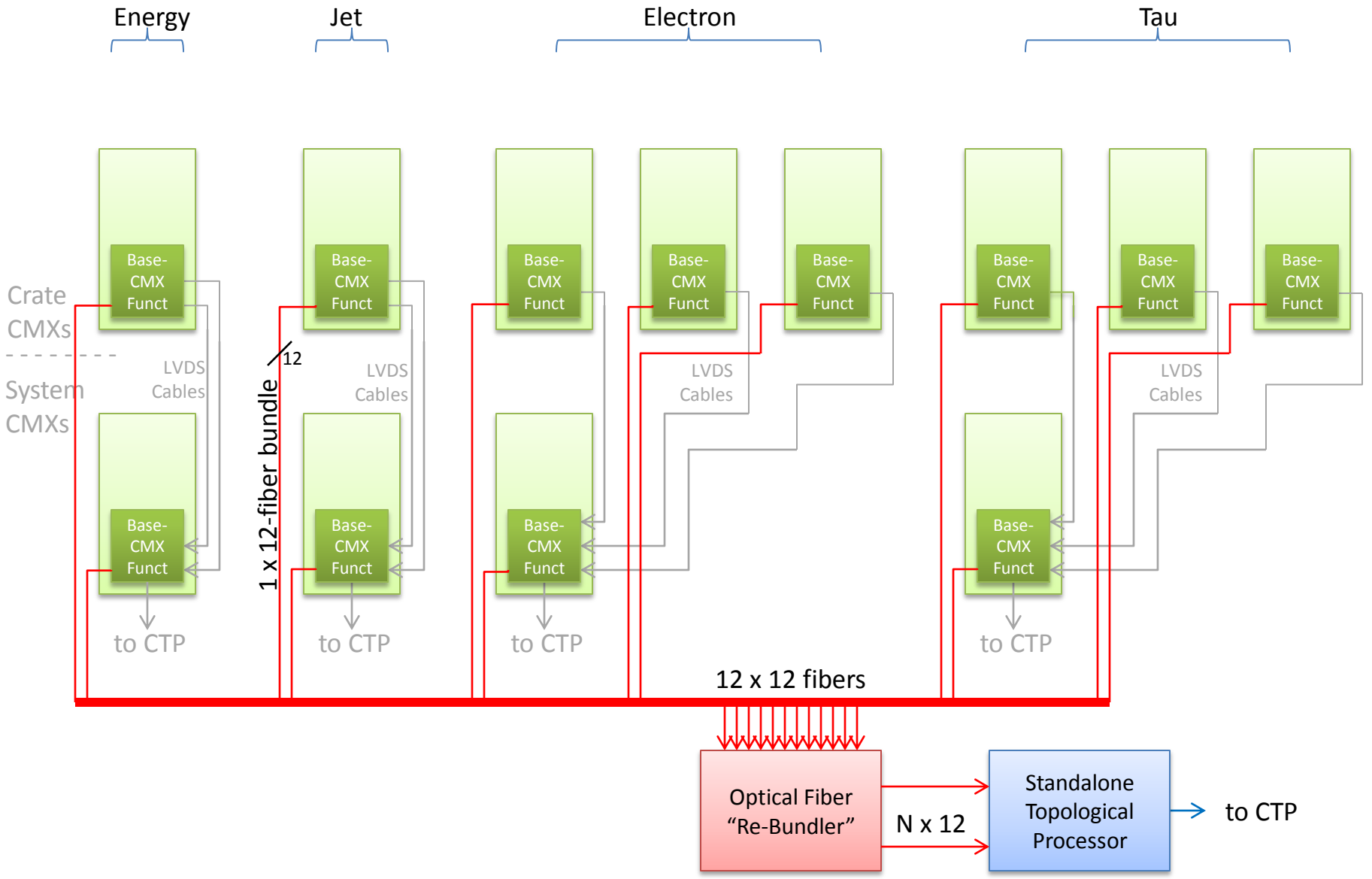
1. CMX emulation of CMM functionality (no TP involved)



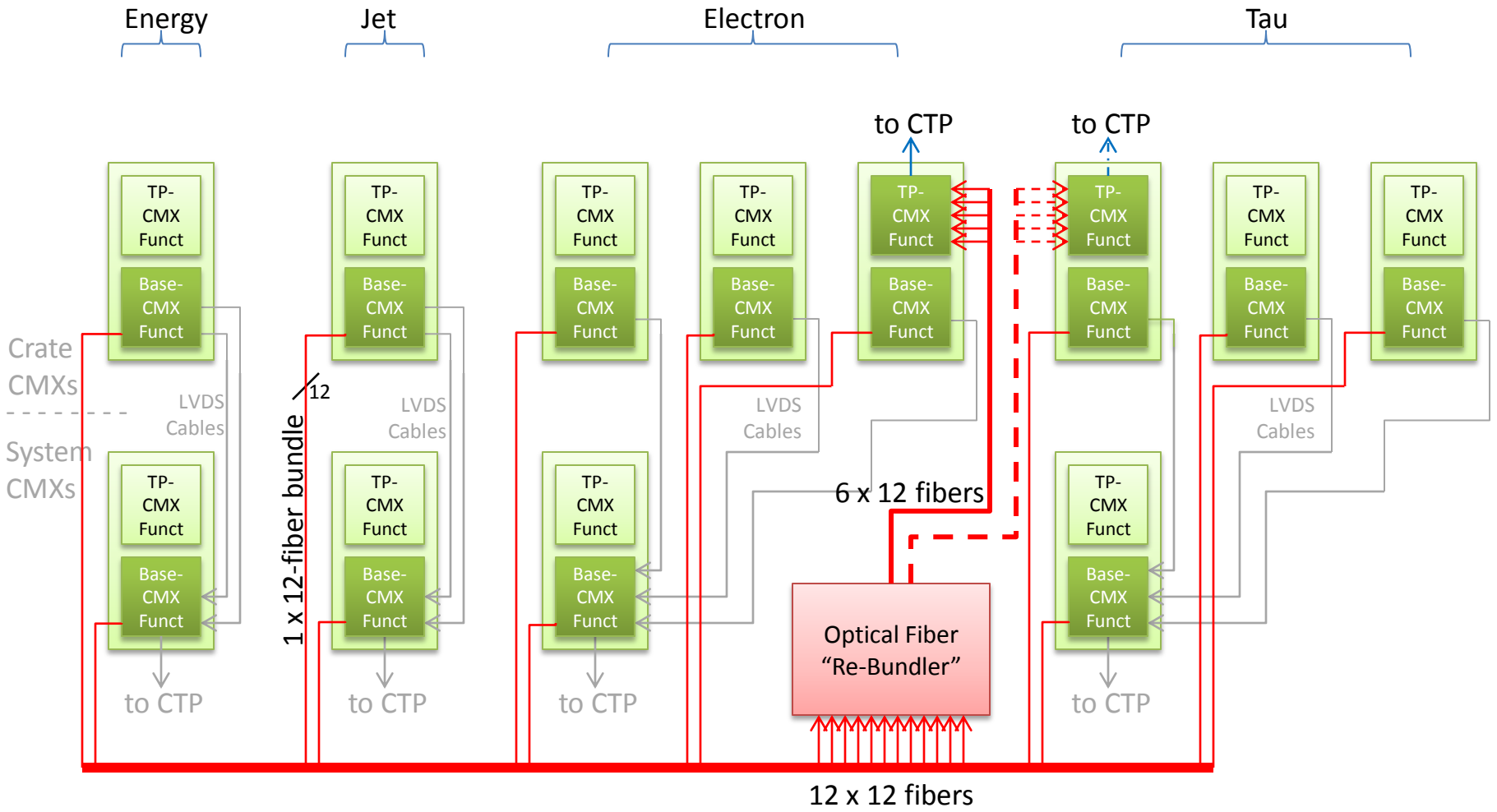
2. Standalone TP receiving Raw CMX Inputs



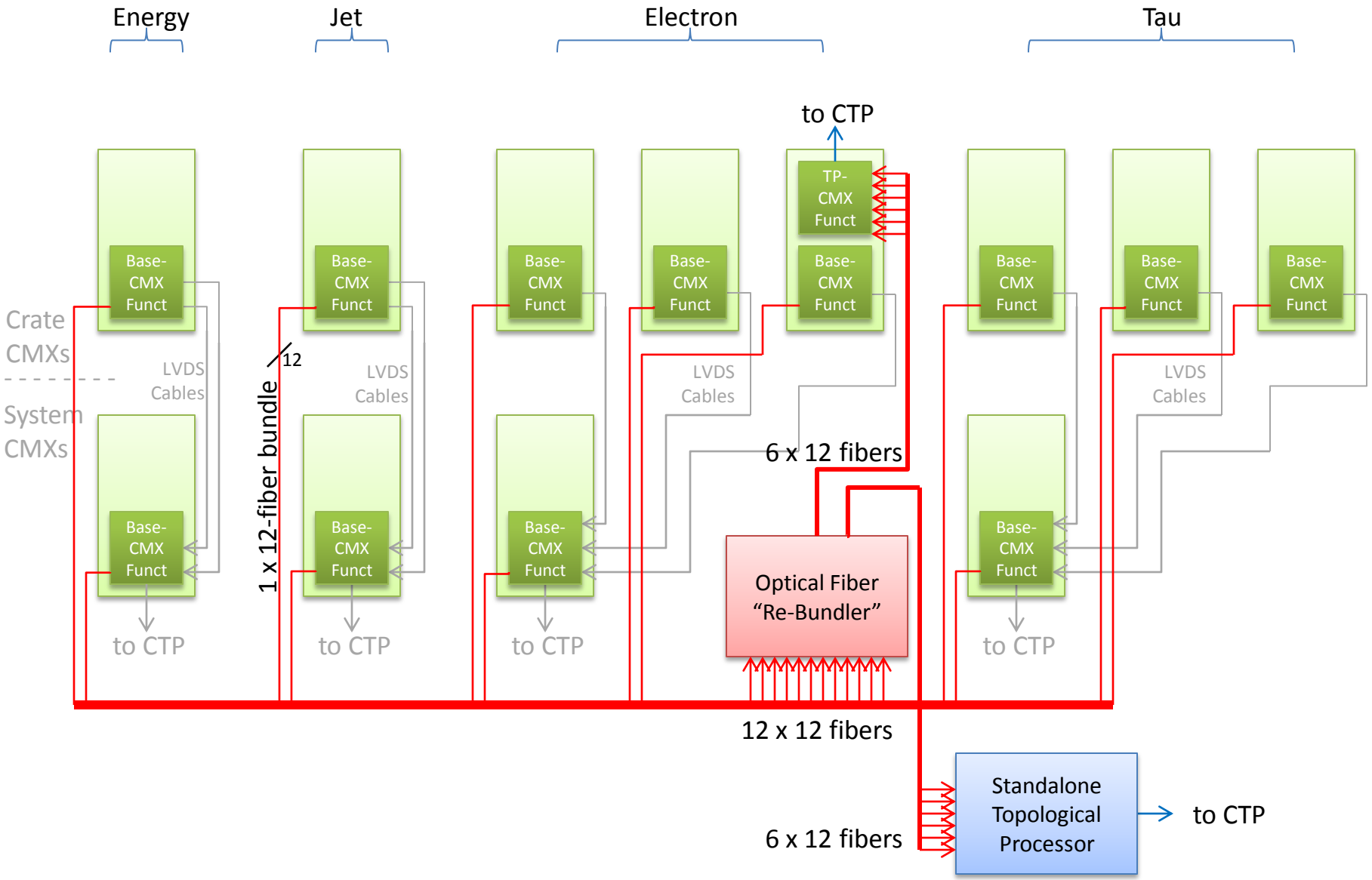
3. Standalone TP receiving Zero-Suppressed CMX Inputs



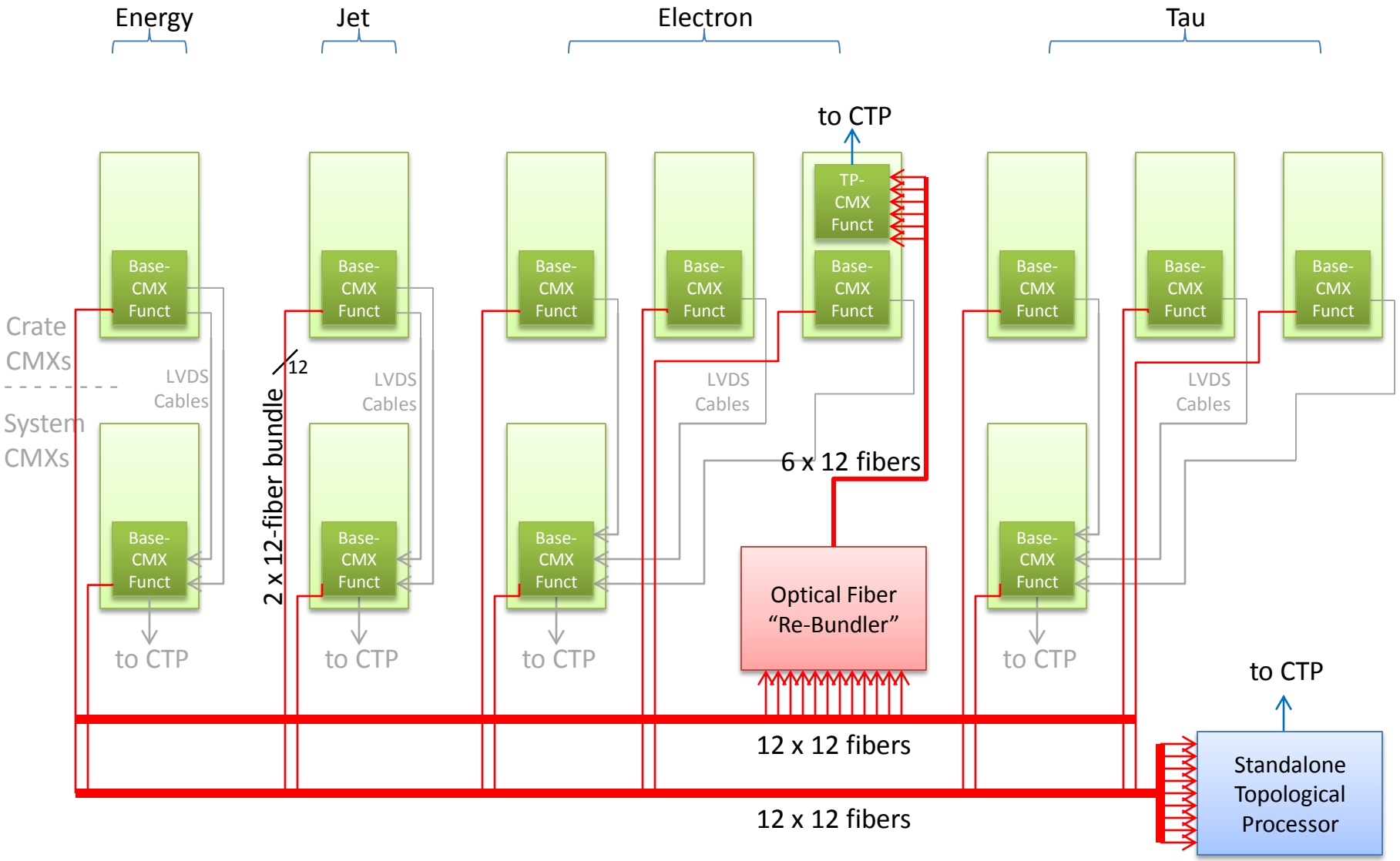
4. One (or more) CMX TP receiving Zero-Suppressed Inputs



5. CMX TP & Standalone TP receiving Zero-Suppressed Inputs



6. CMX TP receiving Zero-Suppressed Inputs & Standalone TP raw inputs



Base-CMX Implementation

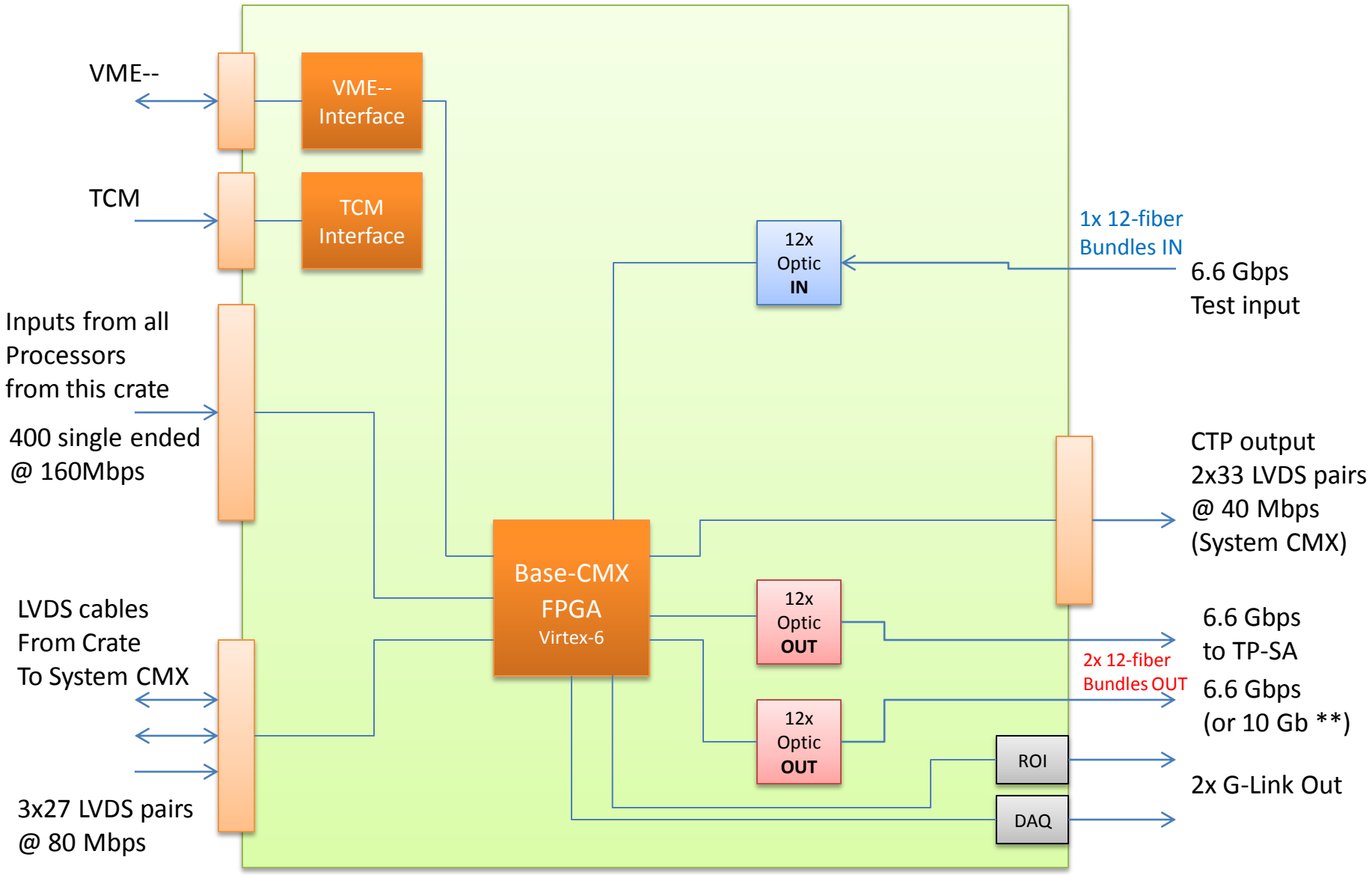
Question #1:

FPGA choice for implementing the Base-CMX functionality

Base-CMX Implementation

- 400x 160Mbps backplane inputs
  - routed directly to FPGA, no termination on CMX
  - merged parity and clock
    - cannot afford 1x IO block per source JEM/CPM processor
    - but need regrouping in neighbor IO blocks
  - Processor sources spread out on backplane connectors
- Up to 3x 12 “6Gb” optical transceivers (2 out, 1 in)
  - multi gigabit transmission lines
    - need careful layout and field simulation tools
  - use mid-board transmitters for shorter traces
    - need optical power study of whole optical distribution
  - compete for access to, and real estate near, FPGA
  - will need protocol to transfer 12x 6.4 Gbps of payload + overhead
    - XILINX notes have example
  - needs external oscillator, not necessarily synchronous with accelerator
- Large FPGA package require many trace layers

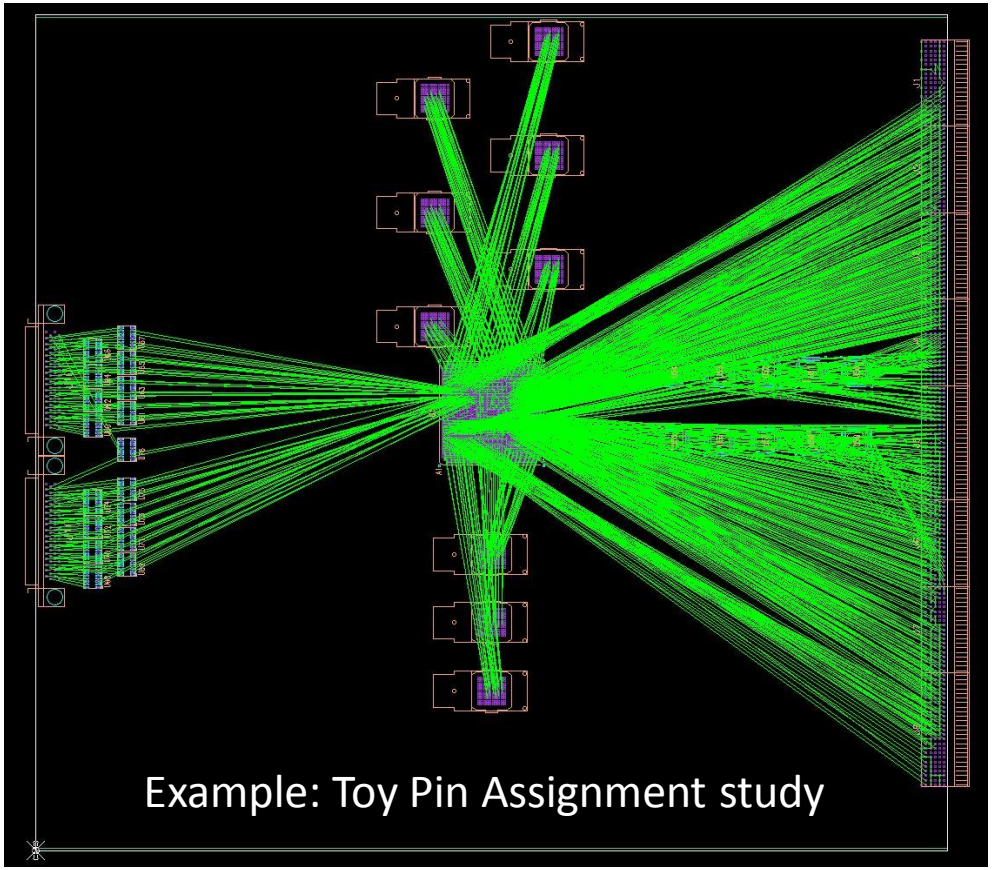
A. CMX Card with only Base-CMX functionality



** 10Gb output to TP-Standalone option to be determined

Package Choice and Pin Assignment

- Made toy layouts using several packages
- Focusing on main signal flow (PreProc In, Cable IO, CTP Out)
- Helps visualizing challenges



FF1924

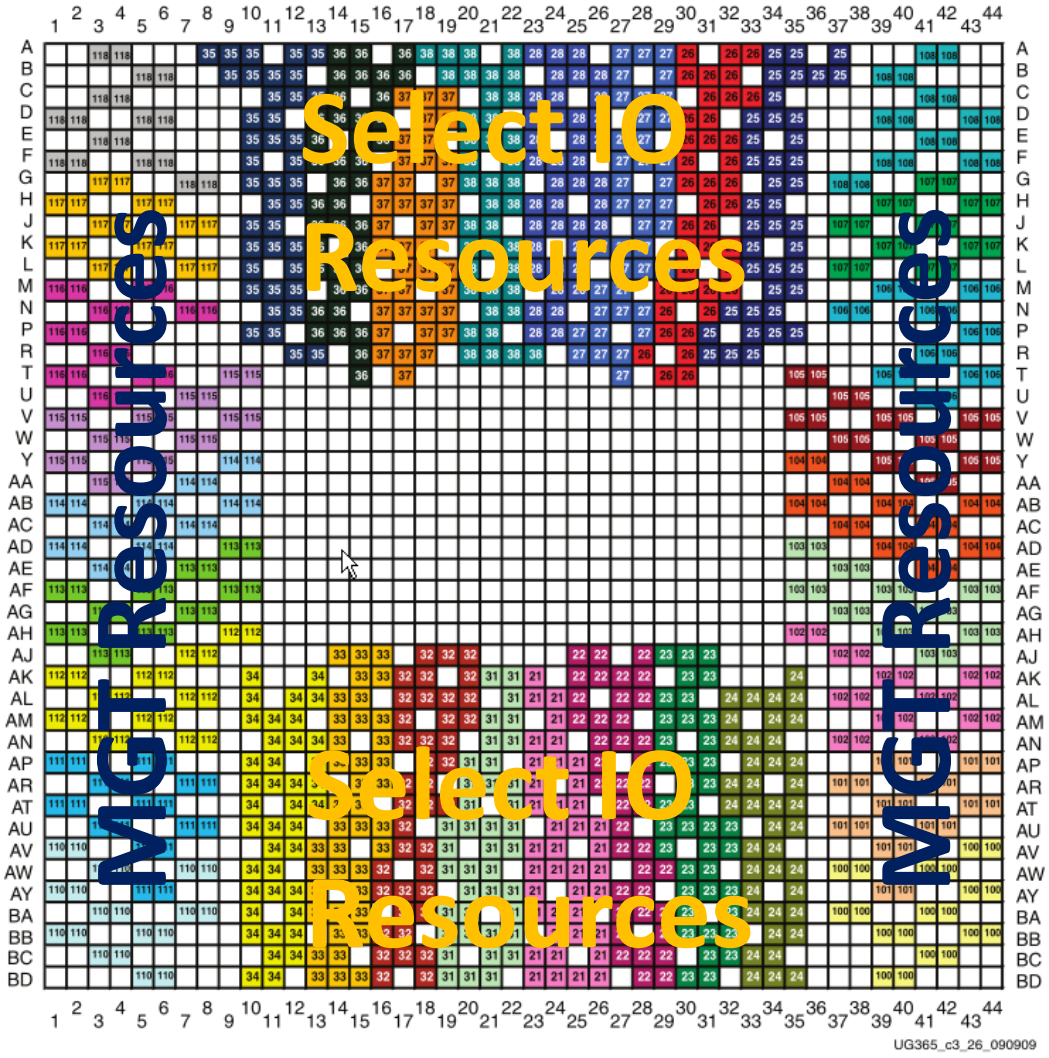


Figure 3-26: **FF1924 Package–HX380T and HX565T I/O Bank Diagram**

FF1924

Front Panel Side

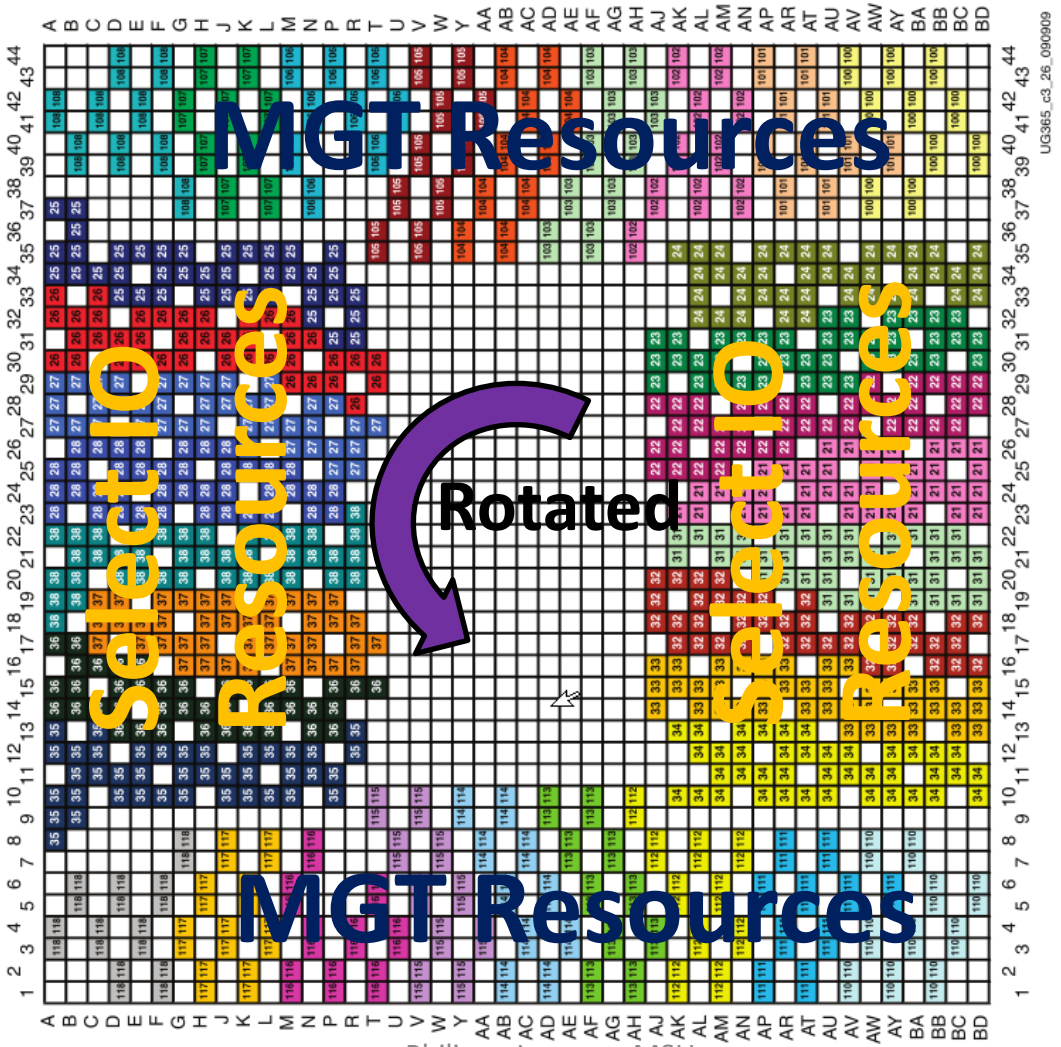


Figure 3-26: **FF1924 Package—HX380T and HX565T I/O Bank Diagram**

Backplane Side

FF1924

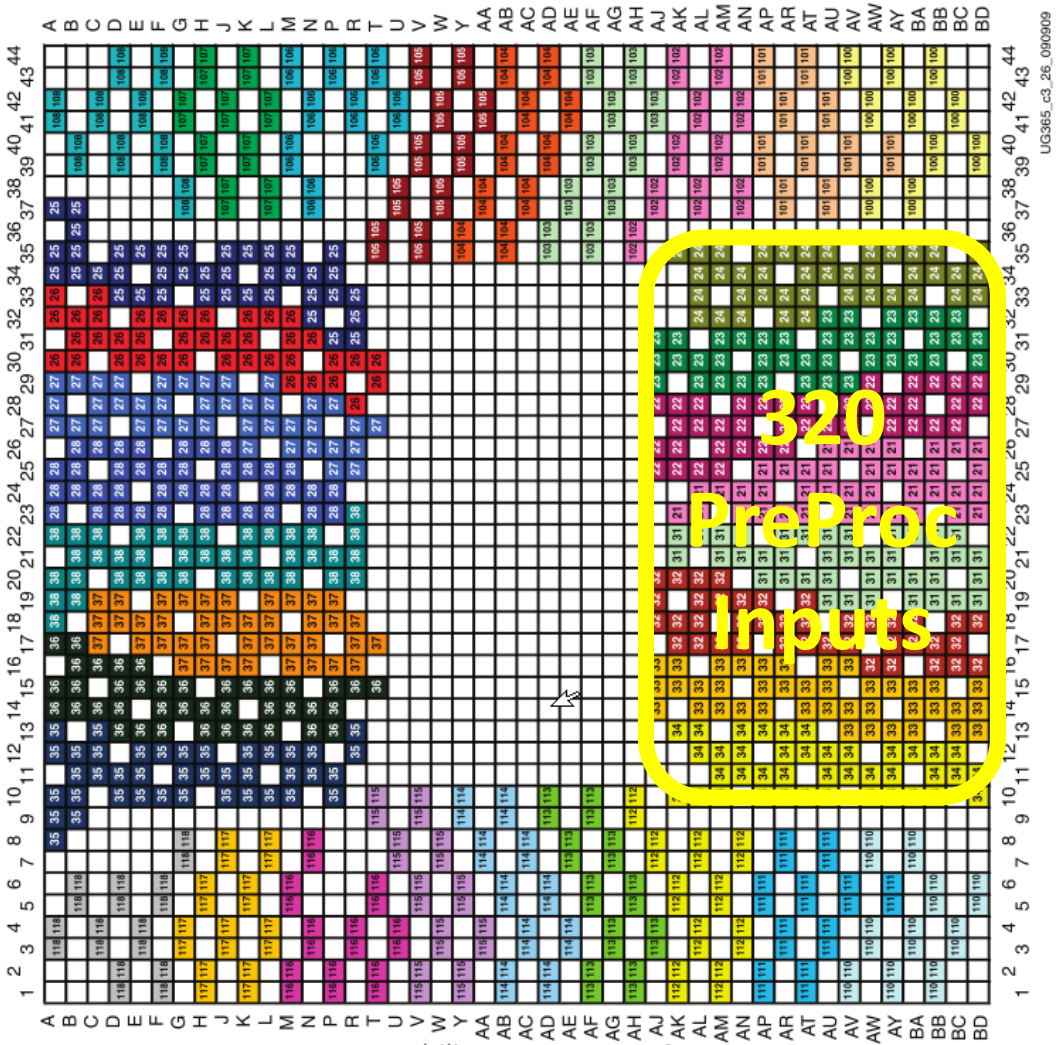


Figure 3-26: **FF1[illegible] Package—HX380T and HX565T[illegible] Bank Diagram**

FF1924

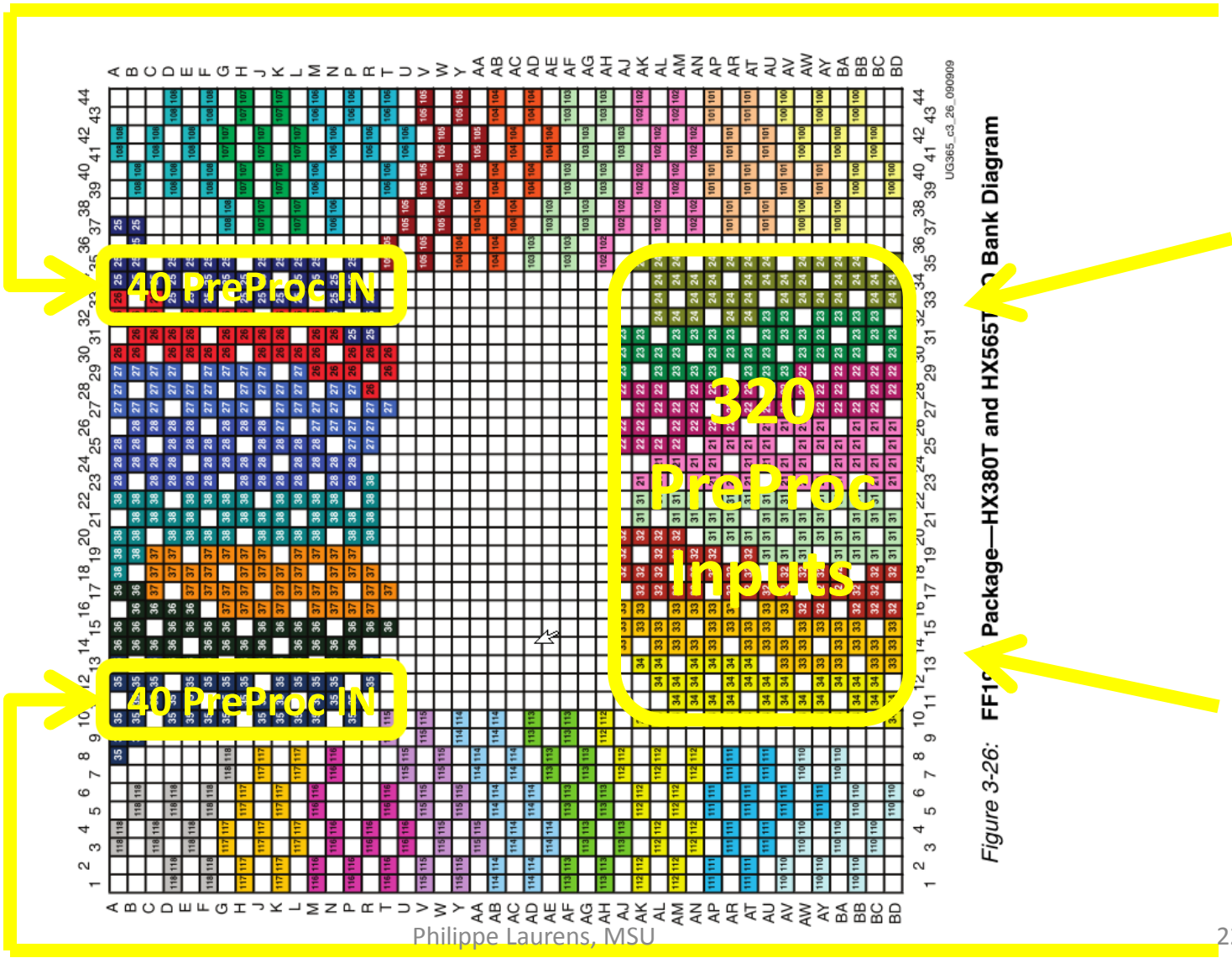


Figure 3-26: **FF1[illegible] Package—HX380T and HX565T[illegible] Bank Diagram**

FF1924

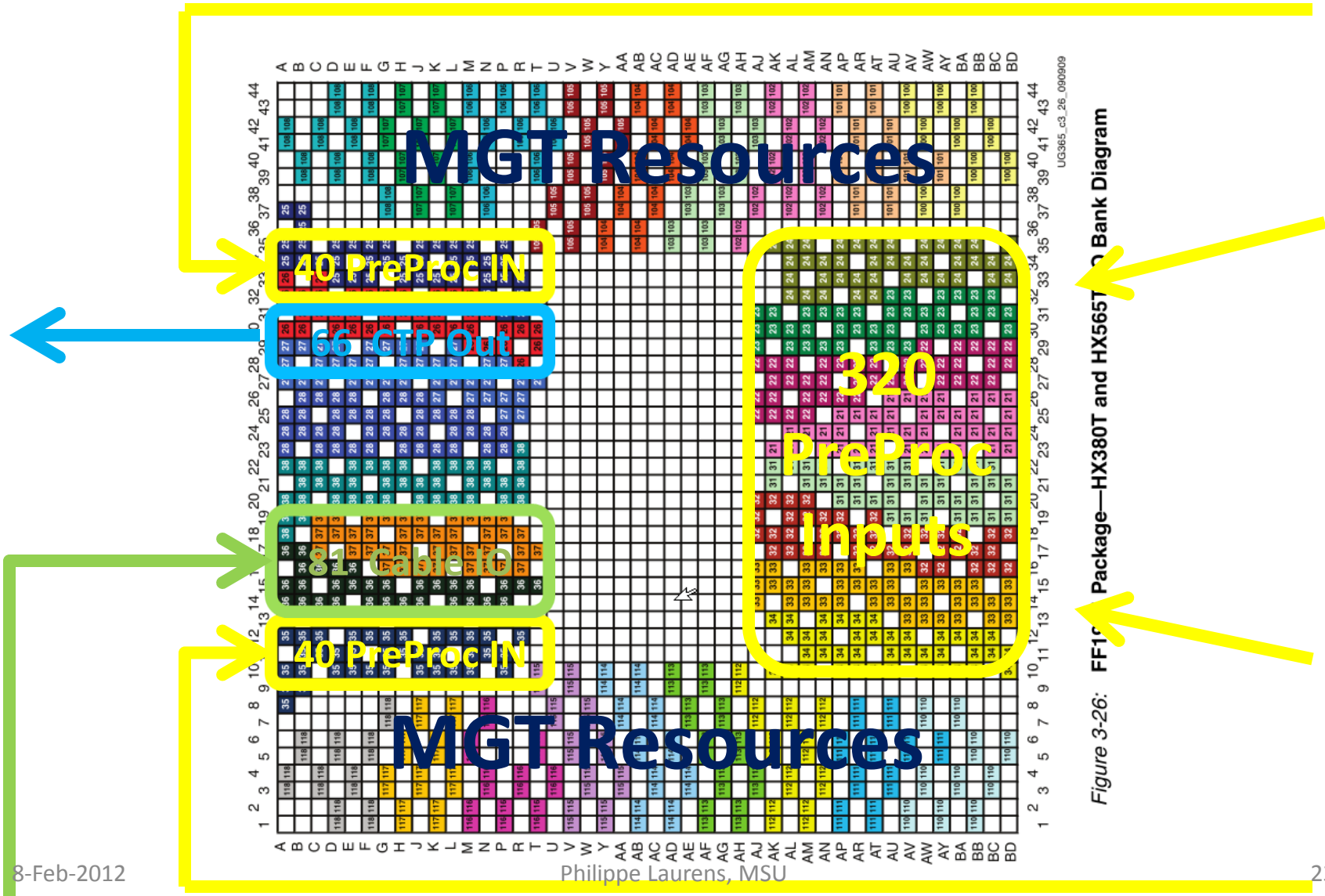
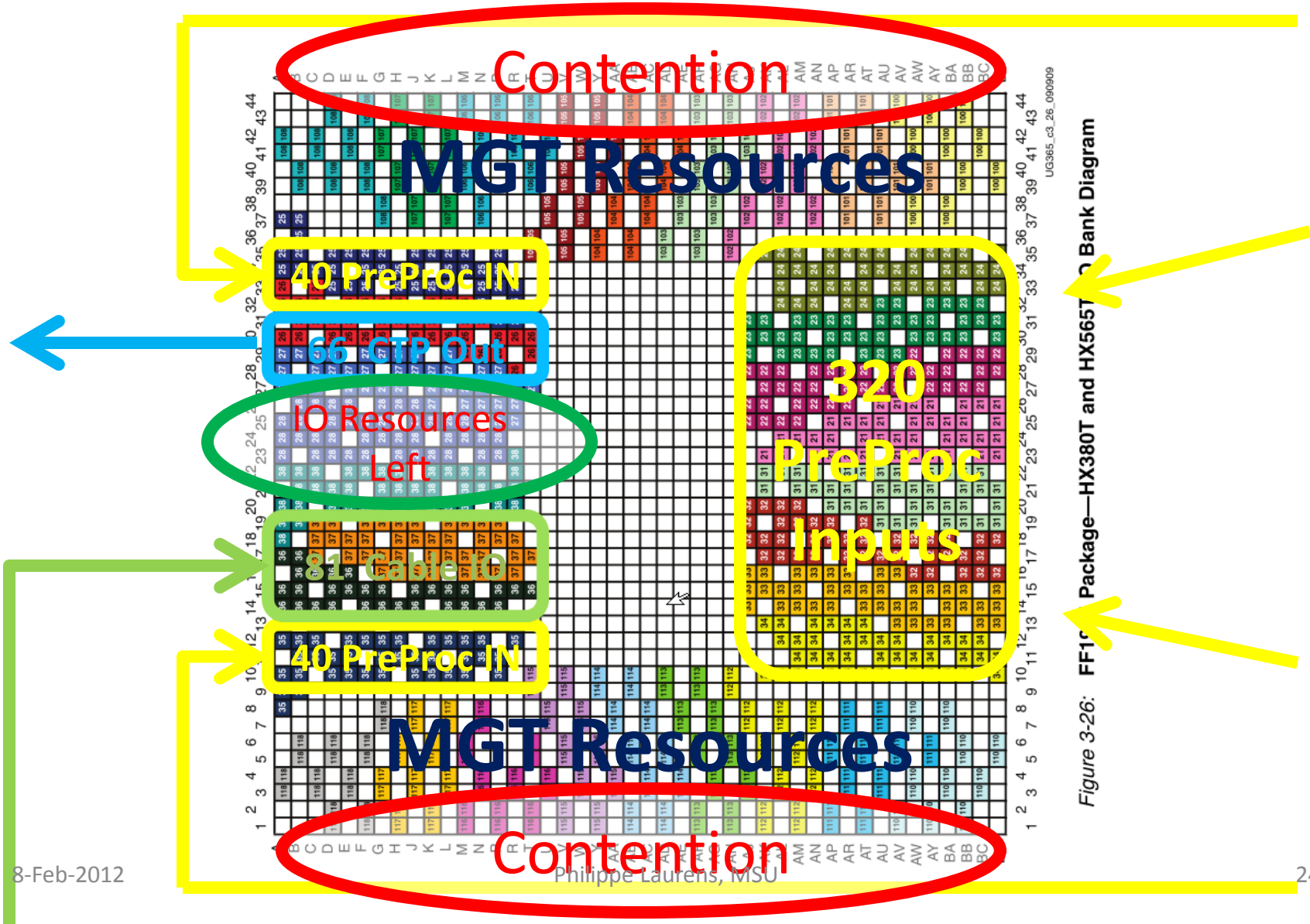


Figure 3-26: **FF1924 Package—HX380T and HX565T Bank Diagram**

FF1924 ➔ Too tight



FF1923

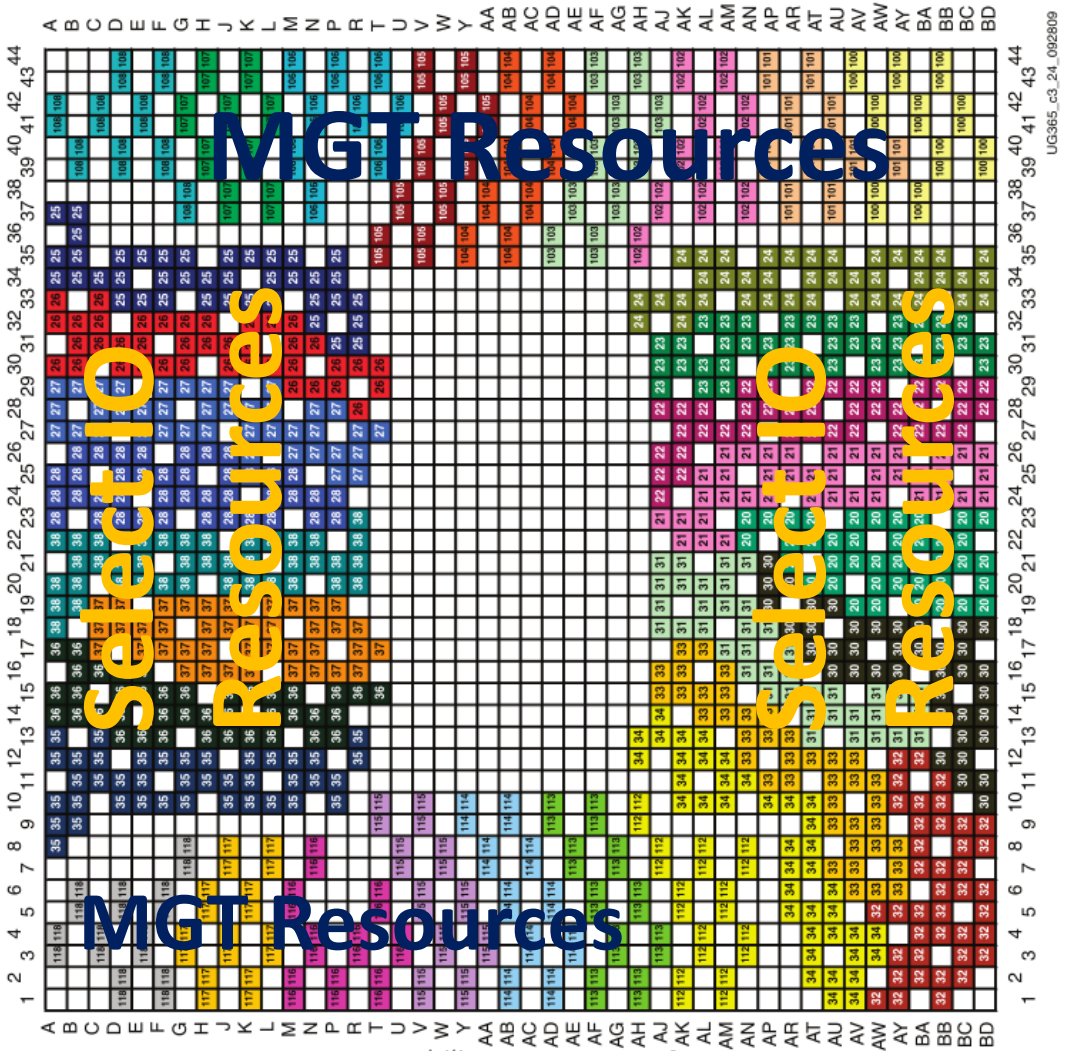


Figure 3-24: **FF1923 Package—HX380T and HX565T I/O Bank Diagram**

FF1923 → Better

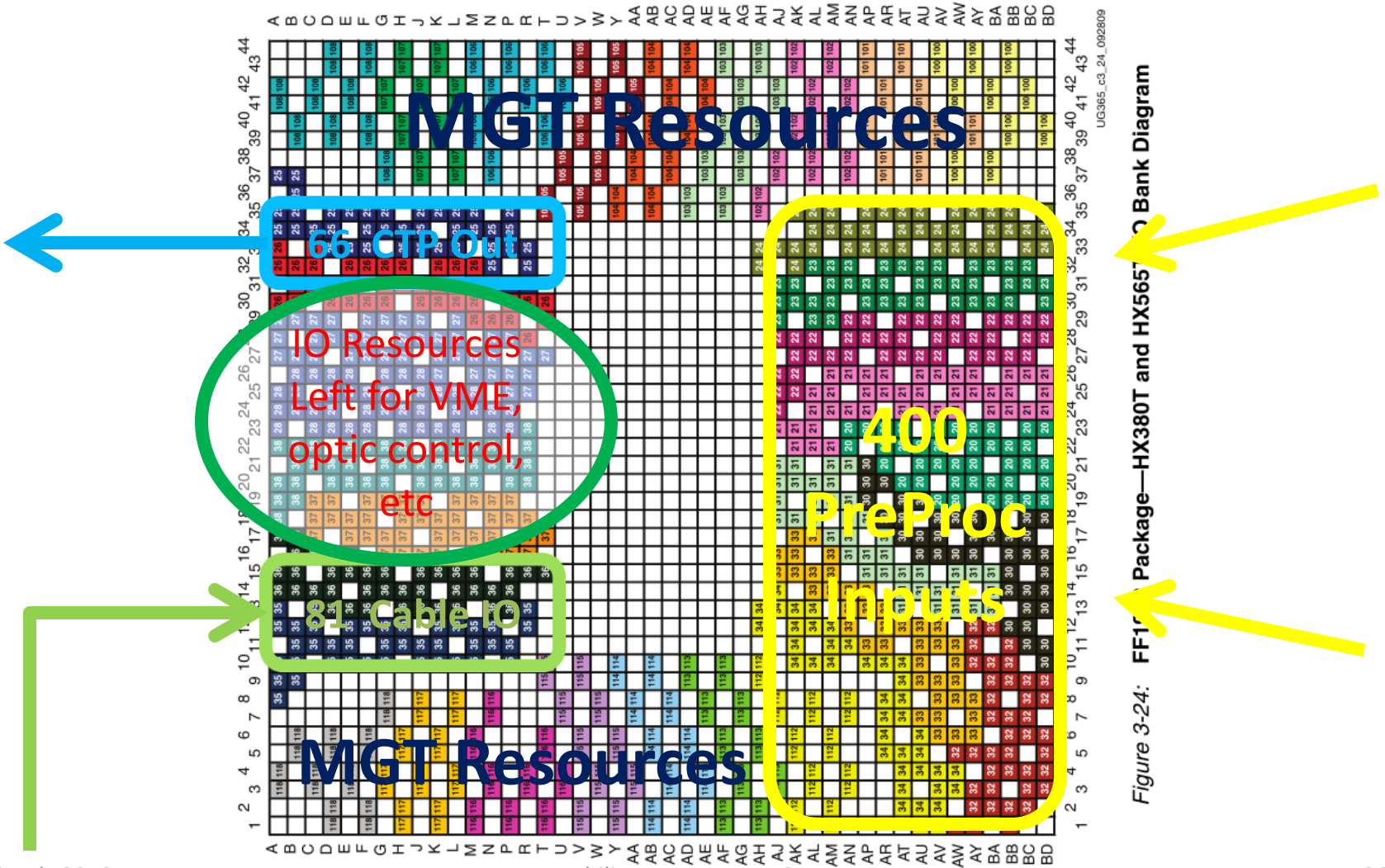


Figure 3-24: **FF1… Package—HX380T and HX565T… Bank Diagram**

Another package…?

- Base-CMX doesn't need/use all the available MGT resources of FF1923
- Especially if CMX does not need to operate as TP, there is another interesting package: **FF1759**
  - Fewer MGT resources
  - More Select IO resources
  - Similar Logic Resources
  - Slightly smaller footprint (→ less trace layers)
  - Cheaper

FF1759

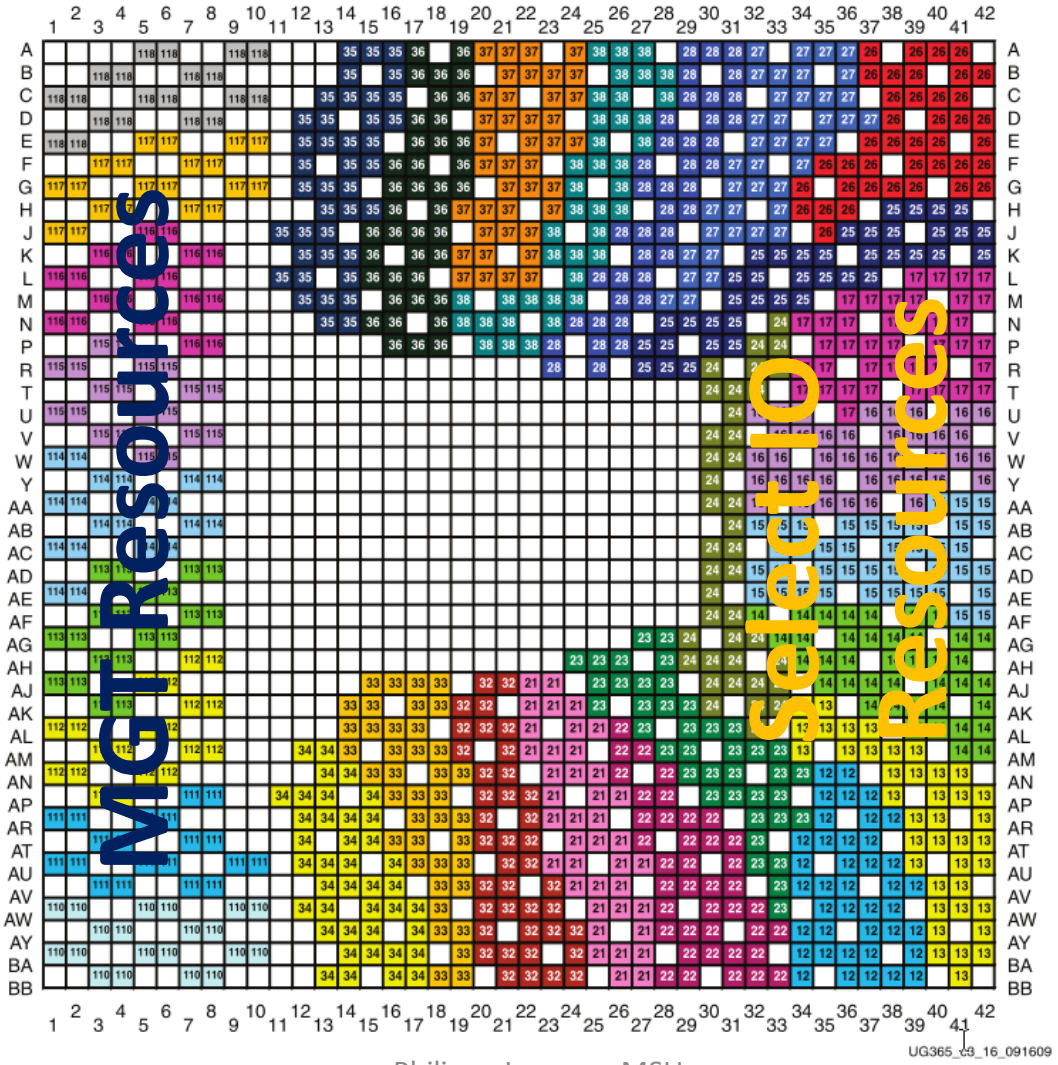
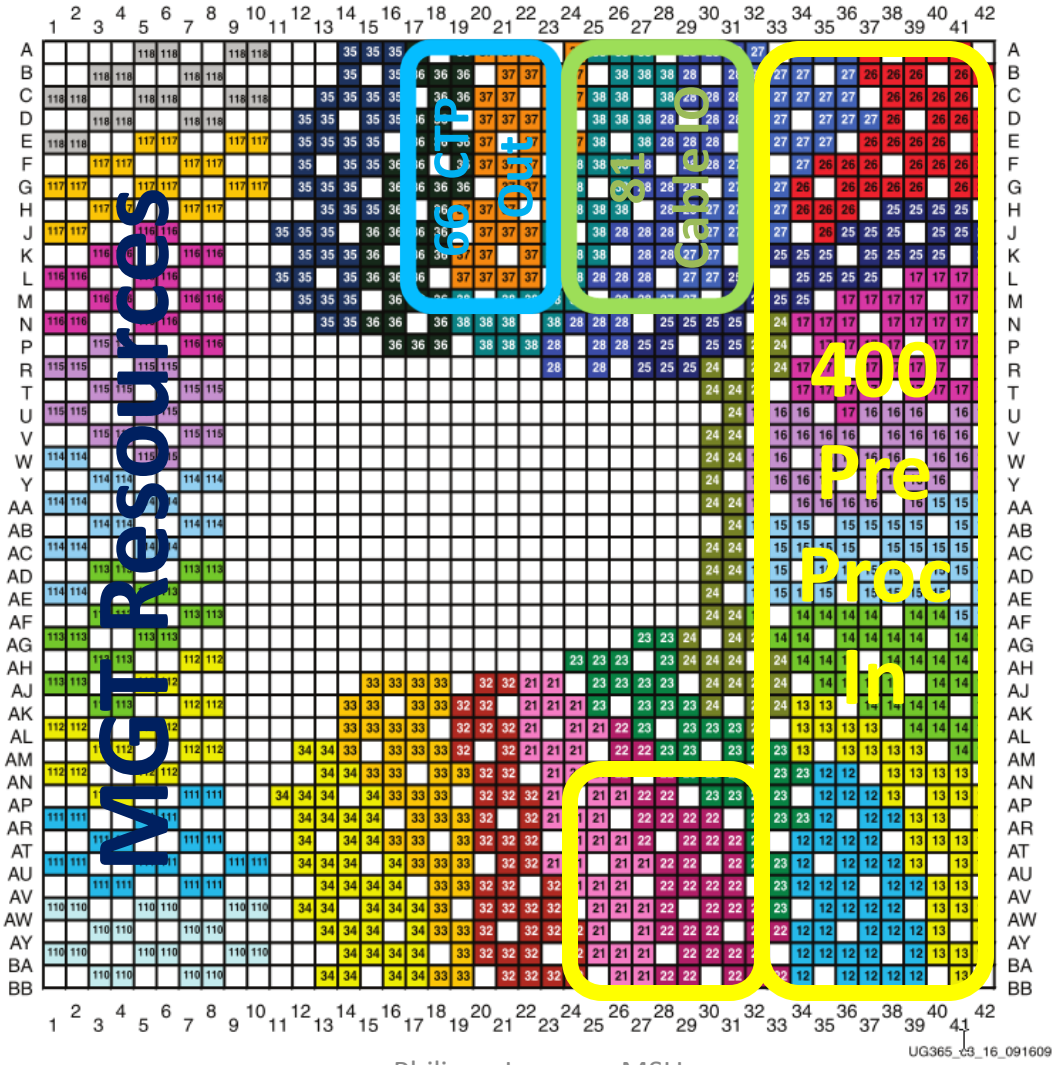


Figure 3-16: **FF1759 Package—LX550T and SX475T I/O Bank Diagram**

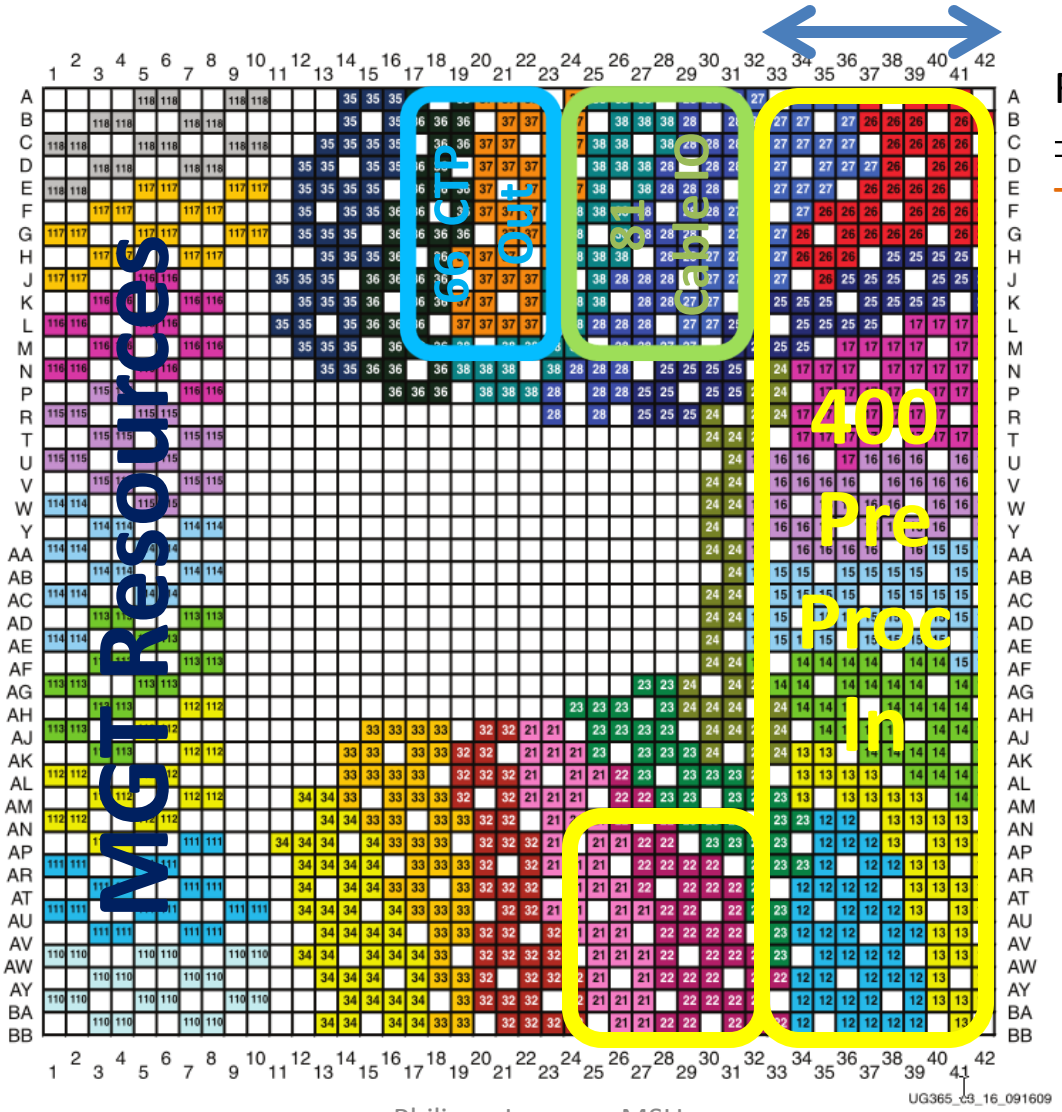
FF1759



boxes shape and location is an approximation for illustration of scale

Figure 3-16: **FF1759 Package—LX550T and SX475T I/O Bank Diagram**

FF1759 ➔ Preferred Choice



Fewer rows of pads
⇒ 4 or 5 Fewer Trace Layers

Figure 3-16: **FF1759 Package—LX550T and SX475T I/O Bank Diagram**

Resource Comparison

FF1759 | FF1924 or FF1923

	Part Number	XC6VLX550T	XC6VHX380T	XC6VHX565T
	EasyPath™ FPGA Cost Reduction Solutions[1]	XCE6VLX550T	XCE6VHX380T	XCE6VHX565T
Logic Resources	Slices[2]	85,920	59,760	88,560
	Logic Cells[3]	549,888	382,464	566,784
	CLB Flip-Flops	687,360	478,080	708,480
Memory Resources	Maximum Distributed RAM (Kb)	6,200	4,570	6,370
	Block RAM/FIFO w/ECC (36 Kb each)	632	768	912
	Total Block RAM (Kb)	22,752	27,648	32,832
Clock Resources	Mixed-Mode Clock Managers (MMCM)	18	18	18
I/O Resources[4,5]	Maximum Single-Ended I/O	1,200	720	720
	Maximum Differential I/O Pairs	600	360	360
Embedded Hard IP Resources[6]	DSP48E1 Slices	864	864	864
	PCI Express® Interface Blocks	2	4	4
	10/100/1000 Ethernet MAC Blocks	4	4	4
	GTX Low-Power Transceivers	36	48	48
	GTH High-Speed Transceivers	—	24	24
Speed Grades	Commercial	-L1, -1, -2	-1, -2, -3	-1, -2
	Extended	-2	-2	—
	Industrial	-L1, -1	-1, -2	-1
Configuration	Configuration Memory (Mb)	144.1	119.8	160.7

Very Similar

Fewer GTX
Zero GTH

Base-CMX Implementation

Question #1:

FPGA choice for implementing the Base-CMX functionality

Recommendation:

Use **LX550T FF1759**

(especially If CMX doesn't need to perform as a TP)

TP-CMX Functionality

Question #2:

Strategies, costs and risks for adding Topological Processing capability to the CMX platform

TP-CMX Functionality

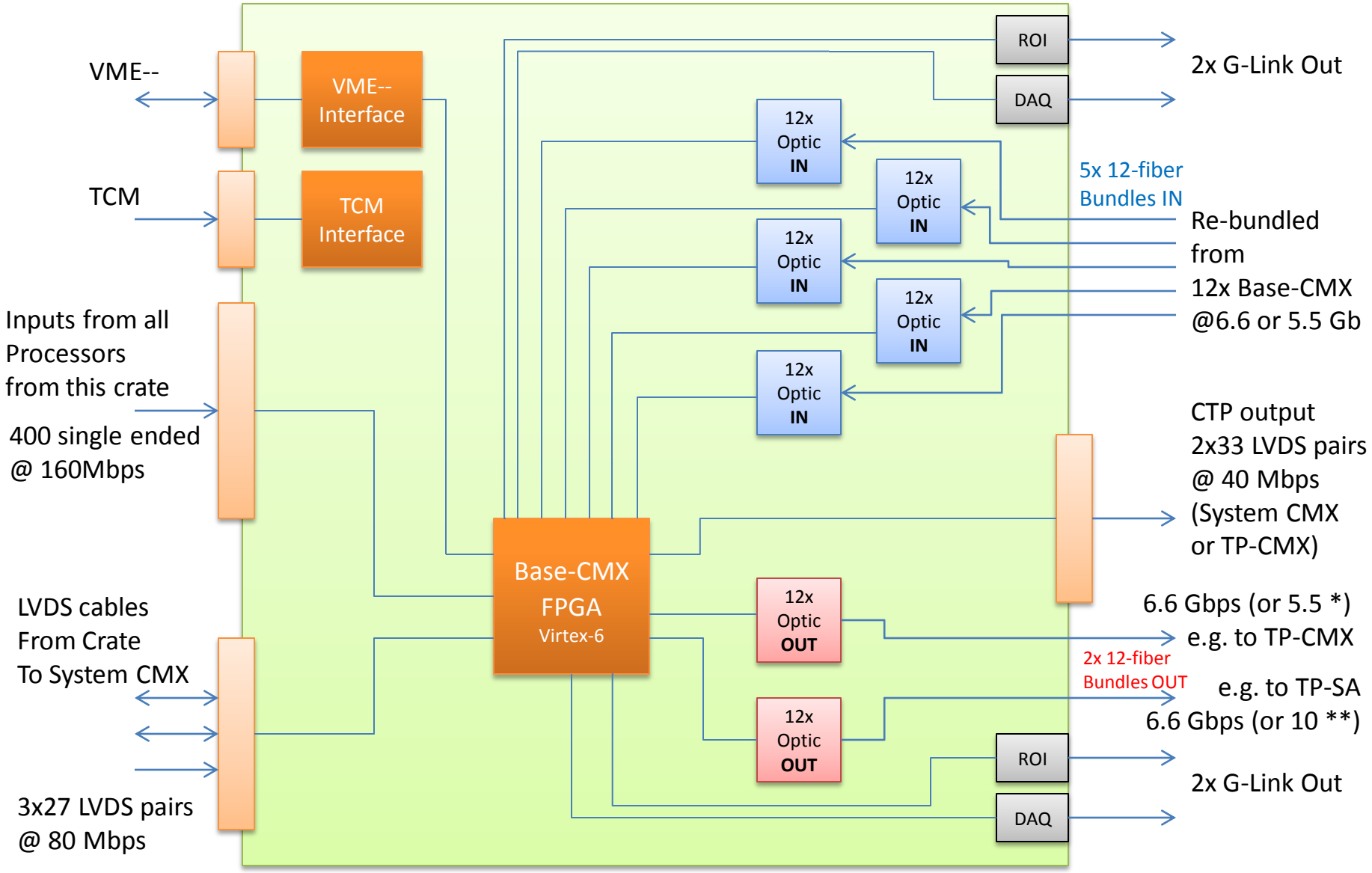
- Add as many optical inputs as possible to receive info from 12x CMX cards
  - requires intermediate fiber re-bundler box to go from 12x12 to 5x or 6x12
  - same box could provide 2x sets of upper/lower outputs without optical split
- Add another 2x GTX outputs for 2 more G-links for TP ROI and DAQ
- Need access to output driver to CTP (not a problem)

- Intrinsic complications when using Virtex 6 GTH resources
  - GTH inputs (2x12 of 5x or 6x) are not capable of 6.6 Gbps operation
    - because internal PLL is narrow range
    - 5.5Gb is compatible with both GTX and GTH
  - need two more power supplies for GTH transceivers
  - higher power (~2x) for GTH (3.6 W per 12) vs GTX (1.9W per 12 at 5.5Gb)

CMX-TP : **Single FPGA** Solution

- Constraints
  - cannot be FF1759, has to be FF1923
  - 5x12 GTX/GTH inputs (i.e. 4 more than Base-CMX only)

B. CMX Card with TP capability on same FPGA



* TP-CMX GTH inputs not capable of 6.6 Gbps
** 10Gb output to TP-Standalone option to be determined

CMX-TP : Single FPGA Solution

Cons

- forego advantages from FF1759 (ruled out because not enough MGT resources)
- total of >= 88 MGT signal pairs; 50 additional from Base-CMX
  - competes with Base-CMX functionality for real estate & access
  - very crowded near FPGA
  - makes Base-CMX layout more complicated
  - increase risk of electrical interference

- **Ties firmware** for Base-CMX with firmware for TP-CMX
  - makes commissioning/evolution of CMX-TP firmware operationally risky for Base-CMX operation
  - share total available logic resources between these two separate functions

CMX-TP vs Base-CMX

So there is contention…

Can this be helped?

CMX-TP vs Base-CMX

Observations

- Base-CMX and TP are totally separate functions
  - logically, don't share inputs or outputs (unlike Crate vs System)
  - operationally in separate latency time segments
  - only share VME bus, TTC, ...
- TP-CMX needs access to CTP output, but we can simply not choose a System CMX to operate as a TP-CMX
- Still not clear if TP-CMX functionality is ultimately needed or desired (as backup) and/or used
- Still not clear how and when we would know for sure that CMX-TP will be used or not
- Merging Base-CMX ant TP-CMX firmware in one design and one bitstream still seems unwise
  - We even originally proposed to use a separate CMX in a separate crate

CMX-TP : **Dual FPGA** Solution

Add a second FPGA for just TP-CMX functionality

- Pick optimal FF1924 package with most MGT resources for TP-CMX
- Keep optimal FF1759 package for Base-CMX

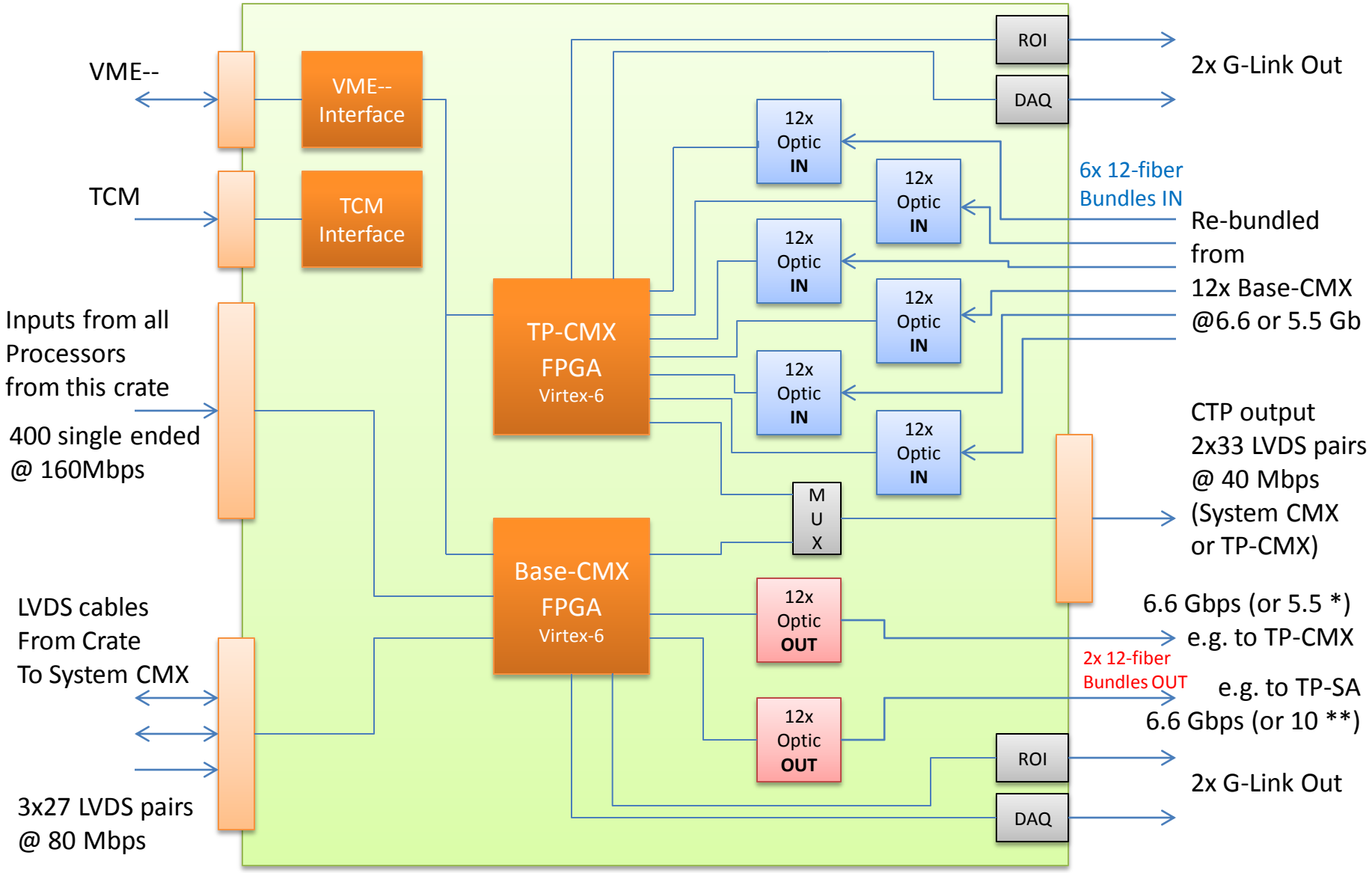
→division of tasks & risks between FPGAs

CMX-TP : Dual FPGA Solution

Pros

- Easier **commissioning**, easier **operation**, easier **firmware** mgmt and upgrade
- One more 12-fiber input bundle for TP-CMX (6x12 instead of 5x for FF1923)
- Leverage advantages of FF1959 package precluded in single FPGA solution
- Divide routing challenges
  - backplane processor and cable inputs located in one area
  - Majority of high frequency requirements of MGT resources in other area
  - Expected to translate into more flexibility, shorter traces
  - lower chances for electrical interferences
- Separate MGT transmitters from receivers
- → Prevent TP-CMX "luxury" from interfering with Base-CMX "necessity"
- …and if decision on Standalone TP needs to be further delayed
  - could abandon TP-CMX part of layout during design phase without impact on Base-CMX
  - rip out or leave unpopulated
- Also could abandon TP-CMX before production assembly
  - not populate TP-CMX location on production boards
  - modify layout if needed or try and prepare for it (cf. modified solution below)

C. CMX Card with TP capability on separate FPGA



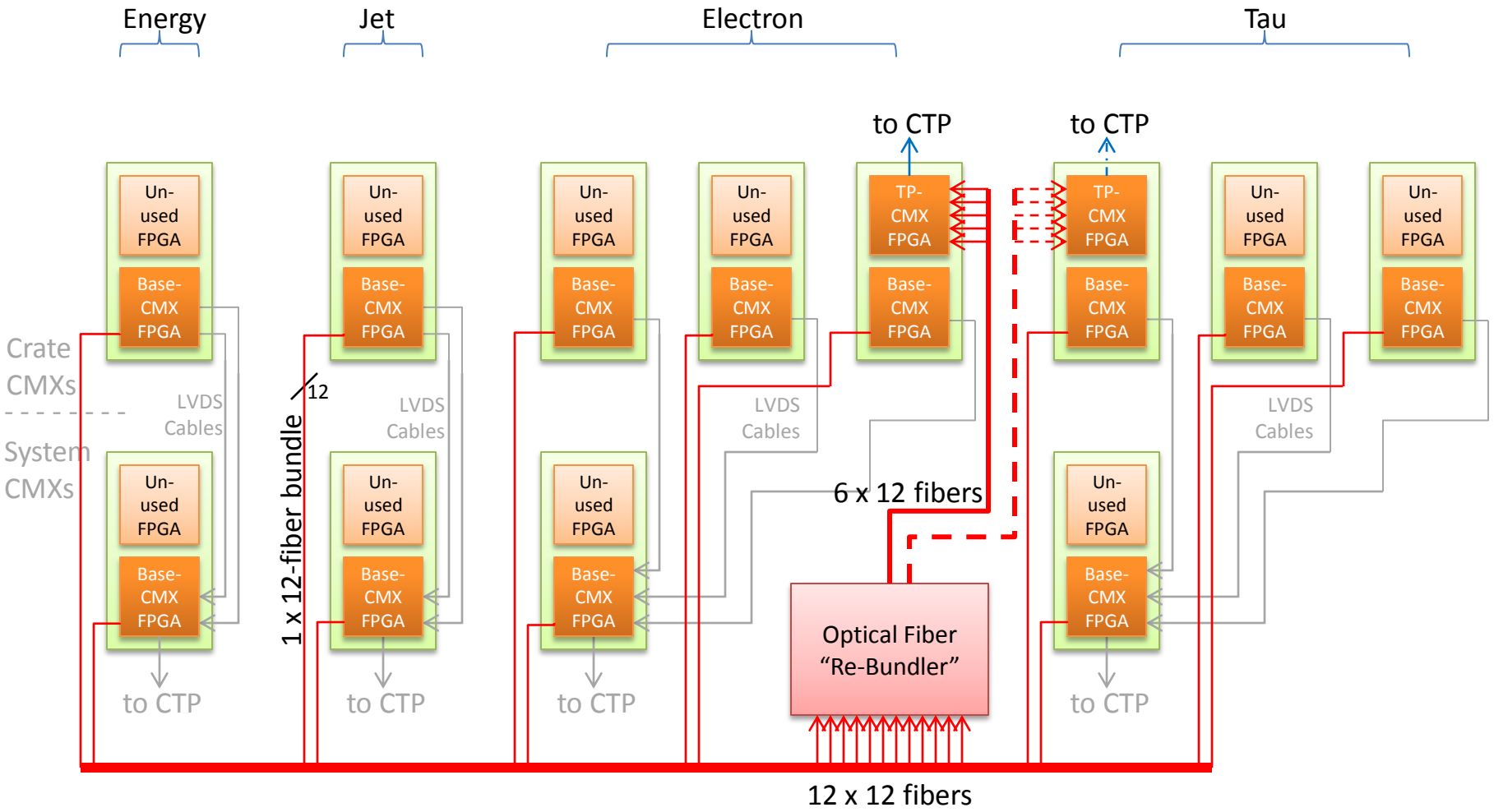
* TP-CMX GTH inputs not capable of 6.6 Gbps
** 10Gb output to TP-Standalone option to be determined

CMX-TP : Dual FPGA Solution

cons

- Two FPGAs means more expensive
  - ~1.5x in FPGA cost (FF1924+FF1759 instead of FF1923)
  - or ~2x in FPGA cost (FF1924+FF1923 instead of FF1923)
  - cf. table later on…

4. One (or more) CMX TP receiving Zero-Suppressed Inputs



Dual FPGA solution = more expensive

Can this be helped?

Modified Dual FPGA Solution

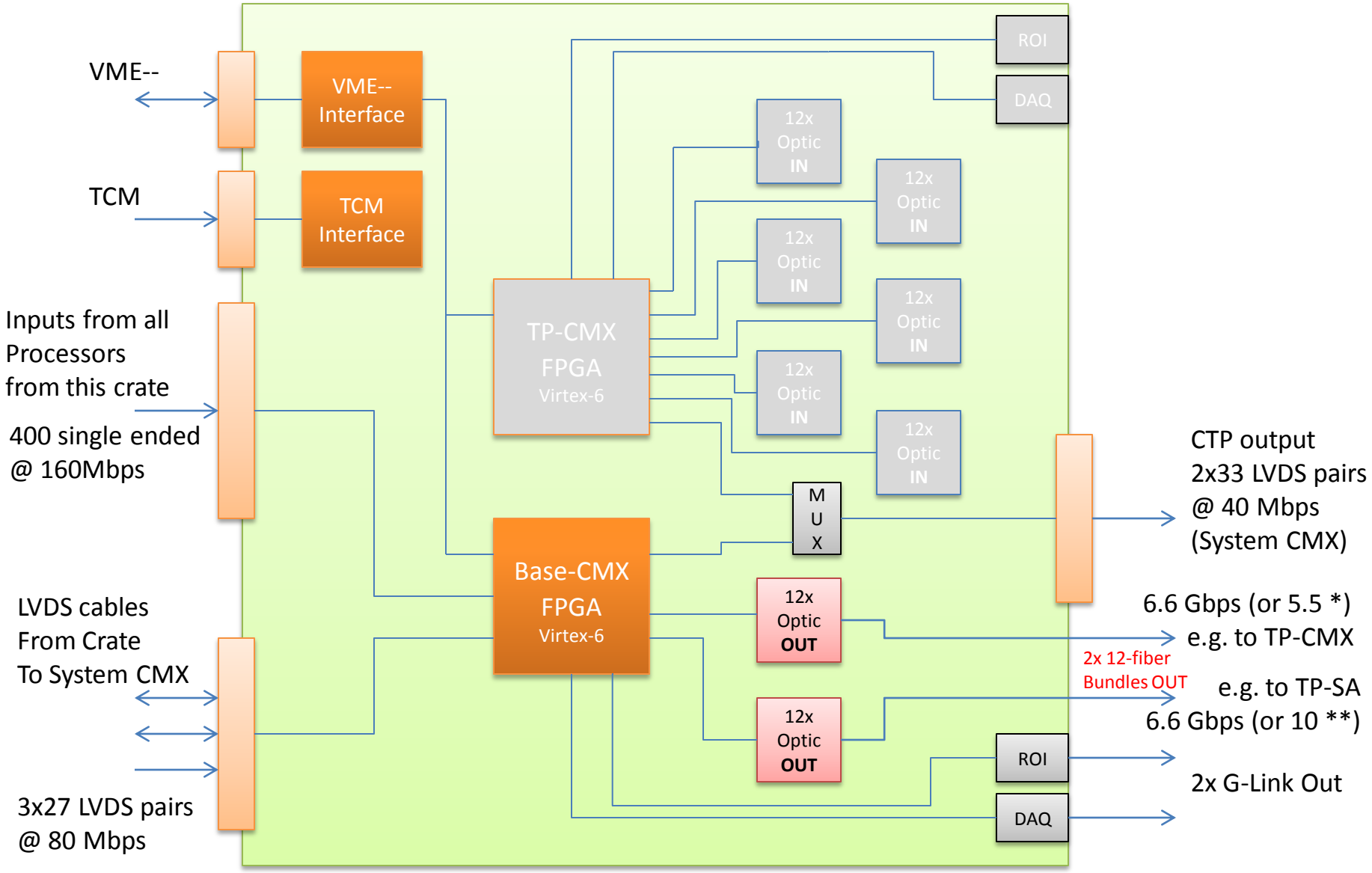
- TP functionality **only used on one** (or few) CMX boards
  - TP-CMX FPGA thus unused in all but few of the boards
- Initial goal was to have all cards be the same…
  - but wasteful/expensive for dual FPGA CMX

- → **Build two flavors** of CMX cards
  - A few (2-4) with both FPGAs
  - The bulk with just the Base-CMX FPGA
- Could be exact same layout or close derivative
  - **NOT** a separate design, and plan for this option from start
  - Intent is that same circuit board can be assembled into either specie
  - Share some of the assembly setup costs (less parts in one)
  - Layout review option between prototype and production

Modified Dual FPGA Solution

- **Pros**
  - keep all advantages of Dual FPGA solution
  - Avoid cost escalation of expensive second FPGA unused on bulk of cards
- **Cons**
  - Breaks l1calo "tradition" of all identical boards
  - Some aspects of operation/mgmt will need tailoring
  - Two types of boards, but one is superset of other

C-prime. CMX Card with TP capability unused/unpopulated



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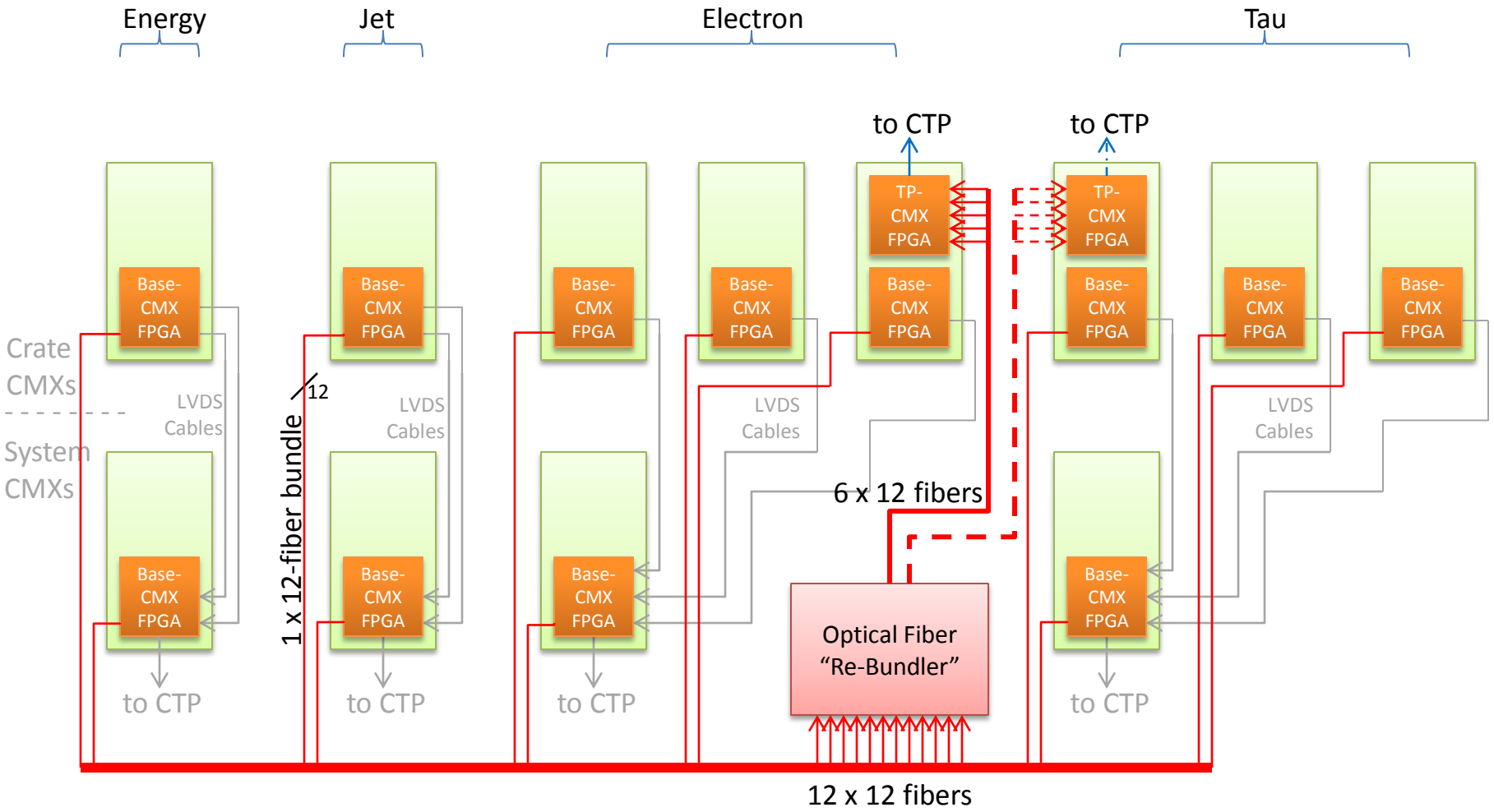
4-prime. One (or more) CMX TP receiving Zero-Suppressed Inputs



Cost Estimate for FPGAs

	Option	FPGA Base	Packg Base	FPGA TP	Packg TP	FPGA(s) Q=1 **	Total Q=15	Total Q=4+11
1	Base CMX, 6Gb out, no TP	LX550T	FF1759			$5.5k	**$83k**	
2	Single FPGA, Base 6Gb out, TP 5Gb in	HX565T	FF1923			$8.5k	$128k	
3	Dual FPGA, Base 6Gb out, TP 5Gb in	LX550T	FF1759	HX565T	FF1924	$14k	$210k	
4	#3, build 2-4 with TP, 11-13 without TP							**$117k**

- **(**)** DigiKey Q=1 price from website, rounded up. May get quantity and/or research discount. Waiting on quotes from AVnet.
- **6Gb out**: need >6.4Gb on 12 fibers to send raw data + link control protocol + payload signaling protocol. GTX specified up to 6.6 Gb.
- **5Gb in**: shortened label for maximum rate that a Base-CMX GTX output can send to a TP-CMX GTH input (5.59 Gb in specs).
- **HX565T** could be replaced with **HX380T**, with less logic resources, but higher speed grade available (+10%), for +$3k each

TP-CMX Functionality

Question #2:

Strategies, costs and risks for adding Topological Processing capability to the CMX platform

Recommendation: Dual FPGA solution

Base-CMX use **LX550T FF1759**

TP-CMX use **LX565T FF1924**

Build majority of CMX without TP-CMX FPGA

Appendix

10Gbps output to Standalone TP

10Gb motivation

- from **TP point of view**
  - Send more data (but not clear what)
  - Or use less fibers
  - Or reduce latency by a fraction of beam crossing
- from **CMX point of view**
  - Why not if GTH resource is present and able
  - Optical transmitter capable of 2.5-10Gb anyway
  - a layout capable of >10Gb should be capable of <10Gb

10Gb output to Standalone TP

- Frequency up by factor ~2
  - higher requirements on transmission lines
  - higher attenuation
  - trace length even more closely matched
  - smaller scale of imperfections that matters (e.g. vias, bends)
  - → more complicated layout work
- 10Gb outputs not compatible with TP-CMX 6.6Gb inputs (5.5 Gb ok)
  - may matter if GTH output replaces one of the 2x12 GTX outputs
- Need additional low jitter external oscillator for each frequency
- Higher current draw for GTH transmitter
  - ~4.25 W per 12-lane GTH at 10Gb (cf. ds152/p16) or 4.3W from XPE spreadsheet
  - vs. ~1.5W per 12-lane GTX at 3Gb (cf. ds152/p9) or 1.9W at 5.5Gb 2.1W at 6.6Gb

→ **Change of scope** with significant impact on our engineering resources and which will take away from insuring that the Base-CMX functionality will be delivered and work on time.

Additional impact on each option

1. **Base-CMX only**
   - Base-CMX FPGA cannot be FF1759; has to be FF1923
     - more layers
     - 2x additional power supplies for GTH (1.1 and 1.8V)
     - additional oscillator
     - more expensive

2. TP-CMX: **single FPGA solution**
   - no difference in FPGA choice (already FF1923)

3&4. TP-CMX: **dual FPGA solution**
   - no difference in TP-CMX FPGA choice
   - Base-CMX FPGA cannot be FF1759; has to be FF1923
     - Cf. above

FPGA Cost increase for 10Gb option

	Option	FPGA Base	Packg Base	FPGA TP	Packg TP	FPGA(s) Q=1	Total Q=15	Total Q=4+11	Delta 10Gb
1	Base CMX, 6Gb out	LX550T	FF1759			$5.5k	$83k		
1b	Base CMX, some 10Gb out	HX565T	**FF1923**			$8.5k	**$128k**		**+$45k**
2	Single FPGA, Base 6Gb out, TP 5Gb in	HX565T	FF1923			$8.5k	$128k		
2b	Single FPGA, Base 10Gb out, TP 5Gb in	HX565T	FF1923			$8.5k	$128k		$0k
3	Dual FPGA, Base 6Gb out, TP 5Gb in	LX550T	FF1759	HX565T	FF1924	$14k	$210k		
3b	Dual FPGA, Base 10Gb out, TP 5Gb in	LX550T	**FF1923**	HX565T	FF1924	$17k	$255k		+$45k
4	#3, build 2-4 with TP, 11-13 without TP							$117k	
4b	#3b, build 2-4 with TP, 11-13 without TP							**$161k**	**+$45k**

10Gb out: maximum frequency of an Avago AFBR-810B SNAP12-style transmitter;or a bit more for Avago miniPOD

10Gb output to Standalone TP

Recommendation:

More stringent layout requirements

Adding risks to Base-CMX timely delivery

Zero benefit for CMX, unclear benefit for TP

Significant cost increase

→ Abandon 10Gb output idea

CMX Project's Goals for this meeting

We would like a short term outcome of this meeting to be:

1. "Yes/No" on continue designing for CMX-TP
   - And agreement on approach
2. Agreement on FPGA choice
3. Agreement on 10Gb output option