

L1Calo Upgrade Technical Workshop

- Important Points -

(8th-9th February 2012 at RAL/Cosener's House)

Introduction

These notes document some key points from the L1Calo Upgrade Technical Workshop held at RAL (and Cosener's House) from 8th to 9th February 2012. They do not pretend to document discussions but are primarily recommendations and actions. For a more complete picture of material presented at the meeting the reader is referred to the CERN Indico agenda from which individual talks may be accessed - <https://indico.cern.ch/conferenceOtherViews.py?view=standard&confId=172073>.

Phase-0

Recommend: the CMX should be designed to accommodate 2 FPGAs, one for merging and one for simplified topological processing (in the event that this is necessary (delays in L1Topo) or desirable (sharing topological processing with L1Topo)).

Recommend: only populate a handful of CMX with both FPGAs to act as CMX receivers (system level CMX, including topological processing); 1 in running system, 1 at institute (for test purposes), 1 in CERN test rig and 1 spare.

Recommend: operate the CMX to CMX electrical links at 4x current speed, i.e. at 160MHz. This will enable the requisite bandwidth for additional information (e.g. energies) and thus avoid the increased latency of an all optical solution. Tests are needed to validate this approach.

Recommend: the TP-CMX function of the CMX should be equipped with 3x 12-fibre inputs. This is perceived achievable and will provide headroom.

Recommend: Outputs from CMX to L1Topo should use 24 fibres (presumably 2x 12-fibre ribbons). This permits data duplication at source consistent with feeding multiple L1Topo processors.

Action: Sam & Steve to develop a Data Formats document to include

- **backplane data formats,**
- **detailed drawing of connections between L1Topo and CMX and with other modules,**
- **zero suppression strategy**

Recommend: to **proceed as fast as possible to the final data formats** (right column) for CP transfers to the CMX when commissioning after the Phase-0 shutdown (see Steve's talk for details pp9&10).

	1 st half 2014 (initial)	2 nd half 2014 ? B/p at 160MHz + Topo	Start of 2015 or earlier Upgraded CMX + Topo
CP	Defined	Defined (p9)	Almost defined (p10)
Jet	Defined	Almost defined	Not defined
Energy	Defined	Almost defined	Not defined
ROD*N	Defined	Not defined	Not defined

Action: Uli to **perform latency checks for duplication of data between FPGAs** using the GTH loopback option. This could be useful if a board is populated with more than 1 FPGA topological processor.

Recommend: **Optical link speed should be 6.4Gb/s.** Designing to use higher speeds is deemed to carry significant risks. It is believed that working at 6.4Gb/s already should have sufficient bandwidth.

Recommend: **Optical links should run synchronously with the LHC frequency, but with control characters** so that automatic link recovery is possible. The details of this recommendation need to be worked out and verified.

Phase-1

Recommend: **the nMCM could use one of the current parity bits to multiplex CP1 and CP2 data to the JEP** (in higher bandwidth operation).

Timescales: completion of the current nMCM work takes highest priority. Double rate tests are anticipated to follow this in late spring 2012. The test are important to verify whether Tilecal information can be sent to the eFEX at full 0.1x0.1 granularity.

Assume: **electromagnetic and hadronic depth information is not needed for the jFEX processor.** No convincing case has emerged (to date !).

Recommend: **baseline for optical connection between RTM and main ATCA board should be the 36-way MTP connector,** though a 48-way MTP connector is not yet ruled out.

Action: Uli to **research viability of the 48-way MTP** option.

Recommend: **Data Sharing (FEX inputs) across the ATCA backplane is not advocated.** Trace lengths and aggregation of connector and via effects are expected to bring signal integrity into question over such distances.

Assume: **'data duplication at source'** is to be favoured in general (certainly for crate and module inputs). This simplifies the optical fibre loom and avoids data sharing across the backplane.

Recommend: **FEX inputs should be brought optically over the RTM to close proximity to the FPGA where they should terminate at MiniPods.** There is an optimum distance for ongoing electrical signals as even very short traces can suffer integrity issues.

Recommend: **Optical link speed is narrowed down to 6.4 or 10Gb/s.** Further work is necessary.

Action: Sam to talk to Steffan Muschter to **understand what Tilecal has achieved in this area.**

Action: Uli to **test PMA loopback on GOLD.**

Recommend: **baseline eFex window size should be 4x4** (trigger towers). Although 3x3 is adequate for R_{η} (a.k.a. Rcore4) algorithms, choosing 4x4 permits the current algorithm to execute in the new eFEX and for the eFEX to more easily interwork with the current CPM data. A 5x5 environment may prove desirable...more study needed. Remaining questions include...

- does 5x5 give (significantly) better physics performance ?
- are the old cluster algorithms still needed (should they be transferred to the eFEX to run in parallel) ?

Action: Alan to **research such questions for EM triggers**

Action: Mark to **research such questions for Tau triggers**

Action: Murrough to **research impact of window size decisions in DPS output fibre organisation**

Action: Steve to ask the "Analogue & Digital TowerBuilder output" committee on **views in providing 1441 and 1141 LAr layer summing configurations.** 1441 clearly provides more flexibility, but no strong case for its use has yet emerged.

Recommend: **a two-crate (ATCA) eFex is adopted as the (conservative) baseline,** though it is agreed that a 1-crate solution is desirable if it can be shown to work without significant risks. More studies are necessary before a less conservative approach can be considered.

Action: Sam to provide **possible fibre routing pictures for both 1 and 2-crate versions.**

Action: ?? to review **pros and cons of performing the Tau trigger in the eFEX or in the jFEX.** For example the higher granularity environment of the eFEX may be of benefit.

Action: ?? to study **pros and cons of direct connection of FEXs to L1Topo .vs. going via a merger module.**

Action: Norman to **review the latency budget** on the basis of the current baseline architecture recommendations (including options).