Atlas Level 1 Calorimeter Trigger

Common Merger eXtended module (CMX)

Prototype Review

Dan Edmunds, Philippe Laurens,

Yuri Ermoline, Chip Brock,

Wojtek Fedorko

Michigan State University & University of British Columbia

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1 Introduction

1.1 Scope

The CMX project is part of the Phase-0 upgrade of the Atlas Level-1 Calorimeter Trigger system (L1calo). The CMX module is designed as a replacement for the Common Merger Module (CMM). The CMX modules must be able to replace the existing CMM modules, provide an increase in performance and add new functionality as described in this document.

This Introduction (1) covers the historical evolution of this project and is followed by (2) a general description of the CMX card and its main features, (3) a description of the real-time data path and usage in L1calo, (4) a description of the board control, configuration and monitoring, (5) a description of the powering of the components on the card, (6) a description of the Card Layout and finally (7) a table of the number of CMX cards to be built.

This document also contains appendices which include circuit diagrams and engineering notes used to design the card.

The use of large FPGAs with well over a thousand pins per device does not make the standard schematic entry methods very practical for the designer or welcoming to the outside reader. The CMX was instead entered in the Mentor CAD system directly as a keyed-in net list, i.e. a text file describing all the connections in the plain ASCII file format used by the CAD system. The overall net list was assembled from a collection of “bite-sized” smaller files including the comments and annotations found useful to design and document the card. Schematic diagrams are still a critical part of the process and circuit diagrams are created using a more flexible format. A circuit diagram was made for each sub-sections of the design to help in the detailed design and the documentation of the project. A current snapshot of these circuit diagrams is included in the appendices of this document. The key-in net list is not included here but available via the references below.

The appendices form a snapshot of the current state of all these design documents. Collecting all these sub-documents and organizing them into one common document was intended to help the reviewers and also remain as an archive of this stage of the design. The appendices include references to the locations where the source documents will continue to evolve as the project continues through the manufacturing of the prototypes and production of the final

modules. The reviewers are also free access and browse through the individual sub-documents directly following the URLs below.

References:

The main URL for the CMX project is
http://www.pa.msu.edu/hep/atlas/l1calo/

The CMX project specifications (including previous reviews) can be found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/specification/
The CMX block diagrams will continue to evolve in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/block_diagrams/
The circuit diagrams will continue to evolve in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/
The key-in net list files will continue to evolve in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/net_lists/
The detail engineering notes will continue to evolve in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/
The mechanical drawings of the front panel and stiffener bars are in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/mechanical/
Device datasheets and documentation for parts used on CMX are in
http://www.pa.msu.edu/hep/atlas/l1calo/reference/other/

The CMM documentation contains a lot of relevant information not repeated in this document and a copy of the CMM documentation is available here
http://www.pa.msu.edu/hep/atlas/l1calo/reference/l1calo/cmm/

This review document and the comments and recommendations are in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/specification/3_prototype_review/

1.2 Preliminary Design Review

The CMX project was presented to a Preliminary Design Review (PDR) in July 2011 in Stockholm. The PDR specification document and the review report are available in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/specification/1_preliminary_design_review/

1.3 Design Study and Report

A design study phase followed the PDR to determine an optimal choice for implementing the base functionality required to replace the CMM and to explore the feasibility of implementing some topological processing using the CMX as a platform. The results of this study were presented during a workshop at the Rutherford Appleton Laboratory in February 2012.

The main outcome of this study was the decision to separate the topological processing functions on CMX from the base function on CMX. Instead of using one of the largest Virtex 6 FPGAs (XC6VHX565T) the CMX is being implemented on two medium size Virtex 6 devices (both being XC6VHX550T). One FPGA implements the Base Function (BF FPGA) required of all CMX modules, and the other FPGA implements the Topological Processing Function (TP FPGA) optionally required on only one or a few CMX modules. Most CMX cards will be built with only the Base Function FPGA installed and only a few cards will have both FPGAs installed.

The recommendations from this workshop also specified that the CMX BF FPGA should provide High Speed outputs for two 12-fiber ribbons and that the TP FPGA should receive High-Speed inputs from three 12-fiber ribbons. All optical links must operate at 6.4 Gbps with a reference clock derived as a multiple of the LHC clock.

The material presented at the workshop, the resulting recommendation and a more detailed study report are available in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/specification/2_design_study/

1.4 Requirements changes since then

One additional requirement which was not explicitly part of the original PDR nor part of the RAL workshop recommendations is the option of operating the CTP output at speeds higher than the current 40 Mbps on CMM, namely 80 or 160 Mbps. This option may not be usable in practice as the CTP hardware used during Phase 0 will likely not support these higher transfer rates.

A self-imposed requirement was also added to the CMX hardware such that the BF FPGA be able to operate the three Cable IO ports of the CMX card independently, separately controlling the direction of each cable. This additional capability will help for testing individual cards and

verify the cable IO connectivity and operation. This option could prove particularly useful since the higher speed LVDS transceiver devices used on of the CMX card do not offer the boundary scan access which is available on the LVDS parts used for the CMM card.

In order to reduce the total number of component types used on the CMX card the CTP output circuitry uses the same level translators and the same LVDS transceiver devices as the Cable IO circuitry does. The same requirement was also added that the BF FPGA (or the TP FPGA) should be able to operate the two CTP output ports independently as input or output.

It was noticed that the backplane pinout defines three additional Cable IO signals that were not routed on the CMM card and are not handled by the Rear Transition Module (RTM) cards. There were unused channels in the Cable IO circuitry used on CMX and one signal was added to each port. This extra bit or lane of communication between a Crate CMX and a System CMX will not be usable without building new RTM cards.

The merged clock-parity scheme described in the PDR for operation of the backplane input is no longer considered as the preferred mode of operation. An explicit clock signal will be transmitted and one bit on each cable is now dedicated to that purpose. The CMX hardware has been designed to be compatible with either scheme.

1.5 Parallel Support Projects

1.5.1 VAT Card

A project was started in parallel to the CMX design as a prototype of some of the aspects of the full CMX card. The VAT card (VME/ACE/TTC) was created to redesign some of the CMM hardware circuitry using new components and replace several discrete components with a single FPGA device which is now called the Board Support FPGA on CMX. The VAT card is a test card in 6U VME form factor which implements the interface to the ACE and TTC sub-sections and includes a small Virtex-6 FPGA device as a target for configuration.

The VAT card is being used to design the VME Interface Firmware and practice controlling the System ACE and configuration of the Virtex-6 FPGA from the Board Support FPGA. It is also used to practice working with the test stand.

The hardware and firmware details learned from the VAT project are being implemented in the CMX design.

The VAT card design files can be found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/vat_card/

1.5.2 Mechanical-Only CMX Card and Stiffener Bars

A Mechanical-Only CMX Card was produced including all backplane components. The purpose of this card was to verify that the CMM Gerber files had been properly interpreted and the measurement properly transferred to the CMX design. It was a verification of the exact placement of the backplane 5-row connectors, the power connector and the metal guide module.

A card the size of CMX with large Ball Grid Array components and with a large number of backplane pins needs to be mechanically stiff to allow proper insertion and to protect the Ball Grid connection. Stiffener bars are thus required along the sides and the back of the card. These bars also help in transferring and distributing the force exerted on the front panel ejector handles during card insertion and card extraction.

The FPGAs and the optical transceivers will generate heat and the stiffener bars must be designed for minimal interference with the airflow across the board. Much of the metal has been removed from the stiffener bars installed on the top and bottom edges of the card. The posts where the bars attach to the circuit board have also been aligned with the mechanical structures of the VME card cage which are already impeding airflow.

This Mechanical-Only CMX Card was fitted with a prototype of the full set of the stiffener bars designed for use on CMX. The stiffener bars are bolted to the board and to a front-panel with the required all-metal handles.

Pictures of the Mechanical-Only CMX Card installed in the MSU test rack can be found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/mechanical_only_card/

Views of the mechanical model of the CMX including front panel and stiffener bars are in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/mechanical/

1.5.3 Virtex-6 Evaluation Board Studies

A Xilinx M605 Evaluation Board for the Virtex-6 is being used as a test platform for designing and validating the firmware of the Base Function FPGA and making timing and power usage measurements.

2 General Description

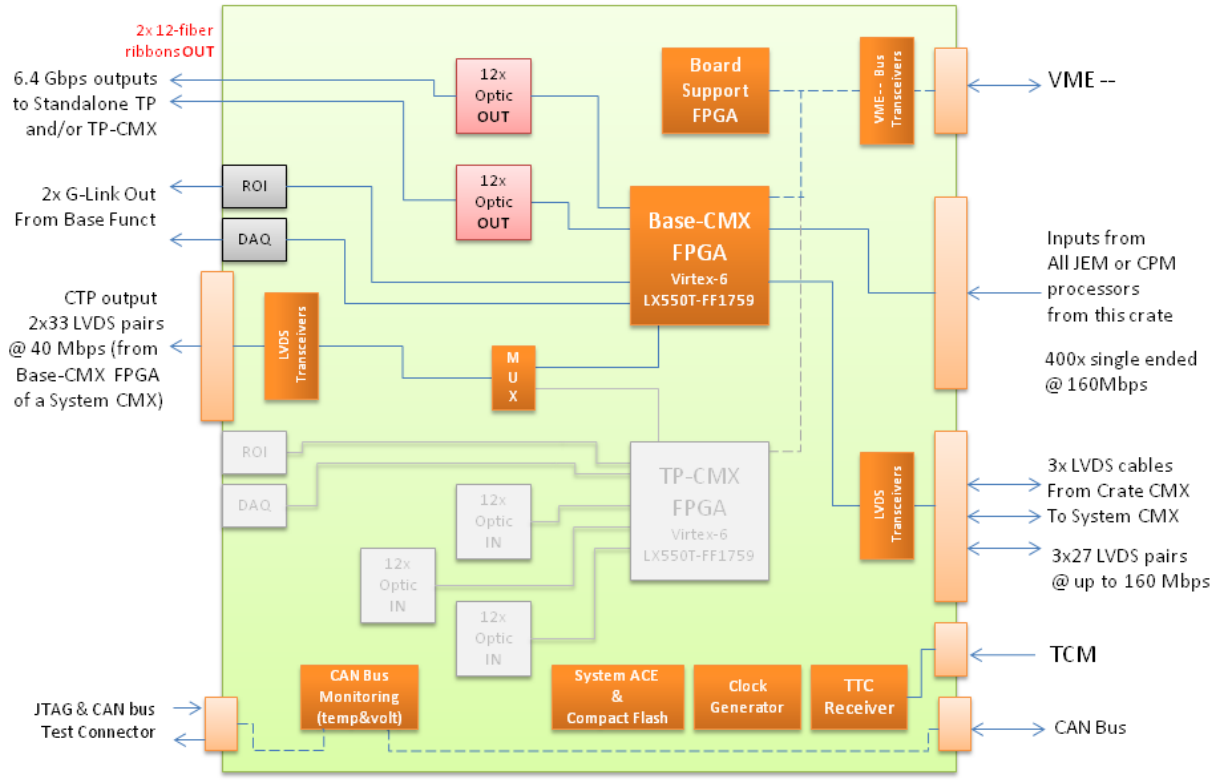

Figure 1 CMX block diagram for Base Function operation

The CMX must:

1- Be able to perform all tasks currently handled by any CMM.
2- Be able to perform these CMM tasks at higher input and output line rates.
3- Provide more computing power to support additional algorithms.
4- Provide new functionality to send a raw or processed copy of its inputs out optically.
5- Provide optional functionality to perform Topological Processing on CMX data.

2.1 CMM Emulation

In order to become a replacement for the CMM card, the CMX module must be able to operate in the CMM slots of the L1calo crates. It must use the same backplane pinout for all its backplane VME--, power, signal, control and monitoring pins. Signal names were carried over from the CMM to the CMX to avoid confusion.

The CMX must also provide the same LVDS connectors as CMM for sending its results to the CTP over the existing cable plant.

The CMX must be able to provide the same backplane Cable IO capabilities as the CMM and it must be able to operate as Crate CMX or System CMX. The set of CMX cards installed in L1calo must be able to use the existing RTM modules and Crate CMX to System CMX cable plant.

Like the CMM the CMX provides G-link ports for optical DAQ and ROI outputs to the existing RODs over the existing fibers.

Like the CMM the CMX uses System ACE for configuring the Virtex-6 FPGA firmware.

Like the CMM the CMX supports CAN bus monitoring of temperature and voltages on the board, but the quantities being monitored are different.

The CMX is however not be able to present the same set of VME control registers as the CMM, and the online software will thus have to be modified and extended to control and monitor the CMX cards.

2.2 Increased Bandwidth

The CMX is able to run at the speed of the CMM card, but also supports a new mode of operation with higher line rates

1- for the backplane signals it receives from the JEM or CPM modules
2- for the cable IO connecting a Crate CMX to its corresponding System CMX
3- for the CTP output

2.2.1 Inputs from JEM or CPM modules

The CMX receives over the backplane inputs from up to 16 JEM or CPM processor modules present in the same crate. 25 signals are received from each processor module for a total of 400 (16 x 25) backplane input signals. The CMM operation is based on receiving one bit of information on each backplane input line for each beam crossing, i.e. one bit every 25 ns or 40 Mbps. One bit out of the 25 bits received from each source processor module is currently dedicated to parity.

The CMX needs to receive 4 bits of information on every backplane line for every beam crossing, i.e. one bit every 6.75 ns or 160 Mbps. The bit that was previously used for parity is now dedicated to carry a clock signal, alternating between low and high every 6.25 ns, i.e. an 80 MHz clock.

We believe the characteristic impedance of the 400 processor input lines is 65 Ohms. The CMX tries to maintain a 65 Ohm characteristic impedance from the backplane pins to the FPGA input pins. This turned out to be impractical and compromises had to be made for the last ~ 1cm which are described in section 3.

2.2.2 Crate CMX to System CMX Cable IO

The CMX card is able to send or receive parallel LVDS data to or from other CMX cards. The direction of data flow depends on whether the CMX card is used as a Crate CMX or a System CMX as will be described in more details in section 3. Up to three LVDS cables can be connected to a CMX card via a Rear Transition Module (RTM) plugged in the back of the crate that route the cable LVDS signals to the backplane pins.

On the CMM card three sets of 27 LVDS signals are operated together as inputs or as outputs. The CMM operation is based on sending or receiving one bit of information on each Cable IO LVDS line for each beam crossing, i.e. one bit every 25 ns or 40 Mbps, with one bit out of the 27 bits from each cable being dedicated to parity and one bit being reserved.

The CMX is able to send or receive up to 4 bits of information on every LVDS line for every beam crossing, i.e. one bit every 6.75 ns or 160 Mbps. A bit from each cable that was previously reserved could be used as a clock signal if necessary. The current plan is to operate the Cable IO links at 80 Mbps. The existing RTMs and cable plant are expected to be able to support operation at 80Mbps. New RTM modules might be required if operation at 160Mpbs becomes desirable.

The direction of the LVDS transceivers used for each IO Cable is controllable from the Base Function FPGA, and each cable can be controlled independently to operate as input or output. This feature is pictured to be useful during initial card testing and commissioning. The DS91M040 does not offer the boundary scan feature that exists for the SCAN92LV090 used on the CMM. Special test firmware and loopback cables could thus be used to achieve a similar test feature.

2.2.3 Output to CTP

The CMX card is able to send parallel LVDS data to the CTP system. Only the System CMX cards send trigger information to the CTP as will be illustrated in more details in section 3. Up to two LVDS cables can be connected to a CMX card via the two front panel connectors.

On the CMM card two sets of 33 LVDS signals are used as outputs. The CMM operation is based on sending one bit of information on each CTP Output LVDS line for each beam crossing, i.e. one bit every 25 ns or 40 Mbps, with one bit out of the 33 bits in each cable being dedicated to parity.

The CMX is able to send up to 4 bits of information on every LVDS line for every beam crossing, i.e. one bit every 6.75 ns or 160 Mbps. The current usage plan is to operate the CTP Outputs at 40 Mbps.

The direction of the LVDS transceivers used for each CTP Output connector is controllable from the BF FPGA (or the TP FPGA when present), and each cable can be controlled independently to operate as input or output. This feature is pictured to be useful during initial card testing and commissioning. The CMM provides boundary scan for this port, but CMX test firmware and loopback cables could be used to achieve a similar test feature.

2.3 Increased Processing Power

One advantage of redesigning the CMM module using newer FPGA technology is that more logic blocks and thus more processing power is available on the CMX than on CMM by a factor of between one and two orders of magnitude, depending on what is being considered cf. Figure 2. This document does not attempt to explore the possible usage of these resources which may include implementing thresholds on CMX in addition to those available on JEM and CPM.

	Part Number	XC6VLX550T
	EasyPath™ FPGA Cost Reduction Solutions(1)	XCE6VLX550T
Logic Resources	Slices(2)	85,920
	Logic Cells(3)	549,888
	CLB Flip-Flops	687,360
Memory Resources	Maximum Distributed RAM (Kb)	6,200
	Block RAM/FIFO w/ECC (36 Kb each)	632
	Total Block RAM (Kb)	22,752
Clock Resources	Mixed-Mode Clock Managers (MMCM)	18
I/O Resources(4,5)	Maximum Single-Ended I/O	1,200
	Maximum Differential I/O Pairs	600
Embedded Hard IP Resources(6)	DSP48E1 Slices	864
	PCI Express® Interface Blocks	2
	10/100/1000 Ethernet MAC Blocks	4
	GTX Low-Power Transceivers	36
	GTH High-Speed Transceivers	—
Speed Grades	Commercial	-L1, -1, -2
	Extended	-2
	Industrial	-L1, -1
Configuration	Configuration Memory (Mb)	144.1

Figure 2 Resources available on the Virtex-6 XC6VLX550T

2.4 Added Functionality

In addition to reproducing and extending the functionality existing on the CMM card, the CMX card provides new functionality. The main motivation for replacing the CMM cards was to send the backplane input information that is received on the CMX card to an external L1 Topological Processor system (L1topo).

A given CMX card only sees information local to its crate and only information of one type (electron, tau, or jets objects, or energy). The key characteristic of a L1topo system is concentrating the information from all 12 CMX cards (plus other sources as they become available). Using more complex algorithms L1topo is able to compare and combine information including the full geographic coverage (e.g. for invariant masses or angle of

separation) and combining multiple types of information (e.g. electrons and jets). This document does not discuss the operation or usage of any form or L1topo system.

Originally requested as a backup plan in case a dedicated L1topo system would not be built or would not become available on time, some Topological Processing ability was proposed for the CMX card. The design study described in section 1 was carried to explore the feasibility with regard to cost and architecture and to come up with a plan to implement this desired feature.

Topological Processing on the CMX platform is no longer likely to be used because a dedicated L1topo is being designed and built. The functionality required for supporting a reduced L1topo system on the CMX platform is still being requested for future undefined optional usage. This feature provides some attractive flexibility for interconnecting CMX cards and concentrating in one place information from geographically separate sources. It could for example be viewed as an alternate and higher bandwidth method of connecting Crate CMX cards to their System CMX card. This document does not try to explore the operation or usage of the CMX platform as a L1topo system.

2.4.1 Cluster information sent by each CMX to Topological Processor

Each CMX card is able to drive 24 independent optical outputs arranged as two 12-fiber optical ribbon cables operating at 6.4 Gbps with a reference clock synchronous to the LHC clock.

One 12-fiber ribbon used with 8b/10b encoding is able to send all the raw input backplane data to an external L1topo system. There are however several possible motivations for sending less than 12 fibers from each CMX card. For example one could zero-suppress the input data or perhaps re-order the information to send the highest energy objects first.

The output fibers are ganged in two 12-fiber ribbons, but the 24 optical outputs can be independently driven to form arbitrary subsets of e.g. 4 or 6 fibers with each set sending identical or different information to multiple destinations. If some subset(s) of the 12 fibers from a given ribbon need to be split and sent to separate destinations, some kind of external splitting and re-bundling patch panel system will need to be devised and built.

The data format and protocols used over the optical links are described elsewhere.

This additional functionality is implemented by the Base Function FPGA.

2.4.2 Optional limited TP capability included

Some optional circuitry is added to the CMX platform so that it can operate in a manner similar to the standalone L1 Topological Processor but with a reduced input bandwidth and reduced processing power. This means that a CMX card should be able to receive the optical information sent out optically by some (or all) of the other CMX cards of the L1calo system.

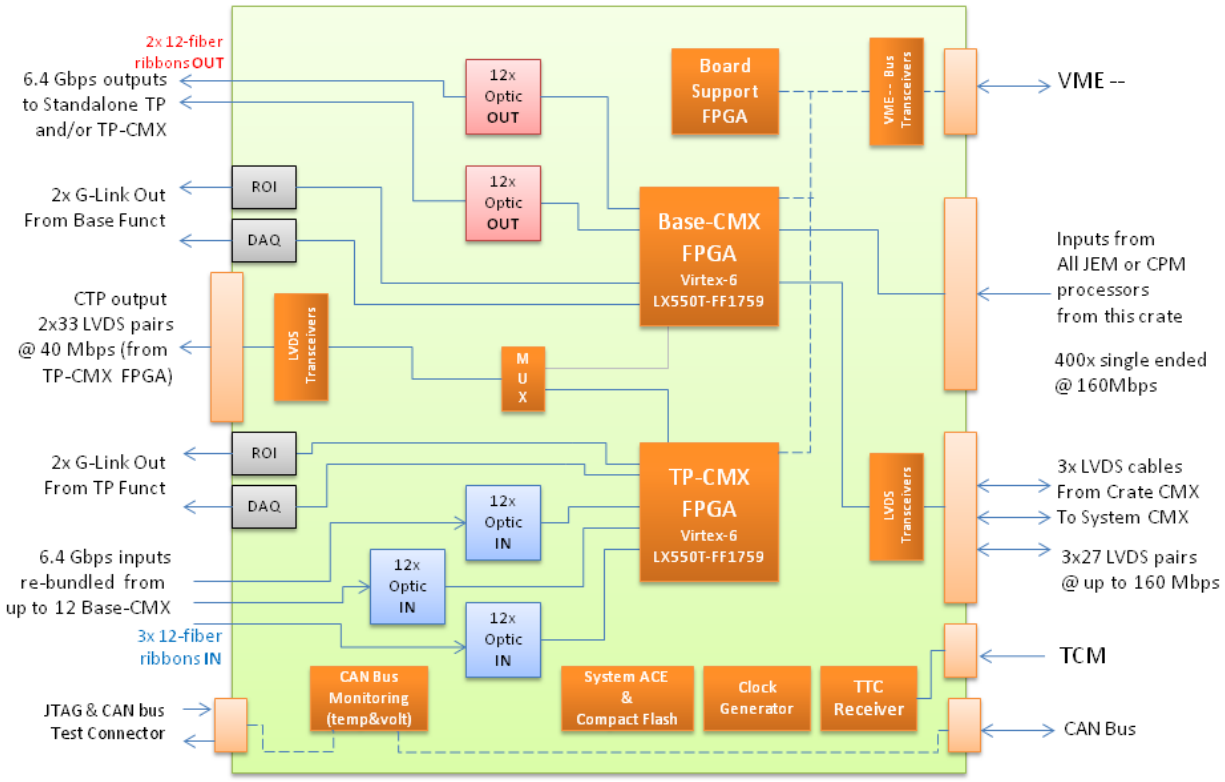

Figure 3 CMX block diagram with TP FPGA installed

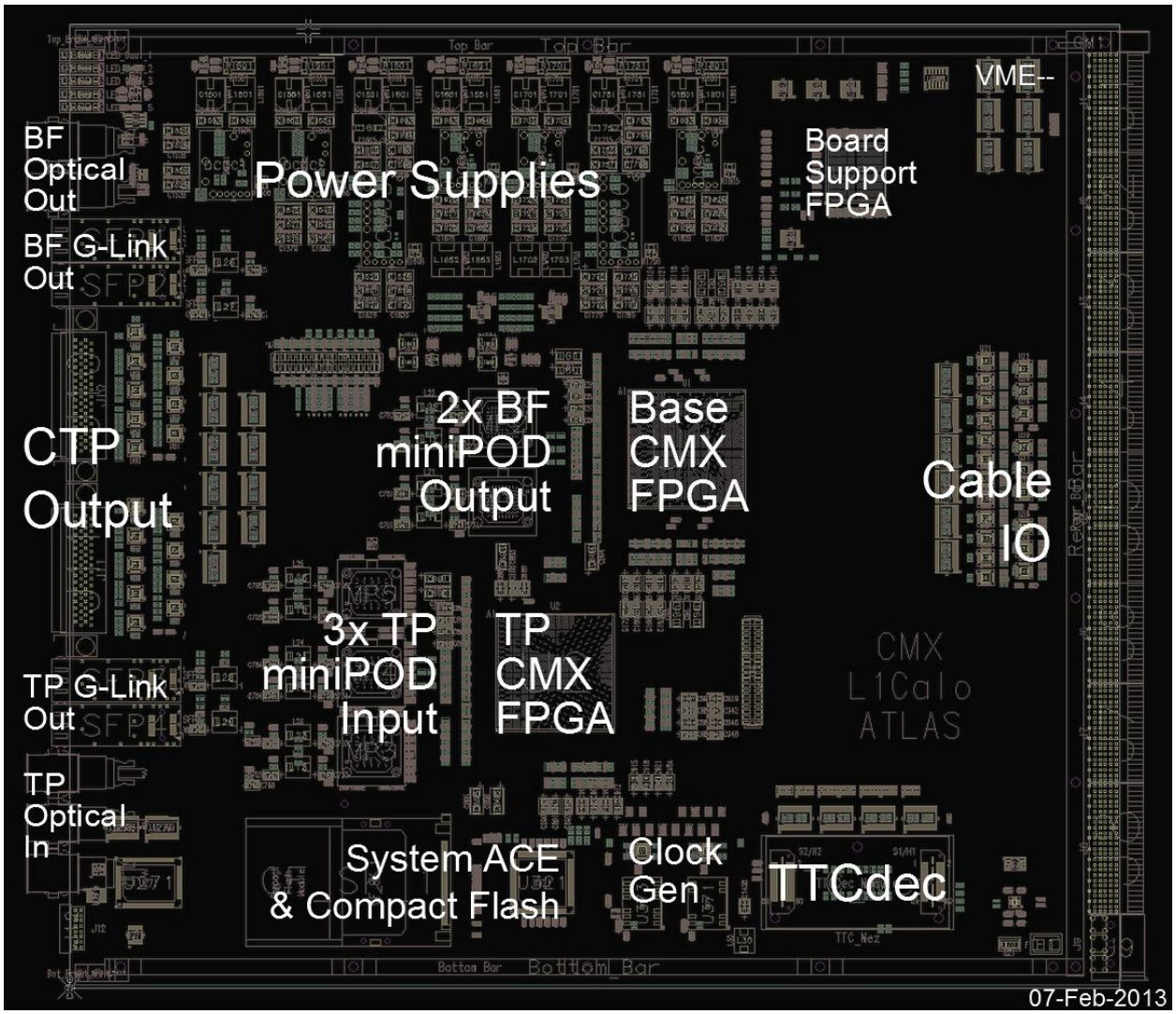

Figure 4 Board Layout view of CMX

This additional Topological Processing functionality is implemented in a separate Topological Processing FPGA (TP FPGA, cf. Figure 3 and Figure 4). There will be no real-time communication between the BF and TP FPGAs and this means that any trigger information from the local BF FPGA that needs to be sent to the TP FPGA on the same card needs to be sent over optical fibers just like the trigger information coming from all other participating CMX cards.

Each CMX card with TP capability is able to receive 36 optical inputs arranged as three 12-fiber optical ribbon cables operating at 6.4 Gbps coming from sources that are expected to use a reference clock synchronous to the LHC clock.

The TP FPGA will be installed on only a subset of the CMX cards that will be produced (cf. section 7). The presence or absence of the TP FPGA device is the only difference between CMX cards assembled for use as Base Function Only and CMX cards assembled with Topological

Processing capability. The passive sockets for the MiniPOD devices and the passive cages for the SFP transceivers used with the L1topo feature will be assembled on all cards while the active optical devices will only be installed on the few CMX cards with TP FPGAs. This aspect is illustrated in the difference between Figure 1 and Figure 3.

Any CMX card with a TP FPGA is able to operate as a Crate CMX. Any CMX card with a TP FPGA could operate as a System CMX, but only if the TP functionality is not being used such that there is no contention for the CTP Output driver resources. If Atlas decides to use the TP functionality on one (or more) CMX card in the full system including sending triggering information to CTP, one of the Crate CMX cards should then be selected for that purpose.

2.5 Board Control

Ancillary tasks which are not part of the real-time operation of the CMX card are implemented in a separate smaller FPGA called the Board Support FPGA (BSPT).

The BSPT is responsible for controlling the configuration of the Virtex-6 FPGAs and presents a number of registers on the VME-- Bus to provide control and monitoring of the devices on the board. This function is sometime referred to as the VME interface, but it is not an interface in the full sense of the word where the VME-- Bus would be on one side and the internals of the card on the other side. Buffers and level translators form the physical interface between the VME-- Bus and the On-Card Bus. The BSPT FPGA manages that physical interface. All three FPGAs (BF, TP, and BSPT) are targets for VME-- Bus cycles via the same On-Card Bus and each presents its own set of VME-- addressable registers. More details appear in section 3.

3 Real-time Data Path

3.1 Overview and usage in L1calo

There are two separate usages for the CMM/CMX cards in the L1calo system. Some CMM/CMX cards act as Crate CMM/CMX cards and others as System CMX cards. Consequently there are two separate patterns for the real-time data paths possible in the operation of the Base Function tasks performed by the CMX.

There is a total of twelve CMX cards in the full L1calo system inter-connected as 4 groups, with each group handling the trigger information concerning a particular object type: electron, tau, Jet or Energy (cf. Figure 5).

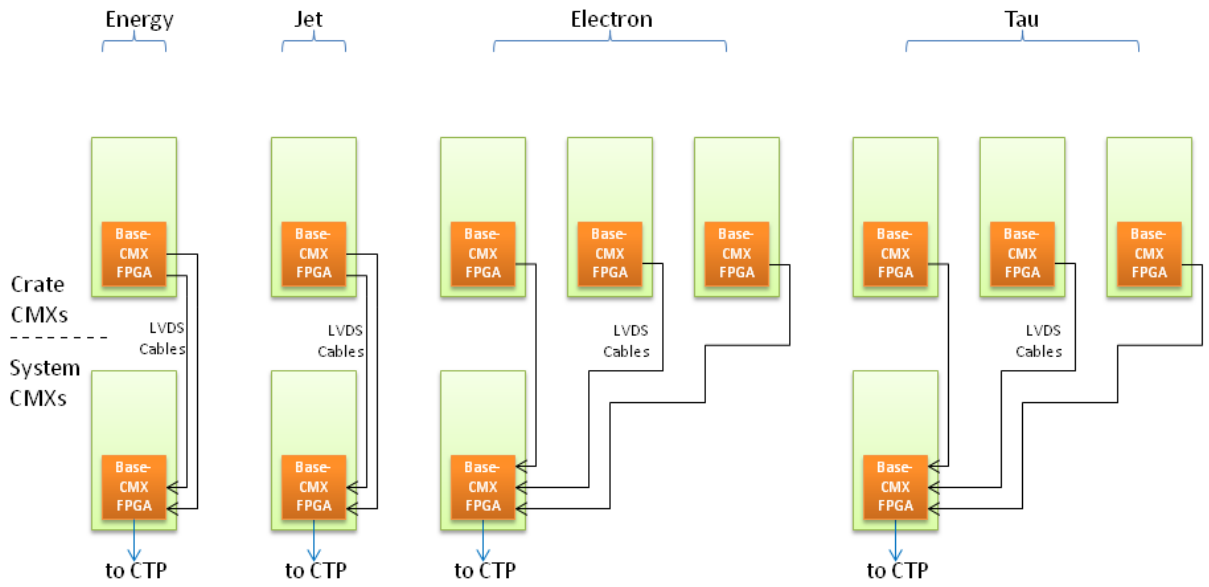

Figure 5 Crate CMX and System CMX arrangement in L1Calo

3.1.1 Crate CMX

A CMX acting as a Crate CMX receives the 400 backplane inputs coming from the 16 processor modules slots in that crate (yellow in Figure 6) and computes local counts of objects and sends that information out through the backplane over one or two LVDS cables to a System CMX (blue in Figure 6).

A Crate CMX (as every CMX card in the L1calo system) sends this local trigger information out optically to L1topo (green path in Figure 6). Information going to the L1topo is serialized by the Base Function FPGA which drives two Avago MiniPOD optical transmitters. Two 12-fiber ribbon "pigtails" connect the MiniPODs to two feed-through MTP connectors on the front-panel.

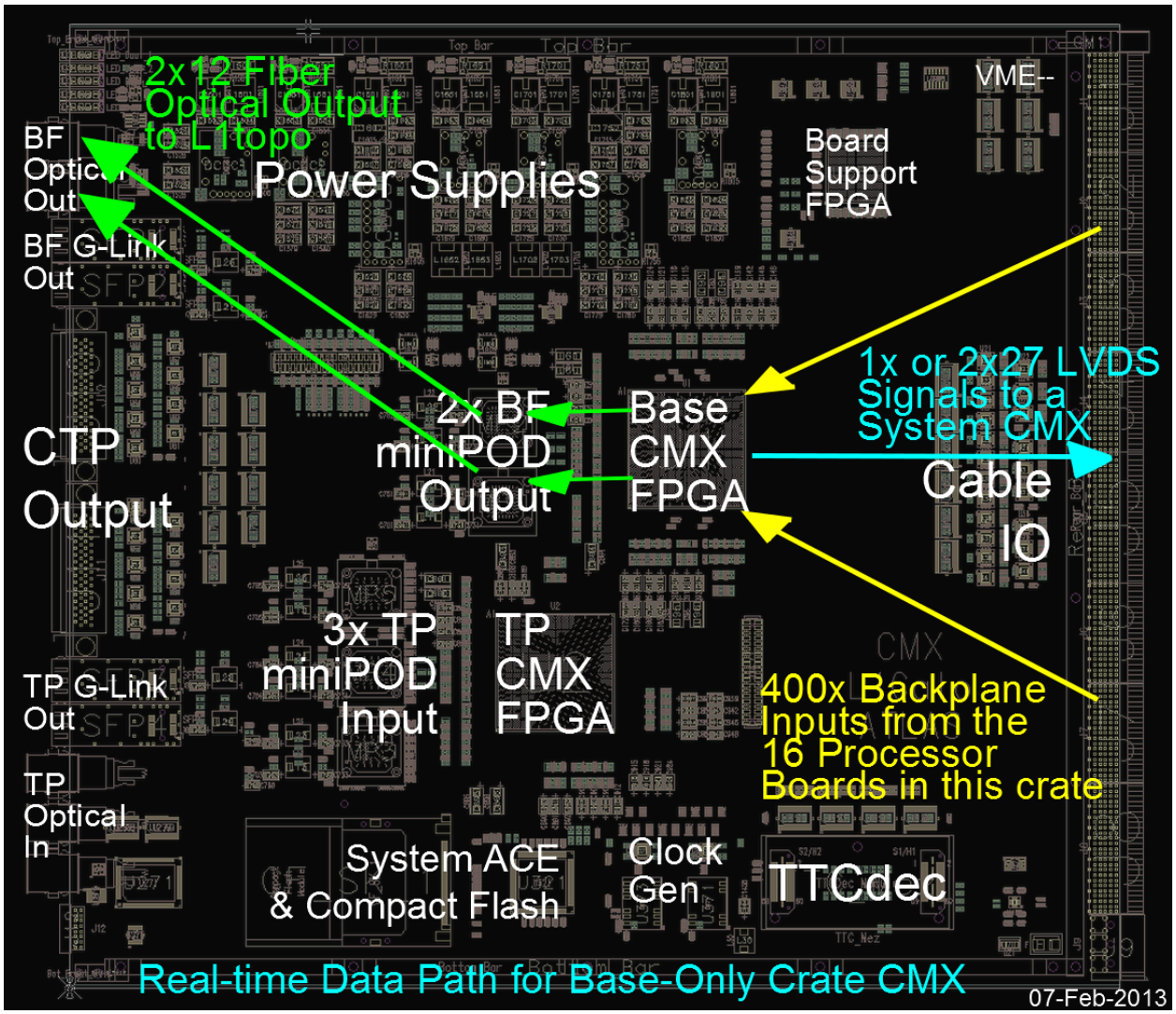

Figure 6 Real-time Data Path for the Base Function on a Crate CMX

3.1.2 System CMX

A CMX acting as a System CMX receives the 400 backplane inputs coming from the processor modules in the crate (yellow in Figure 7) and sends this local trigger information out optically to L1topo (green in Figure 7) exactly like a Crate CMX does.

A System CMX computes its counts of local objects as well but does not send that information out. Rather it merges its own count information with the count information it receives through the backplane over 2 or 3 LVDS cables (cf. Figure 5) coming from all the Crate CMXs handling the same type of information (blue in Figure 7).

A System CMX forms the final trigger information for the object type it handles and sends it to the CTP over 1 or 2 LVDS cables attached to the front panel (red in Figure 7).

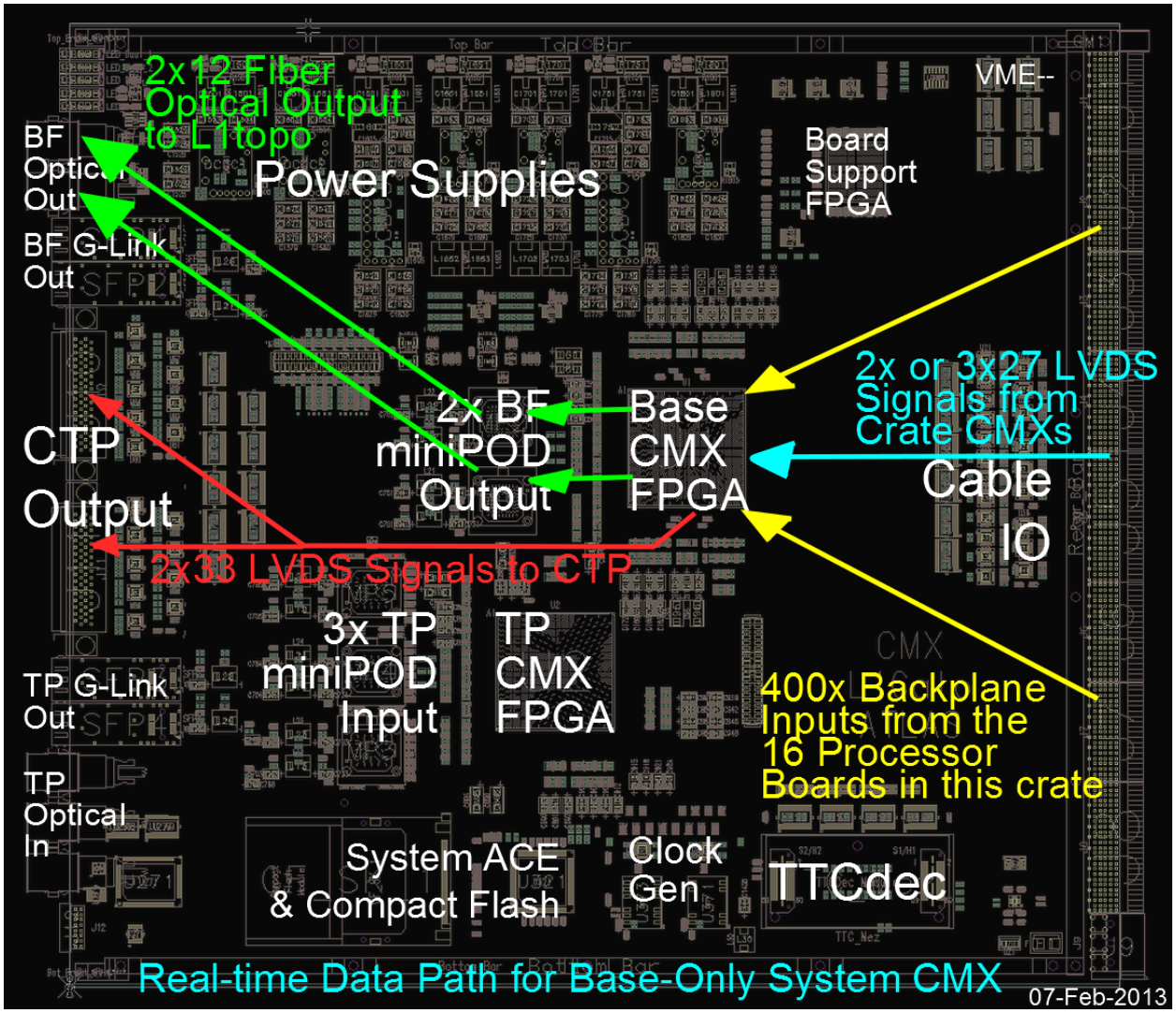

Figure 7 Real-time Data Path for the Base Function on a System CMX

All twelve CMX cards in the full L1calo system send optical information to the external L1topo (green in Figure 6 and Figure 7). This connection could be direct, using one full 12-fiber ribbon from each CMX card. If fewer than 12 fibers are needed from each CMX card (6 fibers as currently planned) a patch panel will be necessary for splitting and re-bundling the 12-fiber ribbons as shown in Figure 8.

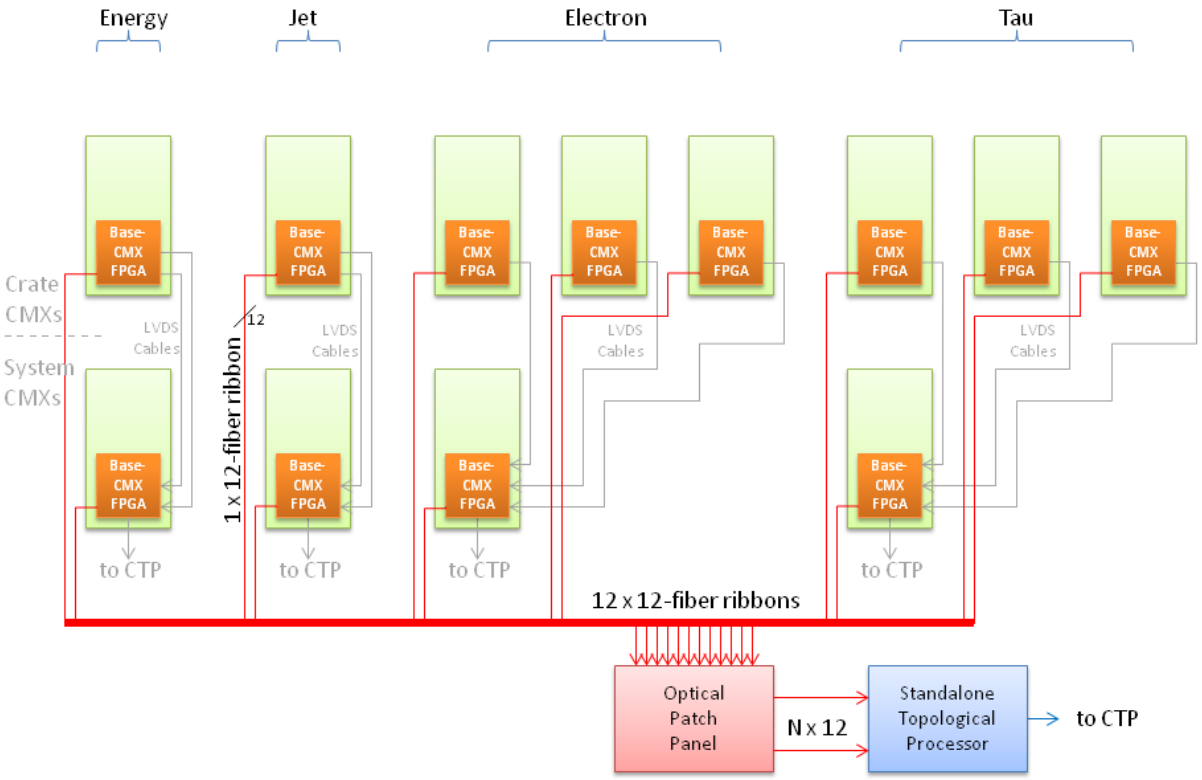

Figure 8 Twelve CMX sending information to L1topo via an optional patch panel

3.1.3 L1topo CMX

A CMX equipped with a TP FPGA can also be used as a L1topo CMX. The TP functionality is independent from and in addition to the Base functionality but requires sending output to CTP and thus should be used on a Crate CMX card (as opposed to a System CMX card), i.e. on a CMX cards whose Base Function does not already need to use the CTP Output LVDS resources.

The TP input information is received over up to three 12-fiber ribbons, translated to electrical signals by three Avago MiniPOD Receivers connected to the TP FPGA (orange in Figure 9). The TP FPGA de-serializes this trigger information, performs all sorting and processing needed to implement the desired trigger algorithms and sends its results to the CTP over 1 or 2 LVDS cables attached to the front panel connectors (red in Figure 9).

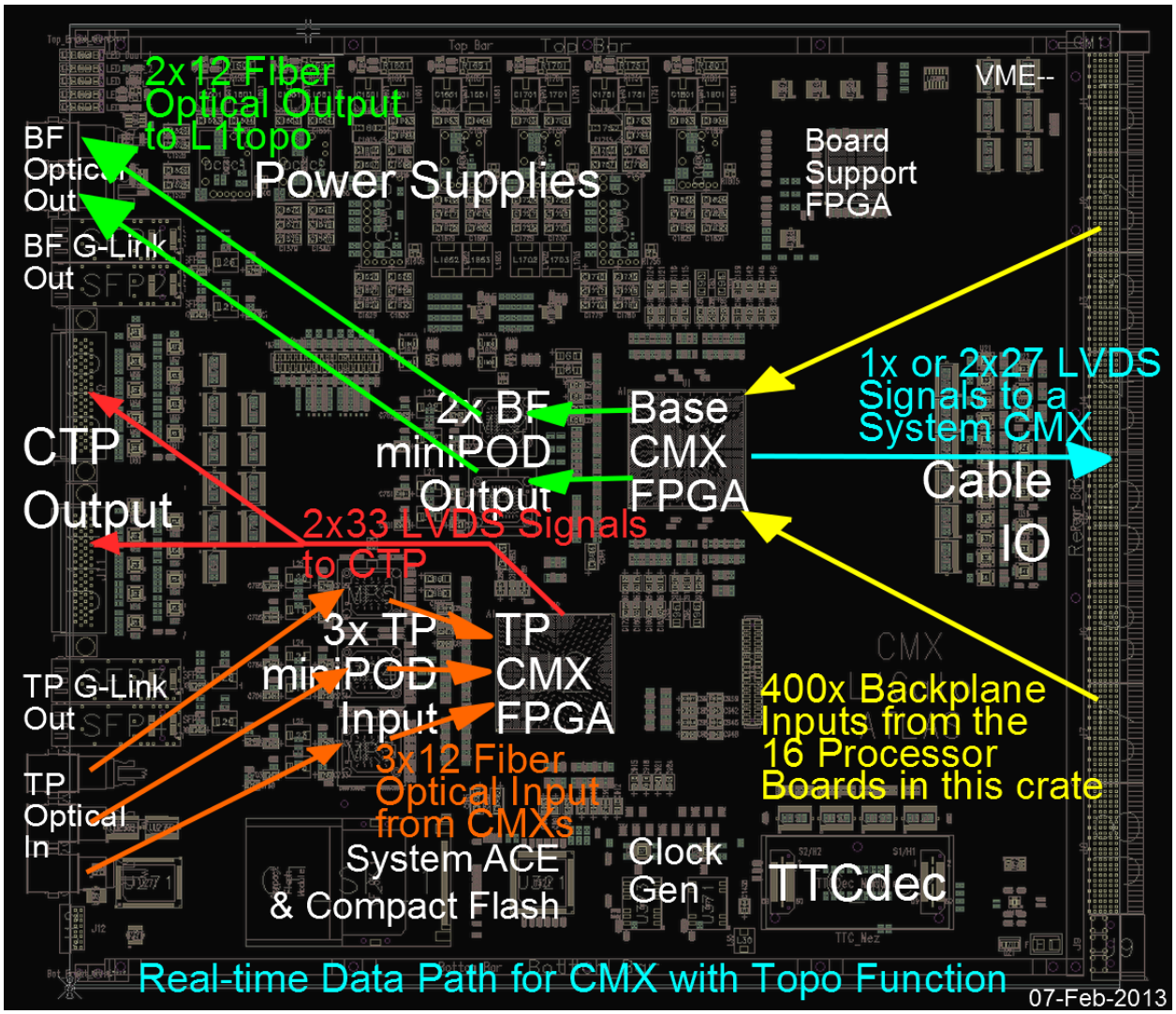

Figure 9 Real-time Data Path for a Crate CMX also using its TP Function

All or a subset of the twelve CMX cards in the L1calo system could be sending input information to the L1topo CMX's TP FPGA. A source CMX card sends its information out on a 12-fiber ribbon and a patch panel would presumably be required to split a subset of the 12 fibers from each source CMX and re-bundle the resulting set of fibers in up to three 12-fiber ribbons that can then be connected to a L1topo CMX.

More than one L1topo CMX could be operating in parallel if desired as illustrated in Figure 10.

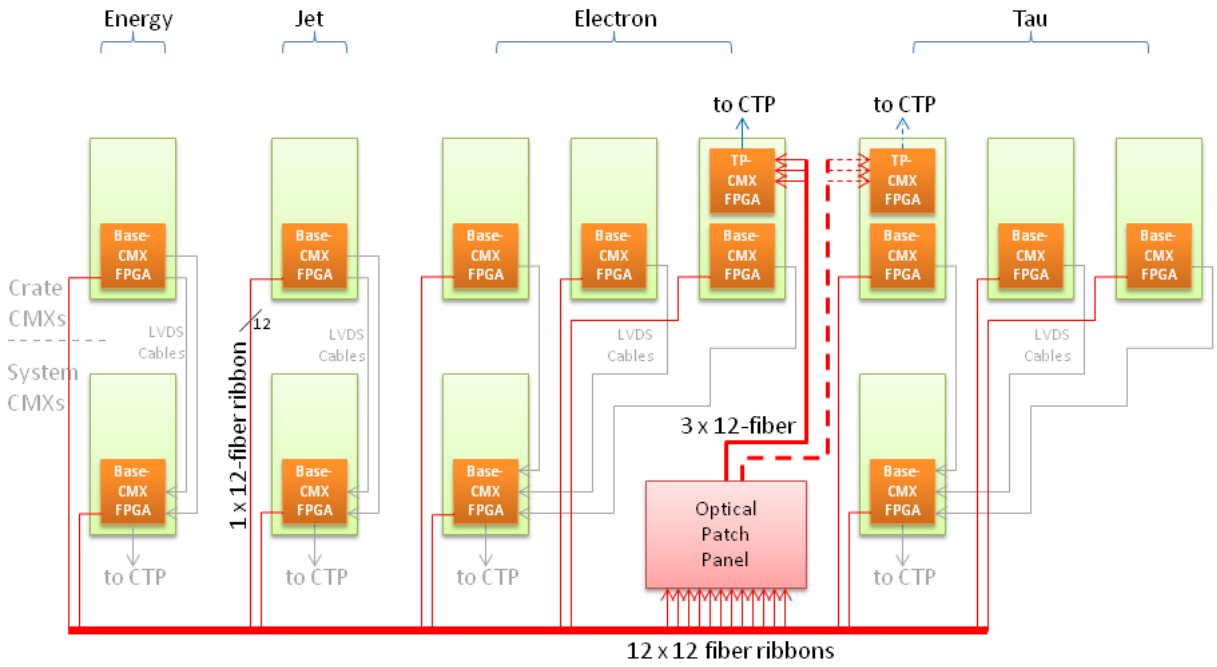

Figure 10 Twelve CMX cards sending TP information to one (or more) CMX L1topo

The standalone L1topo and a CMX L1topo could also be used at the same time as illustrated in Figure 11.

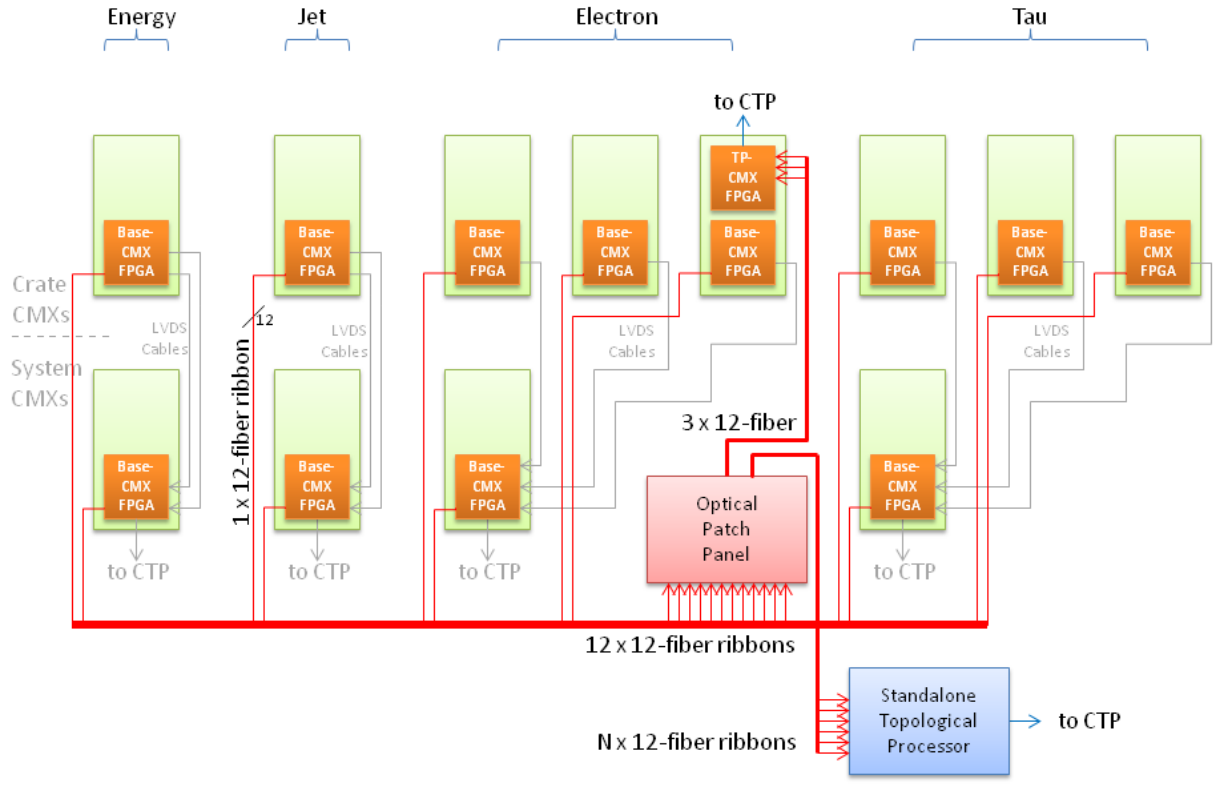

Figure 11 Twelve CMX cards sending TP information to a Standalone L1topo and a CMX L1topo

3.2 Backplane Inputs

The CMX card receives 400 (25 from each of the 16 Processor modules in the crate) source terminated single-ended signals with a line impedance nominally specified as 65 Ohms. The Phase 0 upgrade involves an increase in line rate on these 400 lines from the current 40 Mbps to 160 Mbps, i.e. 6.25 ns per bit of information transferred.

These signals are routed directly from the backplane to the Base Function FPGA. Every known precaution is being taken to maintain signal integrity and insure signal recovery for all 400 inputs.

In each group of contiguous IO banks handling one set of Processor inputs, one pair of VRN and VRP IO pins is connected to a pair of external resistors to provide the reference impedance for the line termination implemented by the Virtex-6 Digitally Control Impedance (DCI) technology. This feature was implemented and is available if needed to help with the reception of the 400 Processor input signals.

In all IO banks handling Processor inputs the VREF pins are connected to an adjustable power supply on the card which provides a reference voltage of 1.25 V +/- 0.5V. This will allow for fine control of the threshold voltage used with the differential input receiver of the Select IO pins used for the 400 backplane inputs. This adjustable reference voltage will let us adjust the threshold to something other than the middle of the 0-2.5 V logic range if difficulties are encountered at the 160 Mbps line rate.

The PDR document specifies that one signal from each set of 25 input signals be used as a combined clock and parity signal and that the incoming clock and timing information should be recovered from this clock/parity signal. This protocol had the advantage of dedicating only one of the 25 lines for a purpose other than carrying trigger information thus leaving 4*24 bits (for a 160 Mbps line rate) of information available from each source for each beam crossing. Implementing this clock/parity communication protocol requires using one Mixed-Mode Clock Manager (MMCM) per source Processor Module.

After extensive firmware studies it became apparent that (1) the MMCM used had to be on the same horizontal row of inside the FPGA logic as the clock/parity line, (2) the IO banks used to receive all backplane inputs had to be on the inner vertical rows of logic inside the FPGA and (3) the clock/parity lines had to be connected to regional clock inputs to be compatible with all proposed clocking schemes. After several iterations a satisfactory allocation of the IO banks and IO pins was found that satisfied board layout constraints while only using the inner

columns of IO banks for the processor inputs and while receiving exactly two Regional Clocks per horizontal row to match the distribution of MMCMs as illustrated in Figure 12.

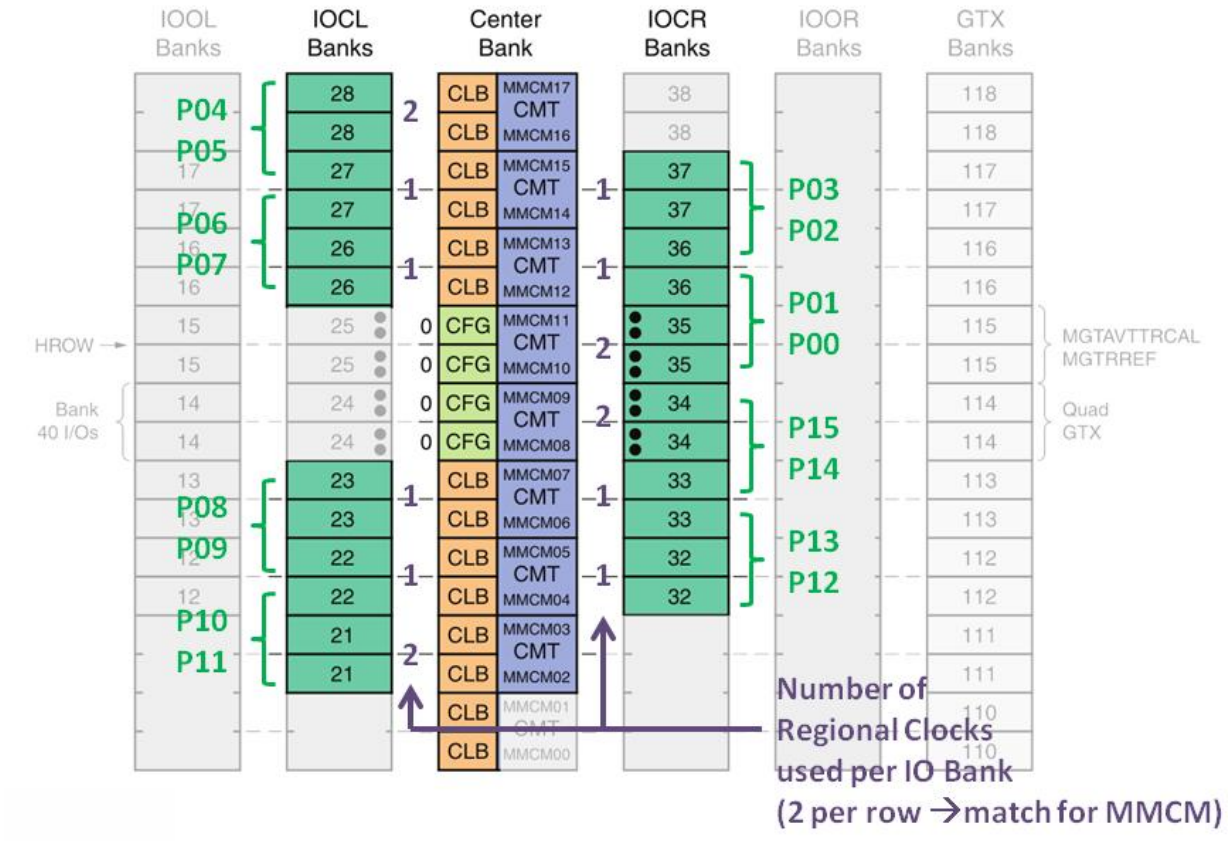

Figure 12 IO Banks Allocation for the 16 sets of Processor inputs

Using this merged clock/parity scheme would use 16 of the 18 MMCM resources of the Virtex-6 leaving two MMCMs for all logic processing and MGT operation on the Base Function FPGA. The merged clock/parity scheme is no longer expected to be used in L1calo but the CMX card has been designed to be compatible with such protocol.

The current plan is to use 23 lines to carry data, one line to carry parity and use the 25th line as a dedicated clock signal switching at 160 Mbps, i.e. an 80 MHz clock. The input data will be latched on both the rising and falling edges of this clock signal. It is our understanding that there is some fixed timing skew among the 24 data and parity lines with respect to the clock edges. With an input signal switching every 6.25 ns the safe window for latching the information might only be 1-2 ns wide. The Base Function firmware must thus use the IODELAY technology available on the Virtex-6 FPGA and individually adjust the time when each input line is being latched with respect to the clock line edges. An algorithm needs to be devised to automatically seek and remember the optimal control value of the IODELAY for each of the

16*24 backplane data lines. These values will likely need to be determined in situ, but are expected to remain stable until the CMX or one of the Processor Modules needs to be replaced.

Maintaining the 65 Ohm line impedance over the full signal trace path turned out not to be practical. In order to maximize signal integrity, the original intention was to route all 400 trace signals on internal layers straight from the backplane pin to a via under the FPGA select IO pin receiving that signal without any additional via in-between. A solution was found that solved the topological requirements and used 10 internal signal layers. It was however not possible to build a card with that many signal layers able to support 65 Ohm traces of reasonable width. The thickness of dielectric required between the trace layers led to a total board thickness not practically usable for a VME card.

The next best strategy was chosen which uses much fewer 65 Ohm trace layers. For all 400 backplane signals either all of the trace path to the Select IO pin or most of the trace path from the backplane pin to within about 1 cm of the Select IO pin is routed with a 65 Ohm trace. A fraction of the backplane signal traces are switching for the last ~1 cm to a different signal layer providing only 50 Ohm of characteristic impedance. This method requires careful management of the “ring of vias” required near the FPGA so that they can remain close to the FPGA perimeter without impeding the path of the majority of the traces routed directly under their target Select IO pins. Short angled rows of 6 to 8 vias provide these access channels.

The CMX card has 8 internal signal layers in addition to the top and bottom signal layers. The top, bottom and 5 of the internal layers are compatible with 65 Ohm traces while the other 3 are not. Two of the 3 internal layers not compatible with 65 Ohm traces are used for the last ~1cm of travel for a small fraction of the 400 backplane inputs. The third is used for all connections to the VREF pins and connections to DCI control resistors.

In summary:

- All backplane input signal traces are routed from their backplane pin to at least within about 1 cm of the FPGA perimeter on 65 Ohm traces located on internal signal layers situated between two ground planes.
- 265 traces (66%) reach all the way to the via located under the FPGA pin
- 136 traces (34%) need to switch layers near the FPGA.
- 43 traces (11%) have a short ~1cm segment not matching the 65 Ohm (50 Ohm).
- All clock lines remain on 65 Ohm traces and do not switch layers

A spice model of a complete transmission line was created to verify that a 50 Ohm impedance bump on the last 1-2 cm of the 65 Ohm line had very little impact on signal integrity.

Section 6 provides more details on the CMX card layers.

3.3 Cable IO

A Crate CMX needs to send its local counts information to a System CMX for merging into global counts.

This communication if performed over 34 pair LVDS cables connected to Rear Transmission Modules (RTM) plugged in the back of the crate. Only 27 of the 34 signal pairs from each cable are currently accessible to the TP FPGA for a total of 81 differential signals passing through the backplane named M_<N>+ and M<N>- with <n>=0 to 80 like on the CMM card.

The CMX uses National Semiconductor DS91M040 LVDS transceivers which are 3.3V devices rated at 250 Mbps. The Virtex-6 IO banks cannot provide 3.3V logic levels and Texas Instrument 74AVCAH164245 level translators are used as an interface to the LVDS transceivers. These bidirectional level translators are managed in three separate groups, one for each cable. Even though the operation of the CMX cards online requires that the cables being used (1, 2 or 3 cables) be operated in one common direction, the CMX provides independent direction control via the Base Function FPGA. This feature will help during commissioning and maintenance of individual boards. The short traces between the transceivers and the backplane pins are routed on internal layers sandwiched between ground planes with a characteristic trace impedance of 50 Ohm and a differential impedance of 100 Ohm. The CMX provides a 100 Ohm differential termination on each line while the DS91M040 drivers provide twice the normal LVDS output current to be able to drive these doubly-terminated CMX to CMX transmission lines.

The RTM schematic shows the LVDS signals names with their assignments to the three cable connectors:

Connector 1		Connector 2		Connector 3	
pair	signal	pair	signal	pair	signal
01	M_00	01	M_27	01	M_54
02	M_01	02	M_28	02	M_55
03	M_02	03	M_29	03	M_56
04	M_03	04	M_30	04	M_57
05	M_04	05	M_31	05	M_58
06	M_05	06	M_32	06	M_59
07	M_06	06	M_33	06	M_60
08	M_07	08	M_34	08	M_61
09	M_08	09	M_35	09	M_62
10	M_09	10	M_36	10	M_63
11	M_10	11	M_37	11	M_64
12	M_11	12	M_38	12	M_65
13	M_12	13	M_39	13	M_66
14	M_13	14	M_40	14	M_67
15	M_14	15	M_41	15	M_68

```
16    M_15        16    M_42        16    M_69
17    M_16        16    M_43        16    M_70
18    M_17        18    M_44        18    M_71
19    M_18        19    M_45        19    M_72
20    M_19        20    M_46        20    M_73
21    M_20        21    M_47        21    M_74
22    M_21        22    M_50 *      22    M_75
23    M_22        23    M_51        23    M_76
24    M_23        24    M_52        24    M_77
25    M_24        25    M_53        25    M_80 *
26    term        26    term        26    term
27    term        26    term        26    term
28    term        28    term        28    term
29    term        29    term        29    term
30    term        30    term        30    term
31    term        31    term        31    term
32    M_25        32    M_48        32    M_78  <-- reserved for use as clock signal
33    M_26        33    M_49        33    M_79  <-- used for parity on all 3 cables
34    GND         34    GND         34    GND

term = 100 ohm termination across the differential pair on the RTM
*    = numbering discontinuities (for some historical cause unknown to us)
```

The L1calo backplane defines three more LVDS IO signals (namely M_81+, M_81-, M_82+, M_82-, M_83+, and M_83-) which are not routed on the CMM card and not routed on the RTM card. All three of these differential signals are routed on the CMX card with one bit assigned to each LVDS Cable. These additional bits could be made available for communication between Crate and System CMX if necessary, but taking advantage of these additional signals will require that new RTM modules be produced. The LVDS transceivers used (National Semiconductor DS91M040) are able to default to a defined state when no input is present.

The circuit diagram for this part of the circuitry and further details regarding the LVDS connections is found in Appendix D: LVDS Connections.

3.4 CTP Output

A System CMX or a L1topo CMX needs to send information to the Central Trigger Processor (CTP). This output is available on two 33-pair LVDS ports accessible on the front panel. This access port uses two 68-pin 3M MDR connectors. The 34th pair on each connector and connected cable can be left unused or grounded on the CMX.

In practice the CTP output cables are either both used, both unused, or only one is used, but in all cases in the online system they only operate as outputs. The CMX however allows for each cable to be independently operated as input or output to help during commissioning and card testing. Furthermore the same LVDS transceivers and level translator parts used for the cable

IO described above are used for the CTP output in order to reduce the total count of part types and simplify assembly.

Two sets of 33 LVDS signals (i.e. 66 differential signals named CN_CTP_<NN>P and CN_CTP_<NN>N on CMM but CN_CTP_<NN>_POS and CN_CTP_<NN>_NEG on CMX, with <NN>=00 to 65) are currently used. One bit on each cable is used for parity (namely <NN>=32 and 64). On CMX one bit from each cable (namely <NN> = 31 and 63) can be used as an input clock signal in the unlikely scenario that these connectors ever need to be operated as inputs at higher rates.

On a System CMX the BF FPGA needs to drive the CTP Output while on a CMX using its L1topo functionality the TP FPGA needs to drive the CTP Output. The multiplexing thus required is performed by the same 74AVCAH164245 ICs already needed for level translation.

The circuit diagram for this part of the circuitry and further details regarding the LVDS connections are found in Appendix D: LVDS Connections.

3.5 High Speed optical

All CMX cards used in L1calo need to send high-speed (6.4 Gbps) optical information out to the standalone L1topo (and optionally to a CMX L1topo). Two AFBR-821FH1Z Avago MiniPOD transmitter devices connected to the BF FPGA can drive up to 24 optical fibers arranged as two 12-fiber ribbons. Two US CONEC MTP adapters mounted on the front-panel provide access to this optical output. We currently assume the CMX card should be equipped with male ends.

A CMX card using its L1topo function needs to receive high-speed (6.4 Gbps) optical information from (presumably) other CMX cards. Three AFBR-811FH1Z Avago MiniPOD receiver devices connected to the TP FPGA can receive up to 36 optical fibers arranged as three 12-fiber ribbons. Three USCONEC MTP adapters mounted on the front-panel provide access to this optical input. We currently assume the CMX card should be equipped with male ends.

The 14.5mm height of the MiniPOD devices is a potential issue for use in the VME environment that the review committee should discuss.

The circuit diagram for this part of the circuitry and further details regarding the high-speed connections is found in Appendix E: High-Speed Optical.

3.6 DAQ and ROI G-link Outputs

All CMX cards need to send their DAQ information to a DAQ ROD and a System CMX additionally needs to send ROI information to an ROI ROD. These connections use the G-link

protocol and two SFP connector cages are connected to the BF FPGA for that purpose. The Virtex-6 performs the G-link encoding of the data sent to the transmitter sections of the SFP transceiver modules plugged in the SFP cages through the front panel.

A CMX card using its L1topo function also needs to send DAQ and ROI information to ROD cards. A separate pair of SFP connector cages is connected to the TP FPGA for that purpose.

The only clock available for implementing the G-link is the 40.08 MHz clock locked to the LHC frequency.

The circuit diagram for this part of the circuitry and further details regarding the low-speed connections is found in Appendix F: Low-Speed Optical.

3.7 Topological Processing

A CMX card using its L1topo function is additionally equipped with a TP FPGA, three MiniPOD receivers, and two SFP transceivers. The TP FPGA receives its inputs over (up to) three 12-fiber optical ribbons and has access to the CTP Output LVDS connectors. The TP FPGA is accessible from VME-- over the On-Card Bus (cf. below) for configuration and monitoring purposes.

No triggering information is exchanged electrically between the BF and TP FPGAs on a CMX card. Any exchange of triggering information would happen through an optical output from the BF FPGA connected to an optical input into the TP FPGA.

The Topological Processing usage and algorithms are not described in this hardware description document. The IO bank assignment for the TP FPGA is shown in Appendix C: IO Banks Assignments for BF and TP FPGA.

4 Board Control, Configuration and Monitoring

4.1 Clocks

The CMX card is equipped with a TTCDec module. After recovery by the TTCDec a narrow range PLL generates a clean copy of the 40.08 MHz accelerator clock. A clock buffer distributes one copy of this clock each to the BF, TP and BSPT FPGA for use as a logic clock, and one more copy each to the BF and TP FPGA for use as a reference clock for the MGT channels driving the G-link outputs. The 40.08 MHz clock is also used to control a second PLL generating a 320.64 MHz clock. This 320.64 MHz is buffered and distributed to the BF and TP FPGAs as a logic clock and to the MGT channels driving and receiving the MiniPOD channels. One copy is sent to the middle Quad of every group of three Quads handling one set of 12 MGT channels connected to a MiniPOD, i.e. 2 copies are required for the BF FPGA and 3 copies for the TP FPGA.

A separate 4 MHz crystal is used for the CAN bus processor.

All control and output lines of the TTCDec mezzanine card are connected to the BSPT FPGA. The two FPGAs of the CMM use only two outputs of the TTCDec, namely the Bunch Counter Reset and the L1accept signal. The CMX connects only these same two lines to the BF and TP FPGAs unless a new requirement is needed specifically for CMX. Level Translators are used to interface the TTCDec module to the FPGA 2.5V IO banks.

The circuit diagram for the TTCDec mezzanine connections and further details regarding the usage of the TTCDec are found in Appendix G: TTCDec data distribution.

The circuit diagram for the clock generation and further details regarding this section of the CMX are found in Appendix H: Clock Generation and Distribution.

4.2 Board Support FPGA

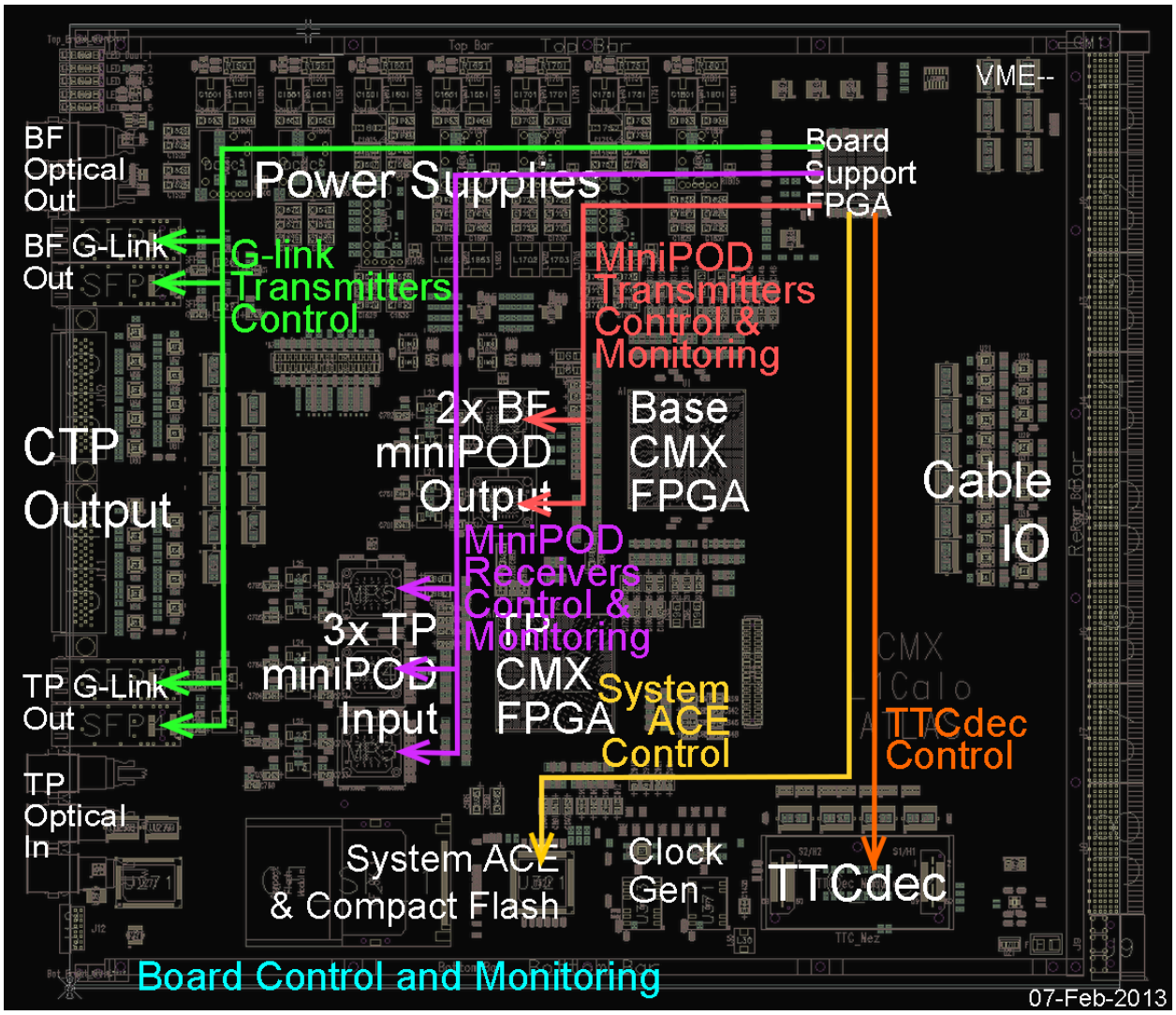

Figure 13 CMX Board Control and Monitoring

The device chosen for the Board Support FPGA (BSPT) is a Xilinx Spartan-3A XC3S400A in the 400 pin FG400 package. It is a larger version of the device used for the VAT prototype project.

The Board Control FPGA is responsible for

1. controlling the operation of the System ACE and thus configuration of the main FPGAs
2. controlling and monitoring the operation of the TTCDec
3. controlling and monitoring the MiniPOD transmitters and receivers
4. controlling and monitoring the G-link optical transmitters
5. presenting registers in VME-- space to access all above control and monitoring features
6. controlling the data bus transceivers to the VME-- bus

7. generating DTACK_B during VME-- Cycles
8. detecting the presence of and configuration of the BF and TP FPGA
9. provide logic as part of the hardwired Transceiver Control Oversight (below)
10. controlling all the front-panel LEDs except one (power)

System ACE Configuration is described below and in Appendix J: JTAG chains and FPGA Configuration.

The TTCDec data connections are described in Appendix G: TTCDec data distribution.

The MiniPOD control and monitoring aspects are described in Appendix E: High-Speed Optical.

The G-Link control and monitoring aspects are described in Appendix F: Low-Speed Optical.

The On-Card Bus is described below and in Appendix I: VME-- and On-Card Bus.

The hardwired transceiver control oversight is described below in 4.6 Transceiver Control.

The CMX Card offers fewer LEDs than CMM (5 dual color LEDs) because of the limited front-panel space left for that purpose. In order to maximize flexibility during commissioning and online operation and to postpone the hard choices to be made, all LEDs on the front-panel are “firmware-defined” via the BSPT FPGA.

4.3 VME-- Bus and On-Card Bus

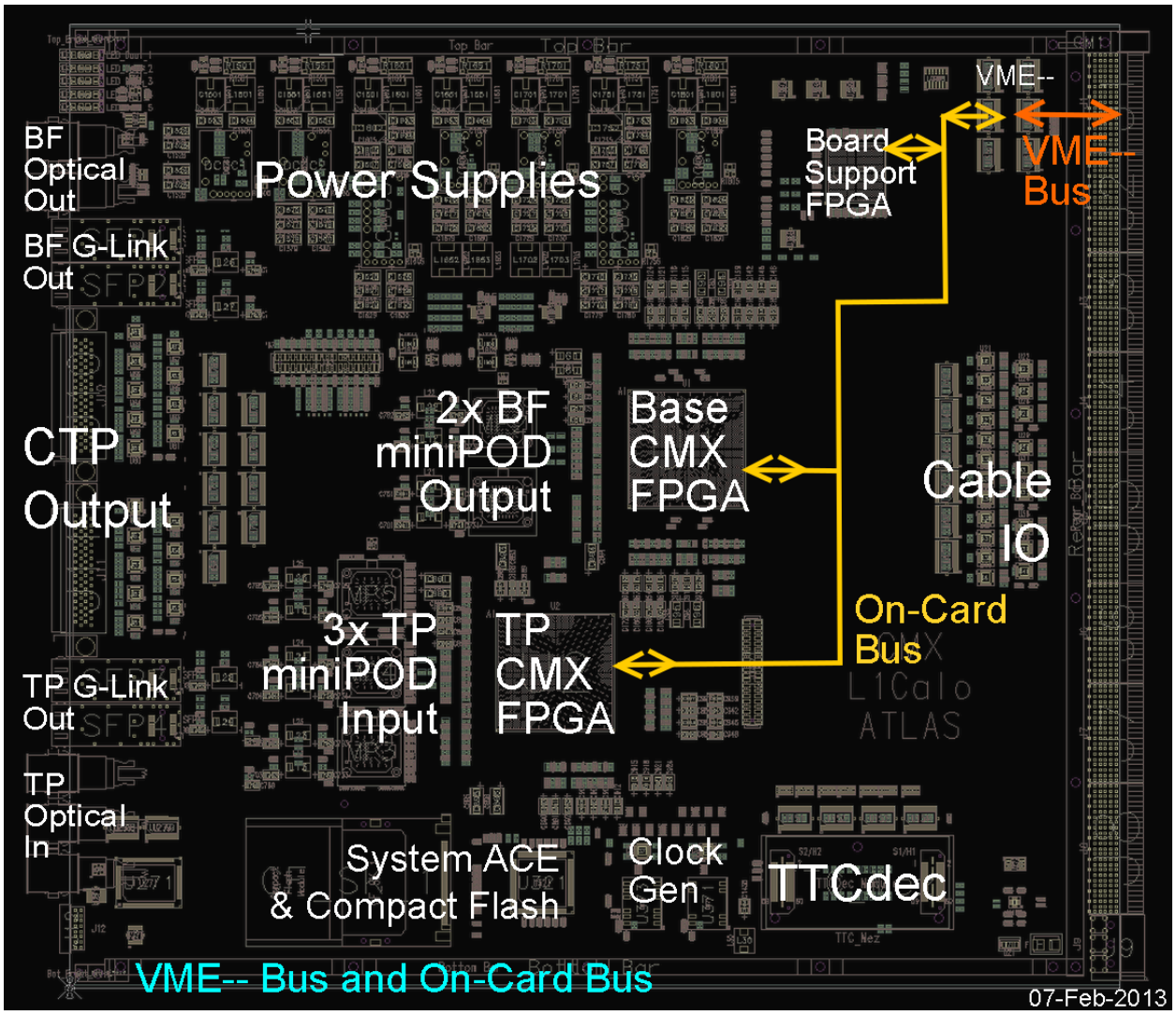

Figure 14 CMX On-Card Bus

The interface from the On-Card Bus to the VME-- Bus is done in two steps with Level Translators and Buffers. The Level Translators are used to connect the 2.5V On-Card bus to the 3.3V signals required by the VME drivers and receivers.

All three FPGAs are targets on the On-Card Bus (as illustrated in Figure 14) making them able to implement VME-- addressable registers.

Geographic Addresses #0, 4, 5 and 6 are provided through the backplane while Geographic Addresses #1, 2, and 3 are controlled by 3 jumpers on the card. All Geographic Address signals are available to all three FPGAs and to the TTCDec module.

The circuit diagram for the On-Card Bus and further details regarding this section of the CMX are found in Appendix I: VME-- and On-Card Bus.

4.4 JTAG and FPGA Configuration

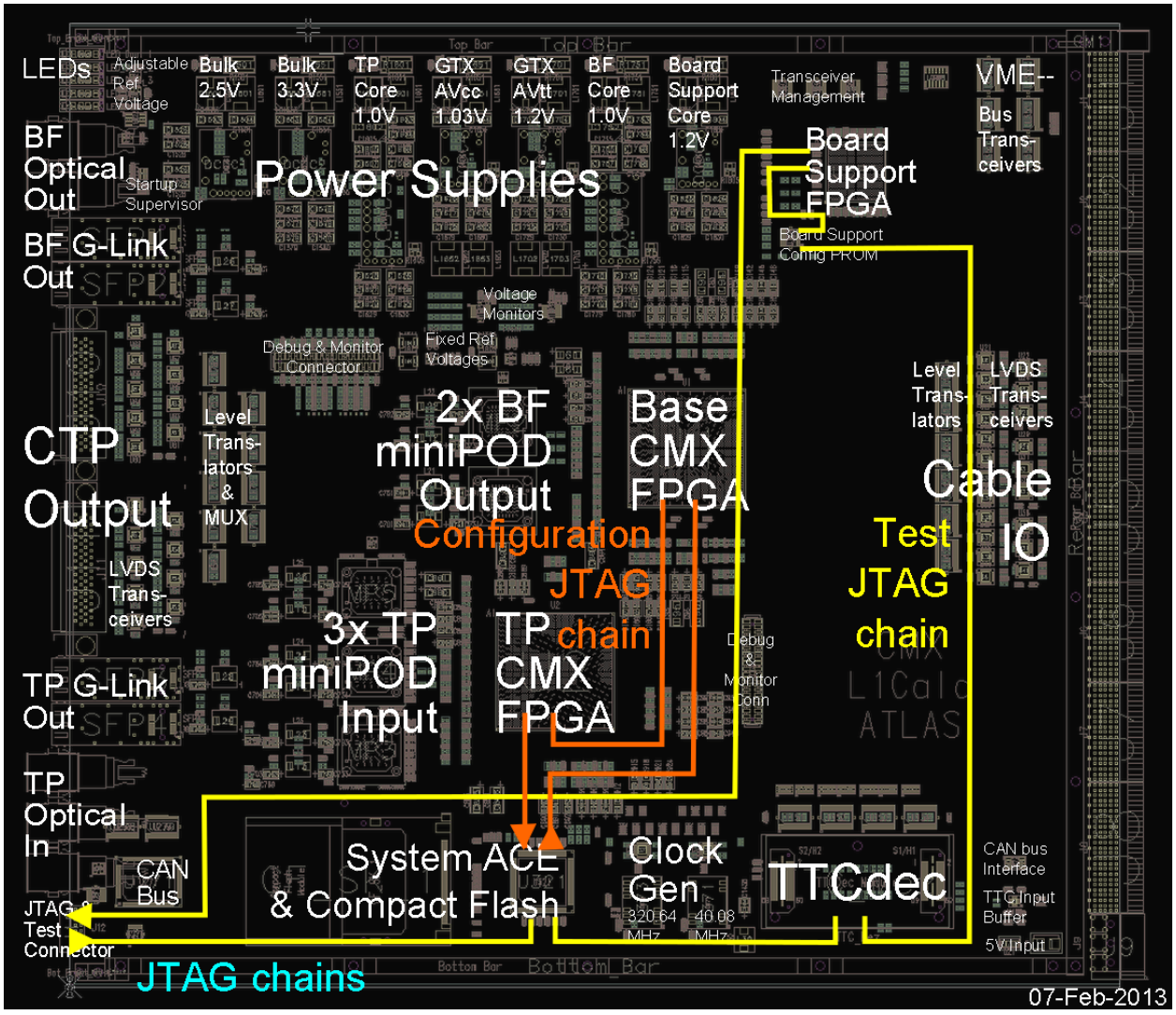

Figure 15 CMX JTAG chains

The CMX includes two JTAG chains: a test chain and a configuration chain.

The Test JTAG chain is accessible through the front-panel test connector. The Test JTAG chain connects the System ACE test port, the TTCDec, the Serial PROM for configuring the BSPT FPGA, and the BSPT FPGA itself. Jumpers are available to individually skip each of these devices along the chain.

The configuration JTAG chain connects the configuration JTAG port of the System ACE to the BF and TP FPGAs. Jumpers are available to skip each of these devices along the chain; including the case where the TP FPGA is not installed.

Updating the BSPT firmware requires using the Test JTAG chain to load the new firmware into the Board Support FPGA serial configuration PROM device.

Normal card configuration after power up starts with the Power Supply Monitor detecting nominal power on the card and allowing the BSPT FPGA to configure itself using its attached serial configuration PROM. The BSPT FPGA then directs the System ACE which configures the BF FPGA and (if present) the TP FPGA.

The BSPT FPGA firmware will be developed during the test and commissioning period and is expected to remain stable during normal operation. All flavors of CMX usage (Crate, System, L1topo) will use the same BSPT FPGA firmware. No configuration problem is anticipated by using a serial PROM configuration method as was used extensively by MSU in the past for the FPGA interface firmware used in all similar previous projects.

The Board Support FPGA presents registers visible from the VME-- bus to control and monitor the System ACE.

Note that the Compact Flash card will not be swappable through the front-panel (unlike the CMM). It is our understanding that the flexibility of the Compact Flash method is helpful in managing spares and being able to quickly configure a card to be used as a Crate CMX or System CMX without having to maintain separate types of spare. This feature is preserved, but it will not be possible to change the compact flash card in the field without partially pulling out the CMX card. The content of the Compact Flash card is accessible from the BSPT FPGA via the System ACE. The BSPT firmware and the control software will need to support updating the BF and TP FPGA firmware on the CF card via the VME-- bus.

The circuit diagram for the JTAG Test and Configuration chains and further details regarding this section of the CMX are found in Appendix J: JTAG chains and FPGA Configuration.

The details regarding all jumpers available on the CMX including the jumpers available to control the JTAG chains are found in Appendix L: CMX Jumpers.

4.5 CAN Bus

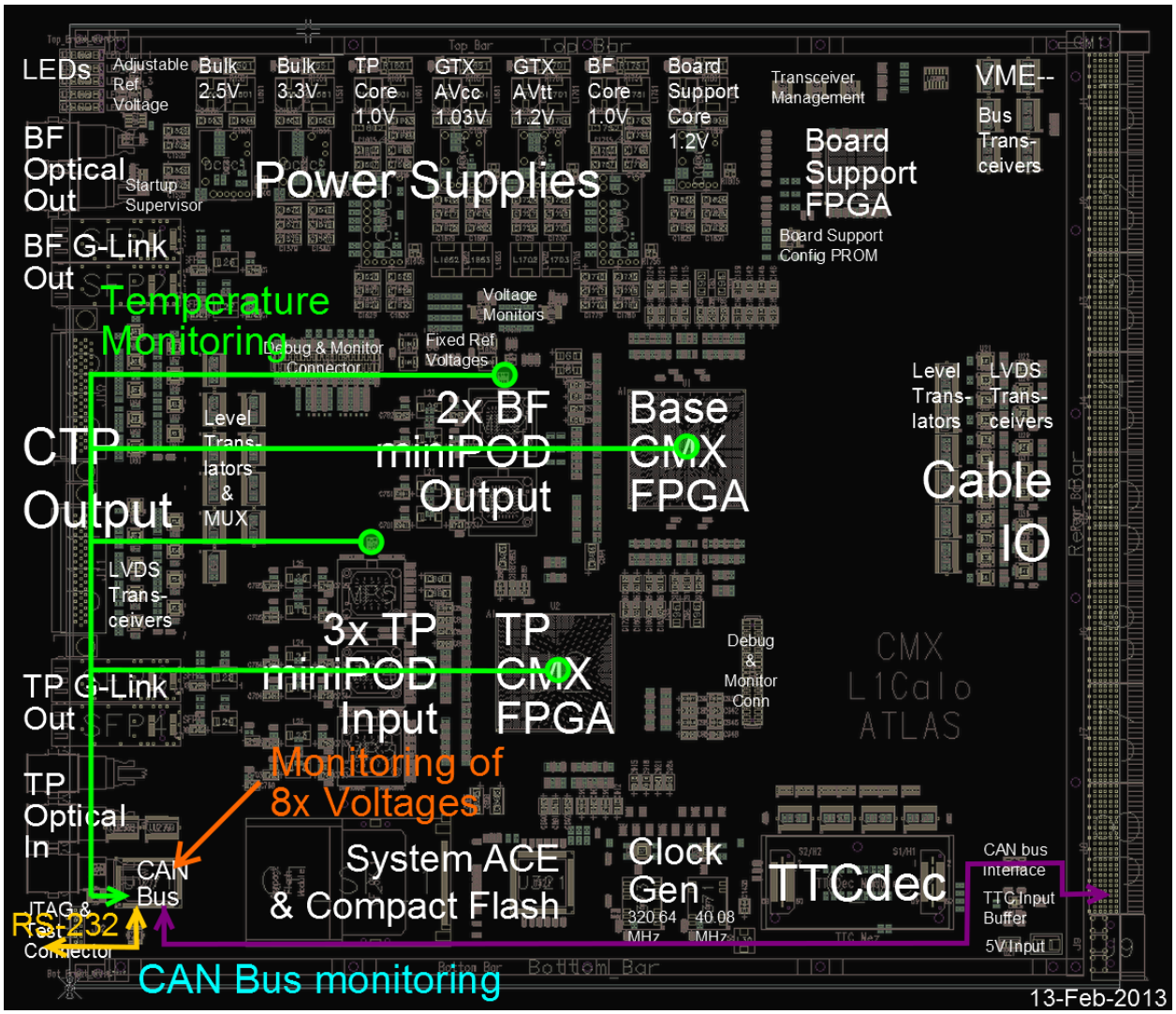

Figure 16 CMX CAN Bus monitoring

The CMX implements monitoring via CAN bus of:

1. The core temperatures of the BF and TP FPGA as well as the temperatures near the MiniPOD transmitters and receivers.
2. All eight power voltages used on the card (5V input and seven DC-DC converters)

The CAN bus is normally accessed via the dedicated backplane pins but also accessible through the front-panel test connector (via an adapter to a standard RS-232 serial connector).

The circuit diagram for the CAN Bus circuitry and further details regarding this section of the CMX are found in Appendix K: CAN Bus.

4.6 Transceiver Control Oversight

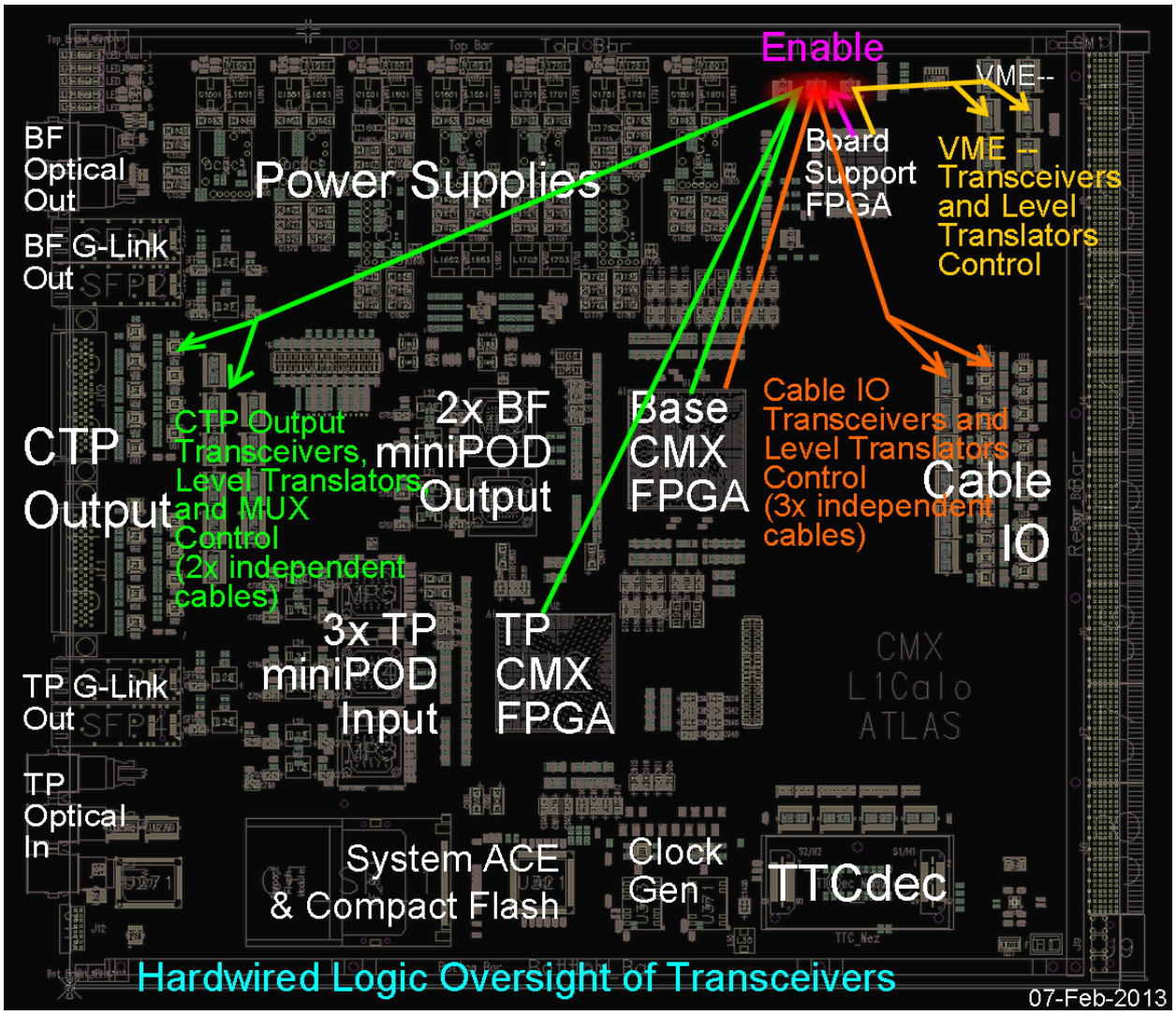

Figure 17 Transceiver management and oversight

Three sets of transceivers on the CMX need to be safely managed:

1. The VME-- bus buffers and level translators
2. The Cable IO LVDS transceivers and level translators
3. The CTP Output LVDS transceivers and level translators

Some specific measures are taken to avoid interfering with the VME-- bus and to prevent the situation where a large number of high-current drivers (e.g. 8 mA from the 2.5V side of the 74AVCAH164245) could be hammering the Select IO pins while the FPGAs are not properly configured and thus not yet able to control the transceivers.

The VME-- bus transceivers will not be enabled until the Board Support FPGA is configured and able to manage the operation of these transceivers. This is to prevent making the VME bus unavailable to other cards in the crate (.e.g. by driving the data bus lines with random states) if there is a configuration problem on a CMX card. DTACK_B generation is also suppressed until the BSPT FPGA is configured.

Control of the direction pins and output enable pins of the several separate transceiver ICs forming a given common set (e.g. the 7 LVDS transceivers plus the 2 level translators for one Backplane Cable) also needs to be concentrated and controllable by one Select IO pin from the FPGA that needs to be in control of this set (the BF FPGA in the above example).

The BSPT FPGA provides a confirmation (called “enable” in Figure 17) that it has detected that the BF FPGA (and TP, if present) have been successfully configured and are operating before this oversight circuitry will release control of the transceivers to the main FPGAs.

Some simple hardwired logic is thus included to provide such assistance and oversight of transceiver management.

4.7 Jumpers

Jumpers are available on CMX to:

1. Set Geographic Address bits 1, 2 and 3
2. Allow the Board Support FPGA to configure from its serial PROM
3. Control the mode for the LVDS receiver thresholds (to handle missing inputs)
4. Force the transceiver oversight circuitry to failsafe mode during initial tests
5. Set the TTCDec Chip ID and Master Mode bits
6. Select the TTCDec Clock used on CMX
7. Set the BF, TP and BSPT FPGA configuration mode pins
8. Skip individual devices on the Test and Configuration JTAG chains
9. Control if the BF and /or TP FPGA are configured by System ACE
10. Disable the DC/DC converter for Core Power to the TP FPGA (when not installed)

A description of all jumpers available on the CMX is found in Appendix L: CMX Jumpers.

5 Power

The CMX only uses the 5.0V input power available from the backplane; the 3.3V backplane pin is not connected. A 20A fuse sets the maximum 5V power consumption on the card.

Only a few parts on the CMX are using the 5V input voltage directly, namely the CAN bus circuitry, the startup supervisor, the voltage monitors and one of the VME-- bus interface components.

The CMX needs to generate 6 additional power voltages on the card:

1. Bulk 2.5V
2. Bulk 3.3V
3. 1.0V Core power to the BF FPGA
4. 1.0V Core power to the TP FPGA
5. 1.2V Core Power to the BSPT FPGA
6. 1.03V AVcc Power to the GTX IO Banks
7. 1.2V AVtt Power to the GTX IO Banks

The CMX also needs to generate 3 reference voltages on the card:

1. 1.25V fixed reference for the System Monitor of the BF FPGA
2. 1.25V fixed reference for the System Monitor of the TP FPGA
3. 1.25V +/- 0.5V adjustable reference for the Select IO VREF pins of the BF FPGA IO Banks used for the Backplane Processor Input signals

The 1.0V Power Supplies for Core Power to the BF and TP FPGAs are 30A supplies.

The 3.3V and 2.5V bulk power are further filtered before usage with the MiniPOD devices. The 3.3V bulk power is also further filtered before usage with the SFP device for G-link output.

A short delay after the 5V power is applied to the card all on-board power supplies ramp up together until they reach their design voltage with a ramping rate suitable to the Xilinx FPGAs.

Heat sink options are being studied for the Virtex-6 FPGAs and the MiniPODs.

The circuit diagram for the power supplies and further details regarding this section of the CMX are found in Appendix M: CMX Power Supplies and Voltage References.

The Virtex-6 FPGA bypass capacitor design details for the CMX are found in Appendix N: Virtex-6 Bypass Capacitors.

The geographical usage of each power supply and voltage reference on the board is illustrated in Appendix O: Geographical View of Power Usage.

6 Card Layout

The CMX is a 22 layer cards.

Ten signal layers are used: eight internal layers plus the top and bottom layers. All signal layers are located between two ground planes.

All signal layers support 50 Ohm traces but only five of the internal signal layers support traces with 65 Ohm characteristic impedance. All of the 400 backplane inputs are routed on the internal 65 Ohm layers either fully or up to ~1cm of their Base FPGA IO pin.

More details concerning the circuit board layers can be found in Appendix P: CMX card layers.

7 Build Count by CMX Card Type

The table below shows the number of prototype and production CMX cards of each type that will be built.

CMX Card Count	Prototype	Production	Total
With TP FPGA	2	4	6
Without TP FPGA (Base-Only)	1	14	15
With no Virtex-6 FPGA	1	0	1
Total	4	18	22

Appendices

Appendix A: Glossary

CMX-0 Glossary

Original Rev. 13-Dec-2012
Current Rev. 14-Feb-2013

A number of acronyms and abbreviations have been used in the design of the CMX card. This file contains the definitions of these terms.

The net_names used in the design of the CMX have been written in all capital letters to prevent the chance of confusion by down stream tools.

ACE System ACE (Advanced Configuration Environment) is a Xilinx product designed to configure Xilinx FPGAs from the content of a Compact Flash memory card.

BF Base Function FPGA the FPGA that implements the CMM functions and in addition can send data to the Topological Processor

BSPT the Board Support FPGA

CAN CAN bus (Controller Area Network) is a bus standard which originated in the automobile industry and designed to allow microcontrollers and devices to communicate with each other. It is used for monitoring voltage and temperatures on CMX

CMM Common Merger Module

CMX Common Merger Extended

CPM Cluster Processor Module. One of two types of modules sending real-time trigger information to the CMX through the backplane.

CTP Central Trigger Processor

DAQ Data Acquisition. Used to identify one of the two types of G-link output ports on CMX by the information they send to a ROD

DTACK_B Data Transmission Acknowledge (the "_B" postfix denotes that a logic low is used to assert the signal). One of the VME bus lines used by slave devices to convey their current status to the master during a bus cycle.

FPGA Field Programmable Gate Array. An integrated circuit designed to be configured with specific firmware at run-time.

G-link A 1Gbps protocol used by CMX to send out information to one or more RODs after every L1Accept.

GTX (not an acronym) The MGT resource type available on the Virtex-6 FPGA used on CMX (XC6VLX550T), and capable of serial IO up to 6.6 Gbps.

JEM Jet/Energy processor Module. One of two types of modules sending real-time trigger information to the CMX through the backplane.

JTAG Joint Test Action Group. A Standard for the Test Access Port and Boundary-Scan Architecture.

L1calo Atlas Level 1 Calorimeter Trigger

L1topo Level 1 Trigger Topological Processor. This term generally refers to a standalone system being built for the Phase 0 upgrade of L1calo. The CMX platform is also designed to be able to operate as a limited L1topo system using inputs from all CMX cards.

LVDS Low-Voltage Differential Signaling. A signaling standard used for the CMX to CMX Cable IO and for the output to CTP.

MGT Multi-Gigabit Transceiver. A special type of IO pin on Virtex-6 for multi-gigabit serial IO (as opposed to Select IO pins). All MGT resources on the Virtex-6 FPGA used on CMX are GTX transceivers.

MiniPOD The name of a family of optical transmitters and receivers manufactured by Avago (formerly Agilent, formerly HP).

MMCM Mixed-Mode Clock Manager. A clock management resource on Virtex-6.

MP MiniPOD the Avago optical transmitters and receivers used for the 6.4 Gb/s "high speed" optical links from the Base Function FPGA and to TP Function FPGA

MPO/MTP Multiple-Fiber Push-On. A multi-fiber connector standard.

ROD Read-Out Driver module. CMX sends information a every L1 Accept to a DAQ ROD and some CMX cards also send information to an ROI ROD.

ROI Region of Interest. Used to identify one of the two types of G-link output ports on CMX by the information they send to a ROD

RS-232 A serial commnunication standard commonly used for computer ports.

RTM Rear Transition Module. A Card plugging in the back of CMX with connectors to plug up to 3 LVDS cables for Crate CMX to System CMX communication

Select IO
The standard type of IO pins on Virtex-6
(as opposed to MGT IO pins)

SFP Small Formfactor Pluggable the optical transmitters that send out the 1 Gb/s "low speed" optical data from the BF and TP functions on the CMX to the ROI and DAQ systems

TP Topological Processor FPGA on the CMX card or a separate Topological Processor circuit board

TTCDec TTC Decoder mezzanine card which recovers the 40.08 MHz accelerator clock, L1 Accept, and Bunch identification information

VAT The VAT card (VME/ACE/TTC) is a parallel prototype project to practice System ACE control and test Board Support FPGA firmware

VME Versa Module Eurocard. A computer bus standard popular in HEP.

VME-- A subset of the VME signals used for communication within L1calo crates.

Appendix B: Mechanical Model and component placement

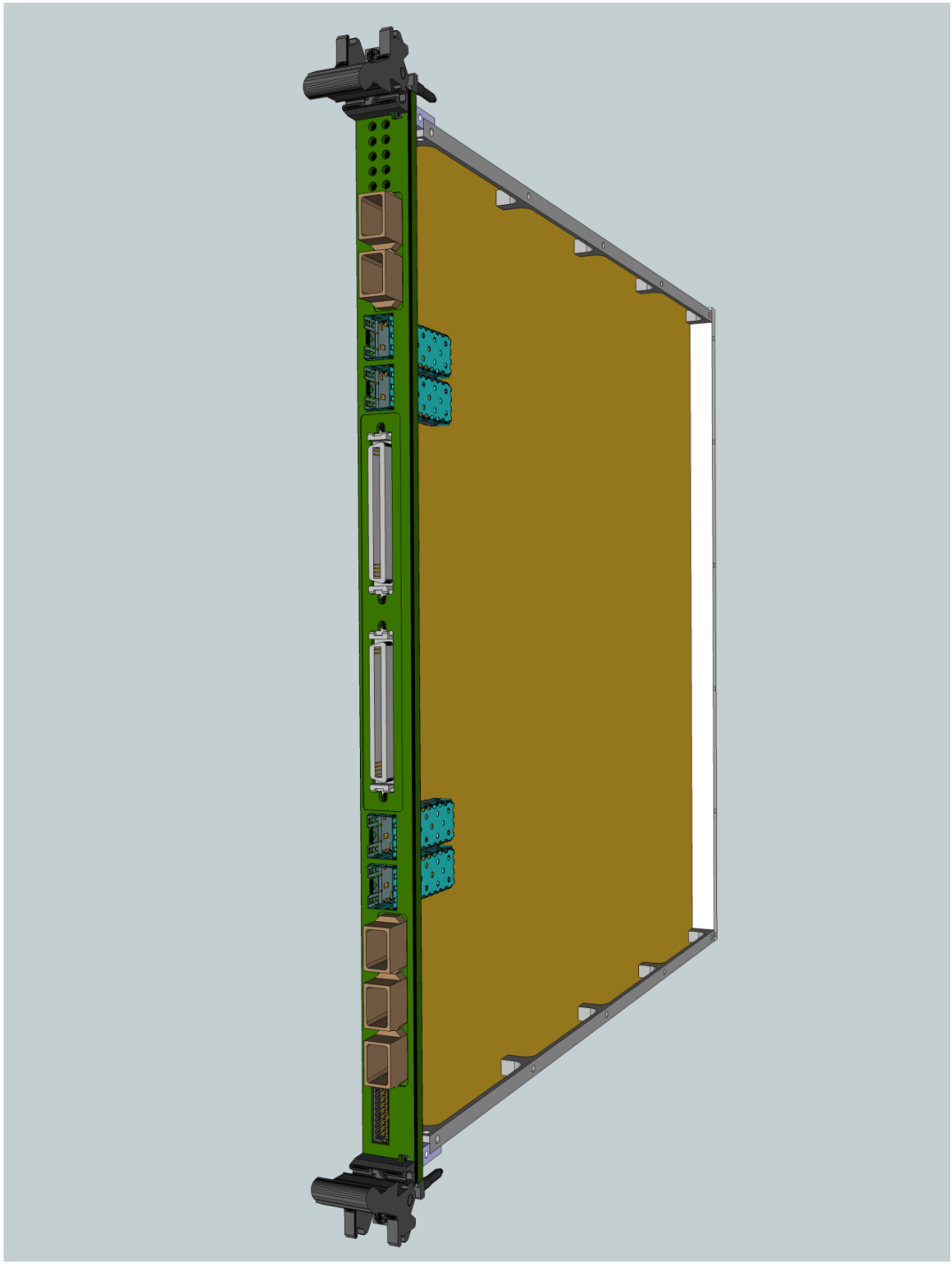

Figure 18 Mechanical Model of CMX with Front Panel and Stiffener Bars

A current snapshot is included above. For more views and future updates check http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/mechanical/

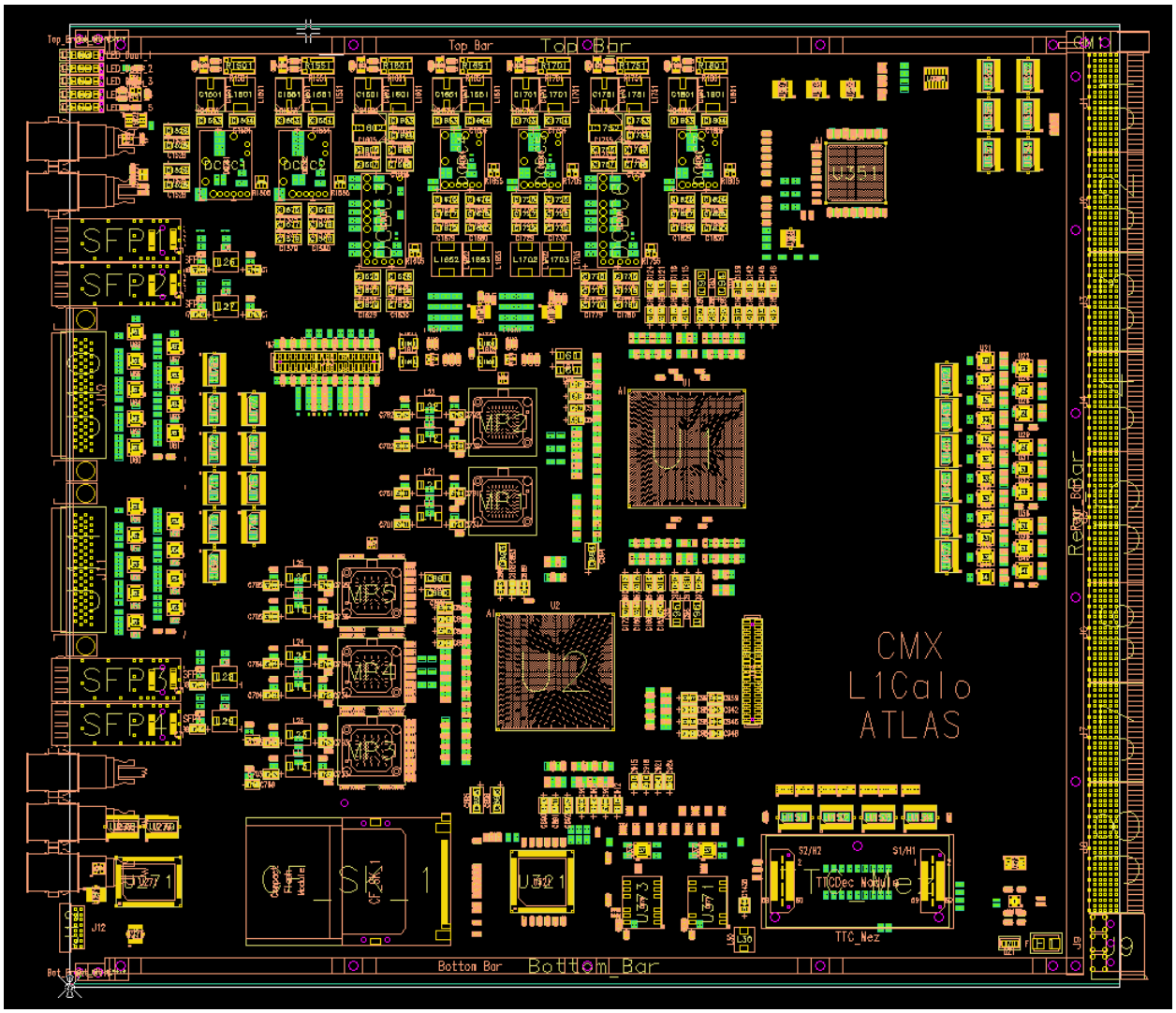

Figure 19 CMX component placement

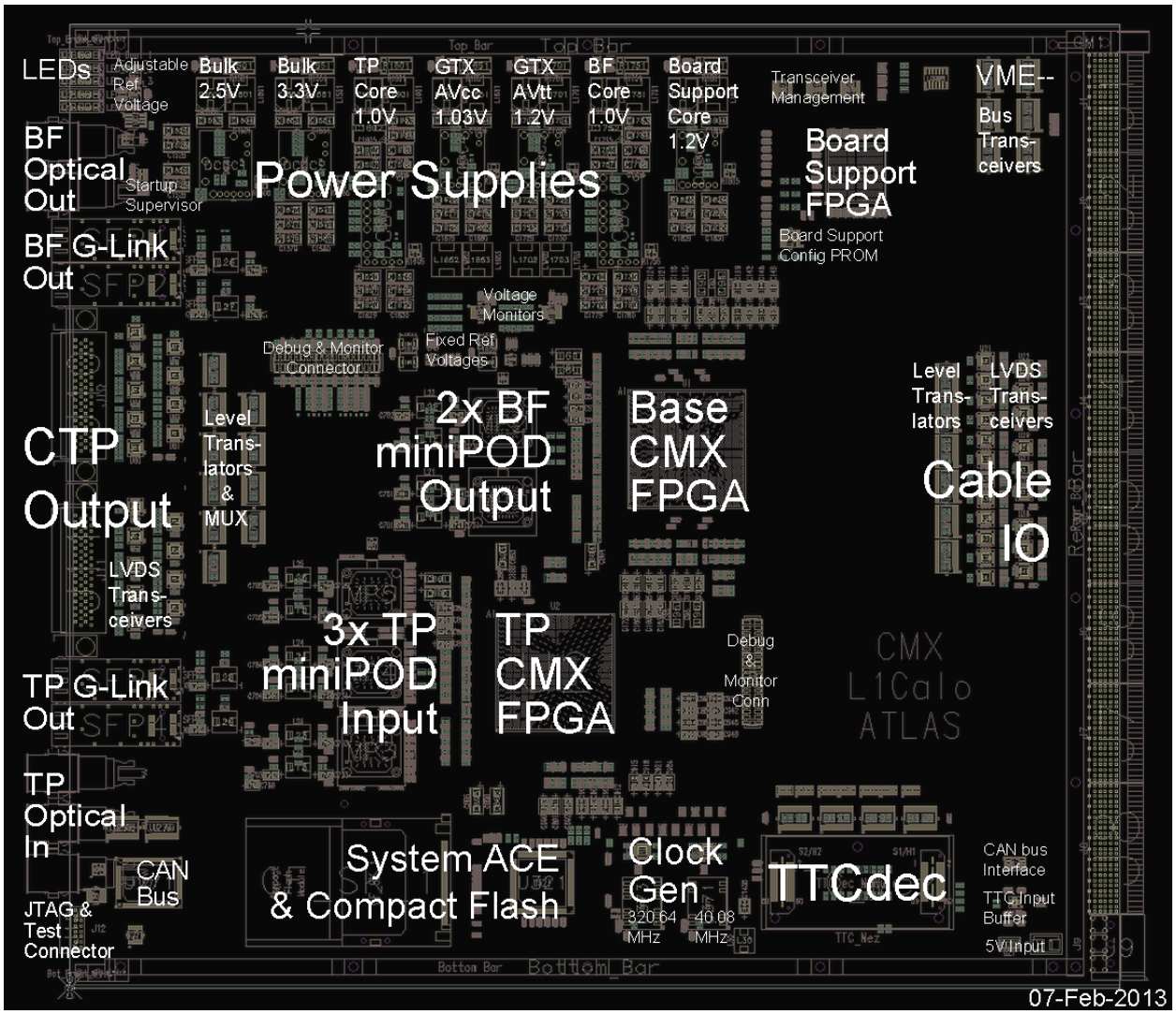

Figure 20 CMX component placement annotated

A current snapshot is included above. For more block diagrams and future updates check http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/block_diagrams/

Appendix C: IO Banks Assignments for BF and TP FPGA

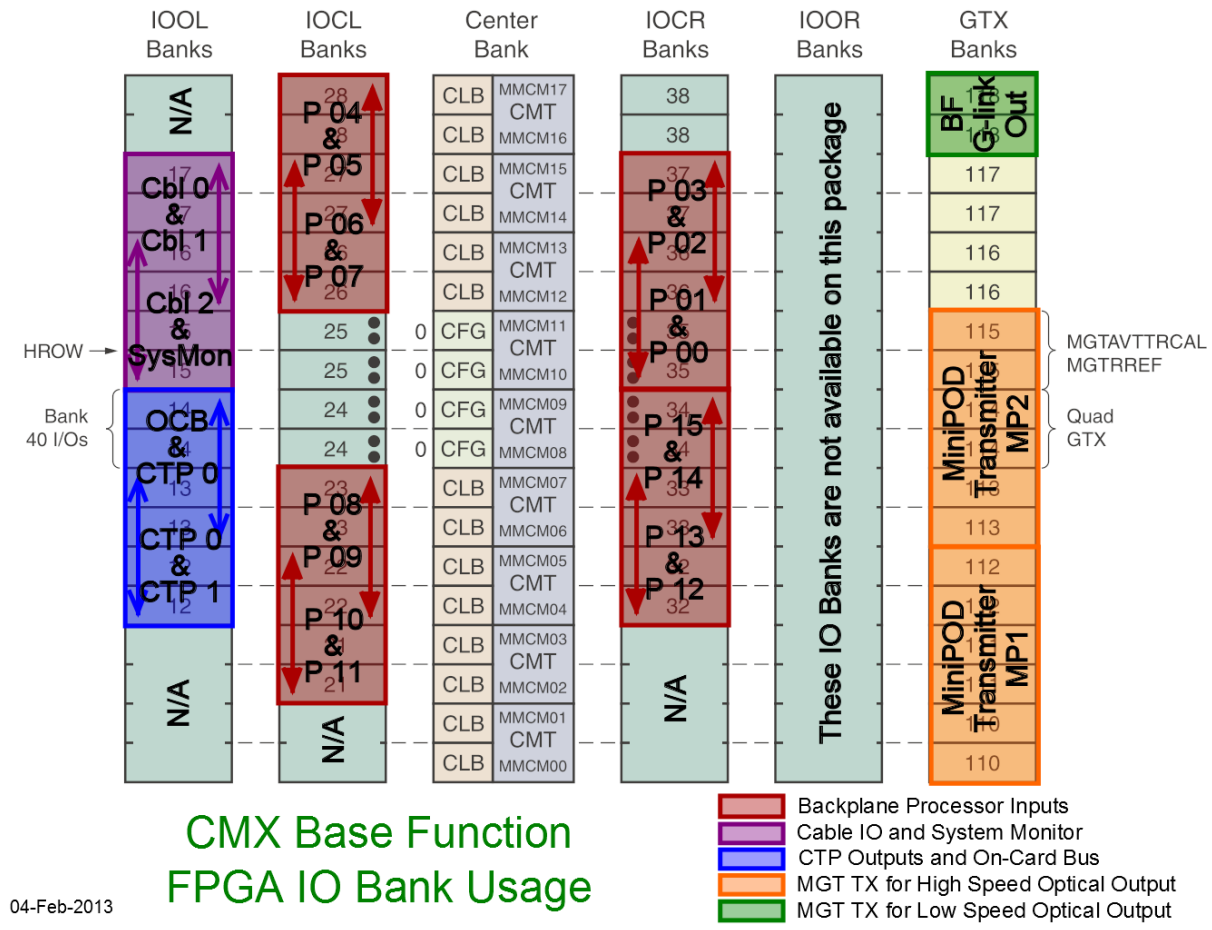

Figure 21 BF FPGA IO Banks Assignments

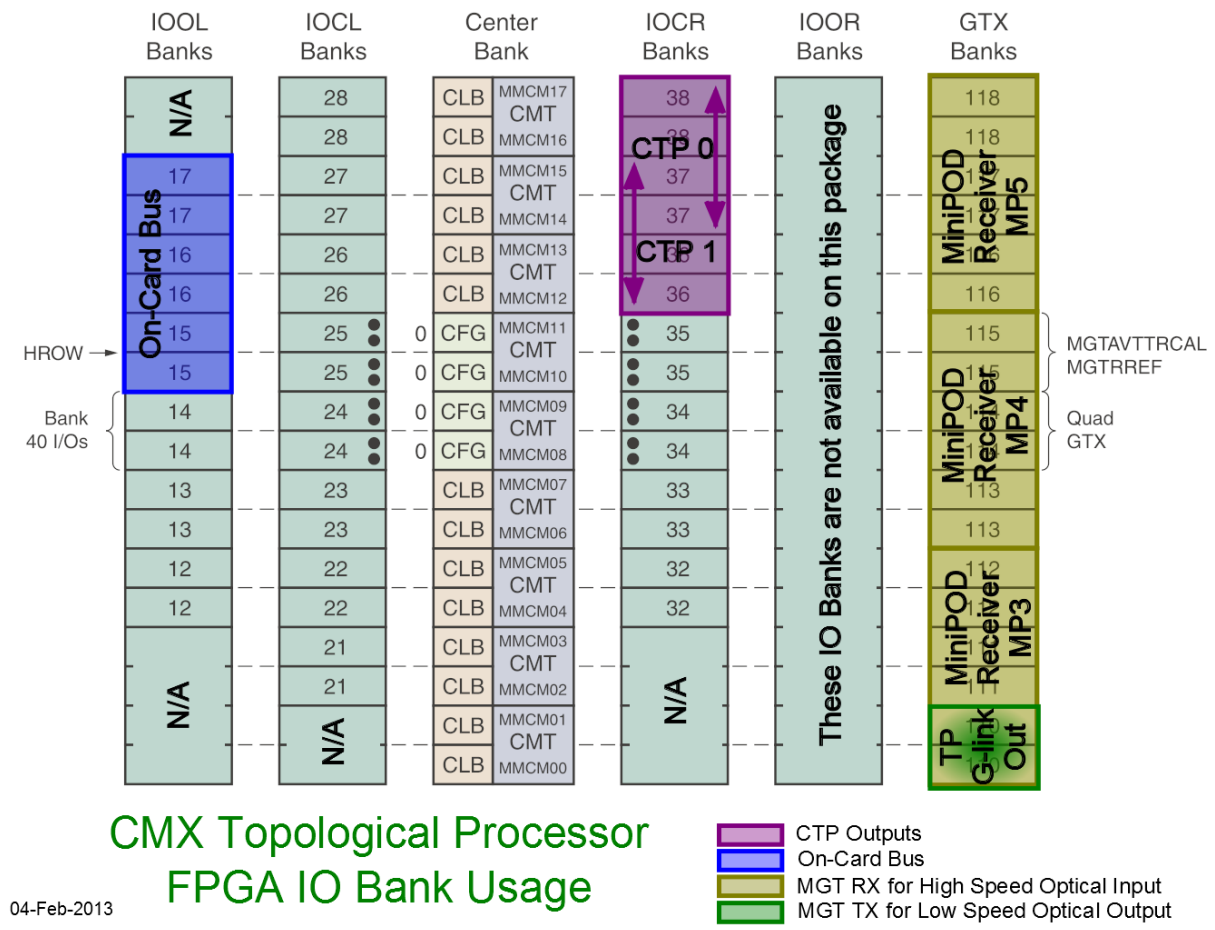

Figure 22 TP FPGA IO Banks Assignment

A current snapshot is included above while future updates to these diagrams will be in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/block_diagrams/

Appendix D: LVDS Connections

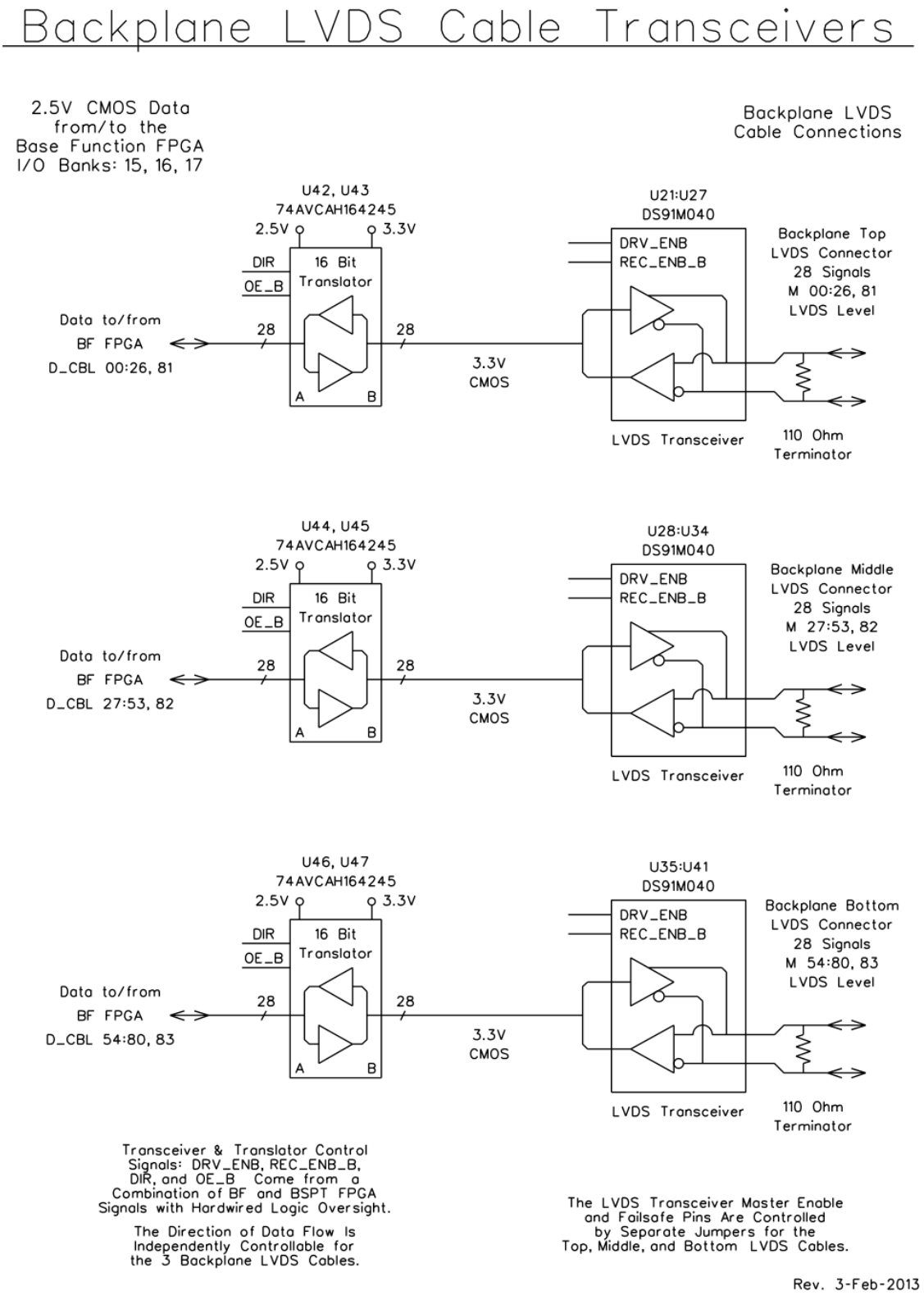

Figure 23 Circuit Diagram for the LVDS Cable IO

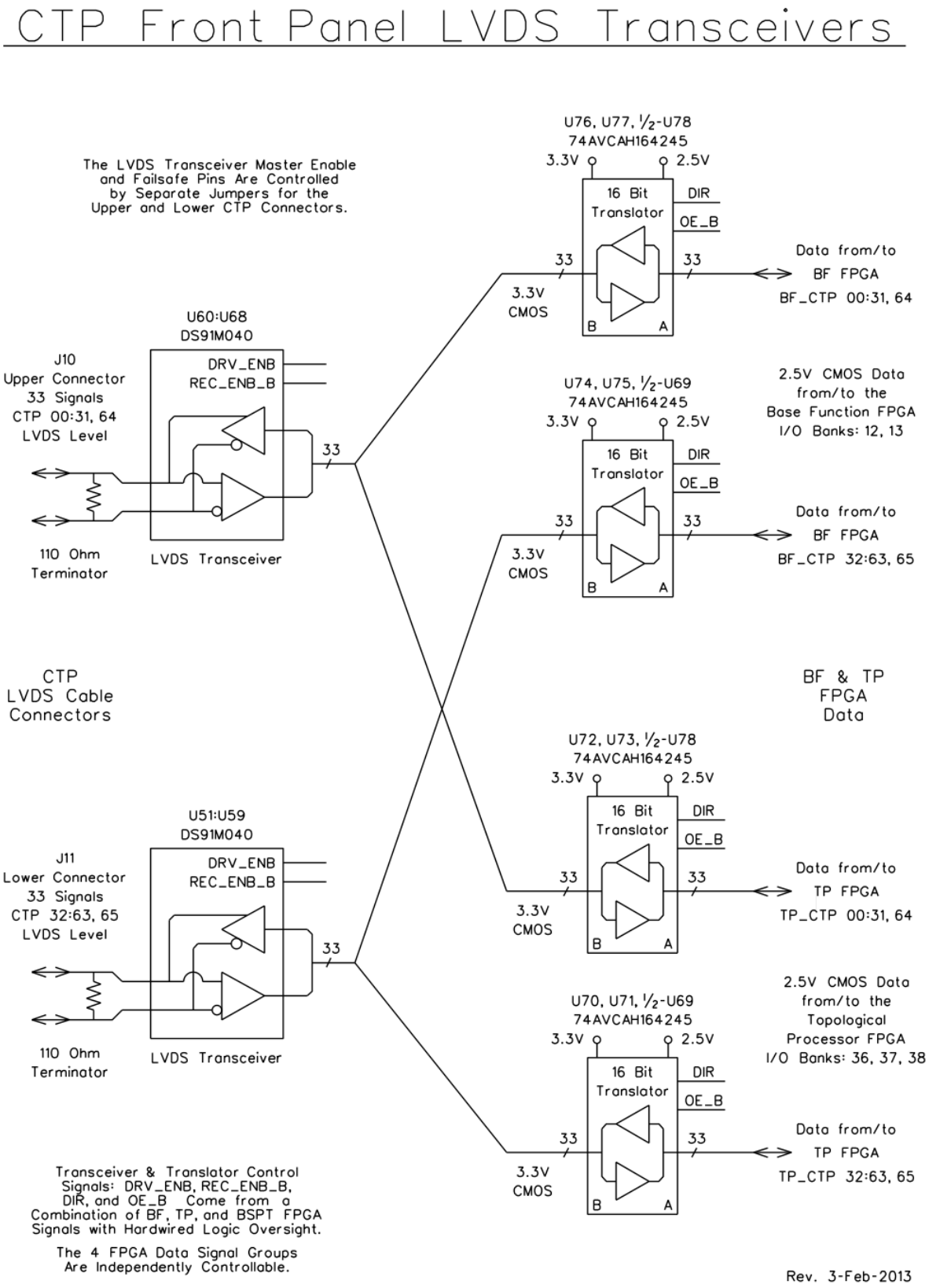

Figure 24 Circuit Diagram for the LVDS CTP Output

A current snapshot is included above while future updates to these circuit diagrams will be in 10_lvds_backplane_cables.pdf and 09_lvds_ctp_output.pdf found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot is included below while future updates to this description will be in cmx_ab_lvds_connections.txt found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
                  CMX  LVDS Connections
                 -------------------------


                                          Original Rev.  13-Dec-2012
                                           Current Rev.  12-Feb-2013


This file describes the LVDS connections to and from the
CMX card.

 - The backplane to the CMX card contains 3 "LVDS Cable
   Connections" of 27 bits each.  All of these signals
   are routed to the Base Function FPGA.

 - The front panel of the CMX card contains 2 "CTP LVDS
   Cable Connections"  of 33 bits each.  All of these
   signals are routed to both the Base Function FPGA and
   to the Topological Processor FPGA.

Note that in some cases the connector pinout signal numbering
scheme that is used in these LVDS connections is not
continuous and skips around a bit.

The CMX card handles both the backplane and the front panel
LVDS connections in the same way.  Specifically:

 - Each LVDS signal is received or transmitted by one channel
   of a quad National  DS91M040  LVDS Transceiver.  This is a
   high speed "M" type LVDS transceiver that provides double
   the normal drive current  (for cables that are terminated
   at both ends)  and has a receiver with wide common mode
   input range for use with cables.

 - The CMX circuit board provides a 100 Ohm differential
   termination resistor on each channel.  In this way the
   LVDS circuits can be used as either transmitters or
   as receivers with no changes to the card.

 - The DS91M040 LVDS transceivers have 3.3V CMOS single ended
   data and control signals.  These 3.3V signals can not be
   used directly with the Virtex-6 BF and TP FPGAs.
```

- Between the Virtex-6 FPGAs and the DS91M040 LVDS transceivers there are bi-directional 2.5V <-> 3.3V level translators. These parts are TI 74AVCAH164245. These translators include hold circuits to avoid the problem of floating CMOS inputs.

- These 74AVCAH164245 translators are also used to provide the multiplexing function that allows either the Base Function FPGA or the Topological Processor FPGA to be connected to the front panel LVDS signals.

  Note that this multiplexing of the front panel LVDS signals is done on a per connector basis. Thus for example the BF FPGA can be sending or receiving LVDS signals on the upper front panel LVDS connector while the TP FPGA is using the lower front panel LVDS connector.

- Management of the National DS91M040 LVDS transceivers.

  Management of the DRIVER_ENB and RECEIVER_ENB_B control signals to the LVDS transceivers comes from the BSPT FPGA and includes hardwired logic oversight to prevent enabling these devices before the BSPT FPGA is configured. In turn the BSPT listens to signals from the BF and TP FPGAs to learn how they want the LVDS transceivers configured. Thus once everything is running the BF and TP have control over these devices with logic in the BSPT enforcing rules to prevent conflicts, e.g. two drivers on the same line at once.

  It is not anticipated that we will frequently need to change the Failsafe and Master Enable control signals to the LVDS transceivers. These control signals are set by jumpers on logical groups of transceivers.

- Management of the TI 74AVCAH164245 level translators.

  Management of the DIRECTION and OUTPUT_ENABLE_B control signals to the level translators comes from the BSPT FPGA and includes hardwired logic oversight to prevent enabling the output of these translators before the BSPT FPGA is configured. In turn the BSPT listens to signals from the BF and TP FPGAs to learn how they want the level translators configured. Thus once everything is running the BF and TP FPGAs have control over these devices with logic in the BSPT enforcing rules to prevent conflicts, e.g. two drivers on the same line at once.

Appendix E: High-Speed Optical

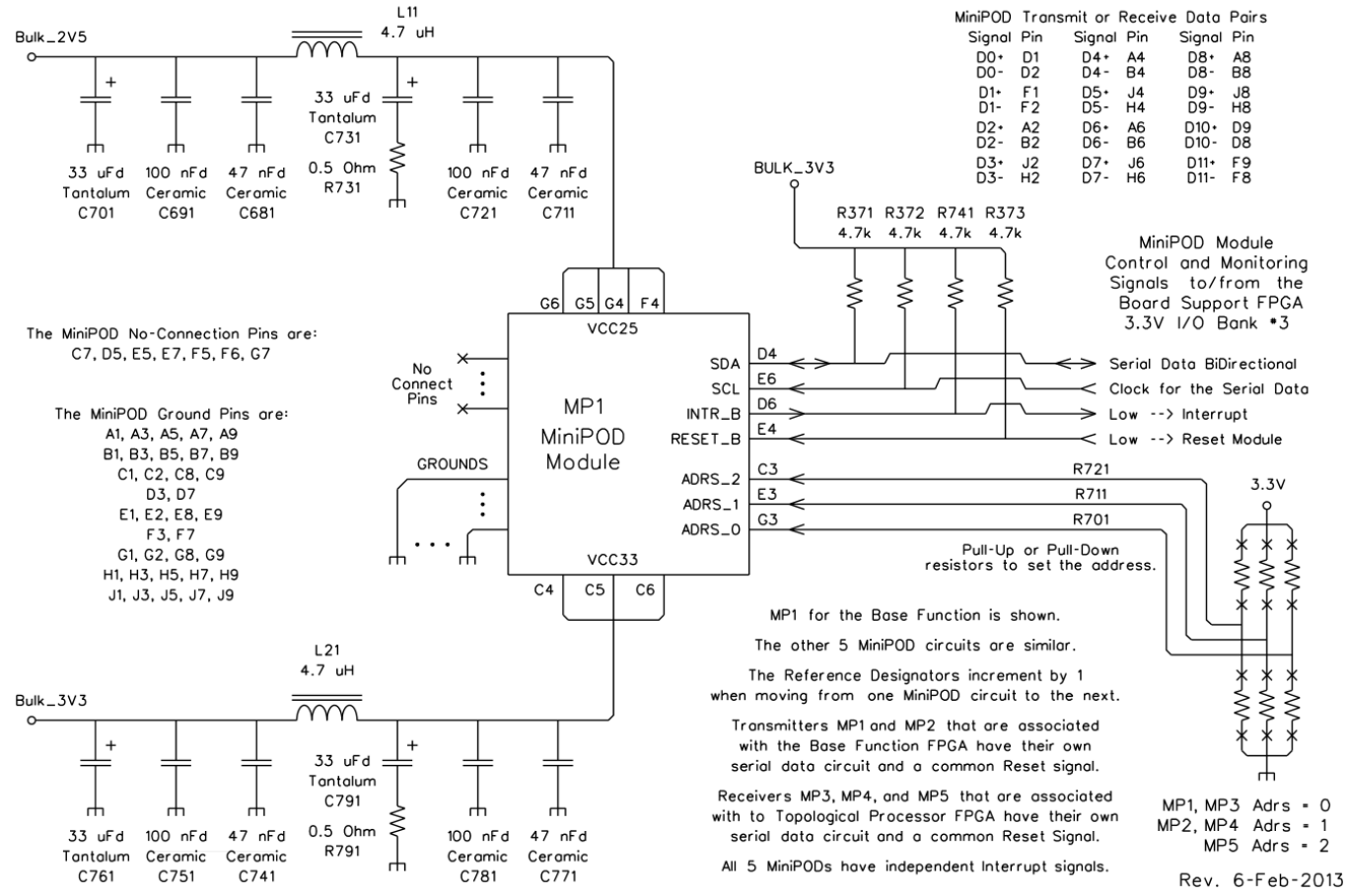

Figure 25: Circuit Diagram for the high-speed optical connections

A current snapshot is included above while future updates to this circuit diagram will be in 14_high_speed_optical.pdf found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot is included below while future updates to this description will be in cmx_ab_high_speed_optical.txt found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

CMX As Built High Speed Optical

Original Rev. 29-Nov-2012
Current Rev. 12-Feb-2013

This intent of this note is to record the engineering information about the high speed optical components on the CMX card.

- MiniPOD Optical Part Numbers:

  The high speed optical parts that are used on the CMX card are the following:

  Transmitter is a 12 channel Avago "MiniPOD" type Avago Part No. AFBR-811FH1Z which translates into: 10 Gbps per lane, Flat ribbon jumper cable, has an attached clip-on heatsink, 100m

  Receiver is a 12 channel Avago "MiniPOD" type Avago Part No. AFBR-821FH1Z which translates into: 10 Gbps per lane, Flat ribbon jumper cable, has an attached clip-on heat sink, 100m

  These are high speed short range parallel devices designed for multimode fiber systems at a nominal 850 nm wavelength.

- Module Pinout:

  The actual module pinout is common to the transmitter and receiver. There is a separate mechanical identification pin hole. There are 2 holes for screws M1.6 to hold the MiniPOD package down again the supporting circuit board.

- Power Filters:

  Power filters for both 2.5V and 3.3V power they want 100 nFd to Gnd, 4.7 uH series, 100 nFd to Gnd and 22 uFd to Gnd through a 0.5 Ohm resistor.

  Use the CMX standard 100 nFd and 47 nFd 0603 ceramic capacitor and B case 33 ufd Tantalum capacitor.

  Use a Wurth No. 7443340470 choke 12.4 mOhm, 7.5 Amp 45 Mhz

  The 0.47 Ohm 0603 resistor is: P.47AJCT-ND ERJ-3RQFR47V

- MEG-Array PCB Mount Socket:

  The CMX needs to have a connector from the FCI series 55714
  for the MiniPOD optical components to plug into.

  I *assume* that the CMX will be built with a leaded process.
  The FCI series 55714 socket specification clearly calls out
  that they do not want you to use their lead free solder ball
  parts on a leaded assembly process. This is Note #4.
  See also FCI Specification: GS-20-033.

  The full exact part number of the 9x9 81 pin FCI MEG-Array
  pcb mount socket that we will use for these MiniPOD optical
  components is:

```
     55714-002   15u" Au over Ni    Solder Ball is SnPb
     55714-102   30u" Au over Ni    Solder Ball is SnPb
     55714-202   Au is Nortel Spec  Solder Ball is SnPb
```

  None of these parts appear to be in stock at DK.

  Note that FCI calls for a 0.58 to 0.64mm pad diameter.
  Copper defined pads with a solder mask that gives 0.15mm
  minimum clearance all around the pad. Via not in pad.
  Tented via. Keep out area of 5.1mm from the perimeter
  of the part. 0.25mm trace from pad to via. 0.64mm via
  land. 0.30mm via drill plated.

  FCI does mark pin A1 on their connectors and on the
  second page of drawings in the drawing file for the 55714
  series of connectors.

  PBC layout escape rules/suggestions from HP ?? none.

- High-Speed Differential Signal Routing on the PCB:

  Between the output of the receivers and the Xilinx GTX
  serial inputs we need to have DC-Blocking capacitors.
  They specify 100 nFd capacitors but say that smaller
  values may work with 8b10b encoding. 100 nFd x 50
  Ohms = 5 usec.   A bit length is about 0.15 nsec.
  Why such a big capacitor ?   I will start by trying
  to place these 96 capacitors as 0402 size. We need
  10 nFd for the Xilinx GTX clocks.

  These differential traces will be routed without
  any cross overs. If this non cross over trace routing
  flips the sign then it can be flipped back on the
  MiniPOD devices by:

    Receiver "polarity flip" is controlled from the
    Receiver Memory Map 01h Upper Page Addresses 226 and 227

Transmitter "polarity flip" is controlled from the
Transmitter Memory Map 01h Upper Page Addresses 226 and 227

The GTX transceivers can also flip the sign of their differential signals. In the GTX user manual see page 167 for the transmitter flip and page 216 for the receiver sign flip.

Trace length matching: Have 6.4 Gb/s data rate but also need corners so we need the 3rd and hopefully the 5th harmonics, i.e. 19.2 or 32.0 GHz. This is a free space wavelength of 15.6mm or 9.4mm. But for a good transmission line we care about stuff at the scale of one tenth wave length (or smaller). One tenth wavelength is 1.56mm or 0.94mm. But the transmission velocity is only about 50% the speed of light so we care about the physical layout of the traces at the scale of 0.78mm or 0.47mm or smaller.

- Physical Mounting:

The Flat Ribbon optical cables version of the MiniPOD module has a height of at least 14.50mm above the supporting pcb. The Round cable version is even taller.

With a 14.50mm height it means that there will only be 1.75mm clearance between the top of the MiniPOD module and the inter-board separation plane.

I believe that each device requires two M1.6 screws that I think run into blind holes so that the length needs to be about correct. Button head with washers would be nice.

- Optical Connection to the MiniPOD:

"The optical interface requires the user to provide a custom designed optical turn 1x12 cable Prizm connector".

"Please contact your Avago sales representative to receive the Prizm cable assembly specification".

We will start testing by using Molex 106267-2001 and Molex 106267-2011 cables.

- TWS Interface:

This is based on Atmel Two Wire Serial EEPROM e.g. AT24C01A but note the difference in the write timing. The MiniPOD module is a "slave" on this bus.

This appears to be basically 3.3V LVTTL logic levels.
But I think it is really:

- 1.2V CMOS logic levels on SDA, SCL, and Reset_B
  that are 3.3V LVTTL tolerant

- 3.3V open drain on Interrupt_B

- 3.3V logic levels on ARDS_2:0

What does Avago mean by "output pull-up and pull-down currents" which are small, e.g. 20 uA min 125 uA max.

Note the strange typical Vcc for 2.5V and 3.3V in the table of specifications for the monitor control interface on page 31. VCC 3.3V = 3.435 Volts. VCC 2.5V = 2.625 Volts.

The 3 Address input pins are used to give an individual module a unique address. The actual 8 bit address of a given module is: 0 1 0 1 Adr2 Adr1 Adr0 R/W

Interrupt_B is an output from the module. This output is either Hi-Z or driven Low. It needs an external pull-up to 3.3V.

The Reset_B input is used to reset everything to default non-volatile settings.

TWS SDA is an open-drain I/O pin that requires an external pull-up e.g. 2.0k to 8.0k to 3.3V

TWS SCL is an input. Pull-up with a 2.0k to 8.0k to 3.3V

In addition they suggest connecting the external case with its threaded bosses to ground.

- TWS Management and Monitoring:

All Management and Monitoring of the High Speed optical components is handled through the Board Support FPGA.

There will be separate TWS serial string for the Base Function transmitters and for the Topological receivers.

There will be separate Reset_B signals from the Board Support FPGA to the Base Function transmitters and to the Topological receivers.

There will be a separate Interrupt_B line from each of the 5 MiniPOD optical components to the Board Support FPGA.

The 3 address lines to each of the 5 MiniPOD optical

components will be brought out to jumpers so that in an emergency things could be changes. There will be only one jumper per address bit, i.e. there is an expected default configuration that will be used - but could be changed in an emergency. That configuration will be:

MiniPOD Device	ADR_2	ADR_1	ADR_0	Function
MP1	low	low	low	Base Function Transmitter
MP2	low	low	hi	Base Function Transmitter
MP3	low	low	low	Topological Receiver
MP4	low	low	hi	Topological Receiver
MP5	low	hi	low	Topological Receiver

- Transmitter:

The Transmitter has 100 Ohm differential inputs, CML signal level, and does not require DC blocking capacitors. VCSEL, Vertical Cavity Surface Emitting Laser. Management and monitoring are through a Two Wire Serial interface TWS. Can measure light output power LOP and elapsed operating time. The signals or pins involved with the transmitter:

12x	high speed differential CML transmit data
	SCL and SDA for the Two Wire Serial interface
1x	Interrupt
3x	Address allow you to set the TWS address
1x	Reset_B
7x	DNC Reserved Do Not Connect
33x	Ground
3x	3.3V power
4x	2.5V power

The transmitter's maximum current draws are 400 mA from 2.5V and 160 mA from 3.3V. Loss of input signal is typically detected at 120 mVpp differential input. TWS clock rate is 400 kHz maximum.

- Receiver:

The Receiver has 100 Ohm differential CML level outputs that may require AC coupling capacitors. The receivers use PIN diodes. Management and monitoring are through a Two Wire Serial interface TWS. It can measure: optical input power, temperature, both supply voltages, elapsed operating time.

12x	high speed differential CML received data

```
          SCL and SDA for the Two Wire Serial interface
       1x  Interrupt
       3x  Address  allow you to set the TWS address
       1x  Reset_B
       7x  DNC  Reserved Do Not Connect
      33x  Ground
       3x  3.3V power
       4x  2.5V power
```

The receiver's maximum current draws are 525 mA from 2.5V and 90 mA from 3.3V. The differential output voltage from the receiver is controllable over the 100 mVpp to 800 mV range. Common Mode output voltage 2.00 V min 2.54 V max.

Note that the differential input to the GTX receiver has a common mode of 2/3 GTX AVTT where AVTT is typically 1.2 Volts --> We must use the AC coupling.

Note that the receiver's data outputs can appear as 2.5V through 50 Ohms anytime that the receiver is powered.

- Power:

No power up sequencing is required. Power down must be to <50mV for both 2.5V and 3.3V or the module may not start up correctly next time.

Appendix F: Low-Speed Optical

SFP Low-Speed Optical Transmitters

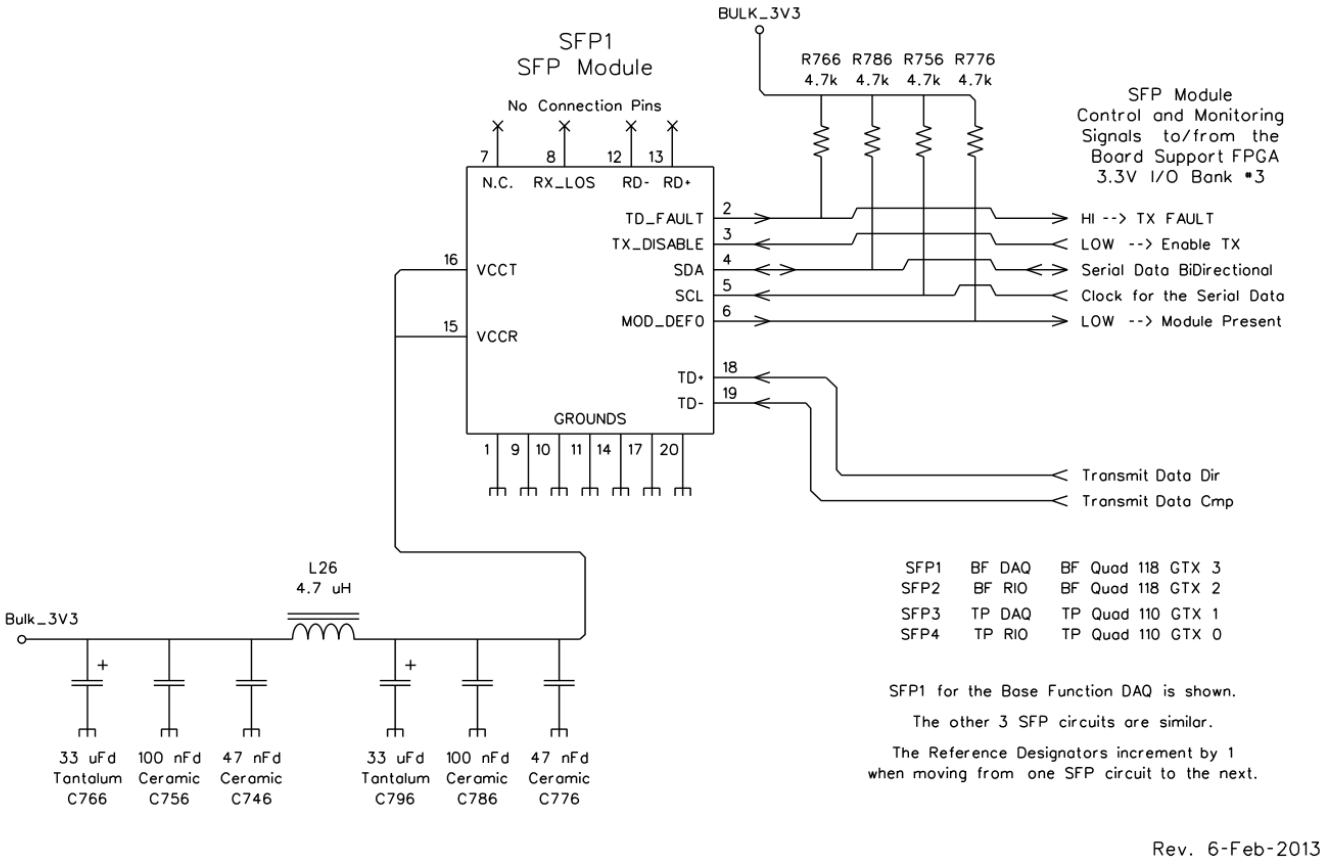

Figure 26 Circuit Diagram for the low-speed optical connections

A current snapshot is included above while future updates to this circuit diagram will be in 13_low_speed_optical.pdf found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot is included below while future updates to this description will be in cmx_ab_low_speed_optical.txt found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

CMX Low Speed Optical Components

Current Rev. 12-Feb-2013

This file describes the Low Speed Optical components that are used on the CMX card to send out DAQ and RIO information from the Base Function and Topological Processor FPGAs. On the CMX card these are components SFP1 through SFP4. These parts are located on the front panel of the CMX card right above and below the cable connectors for the CTP output.

- The actual part that is used on the CMX card is the Avago AFBR-57M5APZ optical transceiver. This Avago part is being used on the CMX card because the original Infineon part that was used on the CMM card is no longer available.

  The AFBR-57M5APZ is a Small Formfactor Pluggable transceiver. The SFP specification covers most of its operation. Only the transmitter section of this device is being used in the CMX application.

- The monitoring and control of the 4 low speed SFP optical parts is done through the Board Support FPGA. 5 control pins from each SFP package are routed to pins in the 3.3V I/O bank of the BSPT FPGA. These 5 control pins are: TX_FAULT, TX_DISABLE, MOD_DEF0, SDA, and SCL.

  The TX_FAULT signal allows the BSPT FPGA to know if there are problems with the laser transmitter. TX_DISABLE allows the BSPT to turn off the laser in the transmitter. The MOD_DEF0 signal tells the BSPT whether or not a component is plugged into the SFP socket. The SDA and SCL lines provide serial communication between the BSPT FPGA and the many registers in the AFBR-57M5APZ optical component.

- Power is supplied individually to each SFP socket through a filter circuit. The receiver section of the AFBR-57M5APZ transceiver is not being used but both the transmitter and receiver sections will be powered because it is not clear in the AFBR-57M5APZ data-sheet whether or not the monitoring and control functions in this device will operate normally if only its transmitter is powered. Because the receiver section is not being used read optical data only one power filter is provided per SFP socket. The AFBR-57M5APZ should draw about 210 mA at 3.3 Volts.

  Because the receiver section is not used the RX_LOSS, R+, and R- pins are not connected to anything on the

SFP sockets.

- The CMX card will not use HP G-Link chips to encode its RIO and DAQ output data. Rather the function of the HP G-Link chip will be implemented by a combination of Virtex FPGA logic and a GTX transmitter. The reference clock to these GTX transmitters is a 40.08 MHz LHC locked clock.

  The longest 100 Ohm differential traces from the BF or TP FPGAs to their SFP optical transmitters are about 185 mm long. This trace length should not be a problem at 1 GHz data rate with the pcb laminate that is used for the CMX pcb. This routing is made simpler because the AFBR-57M5APZ transceiver do not require AC coupling capacitors in their differential data lines.

Appendix G: TTCDec data distribution

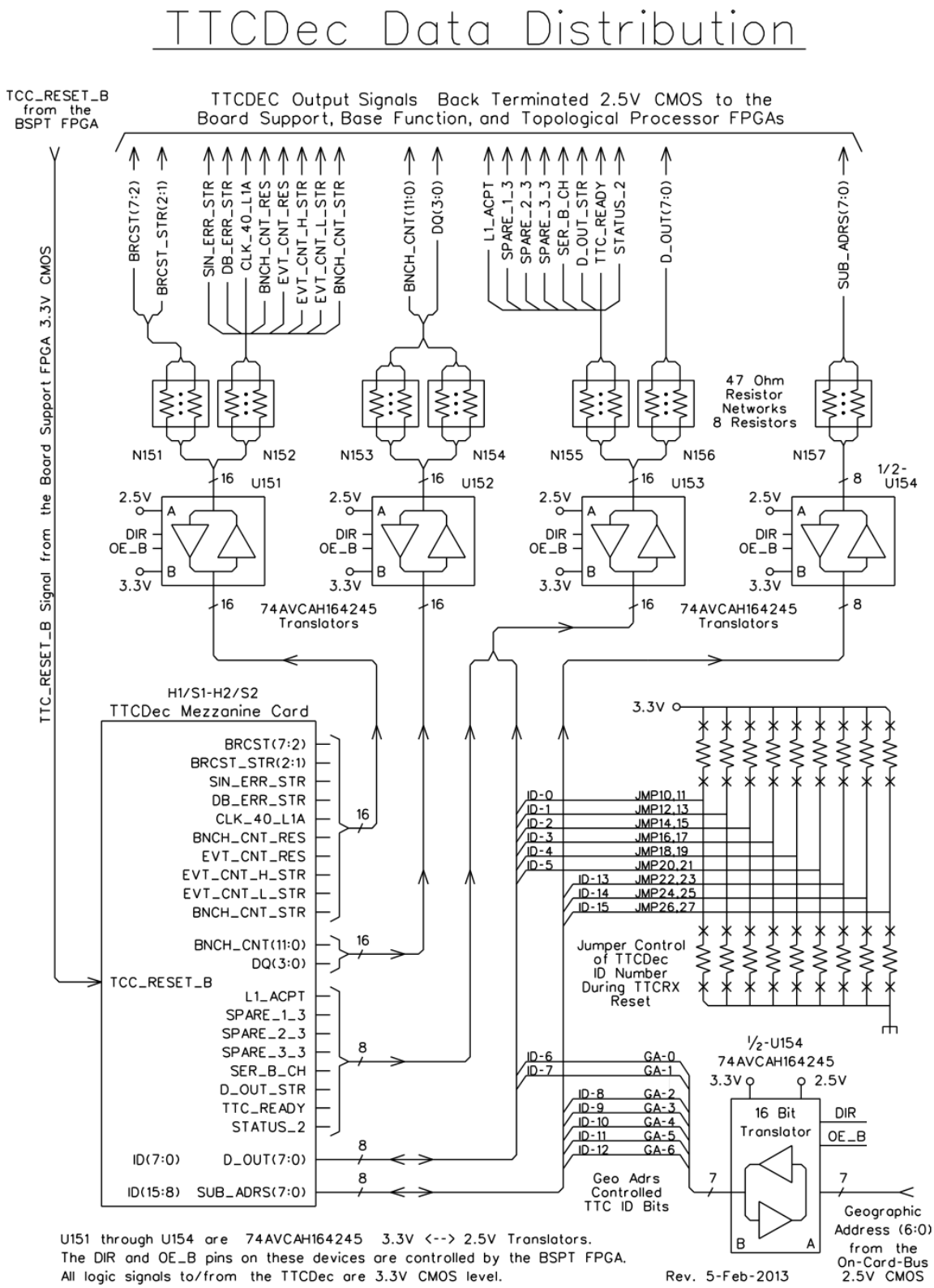

Figure 27 Circuit Diagram for TTCDec data distribution

A current snapshot is included above while future updates to this circuit diagram will be in 12_TTCDec_data_distribution.pdf found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot is included below while future updates to this description will be in cmx_ab_TTCDec_connections.txt found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
                CMX  TTCDec Signal Connections
               --------------------------------


                                                Current Rev. 12-Feb-2013


This file describes the connections to the TTCDec mezzanine
card on the CMX circuit board.  The TTCDec mezzanine card is
located in the lower right-hand corner of the card where it
is close to its input "clock" and were its outputs can run
directly up on the right hand side of the 3 FPGAs that use
the TTCDec output signals.

The TTCDec "clock" enters the CMX card via backplane pins
and is immediately received by a differential buffer chip.
The input to this buffer is AC coupled with 10 nFd capacitors
to help reduce out of band noise.  This NB6L611 buffer
provides an internal input termination.  From the output of
this buffer there is a short direct connection to the clock
input on the TTCDec mezzanine.

A TTCDec clock output provides the time-base for the CMX
card.  Installation of one of the three "jumpers" R254,
R255, or R256 allows use of either the TTCDec:
CLK_40_DES_1, CLK_40_DES_1_PLL_2, or CLK_40_DES_2_PLL_2
signal as the CMX time-base.  These signals come off of the
TTCDec and these jumpers are right next to the Clock
Generation section of the CMX card.  With this physical
location of the TTCDec and the Clock Generation components
the interconnecting traces are kept direct and short and
are located in a quiet part of the CMX card.

All of the TTCDec output signals are buffered by 3.3V to
2.5V translators (74AVCAH164245s) back terminated and run
up the right-hand side of the 3 FPGAs on the CMX card.
All of these TTCDec signals are run to the BSPT FPGA.  All
of the TTCDec output signals that are required for the
operation of the Base Function and Topological Processor
FPGAs will be routed to them.  Because of the high density
of traces in the break-out region of the BF FPGA the intent
is to not route TTCDec signals to the BF that will clearly
never be used by it.  The full list of TTCDec output signals
is listed for reference at the end of this note.
```

The TTCDec can be reset by the BSPT FPGA. The TTCDec_Reset_B signal comes directly from a pin in the 3.3V I/O Bank of the BSPT FPGA. The process of resetting the TTCDec includes sending ID bits 13:0 and the 2 Master Mode bits to the TTCDec. In some documents the 2 Master_Mode bits are referred to as ID bits 14 and 15 probably because this makes a nice round 16 bit quantity.

CMX uses the same basic method of providing the ID and Master Mode bits to the TTCDec during its Reset process as the CMM card does. Considering the ID plus Master Mode information as one 16 bit quantity, bits 15, 14, 13, and bits 5:0 come from a set of resistor "jumpers" JMP27 through JMP10. During Reset the pins in the TTCDec that receive this information become inputs and there logic level is determined by which of these resistor jumpers have been installed. After the Reset process is complete these same pins are outputs with sufficient drive to over come the bias of the installed resistor jumpers.

ID bits 12:6 are handled in basically the same way except that during the Reset process these 7 ID bits come from the output of one half of U154 a 2.5V to 3.3V translator chip. The input to this translator is the 7 bit Geographic Address of the CMX card that comes from the 2.5V On-Card_Bus. During the TTCDec Reset process the BSPT FPGA coordinates enabling the output drivers on this half of the U154 translator in time with the TTCDec_Reset_B signal. After the Reset process the output of this half of the U154 translator is disabled and the TTCDec pins that received ID bits 12:6 return to being outputs.

The CMX card also provides a JTAG connection to the TTCDec mezzanine on the 3.3V Test JTAG chain. No JTAG management of TTCDec is required that I know of. Jumpers can be installed to jump the Test JTAG chain around the TTCDec if desired. The only required management of the TTCDec that I know of is to Reset it.

The 2.5V buffered TTCDec output signals that are available to the 3 FPGAs on the CMX card are the following:

BRCST(7:2), BRCST_STR(2:1), SIN_ERR_STR, DB_ERR_STR,

CLK_40_L1A, BNCH_CNT_RES, EVT_CNT_RES, EVT_CNT_H_STR,

EVT_CNT_L_STR, BNCH_CNT_STR, BNCH_CNT(11:0), DQ(3:0),

L1_ACPT, SPARE_1_3, SPARE_2_3, SPARE_3_3, SER_B_CH,

D_OUT_STR, TTC_READY, STATUS_2, D_OUT(7:0) - ID(7:0),

SUB_ADRS(7:0) - ID(15:8)

Appendix H: Clock Generation and Distribution

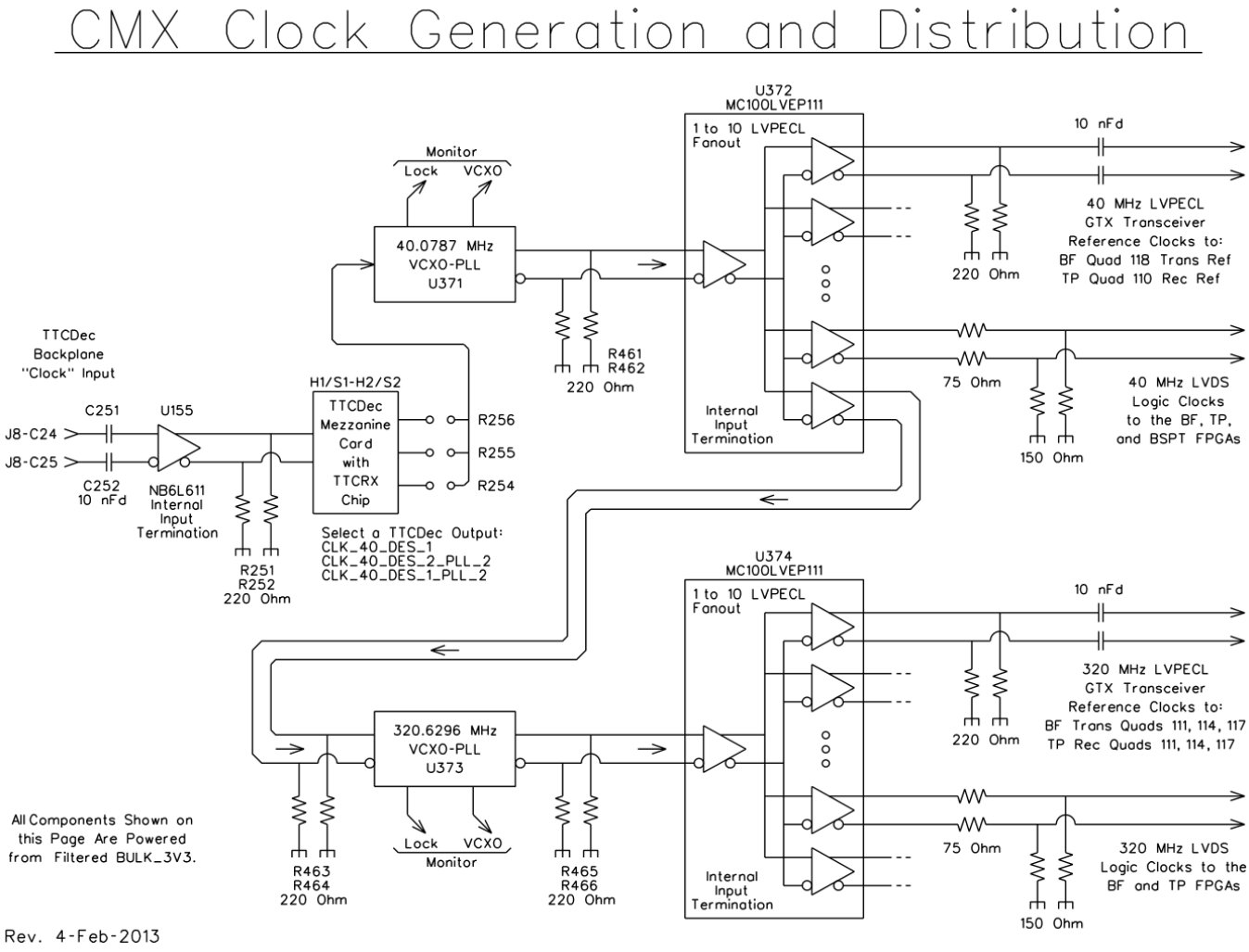

Figure 28 Circuit Diagram for clock generation and distribution

A current snapshot is included above while future updates to this circuit diagram will be in 11_clock_generation_and_distribution.pdf found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot is included below while future updates to this description will be in cmx_ab_clock_gen_and_dist.txt found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

CMX Clock Generation and Distribution

Original Rev. 20-Nov-2012
Current Rev. 12-Feb-2013

This file describes the generation and distribution of the clocks on the CMX circuit board. The main focus of this file is on the 40 MHz and 320 MHz clocks for the Logic and Transceiver functions in the 3 FPGAs on the CMX card. In addition to this we need a clock for the System-ACE and a clock for the CAN-Bus microprocessor.

Basic Design:

- The LHC reference will come from the TTCDec mezzanine. We can use either its: Clock_40_Des_1_PPL, Clock_40_Des_2_PPL, or Clock_40_Des_1 output signals as the reference for generating clocks on the CMX card. There are jumpers on the CMX card to select which of these TCCDec outputs is used by CMX as its reference clock.

- The CMX card uses a narrow band PLL-VCXO to generate a clean phase locked 40 MHz signal. This is the fundamental clock for the CMX card.

- Distribute this clean 40 MHz clock as an LVDS or Differential LVPECL signal to the following 8 places:

  BSPT FPGA Logic - scale to LVDS
  Base Function FPGA Logic - scale to LVDS
  Base Function FPGA GTX Transceiver - Diff LVPECL
  Topological FPGA Logic - scale to LVDS
  Topological FPGA GTX Transceiver - Diff LVPECL
  Reference for 320 MHz Generator - Diff LVPECL
  40 MHz Test/Monitor point - Diff LVPECL
  Spare - scale to LVDS

- Using a narrow band VCXO PLL to multiply the clean 40 MHz by 8 to make the 320 MHz clock for FPGA Logic and GTX Transceivers. Distribute this 320 MHz clock as an LVDS or Differential LVPECL signal to the following 9 places:

  Base Function FPGA Logic - scale to LVDS
  Base Function FPGA GTX Transceiver 3 copies - Diff LVPECL
  Topological FPGA Logic - scale to LVDS
  Topological FPGA GTX Transceiver 3 copies - Diff LVPECL
  320 MHz Test/Monitor point - Diff LVPECL

Virtex-6 Clock Input Signal Levels:

- The requirements for the GTX Transceiver clocks are clearly given in the chapter 5 of the GTX User Guide and in the Virtex-6 DC and Switching Data Sheet. The GTX reference clock input is clearly aimed at AC coupled Differential LVPECL signal levels. In the GTH User Guide this is specifically recommended as a Differential LVPECL signal.

- The Global Clock inputs for the Base Function and Topological Processor logic clocks can be any signal level that is supported by the Virtex-6 Select I/O inputs. It does not appear that the Select I/O inputs will directly accept Differential LVPECL with internal termination. The cleanest solution appears to be to use LVDS_25 signal levels to send the logic clocks to the Virtex-6 parts (and to the Board Support Spartan 3A part). In all cases internal 100 Ohm termination can be used with these LVDS_25 signals.

- The 40 MHz and 320 MHz clock fanout can all be done with Differential LVPECL chips and then the logic clocks to the Virtex-6 parts may be scaled to LVDS_25 levels with simple resistor networks at the sending end and internally differential terminated at the receiving Virtex end.

- The relevant signal specifications are:

  Virtex-6 LVDS_25 Input:

V Input Diff:	100 mV min,	350 mV Typ,	600 mV max
V Input CM:	0.30 V min,	1.25 V Typ,	2.20 V max

  MC100LVEP111 Differential LVPECL Output:

Vout HI:	2.155 V min,	2.280 V Typ,	2.405 V max
Vout LOW:	1.355 V min,	1.530 V Typ,	1.700 V max

Scaling Differential LVPECL to LVDS_25:

- Scaling both the Direct and Complement LVPECL outputs at the sending end by 0.66 makes both the differential and common mode voltages in the correct range for reception by the Xilinx LVDS_25 receivers.

- The expected differential voltage will be 500 mV. The expected common mode voltage will be 1.257 V.

- The resistor network to scale the Differential LVPECL signals can be 75 Ohm series then 150 Ohm to ground.

- This will result in about 10.13 mA of emitter current to the HI side of the Diff LVPECL driver and 6.8 mA to the LOW side. These emitter currents are right in the expected operating range.

- The internal Xilinx 100 Ohm differential LVDS terminator can be used with these clock lines.

Base Function and TP GTX Transceiver Reference Clock:

- The GTX transceiver PLLs can multiply up by a factor in the range from 4 to 25.

- The GTX transceiver PLL output is 1/2 the transceivers line bit rate, e.g. 3.3 GHz PLL output gives 6.6 Gb/s data rate.

- The GTX transceiver PLL's reference must be in the range from 62.5 MHz to 650 MHz, 50/50 duty cycle, 200 ps edge speed, AC coupled, 800 mV typical differential amplitude with range of from 210 to 2000 mV differential, 100 Ohm input resistance. Note the somewhat special way that Xilinx defines differential amplitude for the Transceiver Reference Clocks.

- The GTX transceivers can operate over the data rate range from 480 Mb/s up to 6.6 Gb/s. What internal PLL ratios do they use ?

  At the low end:
  480 Mb/s --> 240 MHz PLL output
  240 MHz divided by 62.5 MHz Ref --> 3.84 ratio

  At the Hi end:
  6.6 Gb/s --> 3.3 GHz PLL output
  3.3 GHz divided by 62.5 MHz Ref --> 52.80 ratio
  3.3 GHz divided by 650 MHz Ref --> 5.08 ratio

- GTX PLL Control Values:

  The reference clock is divided by "M"
  before going into the PLL M = 1 or 2

  The feedback divider is N1 x N2
  where N1 = 4 or 5
  where N2 = 2 or 4 or 5
  and where N1 x N2 must not equal 4 or 5 (duh)

There is a final divider "D" between the PLL output and the transceiver where D is either 1 or 2 or 4

Recall that the line rate is 2x the PLL output frequency.

GTX User Guide 2v6 pg 117 shows typical reference clocks in the range of about 200 to 325 MHz for line rates of about 4 to 6 Gb/s.

We know that for 6.4 Gb/s line data rate we want/need M = 1 and D = 1.

- I *think* that the actual line rate that they want is 6.4 Gb/s --> 3.2 GHz PLL output which is 80 times the "40 MHz" LHC frequency. 80 is 2 x 2 x 2 x 2 x 5

- Example setups from 40 MHz LHC to 6.4 Gb/s:

  40 MHz times 5 external gives 200 MHz reference
  200 MHz reference with N1=4 and N2=4 give 3.2 GHz

  40 MHz times 8 external gives 320 MHz reference
  320 MHz reference with N1=5 and N2=2 give 3.2 GHz

- Reference Clock for the "Slow Optical" RIO and DAQ Outputs

  On the CMM card this is a real HP G-Link chip and I *think* that it runs from the separate on card 40 MHz crystal oscillator that is distributed by a CY7B991V chip.

  On the CMX card the G-Link for the RIO and DAQ outputs will be implemented with GTX transceivers. I have been told that this GTX implementation of the G-Link will need a 40 MHz reference clock.

Board Support FPGA Clock:

- The Spartan 3A Board Support FPGA will receive just one clock. This is a clean 40 MHz clock.

- The Spartan 3A part can receive this clock as an LVDS signal with internal 100 Ohm termination.

- The LVDS input specifications for the Spartan 3A are:
  V Input Differential: 100 mV min, 350 mV Typ, 600 mV max
  V Input Common Mode: 0.30 V min, 1.25 V Typ, 2.35 V max

- This is really an Xilinx LVDS_25 signal going to an I/O Bank with VCCO of 2.5 Volts.

System-ACE Clock:

- The System-Ace typically runs from a 20 MHz clock.

- The 20 MHz clock for the System-ACE needs to be the same as the clock that is running whatever device is connected to the Systen-ACE microprocessor port, i.e. its MPU port.

- On the CMX card it is the Board Support FPGA that provides the connection to the ACE MPU port. The BSPT FPGA runs from the 40 MHz clock and it will provide the 20 MHz clock to the System-ACE. In this way the cycles in the MPU port of the System-ACE will be synchronous with activities in the BSPT FPGA.

- The clock input to the System-ACE is referenced to its VCCL power bus. On the CMX card the System-ACE VCCL bus will be supplied with 2.5 Volts. Thus the pin #93 clock input to the System-ACE must be a 2.5V CMOS level clock signal.

- The System-ACE clock trace will be back terminated at the BSPT FPGA.

CAN-Bus Microprocessor Clock:

- The clock to the MB90F594 CAN-Bus microprocessor can be either a 4 MHz quartz crystal with associated capacitors connected to the X0 and X1 pins or it can be a clock signal connected to only the X0 pin with pin X1 floating.

- Table 3 DC Characteristics page 39 hints that this device has strange input voltage levels, i.e. Vish min of 0.8 x Vcc and Vils max of 0.5 x Vcc. The diagram on page 41 hints that the X0 clock input runs between 0.2 x Vcc and 0.8 x Vcc. Other diagrams e.g. pg 45 indicate TTL type levels of 0.8V and 2.4V.

- CMX will provide a real 5V CMOS 4 MHz clock to the X0 pin (pin No. 82) of the MB90F594 CAN-Bus microprocessor and it will float its X1 pin (pin No. 83).

- CMX will use an ECS-3961-040-AU-TR crystal oscillator to supply this clock for the MB90F594 CAN-Bus microprocessor.

```
Background:
-----------

 - The LHC RF frequency is about:          400.8       MHz

 - The LHC BX frequency is really:
    At 450 GeV Proton Injection:            40.0788790 MHz
    At   7 TeV Proton Physics:              40.0789658 MHz
    At 450 GeV Ion Injection:               40.0784139 MHz
    At   7 TeV Ion Physics:                 40.0789639 MHz

 - Round to the nearest 1 Hz:
    At 450 GeV Proton Injection:            40.078,879  MHz
    At   7 TeV Proton Physics:              40.078,966  MHz
    At 450 GeV Ion Injection:               40.078,414  MHz
    At   7 TeV Ion Physics:                 40.078,964  MHz

 - For all modes the biggest pulls at 40.08 MHz are + 276 Hz

 - For all modes the fastest slew rates at 40.08 MHz are 22 Hz/sec
   The ramp up/down slews are much slower  < 1 Hz/sec

 - The center for Protons is:  40.078,922  MHz   +  43 Hz

 - The center for Ions is:     40.078,689  MHz   + 275 Hz

 - The center for both is:     40.078,690  Mhz   + 276 Hz

 - Order symmetric pull center frequency of:   40.078 700 MHz
     This will require a pull of Hz  - 286 Hz
     This is a pull of about 7.2 ppm

 - Order symmetric pull center frequency of:  320.629 600 MHz
     This is a pull of about 7.2 ppm



Components Used:
----------------

 - 40 MHz input, 40 MHz output VCXO PLL
   3.3V CMOS input signal level
   Differential LVPECL output signal level
   Vectron  FX-401  type A
   3.3 Volt power   19.9mm x 13mm module

 - 40 MHz 1 to 10 Fanout  MC 100 LVEP 111
   Differential LVPECL inputs and outputs
   3.3 Volt power   5mm x 5mm LLP-32  QFN-32

 - 40 MHz input, 320 MHz output VCXO PLL
   Differential LVPECL input signal level
```

Differential LVPECL output signal level
Vectron FX-401 type B
3.3 Volt power 19.9mm x 13mm module

- 320 MHz 1 to 10 Fanout MC 100 LVEP 111
  Differential LVPECL inputs and outputs
  3.3 Volt power 5mm x 5mm LLP-32 QFN-32

- 4 MHz 5 Volt CMOS Crystal Oscillator
  ECS-3961-040-AU-TR

40 MHz and 320 MHz Fanout Channels:

Both the 40 MHz and the 320 MHz use MC100LVEP111 1 to 10 Fanout chips with Differential LVPECL input and output levels. The differential output signal from these fanouts is AC coupled for use by the Virtex Transceiver Clocks and is scaled to LVDS levels for the Logic Clocks to the Virtex parts and for the Spartan 3A Board Support FPGA.

Fan Out Chnl	Dir-Cmp Output Pins	Chip U372 40 MHz Fanout Channel Use	Term	Chip U374 320 Mhz Fanout Channel Use	Term
0	31-30	Ref to 320 PLL	PD	320 MHz Test Pt	PD
1	29-28	Spare 40 MHz	LVDS	TP TRNSCV #1	PDAC
2	27-26	40 MHz TP Logic	LVDS	320MHz TP Logic	LVDS
3	24-23	TP TRNSCV 40	PDAC	TP TRNSCV #2	PDAC
4	22-21	no connection	--	320MHz BF Logic	LVDS
5	20-19	40 MHz BF Logic	LVDS	TP TRNSCV #3	PDAC
6	18-17	BF TRNSCV 40	PDAC	BF TRNSCV #1	PDAC
7	15-14	40MHz BSPT Logic	LVDS	BF TRNSCV #2	PDAC
8	13-12	no connection	--	BF TRNSCV #3	PDAC
9	11-10	40 MHz Test Pt	PD	no connection	--

Terminations: PD --> 220 or 240 Ohm pull-down resistors to Ground

```
                PDAC -->  220 or 240 Ohm pull-down resistors
                          to Ground  then 10 nFd series AC
                          coupling capacitors

                LVDS -->  Scale to LVDS --> 75 Ohm series
                          then signal feed off with 150 Ohm
                          pull-down to Ground.


Heat in the ECL Pull-Down Resistors:
------------------------------------

 - Worst case is 220 Ohm pull-down with output at a static
   high level of  2.405 V max  -->  26.3 mWatts  (10.9 mA)

 - Typical case is 220 Ohm pull-down with 50/50 output of
   typical Vout HI  = 2.280 V  -->  23.6 mWatts  (10.4 mA)
   typical Vout LOW = 1.530 V  -->  10.6 mWatts  ( 6.9 mA)
       Average dissipation is       17.1 mWatts.

 - The 0603 or 0402 resistors are rated to dissipate 62 mWatts.

 - CMX will use 0402 metal film resistors and 0402 10 nFd
   X7R capacitors in these termination networks.
```

Appendix I: VME-- and On-Card Bus

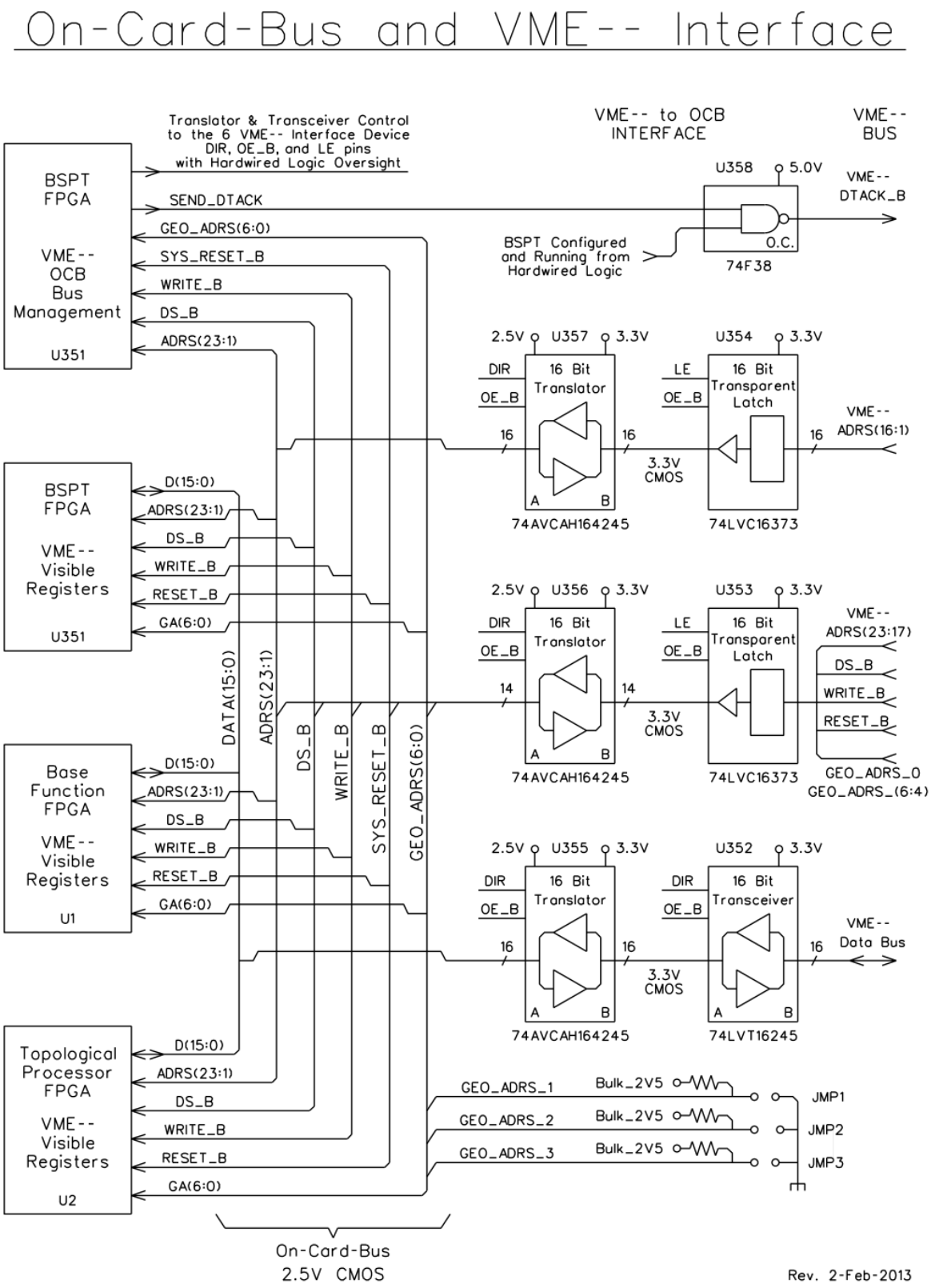

Figure 29 Circuit Diagram for the On-Card Bus

A current snapshot is included above while future updates to this circuit diagram will be in 08_on_card_bus_and_vme_interface.pdf found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot is included below while future updates to this description will be in cmx_ab_on_card_bus_design.txt found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
                  CMX  OCB  On-Card-Bus
                ------------------------


                                          Original Rev.  31-Oct-2012
                                           Current Rev.  12-Feb-2013


This file describes the On-Card_bus on the CMX circuit board.
The OCB is the on card version of the VME Minus Minus bus in the
L1Calo crate backplane.  The CMX card is a slave only, A24D16
only device on the VME Minus Minus bus.


The OCB connects 4 objects on the CMX card:
-------------------------------------------

 - It connects to the VME minus minus backplane bus

 - to the Board Support FPGA  (BSPT_FPGA)  a Spartan 3AN

 - to the Base Function  (BF_FPGA)  a Virtex 6

 - to the Topological Processor  (TP_FPGA)  a Virtex 6


Signals in the On-Card-Bus:
---------------------------

 - OCB_D15:OCB_D00   16 Data Bus lines, bi-directional, 2.5V

 - OCB_A23:OCB_A01   23 Address lines, always driven from
                       the VME-- end,  2.5V

 - OCB_DS_B   Data_Strobe_B, always driven by VME-- end,  2.5V

 - OCB_WRITE_B   Write_B data bus Direction, always driven
                 by the VME-- end,  2.5V

 - OCB_SYS_RESET_B   System_Reset_B, always driven by
```

the VME-- end, 2.5V

- OCB_GEO_ADRS_6:OCB_GEO_ADRS_0 Geographic Address lines, always driven by the VME-- end, 2.5V, 0,4,5,6 come from the backplane, 1,2,3 come from jumpers on the CMX

- Note that only the OCB management function in the BSPT_FPGA sees or controls the DTACK_B signal to the VME-- backplane bus.

FPGA Connections to the On-Card-Bus:

- All FPGA connections to the On-Card-Bus are via 2.5 Volt I/O Banks on the BSPT, BF, and TP FPGAs.

- The BSPT, BF, and TP all connect to the On-Card_Bus to make visible on VME-- a defined set of their internal registers and other memory structures.

- Logical the BSPT makes a second separate connection to the On-Card_Bus to provide certain bus management functions. Inside the BSPT has two separate sections that connect to the On-Card-Bus, normal VME-- register access and bus management.

Bus Management:

The OCB is managed by a small set of logic in the Board Support FPGA. This OCB management consists of the following:

- The BSPT_FPGA recognizes when a VME-- cycle has been started for which this CMX card is the addressed target. The BSPT_FPGA knows its VME-- address range based on the Geographic Address of the crate and slot that it finds itself in.

  A fixed delay after the start of a cycle targeting this CMX card the BSPT will assert the DTACK_B signal to the VME-- bus. The BSPT will then manage the "tear down" of this VME-- cycle when the DS_B signal is released and then it releases this card's DTACK_B signal.

- The BSPT_FPGA manages both the Direction of and the Output Enable of both the level translators and the data bus transceivers that connect the OCB to the VME-- backplane.

  During a VME-- Read cycle that addresses this CMX card

the data bus transceivers drive data to the VME-- bus with their outputs enabled

During a VME-- Write cycle that addresses this CMX card the data bus transceivers drive data to the OCB with their outputs enabled

When no cycle is taking place or there is a cycle taking place that does not address this CMX card the data bus transceivers are in the direction to send data to the VME-- bus with their outputs disabled. Note that the keepers in the 2.5V to 3.3V translators will maintain valid 2.5V logic levels on the OCB data lines.

- Enabling the outputs on any of the translator, receiver, or transceiver chips that connect the OCB with the VME-- bus is qualified by: the Board_Power_OK signal being asserted AND the BSPT_FPGA being configured, i.e. BSPT_DONE asserted.

- This hardwired logic oversight is to prevent the CMX card from hanging the Data Bus or the DTACK_B signal on the VME-- bus when the BSPT FPGA is not configured.

- The VME-- Address lines are received by a part that includes both a receiver and a transparent latch. The OCB management function in the BSPT_FPGA can use the Latch Enable signal to hold the state of the OCB Address lines during cycles on the VME-- bus.

- NOTES:

  The BSPT_FPGA must be configured and running for any VME-- communications to take place with the CMX card.

  The BSPT has two separate functions wrt the OCB:

    It manages the OCB as described above

    It is a device on the OCB, i.e. it may have an address range on the OCB and thus have registers that are visible from the OCB

  Because the DTACK_B signal is centrally managed, the OCB appears as a synchronous bus to all the registers in the 3 FPGA devices that are connected to it.

Physical Layout of the OCB Traces on the CMX Card:

- If the OCB signals were all layout out on one layer in their natural order they would appear as vertical traces running down on the East side of the BSPT, BF, and TP

FPGAs. In their natural order the signals going from West to East are:

GA1:GA3, D00:D15, A23:A17, DS_B, Write_B, Reset_B, GA0, GA4:GA6, A16:A01

- The order of the signals in this text line represents their natural physical order on the CMX pcb if they were all on the same layer.

OCB to Backplane VME-- Connection Details:

- The OCB connects to the VME-- backplane bus via level translator chips followed by bus transceiver and receiver chips.

- The 2.5V logic level of the OCB is converted to the 3.3V level required by the bus transceiver and receivers using 74AVCAH164245 level translators. This is the same level translators that is used on other parts of the CMX card.

- The bus data transceiver chip is a 74LVT16245. The bus receiver chips are 74LVC16373s.

- The DTACK_B line is driven by a 74F38 open collector chip.

Appendix J: JTAG chains and FPGA Configuration

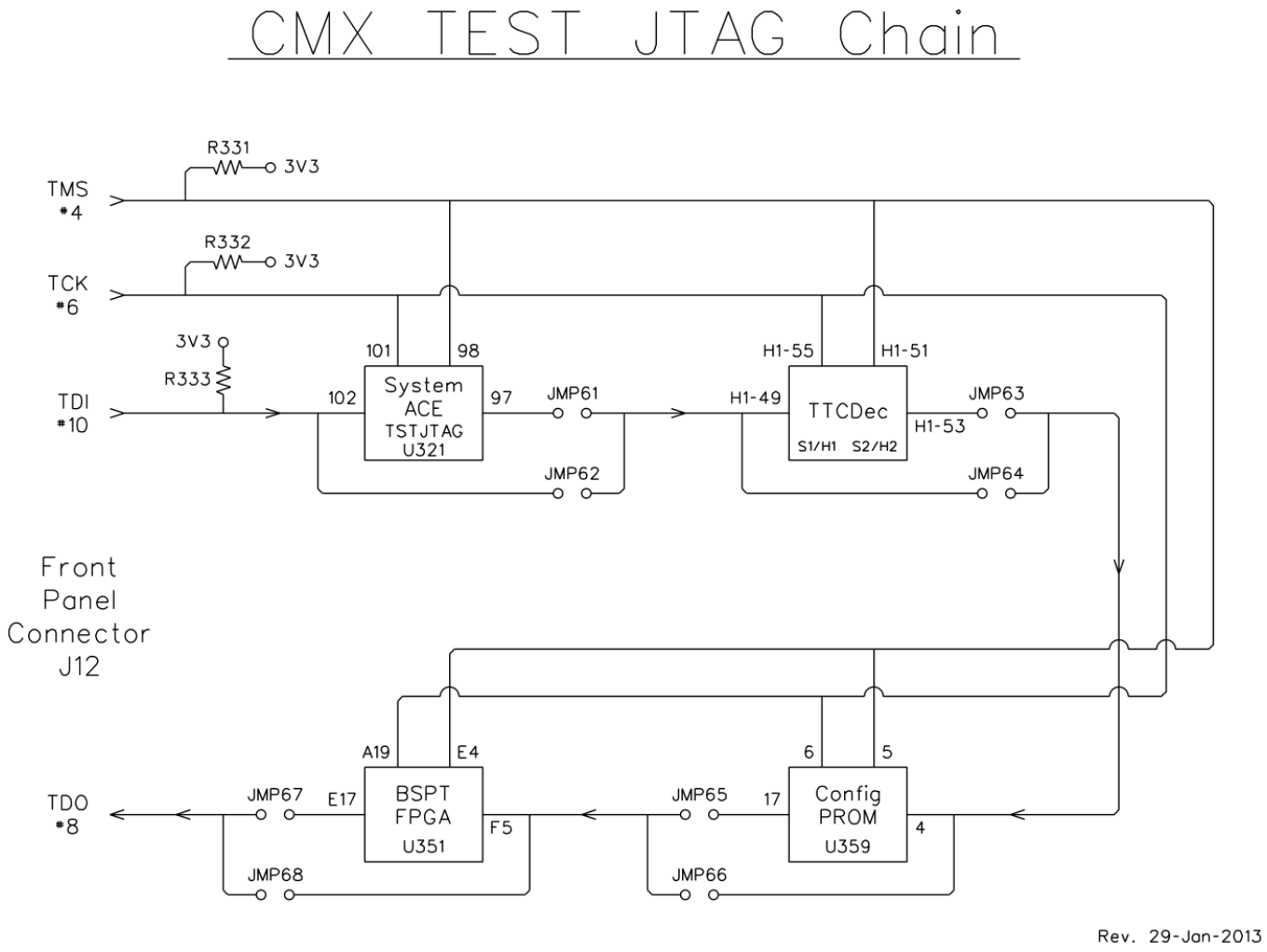

Figure 30 Circuit Diagram for Test JTAG chain

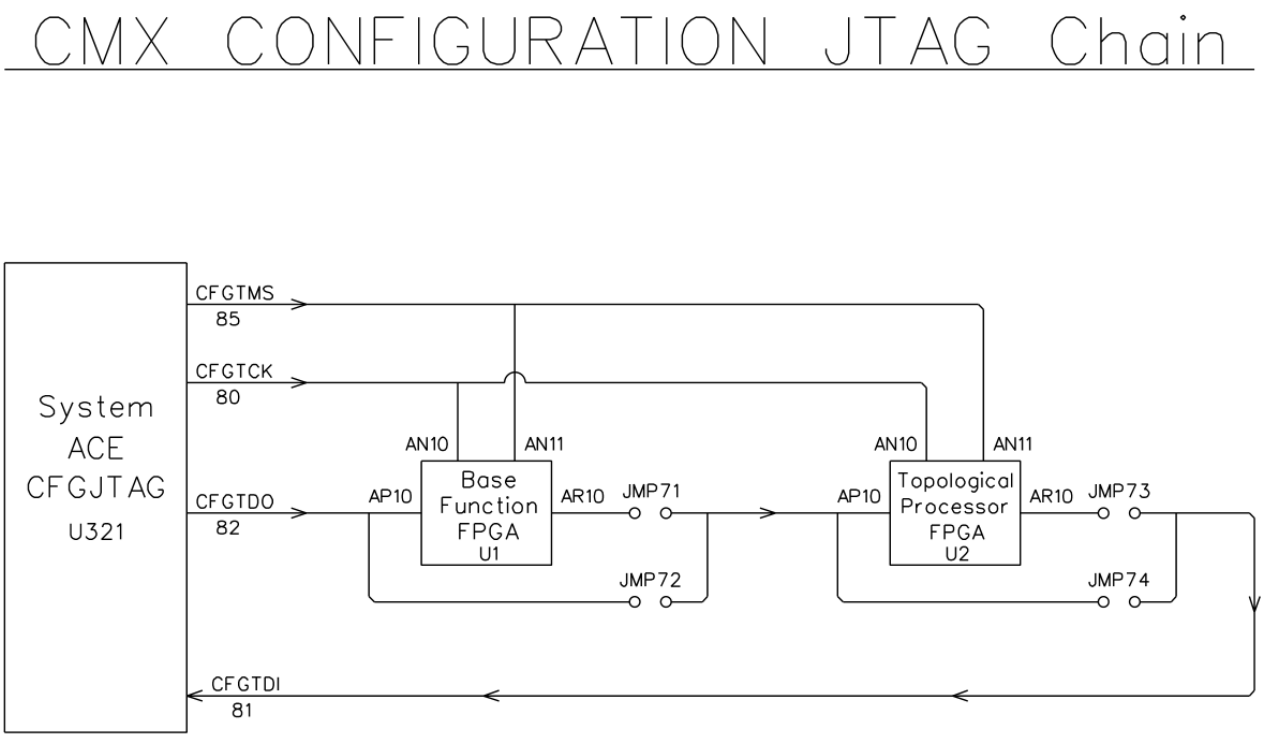

Figure 31 Circuit Diagram for the Virtex-6 FPGAs configuration JTAG chain

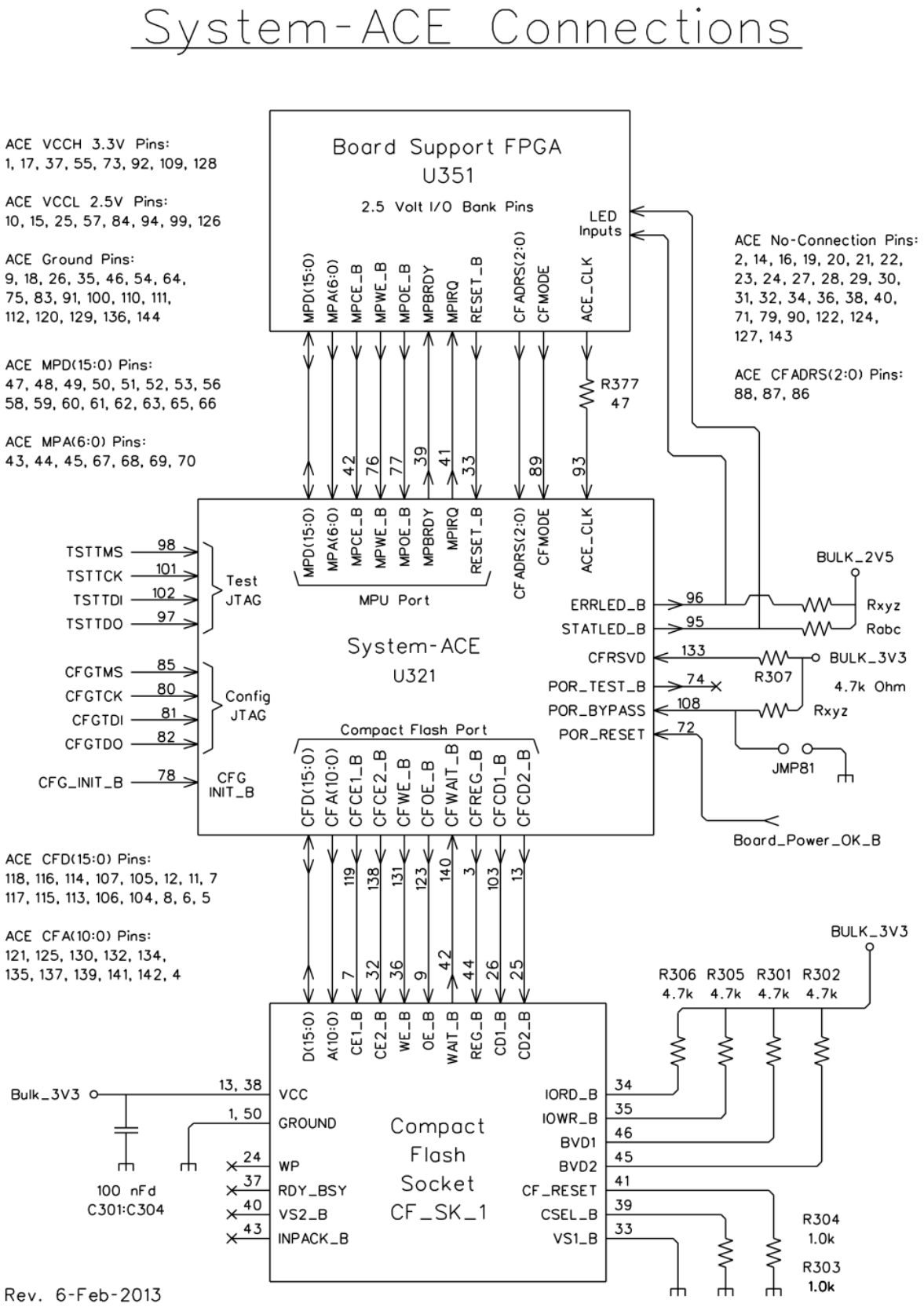

Figure 32 CIrcuit Diagram for System ACE

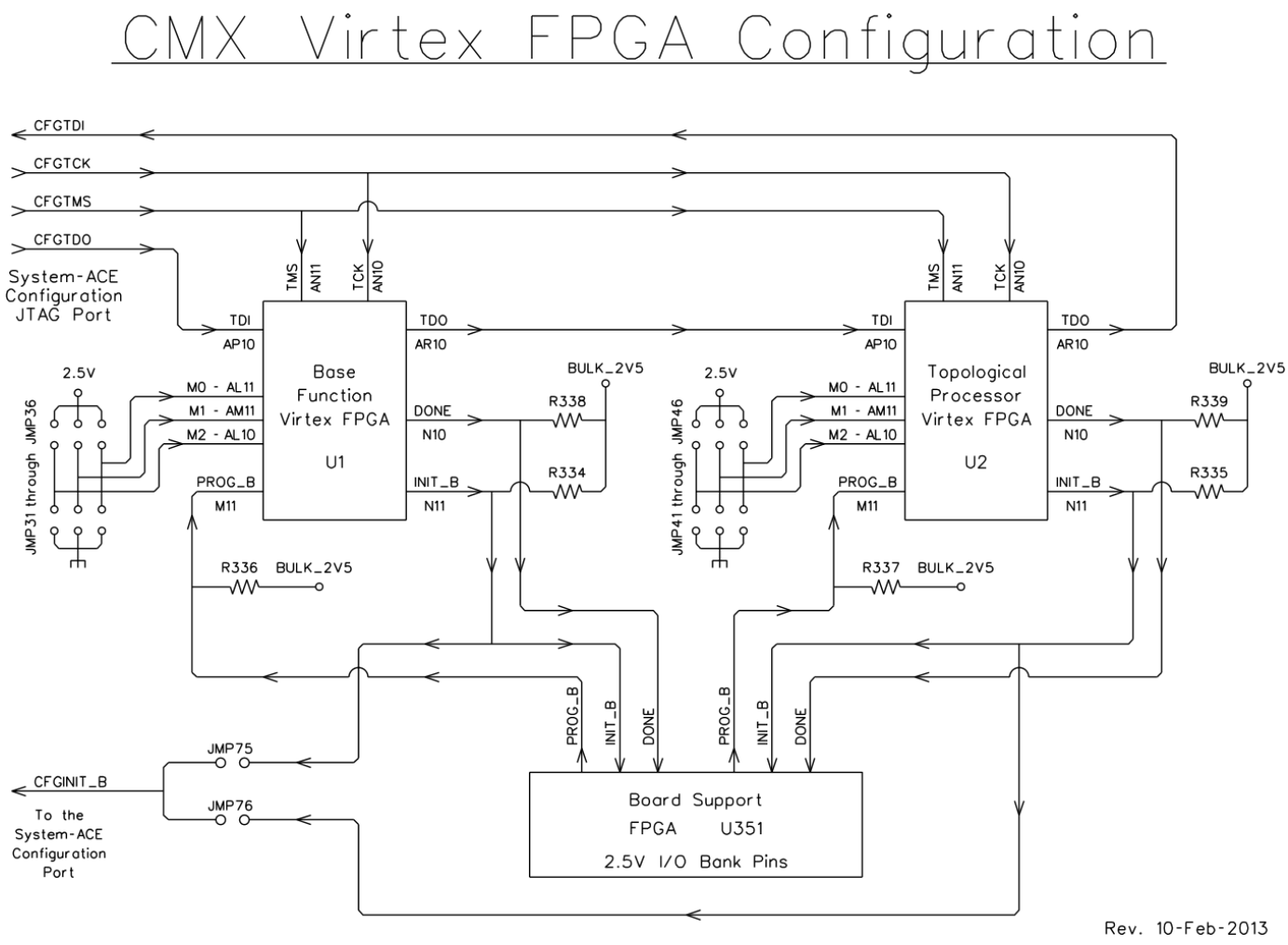

Figure 33 Circuit Diagram for Virtex-6 Configuration

A current snapshot is included above while future updates to these circuit diagrams will be in 01_jtag_chain_test.pdf, 02_jtag_chain_configuration.pdf, 15_system_ace.pdf and 17_virtex_fpga_configuration.pdf found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot is included below while future updates to this description will be in cmx_ab_jtag_and_config.txt found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

CMX JTAG and FPGA Configuration

Current Rev. 12-Feb-2013

This file describes the two JTAG chains on the CMX card and the configuration of the FPGAs on the CMX card.

JTAG Chains:

The arrangement of the two JTAG chains on the CMX card is driven by the requirements of the System-ACE chip.

- The "Test" JTAG chain can be accessed from the front panel J12 connector. This is a 3.3V JTAG chain. The data path in this chain is: J12 input, System-ACE, TTCDec, the Configuration PROM for the BSPT FPGA, the BSPT FPGA itself, and finally J12 data output. There are jumpers on this chain to skip around any of these devices. At the front panel J12 connector to the Test JTAG chain the CMX provides default value pull-up resistors on the TMS, TCK, and TDI signals.

  The pinout of the J12 Test JTAG connection is:

  All odd pins, 1 through 13, are Ground

  pin #2 Fused BULK_3V3 reference to the JTAG pod

  pin #4 TMS with a 4.7k Ohm pull-up on the CMX

  pin #6 TCK with a 4.7k Ohm pull-up on the CMX

  pin #8 TDO Test Data from CMX to the JTAG Pod

  pin #10 TDI with a 4.7k Ohm pull-up on the CMX
  This is JTAG data to the CMX.

  pin #12 Vtst Xilinx Reserved CMX makes no connection.
  pin #14 INIT Xilinx Serial CMX makes no connection.

  Note that the final 2 pins on the J12 connector (pins 15 and 16) provide RS-232 access to the CAN-Bus microprocessor. The JTAG and RS-232 function were combined in this one front panel connector because of the very limited space available on the CMX front panel. Because J12 is a 16 pin connector (vs the normal 14 pin JTAG connector) a slightly modified JTAG cable may be required. The pinout of the JTAG section of J12 on the CMX matches the "standard" for Xilinx JTAG pods.

- The "Configuration" JTAG chain includes only the "CFGJTAG" port on the System-ACE and the two Virtex FPGAs on the CMX card. The data on the Configuration JTAG chain flows from the System-ACE, through the Base Function FPGA U1, then through the Topological Processor FPGA U2, and finally back to the System-ACE. Jumpers are provided to skip this JTAG chain around either U1 or U2. Most CMX cards will not have U2 installed so use of these skip jumpers will be necessary. The Configuration JTAG chain used 2.5V logic levels.

  The System-ACE allows the Configuration JTAG chain to be used either for external access to the BF and/or TP FPGAs from the front panel Test JTAG chain or to configure these FPGAs from data stored in the Compact Flash module that is attached to the System-ACE.

FPGA Configuration:

The CMX card handles the configuration of the Spartan 3A Board Support FPGA in a separate different way from how it handles the configuration of the two Virtex FPGAs, i.e. the Base Function and Topological Processor FPGAs.

- BSPT FPGA Configuration

  The intent is that the BSPT FPGA will be quickly and automatically configured and ready for use whenever the power is turned ON to the CMX. The intent is that the BSPT FPGA on the CMX card will be used in a way that is similar to the use of the CoolRunner CPLDs on the CMM card, i.e. their logic is always available.

  The BSPT FPGA is automatically configured from a Xilinx XCF04S "Platform Flash" PROM whenever the power is turned ON to the CMX card. Configuration of the BSPT begins once all of the DC/DC power converters are running and their output voltages are within the "Board_Power_OK" range. The Master Serial mode configuration of the BSPT FPGA then takes about one second. Once the BSPT is configured then VME-- access to the registers in the BSPT is available. Before the BSPT is configured there is hardwired logic on the CMX to prevent it from hanging the VME-- bus and thus interfering with VME-- communication to other cards in the crate.

  Both the BSPT FPGA itself and the XCF04S "Platform Flash" Configuration PROM appear as devices on the Test JTAG chain. Thus from the front panel new firmware can be loaded into the XCF04S Configuration PROM without

removing the CMX card from the crate.

The intent is that the BSPT firmware will be stable and not need to evolve in the same way that the Base Function or Topological Processor firmware may need to develop over time. The BSPT firmware should have the same place in the operation of the CMX card as the firmware for the CoolRunner CPLDs does in the operation of the CMM card.

- Base Function and Topological Processor FPGA Configuration

The two Virtex FPGAs on the CMX card are configured via their JTAG connection to the CFGJTAG port of the System-ACE chip. Our intent in the CMX design is to implement the standard setup for the configuration of these Virtex FPGAs as is used for FPGA configuration on other L1Calo cards.

The System-ACE is controlled via its MPU port. All signals in the System-ACE's MPU port are routed to pins in a 2.5V I/O bank of the BSPT FPGA. Logic and VME-- visible registers in the BSPT allow control of the System-ACE from the VME-- bus. The 20 MHz clock to the System-ACE comes from the BSPT FPGA so that MPU port operations are synchronized in the required way. The BSPT FPGA also controls the signals to the System-ACE CFGMODE and CFGADRS(2:0) pins.

The BSPT FPGA also has access to 3 pins on each of the Virtex FPGAs that control the configuration of these parts, i.e. their PROG_B, INIT_B, and DONE pins. By monitoring these Virtex FPGA pins the BSPT can monitor the progress of configuring these parts. The 3 "M" pins to each Virtex FPGAs are controlled by jumpers on the CMX card. These jumpers will normally be set for M2, M1, M0 = 101 to specify that JTAG configuration will be used.

The INIT_B pins on the two Virtex FPGAs are also routed to the CFGINIT_B pin on the System-ACE. This signal prevents the System-ACE from starting the configuration process before the Virtex parts are ready to absorb it. Jumpers JMP75 and JMP76 on the CMX control which of the Virtex INIT_B pins is connected to the System-ACE.

The two LED pins on the System-ACE (ERRLED_B and STATLED_B) are also routed to the BSPT. From there this information can be read in a VME-- visible register and can be used to control front panel LEDs if that is desired.

```
The POR_RESET to the System-ACE is removed once DC power
is stable on the CMX card.  The state of the System-ACE's
POR_BYPASS pin is controlled by jumper JMP81.
```

Appendix K: CAN Bus

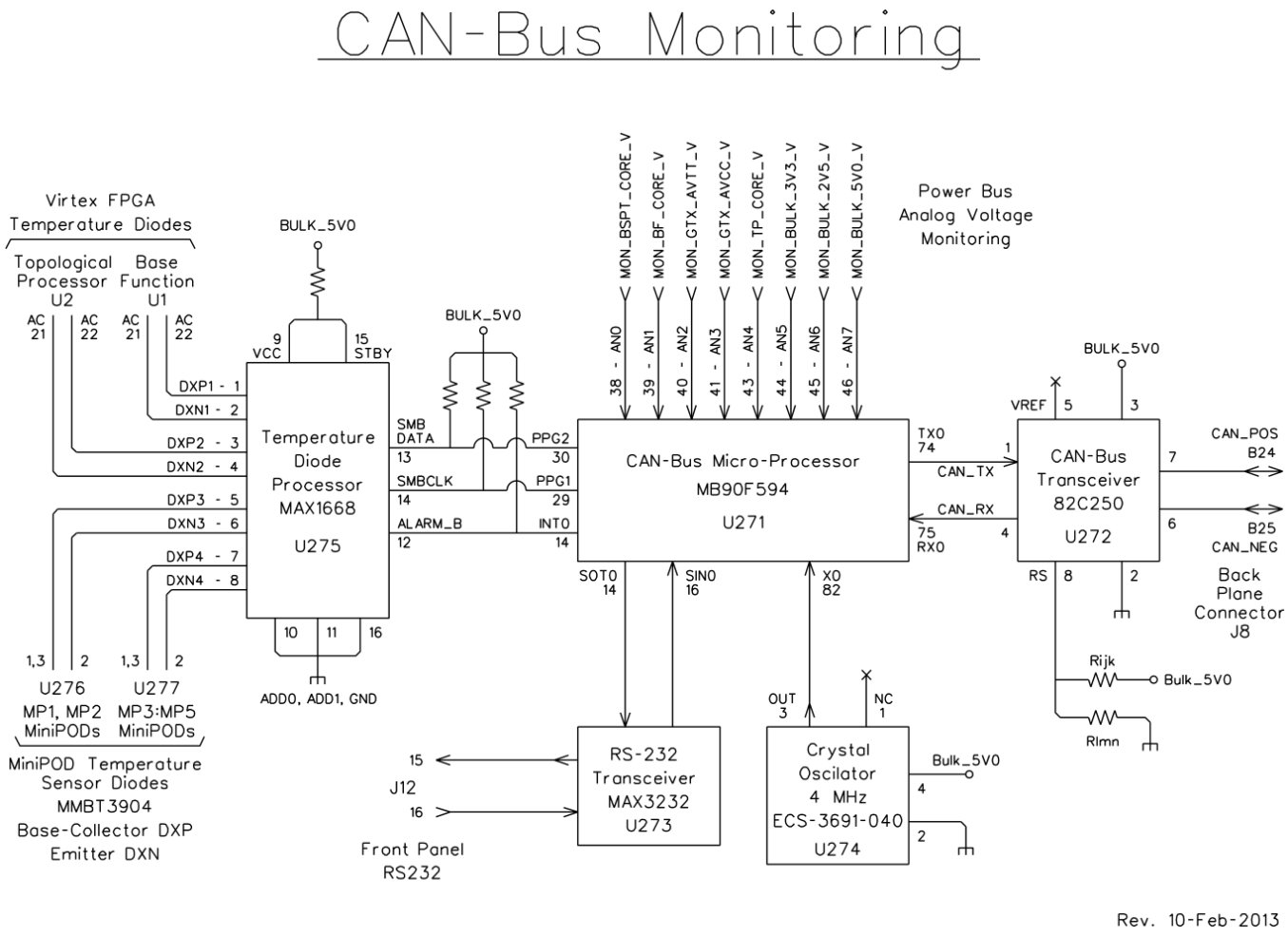

Figure 34 Circuit Diagram for CAN Bus monitoring

A current snapshot is included above while future updates to this circuit diagram will be in 16_can_bus_monitoring.pdf found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot is included below while future updates to this description will be in cmx_ab_can_bus_monitoring.txt located in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

CMX CAN-Bus Monitoring

Current Rev. 12-Feb-2013

This file describes the CAN-Bus Monitoring on the CMX circuit board.

The following components are used to implement the CAN-Bus Monitoring on the CMX circuit board:

- Fujitsu MB90F594 CAN-Bus Microprocessor
- Philips NXP 82C250 CAN-Bus Interface
- Maxim MAX1668 Diode Temperature Sensor Processor
- Maxim MAX3232 RS-232 Interface
- Fairchild MMBT3904 "Diode" Temperature Sensors
- 4 MHz Crystal Oscillator for the Microprocessor

Most of these parts require a 5 Volt Vcc power supply. The 5 Volts for this section of the CMX card is provided through a 3 Amp SMD mount fuse.

The MB90F594 CAN-Bus microprocessor is provided with a 4 MHz clock from a separate 5 Volt crystal oscillator.

This CAN-Bus Monitoring on the CMX card is separate from other sections of the card. Failure of FPGAs to configure or "hangs" in the logic on other parts of the CMX card will not prevent the CAN-Bus Monitoring from working.

There is a front panel RS-232 connection to the CAN-Bus Microprocessor. This connection is through part of the front panel J12 connector. J12 also provides the front panel connection to the Test JTAG chain on the CMX card. An adaptor cable will provide the connection from J12 on the CMX to a normal 9 pin RS-232 "D" connector.

All 8 Analog Inputs to the CAN-Bus Microprocessor are used to monitor power bus voltages on the CMX card. The following table shown which Analog Input is used to monitor which power bus.

CAN-Bus Micro-Processor Analog Input	Power Bus Voltage Monitored by this Input
AN0	BSPT_CORE
AN1	BF_CORE
AN2	GTX_AVTT
AN3	GTX_AVCC
AN4	TP_CORE

AN5	BULK_3V3
AN6	BULK_2V5
AN7	BULK_5V0

The CAN-Bus Monitoring provides readout of the temperature at 4 points on the CMX card. These temperatures are measured by the voltage drop across a BE junction diode at constant current. The diode temperature sensor processing is provided by the Maxim MAX1668 chip. The following table shows what location is measured by which channel of the MAX1668 diode temperature sensor processor.

MAX1668 Channel	Location of the Temperature Sensor
DX1	BF Virtex FPGA Silicon Temperature
DX2	TP Virtex FPGA Silicon Temperature
DX3	MMBT3904 at the "hot end" of MiniPODs MP1, MP2
DX4	MMBT3904 at the "hot end" of MiniPODs MP3:MP5

Appendix L: CMX Jumpers

A current snapshot is included below while future updates to this description will be in cmx_ab_board_jumpers.txt located in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
                CMX Board Jumpers
              --------------------

                                          Original Rev.  5-Nov-2012
                                           Current Rev. 12-Feb-2013

This file describes all of the jumpers that are on the CMX
circuit board.  These jumpers are used to setup and control
various functions of the CMX card.


JMP1, JMP2, JMP3   Geographic Address Jumpers

  Geographic Address lines 0, 4, 5, 6  come from the backplane.
  Geographic Address lines 1, 2, 3  come from jumpers 1, 2, 3.

  When one of these 3 jumpers is installed the corresponding
  Geographic Address line is pulled LOW.  E.G. if JMP2 is
  installed then Geographic_Address_2  is pulled LOW.


JMP4   Board Support FPGA Configuration PROM CF_B signal to PROG_B

  Installing JMP4 allows the JTAG connection to the Configuration
  PROM for the Board Support FPGA to initiate the configuration
  of this FPGA.  When installed, JMP4 connects the PROM's  CF_B
  signal to the BSPT FPGA's PROG_B pin.


JMP5, JMP6, JMP7  Backplane LVDS Receiver Failsafe

  When installed the corresponding set of backplane LVDS
  receivers are in normal "Type 1" mode,  i.e. symmetric
  voltage thresholds.  When removed the corresponding set
  of LVDS receivers are in "Type 2" Failsafe mode with
  offset voltage thresholds.  Normally we expect that all
  3 of these jumpers will be installed.  JMP5 controls
```

the Upper Backplane Cable receivers. JMP6 the Middle and JMP7 the Lower cable receivers.

R181, R182, R183 Backplane LVDS Transceiver Master_Enable

These 3 "jumpers" are really 100 Ohm resistors. When they are installed they pull the Master Enable pin on the associated LVDS transceivers voltage HI there by enabling normal operation of these DS91M040 LVDS transceivers. We expect that normally all 3 of these "jumpers" will be installed. R181 controls the Upper Backplane Cable transceivers. R182 the Middle and R183 the Lower cable transceivers.

JMP8 and JMP9 Front Panel CTP LVDS Receiver Failsafe

When installed the corresponding set of Front Panel CTP LVDS receivers are in normal "Type 1" mode, i.e. symmetric voltage thresholds. When removed the corresponding set of LVDS receivers are in "Type 2" Failsafe mode with offset voltage thresholds. Normally we expect that both of these jumpers will be installed. JMP8 controls the receivers for the Upper CTP connector J10. JMP9 controls the receivers for the Lower CTP connector J11.

R184 and R185 Front Panel CTP LVDS Transceiver Master_Enable

These 2 "jumpers" are really 100 Ohm resistors. When they are installed they pull the Master Enable pin on the associated set of LVDS transceivers voltage HI there by enabling normal operation of these DS91M040 LVDS transceivers. We expect that normally both of these "jumpers" will be installed. R184 controls the LVDS Transceivers for the Upper CTP connector J11. R185 controls the LVDS Transceivers for the Lower CTP connector J11.

JMP10 through JMP27 TTCDec Chip_ID and Master_Mode Bits

These 18 jumpers are used to set 9 of the TTCDec CHIP_ID and MASTER_MODE bits when the TTCDec is Reset. There are setup as follows:

Jumper to	
Pull	Pull

Low	High		
JMP10	JMP11	--->	CHIP_ID(0)
JMP12	JMP13	--->	CHIP_ID(1)
JMP14	JMP15	--->	CHIP_ID(2)
JMP16	JMP17	--->	CHIP_ID(3)
JMP18	JMP19	--->	CHIP_ID(4)
JMP20	JMP21	--->	CHIP_ID(5)
JMP22	JMP23	--->	CHIP_ID(13)
JMP24	JMP25	--->	MASTER_MODE(0) aka CHIP_ID(14)
JMP26	JMP27	--->	MASTER_MODE(1) aka CHIP_ID(15)

The remaining 7 bits of the CHIP_ID i.e. 12:6 are controlled by the 7 Geographic Address lines.

R254, R255, R256 TTCDec CMX Clock Select

These 3 Jumper-Resistors select the output from the TTCDec that will be used as the reference input to the CMX Clock Generator. Only one of these 3 resistors should be installed at a time. This Jumper-Resistor also acts as a series back terminator on the trace that takes the TTCDec clock output to the CMX Clock Generator. This resistor value should be in the 33 to 51 Ohm range.

Install R254 to select TCC_CLK_40_DES_1_PLL_2
Install R255 to select TCC_CLK_40_DES_2_PLL_2
Install R256 to select TCC_CLK_40_DES_1

JMP28 TTCDec Buffer Direction Control

Jumper 28 sets the Direction of the Translator/Buffer chips U151:U154 (only 1/2 of U154) for the TTCDec Output Bus. The TTCDec output signals are converted to 2.5V and driven onto the TCCDec Output Bus to go to the Board Support FPGA and optionally to the Base Function and Topological Processor FPGA. The required Direction is "B"-->"A" so Direction control signal must be LOW. JMP28 is normally always installed, i.e. pull DIR Low.

JMP31 through JMP36 Base Function FPGA M2,M1,M0

These 6 jumpers control the M2, M1, and M0 Configuration signals to the Base Function Virtex FPGA. Normally the Base Function FPGA is Configured via JTAG which requires the M2, M1, M0 signals to be set to "101". Never install both the HI and LOW jumpers for a given signal.

```
    Install JMP31 to pull M2 LOW   JMP32 to pull M2 HI
    Install JMP33 to pull M1 LOW   JMP34 to pull M1 HI
    Install JMP35 to pull M0 LOW   JMP36 to pull M0 HI
```

JMP37 and JMP38 Base Function FPGA HSWAPEN Pin

These 2 jumpers control the state of the HSWAPEN pin on the Base Function FPGA. Install only one of these jumpers - installing both will short the Bulk_2V5 bus.

```
    Install JMP37 to pull HSWAPEN Low
    Install JMP38 to pull HSWAPEN Hi
```

JMP41 through JMP46 Topological FPGA M2,M1,M0

These 6 jumpers control the M2, M1, and M0 Configuration signals to the Topological Processor Virtex FPGA. Normally the Topological Processor FPGA is Configured via JTAG which requires the M2, M1, M0 signals to be set to "101". Never install both the HI and LOW jumpers for a given signal.

```
    Install JMP41 to pull M2 LOW   JMP42 to pull M2 HI
    Install JMP43 to pull M1 LOW   JMP44 to pull M1 HI
    Install JMP45 to pull M0 LOW   JMP46 to pull M0 HI
```

JMP47 and JMP48 Topological Processor FPGA HSWAPEN Pin

These 2 jumpers control the state of the HSWAPEN pin on the Topological Processor FPGA. Install only one of these jumpers - installing both will short the Bulk_2V5 bus.

```
    Install JMP47 to pull HSWAPEN Low
    Install JMP48 to pull HSWAPEN Hi
```

JMP51 through JMP56 Board Support FPGA M2,M1,M0

These 6 jumpers control the M2, M1, and M0 Configuration signals to the Board Support Spartan FPGA. Normally the Board Support FPGA is Configured via Master Serial mode from its dedicated Configuration "Platform FLASH" PROM which requires the M2, M1, M0 signals to be all set LOW. Never install both the HI and LOW jumpers for a given signal.

```
    Install JMP51 to pull M2 LOW   JMP52 to pull M2 HI
    Install JMP53 to pull M1 LOW   JMP54 to pull M1 HI
```

Install JMP55 to pull M0 LOW JMP56 to pull M0 HI

R257 Geographic Address Buffer Direction Control

Jumper R257 is a 1k Ohm resistor that controls the Direction pin of the section of U154 that sends the Geographic Address lines to some of the TTCDec CHIP ID input pins when the TTCDec is being Reset. The Direction of just this section of U154 is always "A"--"B" so the Direction control pin must be HI. R257 is normally always installed, i.e. pull DIR HI.

JMP61 through JMP68 TEST JTAG Chain Device Skip Jumpers

JMP61 and JMP62 allow the front panel TEST JTAG chain to skip across the System-ACE device. Install either JMP61 or JMP62 - not both. Install JMP61 to include the System-ACE. Install JMP62 to skip the System-ACE.

JMP63 and JMP64 allow the front panel TEST JTAG chain to skip across the TTCDec device. Install either JMP63 or JMP64 - not both. Install JMP63 to include the TTCDec. Install JMP64 to skip the TTCDec.

JMP65 and JMP66 allow the front panel TEST JTAG chain to skip across the Configuration PROM for the BSPT FPGA. Install either JMP65 or JMP66 - not both. Install JMP65 to include the Configuration PROM. Install JMP66 to skip the Configuration PROM for the BSPT FPGA.

JMP67 and JMP68 allow the front panel TEST JTAG chain to skip across the BSPT FPGA. Install either JMP67 or JMP68 - not both. Install JMP68 to include the BSPT FPGA. Install JMP68 to skip the BSPT FPGA. Note that to include the BSPT FPGA and provide back termination on the TDO data being sent to the JTAG interface pod that a resistor could be used in JMP67.

JMP71 through JMP74 Configuration JTAG Chain Skip Jumpers

JMP71 and JMP72 allow the System-ACE Configuration JTAG chain to skip across the Base Function FPGA U1. Install either JMP71 or JMP72 - not both. Install JMP71 to include the Base Function FPGA in the Configuration JTAG chain. Install JMP72 to skip the Base Function FPGA.

JMP73 and JMP74 allow the System-ACE Configuration JTAG chain to skip across the Topological Processor FPGA U1.

Install either JMP73 or JMP74 - not both. Install JMP73 to include the Topological Processor FPGA in the Configuration JTAG chain. Install JMP74 to skip the Topological Processor FPGA.

JMP75 and JMP76 BF and TP INIT_B to System-ACE Select

JMP75 and JMP76 allow selection of which Virtex FPGAs have their INIT_B Configuration signals connected to the System-ACE CFGINIT_B pin. This controls which subset of the two Virtex FPGAs the System-ACE will confirm is ready to receive a configuration before starting to send the bitstream to it via the Configuration JTAG.

Installing JMP75 connects the Base Function FPGA's INIT_B signal to the System-ACE's CFGINIT_B pin. Installing JMP76 connects the Topological Processor FPGA's INIT_B signal to the System-ACE's CFGINIT_B pin. Note that the System ACE's CFGINIT_B pin is pulled up to 2.5 Volts with a 4.7k Ohm resistor.

JMP78 and JMP79 TP_CORE DC/DC Converter Disable Jumpers

Jumpers JMP78 and JMP79 are used to disable the TP_CORE DC/DC Converter on CMX cards that do not include a Topological Processor FPGA. JMP78 is associated with this converter's Inhibit pin. JMP79 is associated with this converter's Track pin.

To disable the TP_Core DC/DC Converter install jumper JMP78 to pull this converter's Inhibit pin to Ground, and remove JMP79 to isolate this converter's Track pin from the Track bus that spans the other 6 converters.

For operation of CMX cards with a Topological Processor FPGA remove JMP78 and install JMP79.

JMP81 System-ACE POR_Bypass Pin

Jumper JMP81 controls the state of the Xilinx System-ACE POR_Bypass pin. When JMP81 is installed then the POR_Bypass pin is held LOW and the System-ACE's internal power on reset circuits are used. With JMP81 removed the external POR_Reset signal can be used.

Appendix M: CMX Power Supplies and Voltage References

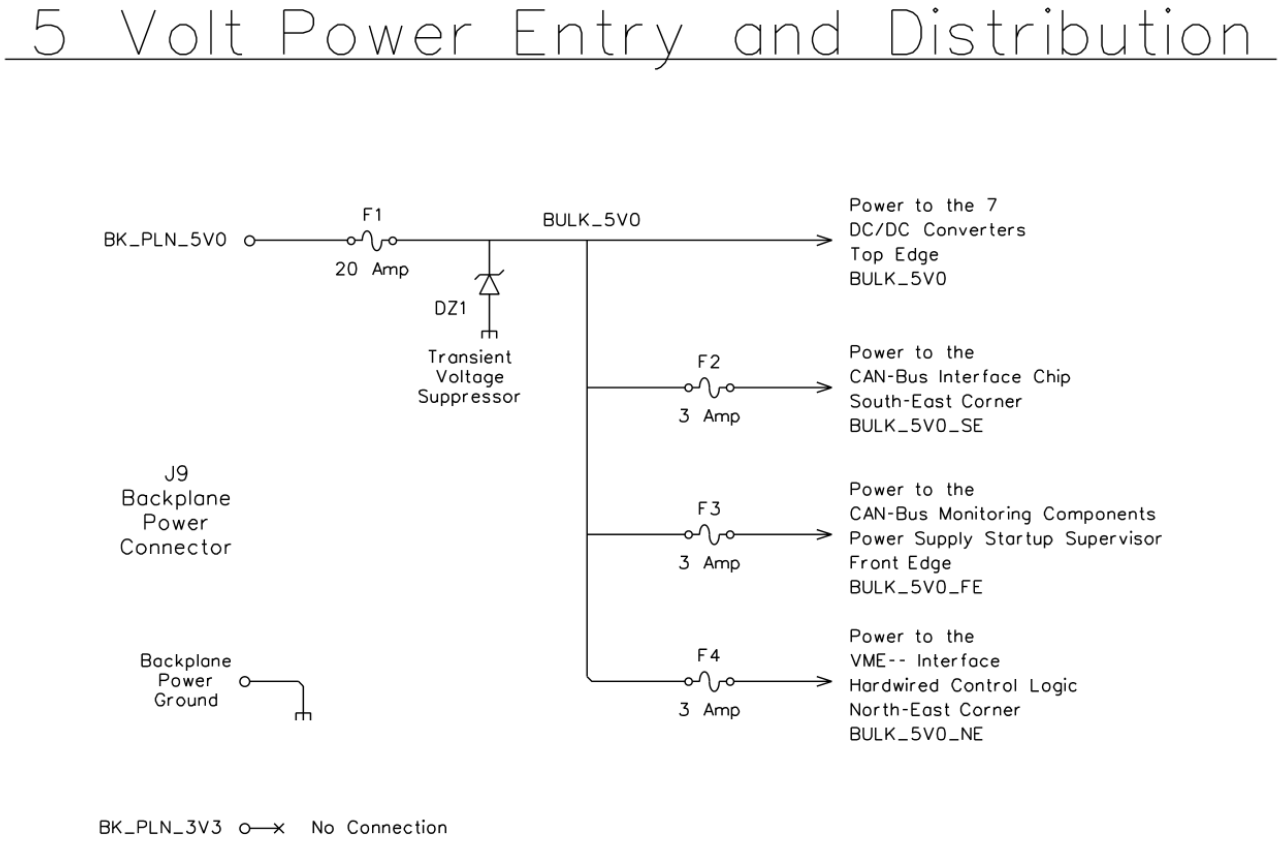

Figure 35 Circuit Diagram for the 5V Power Distribution

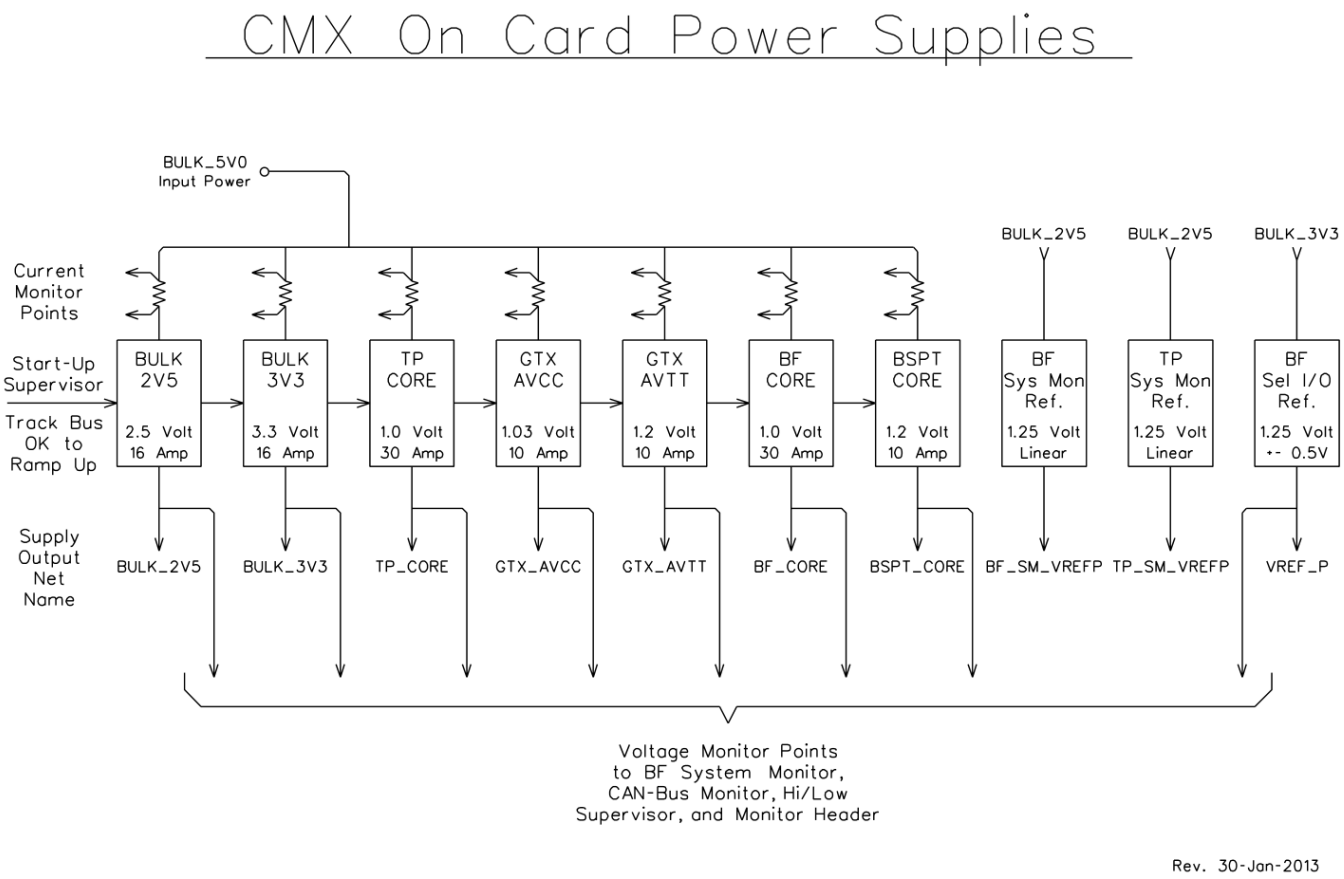

Figure 36 Circuit Diagram of the On-Card Power Supplies

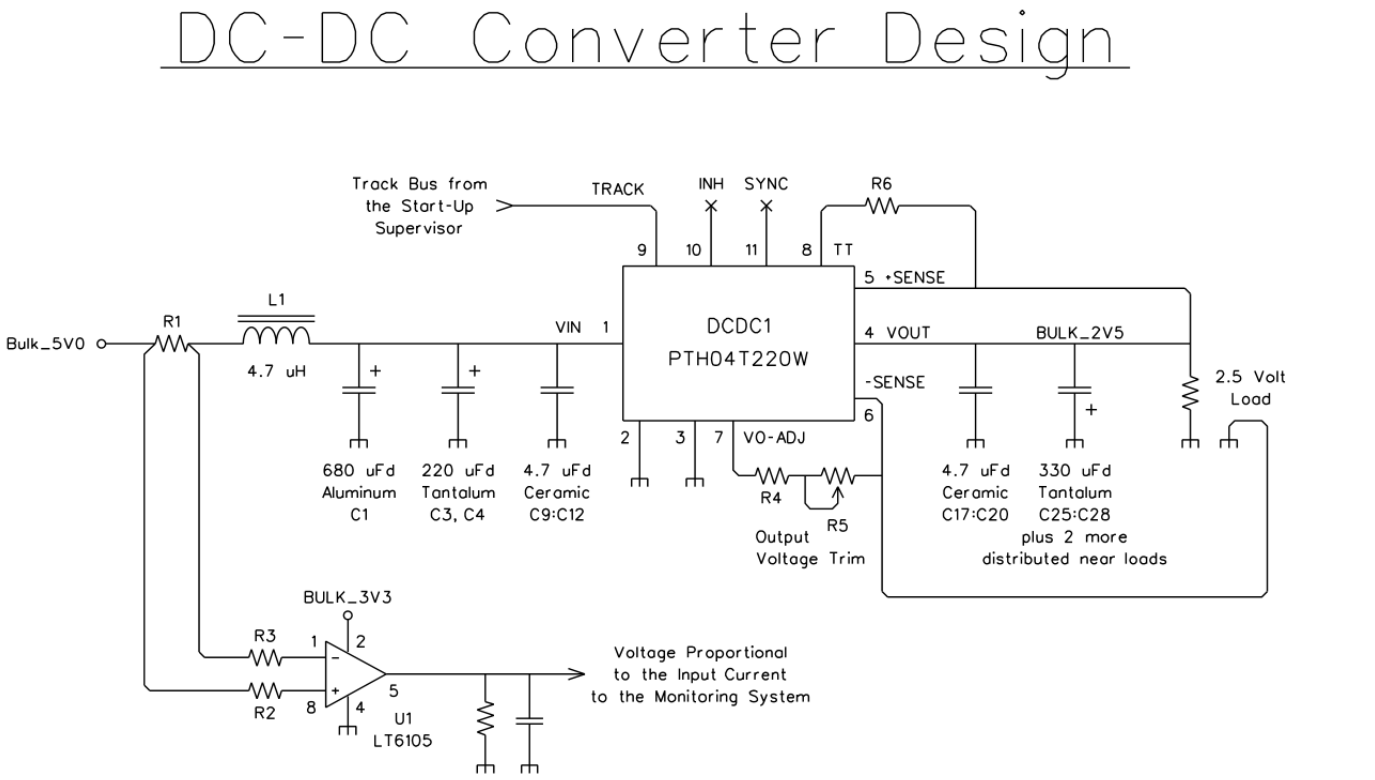

Figure 37 Circuit Diagram for the DC-DC converters

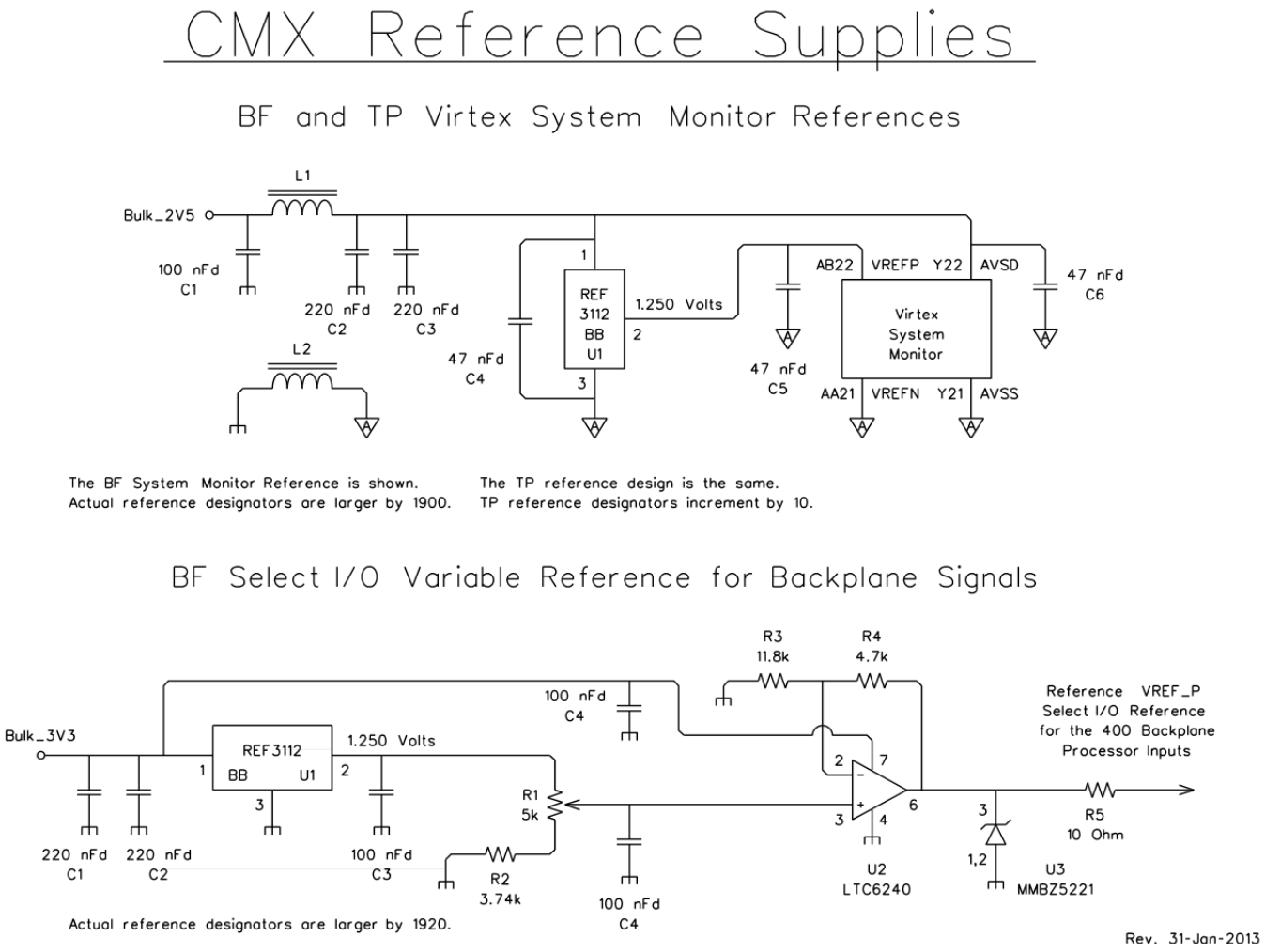

Figure 38 Circuit Diagram for the Reference Supplies

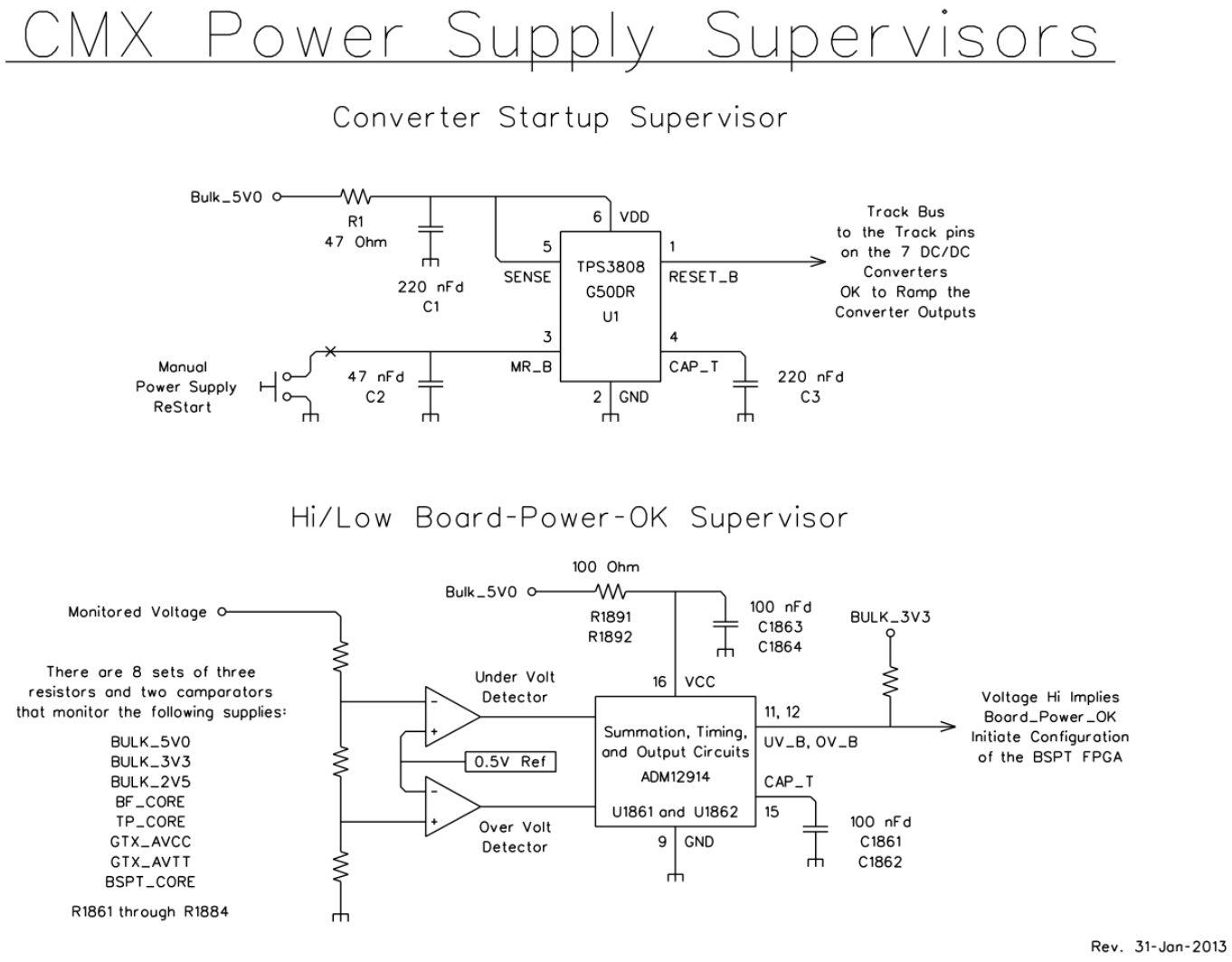

Figure 39 Circuit Diagram for the Power Supply Supervisors

A current snapshot is included above while future updates to these circuit diagrams will be in 03_5v_power_distribution.pdf, 04_on_card_power_supplies.pdf, 05_dc_dc_converter_design.pdf, 06_reference_supplies.pdf, and 07_power_supplies_supervisor.pdf located in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot is included below while future updates to this description will be in cmx_ab_power_supply_design.txt located in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

CMX On-Card Power Supply Design

Original Rev. 17-Sept-2012
Current Rev. 12-Feb-2013

The intent of this file is to describe both the functionality and the implementation details of the on board power supplies for the CMX card.

The following is the list of items that must be powered on the CMX card. The official summation of the expected current loads on the various CMX card power supplies is in another document.

List of Items on CMX that Must Be Powered:

2x	Virtex-6 FPGAs:	AUX, Core, 2.5V I/O, GTX_AVCC, GTX_AVTT, I/O Reference, System Monitor Reference
1x	Spartan XC3S400A FPGA:	AUX, Core, 2.5V I/O, 3.3V I/O
1x	System-ACE:	2.5V, 3.3V
2x	12 Channel FO Trans:	2.5V, 3.3V
3x	12 Channel FO Receiver:	2.5V, 3.3V
4x	"G-Link" FO Transmittr:	3.3V
1x	Compact Flash Module:	3.3V
39x	CMOS<->LVDS Transceiver:	3.3V
24x	2.5V<->3.3V Translator:	2.5V, 3.3V
3x	VME Bus Interface:	3.3V
	CAN-Bus Processor and I/F	5.0V
?x	Logic Chips e.g. DTACK_B	5.0V

List of Power Supply Requirements and Permissions:

- All of the supplies should ramp up together to prevent powering of buses through I/O pins.

- The power supplies must meet the ramp time requirements of the Xilinx FPGAs.

- The high speed serial I/O analog supplies for the Virtex parts must meet the Xilinx specified noise requirements and be separate from other loads.

- The FPGA AUX and I/O supplies may be shared with other loads just as long as these power buses meet certain noise requirements.

- When OFF the 2.5 Volt and 3.3 Volts supplies to the

MiniPOD fiber optic components must fall to within 50 mV of ground. If they do not fall to < +50 mV then the module may fail to start up the next time that it is powered up.

List on CMX On-Card Power Supplies Showing their Converter-Name = Power Bus Net-Name, Loads, Voltage, and Current:

Power Bus Converter Name	Loads Supplied by this Converter		Current Capability
Bulk_2V5	all 2.5V logic, Virtex-6 VCCAUX, all Virtex I/O banks, and some Spartan I/O Banks		16 A
Bulk_3V3	all 3.3V logic, some Spartan I/O Banks, and Spartan VCCAUX		16 A
BF_Core	Base Function Virtex-6 Core	1.000 V nom	30 A
TP_Core	TP Virtex-6 Core	1.000 V nom	30 A
GTX_AVCC	GTX Transceiver AVCC	1.030 V nom	10 A
GTX_AVTT	GTX Transceiver AVTT	1.200 V nom	10 A
BSPT_Core	Board Support Spartan Core	1.200 V nom	10 A
BF_IO_REF	Reference for the 400 backplane signals e.g. 0.75 to 1.75V Adjustable i.e. 2.5V divided by 2 +- 0.5V		Analog
BF_SM_REF	Reference for the System Monitor in the Base Func FPGA 1.250 Volt fixed		Analog
TP_SM_REF	Reference for the System Monitor in the TP FPGA 1.250 Volt fixed		Analog

Notes on the Selection of these Supplies and Power Buses:

- The GTX_AVCC and GTX_AVTT supplies will require converter output filtering (beyond the normally required capacitor bank) to meet the noise requirements for these buses.
- The GTX_AVCC and GTX_AVTT supplies are shared between the Base Function and TP Function FPGAs. This will

require very careful layout to meet noise and voltage tolerance requirements at both loads.

- The GTX_AVCC and GTX_AVTT converters could perhaps have been 6 Amp modules (instead of the selected 10 Amp modules) but they would have been at a 60% limit when running with the TP Function, and these supplies must be very quiet, and it appears that the 10 Amp module design is quieter then the 6 Amp design. Clearly 10 Amps is more than adequate when running only the Base Function.

- The Board Support Core supply clearly could have been a 6 Amp module but using a 10 Amp module saves on the overall part types count for this card.

Functional Description of the Power Supply System on the CMX Card:

1. All power to the CMX card come from the backplane +5 Volt supply that is received on the 3 pin power connector J9. As soon as the backplane +5 Volt power comes onto the CMX card it passes through a 20 Amp main power fuse. The card side of this fuse includes a Transient Voltage Suppressor to help protect circuits on the CMX card from spikes on the +5 Volt supply.

   The principal consumer of the +5 Volt backplane input power is the 7 DC/DC converters that are located along the top edge of the CMX card. The backplane +5 Volt power is used directly by only a few other circuits on the CMX card which include: the CAN-Bus monitoring system, a small part of the VME-- interface, and parts of the supervisor circuits for the 7 DC/DC converters. There are separate 3 Amp fuses to help protect the +5 Volt distribution to these circuits.

   The CMX card makes no connection to the backplane +3.3 Volt supply.

2. There is a delay between when the CMX card first senses that it has valid +5V backplane power and when it begins ramping up the output voltage of its 7 DC/DC Converters. The backplane input power monitoring and DC/DC converter ramp up delay is provided by a Texas Instruments TPS-3808 Power Supervisor circuit U1851.

   The TPS-3808 provides a 4.65 Volt under-volt lock out on the operation of the DC/DC converters. The delay from when the backplane input power is > 4.65V until the start of the DC/DC converter output ramp is about 1.2 seconds.

Although we do not plan to include it in the production build of the CMX cards, pads have been provided on the CMX for a "power re-start switch" to aid in the testing of the card.

3. Once enabled all DC/DC converter output voltages will ramp up in sync on a volt per volt bases and at controlled ramp rate. The 1.0 Volt converters reach their nominal output in about 8 msec. The 3.3 Volt converter reaches its nominal output in about 40 msec. The Xilinx DC Specifications Manual calls for a Ramp Time between 0.20 and 50.0 msec.

   The DC/DC converters use remote sensing to control their output voltage at the load point. The remote sensing also reduces the problems of regulating the converter's output voltage based on noisy signals immediately adjacent to the converter itself.

   The DC/DC converters include ample bulk ceramic, aluminum and tantalum capacitors on there power input lines. The high input switching currents (at a nominal frequency of 300 kHz) will flow mainly in these capacitors. This switching noise is somewhat isolated from the ground plane by slices in the ground plane that restrict the path of these switching currents. The converter inputs are isolated from the backplane +5 Volt power by high current 4.7 uH chokes. Further but limited isolation of the input switching noise is provided by the 5 or 10 mOhm current measuring resistor in series with each DC/DC converter input and by the main backplane +5V fuse.

   The basic circuit layout of all 7 DC/DC Converters is the same. The details of the components used with each converter are shown in a table later in this document.

   All 7 converters include a 3 turn output voltage trim pot with an adjustment range of about +/- 5%. Without such a trim the initial +/- 3% calibration of the supplies is only marginally good enough.

   The Topological Core supply converter includes two jumpers to disable this supply on boards that do not include the TP FPGA.

   The GTX_AVCC and GTX_AVTT supplies include a separate stage of output LC filtering in order to meet the strict low noise requirements on these power buses. The BF_FPGA and TP_FPGA share common DC/DC converters for these supplies but each FPGA has its own LC filter on them.

4. The CMX card includes under-Volt / over-Volt monitors on its 8 basic power supply voltages. This monitoring is done with Analog Devices ADM12914-2 supervisor chips U1861 and U1862. These 8 supply voltages are tested at about the +-5% tolerance level.

   When all 8 voltages are within 5% of their target values, and have remained within tolerance for about 1 second, then the "Board_Power_Good" signal is asserted. Assertion of the Board_Power_Good signal causes a front panel LED to illuminate and causes the configuration of the Board Support Spartan 3A FPGA.

5. The CMX card's power system provides monitoring of the input current to each DC/DC Converter. This will allow us to monitor the CMX card's power consumption at the 5% accuracy level. Monitoring the DC/DC converter output current is more difficult as it would require compensating the converter's servo loop for the additional pole caused by the added RC circuit within its feedback loop.

   DC/DC converter input current monitoring is accomplished with input series resistors R1501, R1551, ... which are either 5 mOhm or 10 mOhm depending on the DC/DC converter 4 terminal Kelvin resistors and Linear Technology type LT6105 high-side sense amplifiers U1501, U1551, ...

   The detailed component values that are used in each of the 7 current monitors and their scaling factors are shown in a table later in this document.

6. The CMX card's power system includes connector J13 that allows one to check all of the voltages and currents on the CMX card using a DVM without needing to probe various hard to locate test points on the card. This is a convenient way to both check that the power system on the card is operating correctly and to confirm that the CAN-Bus based and the Virtex System Monitor based readouts are reporting accurate data.

   A table later in this document shows the pinout of the J13 power system test connector.

Part Types Used in the CMX On-Card Power Supplies:

To help eliminate assembly errors there is a strong desire to control the number of types of components that are used on the CMX card. This design technique will be followed

in the power supply section of the CMX card. The main components that will be used in the power supply section of the CMX are the following:

Power Trends

Part Number	V In	V Out	I Out	Foot Print
PTH04T240W	2.2-5.5V	0.69-3.6 V	10 Amp Max	EAY R-PDSS-T11
PTH04T220W	2.2-5.5V	0.69-3.6 V	16 Amp Max	EBP R-PDSS-T11
PTH05T210W	4.5-5.5V	0.70-3.6 V	30 Amp Max	ECP R-PDSS-T14

CMX will use the through hole version of these supplies so that we have the possibility to replace them in house if necessary.

DC/DC Converters

10 Amp DC/DC Converter with through hole pins
TI Part No. PTH04T240WAD DK Part No. 296-21793-ND about $21 ea

16 Amp DC/DC Converter with through hole pins
TI Part No. PTH04T220WAD DK Part No. 296-21401-ND about $25 ea

30 Amp DC/DC Converter with through hole pins
TI Part No. PTH05T210WAD DK Part No. 296-20425-ND about $41 ea

High Current Filter Inductor

4.7 uH Inductor 15.5 Amp SMD
Wurth Part No. 7443320470 DK Part No. 732-2142-1-ND about $3.38 each

Current Measurement Resistor 4 Wire

5 mill-Ohm 4 terminal resistor Ohmite Part No. FC4L110R005FER
DK Part No. FC4L110R005FERCT-ND about $2.65 each

Overall Start-Up Supervisor: TI TPS 3808 TPS3808G50DBVR
SOT-23-6 case DK Part No. 296-17196-6-ND $1.50 ea

Qual Hi/Low Voltage Monitors: AD ADM12914-2 (non-latched)
AD Part No. ADM12914-2ARQZ
QSOP-16 3.90mm wide DK Part No. ADM12914-2ARQZ-ND $6.28 ea

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Hi-Side Sense Amps:  LT  LT6105              LT6105HMS8#PBF
  MSOP-8  TSSOP-8  3.00mm wide   DK Part No. LT6105HMS8#PBF-ND   $2.86 ea


Reference  1.25V Fixed:  TI     REF3112AIDBZT
  SOT-23-3    DK Part No. 296-18518-6-ND   $2.50 ea


Op-Amp for the 0.75 to 1.75V Adjustable Reference Supply:
LTC6240     LTC6240HVIS8#PBF     SOIC-8   3.90mm wide
DK Part No. LTC6240HVIS8#PBF-ND   $3.40 ea


Trim Pots   Copal model SM-43  Top Adjust 5 Turn  500  5k  20k  Ohm


Tantalum Capacitors:

In the 10 Volt rating  you can get the T520 Kemet Tantalum capacitors
with ESR as low as 18 mill-Ohm  in the "D" case for about $???? each in
500
                  25 mill-Ohm  in the "D" case for about $0.87 each in
500

             Description:  220 uFd  10V  25 mOhm ESR  "D" Case  Tantalum
Cap
  Manufacturer's Part No:  Kemet No. T520D227M010ATE025
        Digi-Key Part No:  399-4046-2-ND
       Quantity to Order:
                   Price:  $0.87 each in quantity of 500


Aluminum Electrolytic

             Description:  680 uFd  16V  80 mOhm ESR  "G" Case  Aluminum
Cap
  Manufacturer's Part No:  Panasonic No. EEE-FK1C681GP
        Digi-Key Part No:  PCE4316TR-ND
       Quantity to Order:
                   Price:  $0.39 each in quantity of 500



Power Requirements Partial Summary:
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      Bulk_2V5

      Bulk_3V3

      For the Virtex 6 parts  (2 of them)  assume all 2.5V I/O:

         VCCINT    1.000 V nominal    0.950 V min   1.050 V max
```

```
                about 4.5 A Quiescent

      VCCAUX    2.500 V nominal    2.375 V min   2.625 V max
                about 0.3 A Quiescent
                use Bulk_2V5 ?

      VCCO      2.500 V nominal    2.375 V min   2.625 V max
                about  3 mA Quiescent (per bank ?)
                use Bulk_2V5 ?

      Reference supply for receiving the 400 backplane lines.
      The DC Specifications Manual says that there is only a
      10 uAmp per pin load on this supply - it really is a
      reference supply.

      Reference supply for the Virtex 6 System Monitor.
      This is a  1.250 Volt reference at 50 uAmp.  Parts like
      a REF3012 or REF3112 or MAX6018 are good.  The AVdd supply
      to the FPGA's System Monitor is just filtered VCCAUX and
      it requires about 12 mAmp.  See the System Monitor book
      page 12 and 46.


      GTX  MGTAVCC   1.030 V nominal    1.000 V min   1.060 V max
                     about 56 mA per transceiver
                     about 1.6 Amps for 24 + 2  Base Function
                     about 3.6 Amps for 24+36+4 Base and TP Function
                     +/- 2.9% set point

      GTX  MGTAVTT   1.200 V nominal    1.140 V min   1.260 V max
                     about 56 mA per transceiver
                     about 1.6 Amps for 24 + 2  Base Function
                     about 3.6 Amps for 24+36+4 Base and TP Function


   For the Spartan 3a Board Support FPGA  XC3S400A in the
   FG400/FGG400 package  will have mixed 2.5V and 3.3V I/O:

      VCCINT    1.200 V nominal    1.140 V min   1.260 V max

      VCCAUX    2.500 V or 3.300 V nominal    2.250 V min   2.750 V max
                                         or  3.000 V min   3.600 V max
                This part can use either 2.5V or 3.3V VCCAUX.
                We are using 3.3V VCCAUX so that BSPT JTAG is 3.3V
                Spartan 3A BSPT VCCAUX power comes from BULK_3V3.

      VCCO      2.500 V and 3.300 V nominal   1.100 V min   3.600 V max
                use Bulk_2V5 and Bulk_3V3



Components Requiring +5V Power:
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There are a few components on the CMX card that will require normal old +5 Volt power. These components include:

DTACK_B driver chip	probably 74F38
HW I/O Enable Control chips	probably 74F38
CAN-Bus Interface chip	PCA82C250
CAN-Bus Microprocessor	MB90F594
4 MHz Xtal Osc for CAN Microprocessor	
Temperature Sensors	LM35
Diode IC Temp Sensor chip	MAX1668
RS-232 Transceiver MAC3232	MAX3232EUE+
7 Geo Adrs for 2.5V to 5V	??
VME Data Read from CAN Bus uPROC 5V to 2.5V	??
IRQs to the from CAN Bus uPROC ?v to 5V	??
Power Supply Startup Supervisor	

Power Entry and +5V Power Net Names:

The CMX receives +5V DC power and it is immediately routed to a 20 Amp fuse of holder and type ??. This is net BPLN_5V0.

From the 20 Amp fuse there is a Transit Voltage Suppressor to Ground. This is net BULK_5V0.

The +5V out of the 20 Amp fuse then:

- Directly feeds all 7 of the DC/DC power converters

- Feeds a 3 Amp SMD fuse that powers the +5V CAN-Bus Interface chip in the lower right-hand corner. This is net BULK_5V0_SE.

- Feeds a 3 Amp SMD fuse that powers the +5V Logic, e.g. DTACK_B driver in the upper right-hand corner. This is net BULK_5V0_NE.

- Feeds a 3 Amp SMD fuse that powers the CAN-Bus monitoring system chips in the lower left-hand corner, feeds the 3 low current reference supplies in the power supply section of the CMX card, and feeds the sense and Vdd of the TPS-3808 Power Supply Supervisor. This is net BULK_5V0_FE.

- +5V Power Net Names

Net Name	Function

BK_PLN_5V0	+5V Power Entry from the J9 Power Connector
BULK_5V0	20 Amp Fused Bulk +5V Power, e.g. DC/DC Convter
BULK_5V0_SE	3 Amp Fused power for the Lower Rear Corner SE
BULK_5V0_NE	3 Amp Fuses power for the Upper Rear Corner NE
BULK_5V0_FE	3 Amp Fused power for the Front Edge

Design of the Power Trends DC/DC Converters:

There are 7 Power Trends DC/DC converters on the CMX card:

Supplies Power Bus	Output Voltage	Current Capacity	Power Trends Model Number
Bulk_2V5	2.500 V	16 A	PTH04T220WAD
Bulk_3V3	3.300 V	16 A	PTH04T220WAD
BF_Core	1.000 V	30 A	PTH05T210WAD
TP_Core	1.000 V	30 A	PTH05T210WAD
GTX_AVCC	1.030 V	10 A	PTH04T240WAD
GTX_AVTT	1.200 V	10 A	PTH04T240WAD
BSPT_Core	1.200 V	10 A	PTH04T240WAD

We want to provide about a +-5% adjustment range on all 7 of these supplies to take care of their initial calibration error (about +- 2%) and the 1% tolerance resistors in their feedback networks. The output voltage trim resistor can be a one-turn pot. One-turn will give about a 1% change in 30 degrees.

The following table list the specifications of the various components in each type of supply.

Component	16 Amp PTH04T220WAD 2.50V & 3.30V	30 Amp PTH05T210WAD 1.000V	10 Amp PTH04T240WAD 1.03V and 1.20V
Cin Total Min	330 uFd Min. 680 uFd Recom	1000 uFd Min. 2000 uFd Recom	220 uFd Min. 680 uFd Recom
Cin Al	1x 680 uF 16V F	2x 680 uF 16V F	1x 680 uF 16V F
Cin Tant	2x 220 uF 10V D	6x 220 uF 10V D	2x 220 uF 10V D
Cin Cerm	4x 4.7uF 16V 85	8x 4.7uF 16V 85	4x 4.7uF 16v 85

Cin Installed	1120 uFd	2680 uFd	1120 uFd
Cout Total Min	220 uFd Min.	470 uFd Min.	220 uFd Min.
Cout Total Max	-	12000 uFd Max.	10000 uFd Max.
Cout Tant	4x 330 uF 6V3 D or 6x 220 uF 10V D	6x 330 uF 6V3 D	6x 330 uF 6V3 D 6x 330 uF 6V3 D
Cout Cerm	4x 4.7uF 16v 85	8x 4.7uF 16v 85	4x 4.7uF 16v 85
Cout @ Load	2x 330 uF 6V3 D or 3x 220 uF 10V D	4x 330 uF 6V3 D	Output Filter Output Filter
Cout Installed	1980 uFd 1980 uFd	3300 uFd	1980 uFd
Min Cout for Rtt=0	1100 uFd	2350 uFd	1100 uFd
Resistor Rtt	0 Ohm	0 Ohm	0 Ohm
Vout Rset	1.21k Ohm @3V3 2.37k Ohm @2V5	63.4k Ohm @1V0	18.86k Ohm @1V03 12.1k Ohm @1V20
Rset Slope	1.15kOhm/V @3V3 2.30kOhm/V @2V5	215kOhm/V @1V0	54kOhm/V @1V03 30kOhm/V @1V20
10% of Vout is	0.33 Volt @3V3 0.25 Volt @2V5	0.10 Volt @1V0	0.103 Volt @1V03 0.120 Volt @1V20
--> Rset Var	380 Ohm @3V3 575 Ohm @2V5	21.5k Ohm @1V0	5.56k Ohm @1V03 3.6k Ohm @1V20
Vout Rset Var	500 Ohm @3V3 500 Ohm @2V5	20.0k Ohm @1V0	5.0k Ohm @1V03 5.0k Ohm @1V20
Vout Rset Fix	953 Ohm @3V3 2.10k Ohm @2V5	53.6k Ohm @1V0	16.5k Ohm @1V03 9.76k Ohm @1V20
Track Pin Bus	9	14	10
Inh/UVLO Float	10	1	11
Sync Float	11	-	1
Vin	1	2,6	2

Ground	2,3	3,4,7,8	3,4
Vout	4	5,9	5
Vo Adjust	7	12	8
+ Sense	5	10	6
- Sense	6	11	7
Trans Resistor	8	13	9
Notes:	-	Rset to Gnd	Output Filter

The 10 Amp 4T240 and the 16 Amp 4T220 have the same relationship between the value of the Vo Rset resistor value and the output voltage. The 30 Amp 5T210 has a different relationship between Rset and the output voltage and it requires significant higher value resistors for a 1 Volt output than the lower current models.

On the DC/DC converters, the Inhibit/Under_Volt_Lockout pins should be floated, the Synchronization pins are also floated on all 7 converters.

It is only the Track pin that is used to manage these supplies. We need to be able to isolate the Track pin on the TP_CORE supply.

Include an rc0603 in the layout for the connection to the "Turbo-Trans" pins on all converters just in case we need something other than zero Ohms Rtt.

We need to be able to disable the TP_CORE converter on CMX cards that do not include the Topological FPGA. The TP_CORE converter is disabled by installing jumper JMP78 that ties this converter's Inhibit/Under_Volt_Lockout pin to ground and by removing jumper JMP79 which disconnects this converter's Track pin from the Track bus that connects the other 6 DC/DC converters.

The ground plane under each DC/DC converter and its input and output capacitor banks will be slit to control and isolate the ground noise from the large circulating currents generated by these converters.

LC Filter Design:

Order of magnitude, at what frequency do the LC filters become resonant and not effective ? The inductor is about 5 uH. The capacitor is about 1000 uFd. This gives a series resonant at about 2252 Hz.

For the Wurth 7443340470 4.7uH SMD Inductor
Maximum Current is 7.5 Amps.
The DC resistance of this choke is about 12.4 mOhm.
Estimated AC resistance of this choke at 2 kHz is about ?? mOhm.

For the Wurth 7443320470 4.7uH SMD Inductor
Maximum Current is 15.5 Amps.
The DC resistance of this choke is about 6.35 mOhm.
Estimated AC resistance of this choke at 2 kHz is about ?? mOhm.

The switching frequency of these DC/DC converters is typically 300 kHz.

Current Sense Circuits:

Each of the 7 DC/DC converters will have a Kelvin current sense resistor and a "high-side" current sense circuit at its input.

				Full Load		
Converter	Output Voltage	Max. Output Currnt	Max. Output Power	+5 Volt Input Current	Sense Resist V Drop	Required Gain to 1.000 Volt
Bulk_2V5	2.500 V	16 A	40.0 W	8.0 A	40 mV *	25.0
Bulk_3V3	3.300 V	16 A	52.8 W	10.6 A	53 mV *	18.9
BF_Core	1.000 V	30 A	30.0 W	6.0 A	30 mV *	33.3
TP_Core	1.000 V	30 A	30.0 W	6.0 A	30 mV *	33.3
GTX_AVCC	1.030 V	10 A	10.3 W	2.1 A	21 mV #	47.6
GTX_AVTT	1.200 V	10 A	12.0 W	2.4 A	24 mV #	41.7
BSPT_Core	1.200 V	10 A	12.0 W	2.4 A	24 mV #	41.7
		+		+		
Totals:			187 Watts	37.5 Amps		

* ---> 5 mOhm Sense Resistor

\# ---> 10 mOhm Sense Resistor

Converter	Sense Resist V Drop	Required Gain to 1.000 Volt	Required Rin for this Gain with 4.99k Rout	Nearest Standard Value	Result 1.0 V Out Equals
Bulk_2V5	40 mV *	25.0	199.6 Ohm	200 Ohm	8.016 Amps
Bulk_3V3	53 mV *	18.9	263.5	261	10.46
BF_Core	30 mV *	33.3	149.7	150	6.012
TP_Core	30 mV *	33.3	149.7	150	6.012
GTX_AVCC	21 mV #	47.6	104.8	105	2.104
GTX_AVTT	24 mV #	41.7	119.7	121	2.425
BSPT_Core	24 mV #	41.7	119.7	121	2.425

- It's assumed that the Virtex-6 System Monitor will be used to readout these currents. The analog inputs to the System Monitor are *basically* 1.000 Volt full scale and 10 bit ADC. Besides the 1 dedicated analog input, there are 16 mixed use pin analog inputs. On CMX we will have access to 12 of the mixed use pin analog inputs.

- The LT6105 high-side current sense amplifiers will be powered from BULK_3V3 power and will all use 4.99k Ohm output resistors. Because the output of these high-side amps could swing higher than +2.5V a series resistor of 1k Ohm is used between the current sense amp and the Virtex-6 System Monitor analog inputs. 10 nFd low-pass filter capacitors are used after the 1k Ohm resistors.

- Note that both Differential Analog routing and a separate Analog Ground are needed in the pcb layout of the System Monitor.

- The one dedicated analog input to the System Monitor has an input current of 1 uAmp. The mixed use pin analog inputs have an input current of 10 uAmps.

Reference Supplies and Their Design:

- The Reference Inputs to the Virtex-6 System Monitor are high impedance. These are pins Vrefp and Vrefn. The voltage between these pins is to be 1.250 Volts. The Reference supply current draw is 100 uAmp maximum. Pin Vrefn must be in the range of -50 mV to +100 mV of ground.

- In the System Monitor circuit there is an inductor to isolate the CMX GROUND plane from the System Monitor AVSS "analog ground". There is also an inductor to isolate the BULK_2V5 supply from the System Monitor AVDD pin. Page 46 of the System Monitor reference book indicate the requirements for these inductors. They have a reactance of about 500 Ohms at 100 MHz. This works out to about 1 uH.

- The Select I/O Reference Supply needs to be able to provide 10 uAmp of current per pin. There are 24 reference pins that must be supplied on the Base Function FPGA for the I/O Banks that handle the 400 Processor inputs. This means that the 0.75 to 1.75 Volt Reference Supply needs to provide 240 uAmp of current.

- Xilinx wants a 22 nFd to 470 nFd capacitor on each of the reference pins. With 24 reference pins on the Base Function FPGA this implies that the 0.75 to 1.75 Volt Reference Supply needs to work into a 0.528 uFd to 11.28 uFd capacitive load.

Physical Layout Location of the DC/DC Converters:

- The DC/DC Converters are located along the top edge of the CMX circuit board.

- Working from West to East the converters are:

  Bulk_2V5, Bulk_3V3, TP_Core, GTX_AVCC,
  16 Amp 16 Amp 30 Amp 10 Amp

  followed by

  GTX_AVTT, BF_Core, BSPT_Core
  10 Amp 30 Amp 10 Amp

Design of the Voltage Monitor Circuits:

The CMX card includes Under-Volt / Over-Volt monitors on 8 of its power supplies. When all 8 of these supplies are operating within their required range then the BOARD_POWER_GOOD signal is asserted high. There is a delay of about 1 second between all 8 monitored supplies becoming stable within their required operating range and the assertion of the BOARD_POWER_GOOD signal.

Analog Devices type AD12914-2 quad voltage monitors are are used to generate the BOARD_POWER_GOOD signal. All signals sent to these voltage monitors are compared to an internal 500 mV reference.

A separate resistor divider on each monitored supply provides the comparator input signals to the voltage monitor. The standing current in these resistor dividers must be significantly greater than the 10 nA input current to the comparators. The CMX card will use a standing current of about 100 uA in its resistor dividers, i.e. swamp the input current but still avoid and heating of the resistors.

The resistor values selected for these dividers sets the "OK" operating range for each supply. On all critical supplies, e.g. GTX_AVCC, Virtex CORE, the voltage monitor "OK" operating range will be narrower than the allowable range specified by the manufacturer of the components that use the associated power supply.

The design of these resistor dividers is the following:

Supply	Under-Volt Limit	Over-Volt Limit	Static Current uAmps	Rx Top Ohms	Ry Mid Ohms	Rz Gnd Ohms
				R1861	R1862	R1863
Bulk_2V5						
				R1864	R1865	R1866
Bulk_3V3						
				R1867	R1868	R1869
TP_Core						
				R1870	R1871	R1872
GTX_AVCC	0.95	1.05	500	947.4	100.3	952.4
	0.952	1.054	510	931	100	931

	R1873	R1874	R1875
GTX_AVTT			
	R1876	R1877	R1878
BF_Core			
	R1879	R1880	R1881
BSPT_Core			
	R1882	R1883	R1884
Bulk_5V0			

Voltage and Current Monitoring Points:

The following 3 tables list the various Voltage and Current Monitoring Points that are on the CMX card.

CAN-Bus Micro-Processor Analog Input
Power Bus Voltage Monitoring

CAN-Bus Micro-Processor Analog Input	Power Bus Voltage Monitored by this Input
AN0	BSPT_CORE
AN1	BF_CORE
AN2	GTX_AVTT
AN3	GTX_AVCC
AN4	TP_CORE
AN5	BULK_3V3
AN6	BULK_2V5
AN7	BULK_5V0

Base Function System Monitor
Auxiliary Analog Input
Power Bus Voltage and Current Monitoring

BF FPGA System Monitor Input	Power Bus Voltage or Current Monitored by this Input
SYSMON_00	pin not used for monitoring
SYSMON_01	BF_CORE Voltage
SYSMON_02	pin not used for monitoring
SYSMON_03	BF_CORE Current
SYSMON_04	GTX_AVTT Voltage
SYSMON_05	pin not used for monitoring
SYSMON_06	pin not used for monitoring
SYSMON_07	GTX_AVTT Current
SYSMON_08	GTX_AVCC Voltage

SYSMON_09	GTX_AVCC Current
SYSMON_10	TP_CORE Current
SYSMON_11	BULK_3V3 Voltage
SYSMON_12	BULK_3V3 Current
SYSMON_13	BULK_2V5 Voltage
SYSMON_14	BULK_2V5 Current
SYSMON_15	V_REFP Voltage Select I/O Ref

Power Bus Voltage and Current Monitoring Via the J13 Header Connector

J13 Pin	Monitor Connection
1	BSPT_CORE Voltage
3	BSPT_CORE Current
5	BF_CORE Voltage
7	BF_CORE Current
9	GTX_AVTT Voltage
11	GTX_AVTT Current
13	GTX_AVCC Voltage
15	GTX_AVCC Current
17	TP_CORE Voltage
19	TP_CORE Current
21	BULK_3V3 Voltage
23	BULK_3V3 Current
25	BULK_2V5 Voltage
27	BULK_2V5 Current
29	BULK_5V0 Voltage
31	V_REFP Voltage Select I/O Ref
33	not currently assigned
35	not currently assigned
37	not currently assigned
39	not currently assigned

All even pin numbers on J13 are Ground.

Appendix N: Virtex-6 Bypass Capacitors

A current snapshot is included below while future updates to this description will be in cmx_ab_fpga_bypass_caps.txt located in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
      CMX  Virtex-6 FPGA  Bypass Capacitor  Design Layout
     ------------------------------------------------------


                                        Original Rev.  22-June-2012
                                         Current Rev.  12-Feb-2013


This file gives both the background and then the full details
of the bypass capacitor design layout that is used on the CMX
card's Virtex-6 FPGAs.


Virtex-6 Bypass Capacitor Rules from Xilinx:
--------------------------------------------

Most of this information is from Chapter 2 of the, "Virtex-6
PCB Design Guide".   Stired into this will be the capacitor
requirements on the output of the DC/DC power converters that
will be used on the CMX card.

Their table 2.1 in Chapter 2 does not show the need for any
bulk or high frequency VCCAUX or VCCO bypass capacitors.
They do have VCCAUX and VCCO bypass capacitors on their
demo boards as noted below.

Chapter 2 says that as long as the plane noise is under 5%
(250 mVpp on a 2.5 Volt supply)  then the same power plane
may be used for VCCAUX and VCCO  with the Virtex-6 device.

Information about the required bypass capacitors on the
analog supplies for the high speed serial transceivers
comes from Chapter 5 of the GTX Transceiver User's Guide.



VCCINT from the CMX Base_Core and TP_Core Supplies:
---------------------------------------------------

 - Xilinx says that for the XC6VLX550T FPGA in the FF1759
   package they want  9x  330 uFd caps  on the VCCINT core
   supply pins

     By 330 uFd Xilinx means,  330 uFd  Tantalum  V-Case
     15 mill-Ohm < ESR < 40 mill-Ohm  2.5 Volt  for  VCCINT
```

T520V337M2R5ATE025

- The Xilinx ml623 demo board explicitly uses the following on its VCCINT Core supply:

  2x 330 uFd 2.5V Tant Kemet T520V337M2R5ATE025
  4x 2.2 uFd 10V X7R Kemet C0805C225K8RACTU
  8x 220 nFd 10V X7R Panisonic ECJ-0EF1A224Z

  The Xilinx ml623 demo board has a XC6LVX240T FPGA in a FFG1156 package.

- We are using a 30 Amp Power Trends PTH05T210WAD DC/DC converter to supply the VCCINT Core power. This supply has a complicated set of output capacitor requirements that depend on how good of a transient responce you want and on how much of its "Turbo-Trans" function you are using. A quality setup of this converter requires:

  Capacitors with a capacitance uFd times ESR mOhm of less than 10,000 uFd_mOhm are reqiored

  The absolute minimum capacitance is 470 uFd and the maximum capacitance is 12,000 uFd.

  The bulk of the output capacitance on the CMX will be tantalum T520 with a uFd_mOhm in the range 5,000 to 10,000 i.e. type "C" in Power Trends speak.

  Power Trends is happy with Kemet T520 series capacitors. Specifically the T520D337M006ATE015 looks good, i.e. it is 6.3V so it can also be used on the 3.3V bus and it is the standard "D" case instead of the special and expensive "V" case.

  For Cout > 2350 uFd the converter's Rtt feedback resistor can be a short.

- Remote sensing feedback from immediately under the FPGA will be needed for both the Base_Core and TP_Core supplies.

- Final Definitive VCCINT Core Bypass Capacitor Design:

  10x 330 uFd 6.3V D Case T520 Tantalum 3300 uFd total location split between FPGA and converter output.

  6x 33 uFd 10V Tant B Kemet T520B336M010ATE025

  6x 4.7 uFd 16V X7R 0805 Kemet C0805C475K4RACTU

  10x 220 nFd 10V X7R 0603 Kemet C0603C224K8RACTU

VCCAUX from the CMX BULK_2V5 Supply:

- Xilinx table 2.1 says that the XC6VLX550T FPGA in the FF1759 package needs Zero bypass capacitors on its VCCAUX supply pins.

- But the Xilinx ml623 demo board explicitly uses the following on its VCCAUX supply:

  1x 33 uFd 6.3V Tant Kemet T520B336M006ATE040
  1x 2.2 uFd 10V X7R Kemet C0805C225K8RACTU
  1x 220 nFd 10V X7R Panisonic ECJ-0EF1A224Z

- The output capacitors on the DC/DC converter for the BULK_2V5 supply are not included in this Virtex-6 VCCAUX bypass calculation.

- Final Definitive VCCAUX Bypass Capacitor Design:

  1x 33 uFd 10V Tant B Kemet T520B336M010ATE025

  1x 4.7 uFd 16V X7R 0805 Kemet C0805C475K4RACTU

  1x 220 nFd 10V X7R 0603 Kemet C0603C224K8RACTU

VCCO from the CMX BULK_2V5 Supply:

- Xilinx table 2.1 says that the XC6VLX550T FPGA in the FF1759 package needs Zero bypass capacitors on its VCCO supply pins.

- But the Xilinx ml623 demo board explicitly uses the following on its VCCO supply pins:

  1x 47 uFd 6.3V Tant Kemet T520B476M006ATE070
  1x 2.2 uFd 10V X7R Kemet C0805C225K8RACTU
  1x 220 nFd 10V X7R Panisonic ECJ-0EF1A224Z

  The VCCO caps are per I/O Bank: there are 16 sets of these 3 capacitors on the Xilinx ml623 Demo Card. 3 capacitors per I/O bank all powered from a common VCCO power supply module.

- The CMX XC6VLX550T FPGA in the FF1759 package has 21 I/O Banks. The bulk of the Select I/O pins on the CMX Virtex-6 FPGAs will be inputs. Simultaniously switched outputs on the Base Function FPGA will include:

  66 lines to the CTP outputs from I/O Banks ?? ??
  16 data lines to the On-Card-Bus from I/O Bank ??

?? lines to the Backplane LVDS cables from I/O Banks ?? ??

- The output capacitors on the DC/DC converter for the BULK_2V5 supply are not included in this Virtex-6 VCCO bypass calculation.

- Final Definitive VCCO Bypass Capacitor Design per Bank:

1x	33 uFd	10V	Tant	B	Kemet	T520B336M010ATE025
1x	4.7 uFd	16V	X7R	0805	Kemet	C0805C475K4RACTU
1x	220 nFd	10V	X7R	0603	Kemet	C0603C224K8RACTU

Select I/O Bank Reference Pin Bypass Capacitors:

- For VREF supplies they want one capacitor per pin placed as close to the pin as possible. The capacitor should be in the 22 nFd to 470 nFd range. Its purpose is to reduce the VREF node impedance. No low frequency energy is needed on VREF so no bulk capacitors are needed.

MGTAVCC from the CMX GTX_AVTT Supply:
MGTAVTT from the CMX GTX_AVTT Supply:

- These are the analog supplies for the high speed serial GTX transceivers in the Virtex-6 FPGAs.

- Although both VCCINT and AVCC are nominally 1.0 Volt separate supplies should be used for these 2 loads. (and separate planes - duh)

- The noise on the AVCC and AVTT planes must be under 10 mVpp in the 10 kHz to 80 MHz range.

- Switching regulators generally require additional filtering before their power is delivered to the GTX Transceivers.

- The AVCC and AVTT supplies need their own private plane islands which must not run under the Select I/O section of the FPGA's footprint.

- We will always be using a large enough fraction of the GTX Transceivers that it makes sense to always power both the North and South Quads.

- The minimum bypassing of the AVCC and AVTT supplies

```
  that is specified in Chapter 5 is the following:

    1x  220 nFd  0402  ceramic per power supply pin
    1x  4.7 uFd  0402  ceramic per two quads
    1x  330 uFd  bulk capacitor per supply

- The XC6LVX550T-2FFG1759C  has 9 quads.   It has:

      9 pins for AVCC_N      9 pins for AVCC_S
     13 pins for AVTT_N     14 pins for AVTT_S

- So the minimum suggested AVCC and AVTT bypassing for
  the GTX supplies is:

     On AVCC:   18x  220 nFd
                 5x  4.7 uFd
                 1x  330 uFd  bulk

     On AVTT:   27x  220 nFd
                 5x  4.7 uFd
                 1x  330 uFd  bulk

- The ml623  with its 5 Quads  used 16 bypass capacitors of
  220 nFd  on its AVCC island and 16x 220 nFd capacitors on
  its AVTT island.  Scale this up to the CMX's 9 Quads -->
  29 capacitors on each power island.

- The ml623  also used the following on both its AVCC and AVTT:

    1x   47 uFd  6.3V Tant-B "DNP"   and
    3x    1 uFd   16V X5R ceramics   and
    1x   33 uFd   16V Tant-C "DNP"   and
    1x  330 uFd   10V Tant-D "DUP"

- The intent on the CMX is to use a common GTX_AVcc supply
  and a common GTX_AVtt supply for the GTX Transceivers in
  both the Base Function and Topological Processor FPGAs.
  Remote sensing and balanced IR drop past the sense point
  will be required.  This remote sensing will need to
  compensate for the pole that it will see from the additional
  (post converter)  noise filtering that will be required.

- Final Definitive  GTX_AVCC and GTX_AVTT  Bypass Capacitor
  Design:

     On GTX_AVCC:  18x  220 nFd
                    5x  4.7 uFd
                    2x   33 uFd  bulk
                    1x  330 uFd  bulk

     On GTX_AVTT:  27x  220 nFd
                    5x  4.7 uFd
                    2x   33 uFd  bulk
                    1x  330 uFd  bulk
```

```
List of ByPass Capacitors that we will actually use on CMX_0:
---------------------------------------------------------

            Description:  330 uFd  6.3V  15 mOhm ESR  "D" Case  Tantalum
Cap
  Manufacturer's Part No:  Kemet No. T520D337M006ATE015
        Digi-Key Part No:  399-4052-2-ND
       Quantity to Order:
                   Price:  $0.84 each in quantity of 500

       In the 6.3 Volt rating  you can get the T520 Kemet Tantalum
       capacitors with ESR as low as
                   15 mill-Ohm  in the "D" case for about $0.84 each in
500
                   25 mill-Ohm  in the "D" case for about $0.80 each in
500


       33 uFd    10V  Tant  B     Kemet  T520B336M010ATE025   0.48 ea


      4.7 uFd    16V  X7R  0805   Kemet  C0805C475K4RACTU    0.10 ea

          To get 4.7 uFd in X7R  you are forced to the 0805 case.
          Going down to 10V or 6.3V does not help.  The only way to
          get 4.7 uFd in a 0603 package is to go to X5R dielectric,
          e.g.

  --> 4.7 uFd    10V  X5R  0603   Kemet  C0603C475K8PACTU    0.05 ea


      2.2 uFd   6.3V  X7R  0603     AVX  06036C225KAT2A      0.04 ea

          You can not get this in 10 V  and stay in X7R  0603


      220 nFd    10V  X7R  0603   Kemet  C0603C224K8RACTU    0.02 ea

      220 nFd   6.3V  X5R  0402   Kemet  C0402C224K9PACTU    0.01 ea

          The only 220 nFd in 0402 is X5R at 6.3V


      100 nFd    25V  X7R  0603   Kemet  C0603C104K3RACTU    0.01 ea


      100 nFd    16V  X7R  0402   Kemet  C0402C104K4RACTU    0.02 ea


       47 nFd    25V  X7R  0603   Kemet  C0603C473K3RACTU    0.01 ea
```

```
       47 nFd    25V  X7R  0402   Kemet  C0402C473K3RACTU    0.04 ea

       10 nFd    25V  X7R  0402   Kemet  C0402C103K3RACTU    0.01 ea


Development Information:
------------------------

 - Parts from earlier work:

      220 nFd   10V  Y5V  0402  Panasonic  ECJ-0EF1A224Z     DK=N
      220 nFd   10V  X7R  0402  10%   TDK  C1005X7R1A224K    D-K 445-5938-
2-ND

        1 uFd     V       0402  Panasonic  ECJ-0EB0J105M
        1 uFd     V       0603  Panasonic  ECJ-1VB1E105K

      4.7 uFd     V       0402  Taiyo      AMK105BJ475MV-F   DK=Y
      4.7 uFd     V       0603  Taiyo      LMK107BJ475KA-T   DK=Y

      4.7 uFd   10V  X5R  0603  Kemet      C0603C475K8PACTU  DK=Y
      4.7 uFd  6.3V  X5R  0603  Johnson    6R3R14X475KV4T

      330 uFd     2.5 V   Tantalum  V7343   Kement  T520V337M2R5ATE025


 - Some More Xilinx Suggested Bypass Capacitors:

      220 nFd  6.3V  X5R  0402     AVX   04026D224KAT2A      DK=Y
               6.3V  X5R  0402   Kemet   C0402C224K9PAC      DK=Y
               6.3V  X5R  0402  Murata   GRM155R60J224KE01   DK=?

       10 uFd   10V  X5R  1206     AVX   1206YD106KAT2A      DK=Y
                10V  X5R  1206   Kemet   C1206C106K4PAC      DK=Y
                10V  X5R  1206  Murata   GRM31CR61C106KA88   DK=N
```

Appendix O: Geographical View of Power Usage

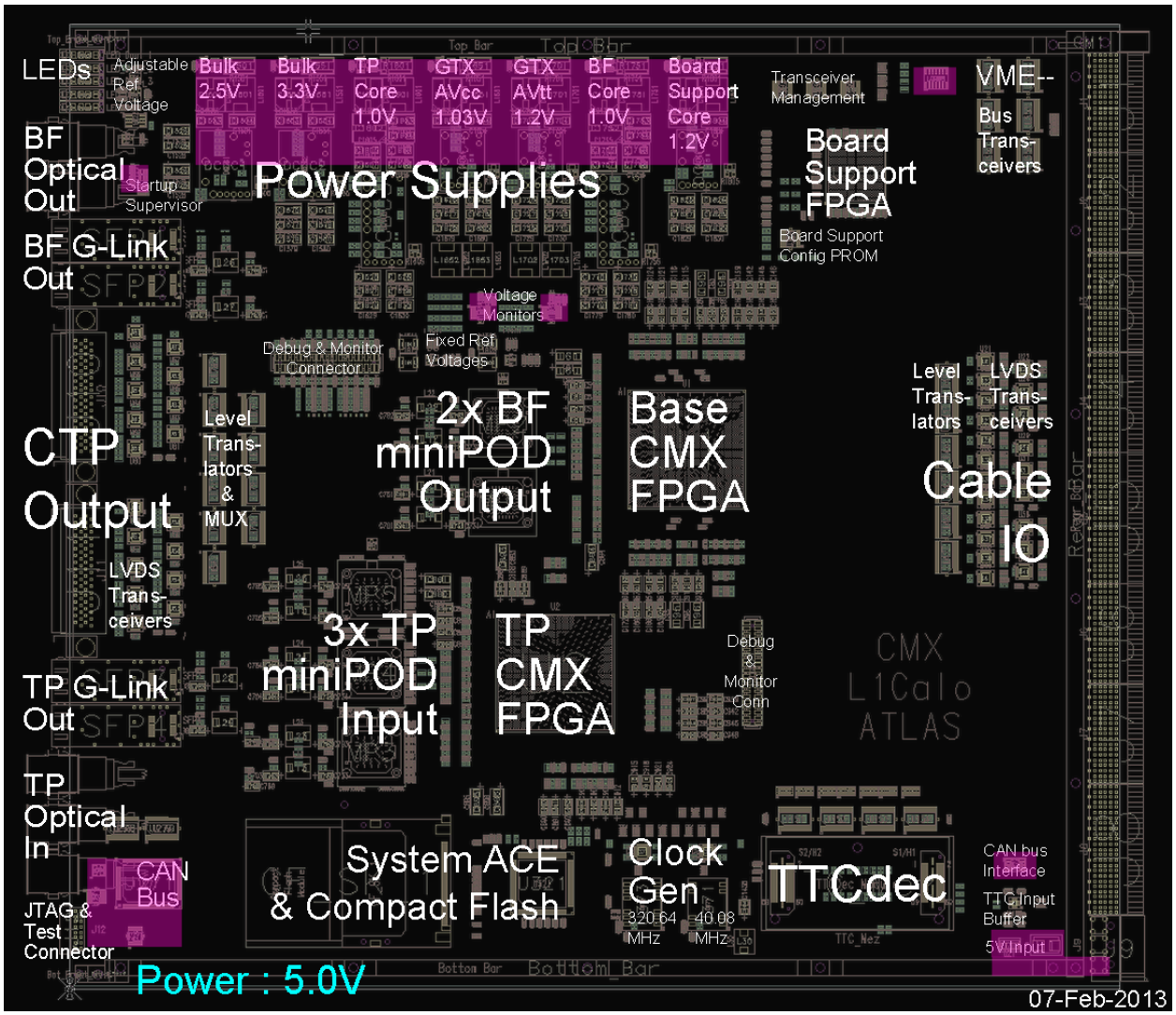

Figure 40 Power: 5.0V Input power

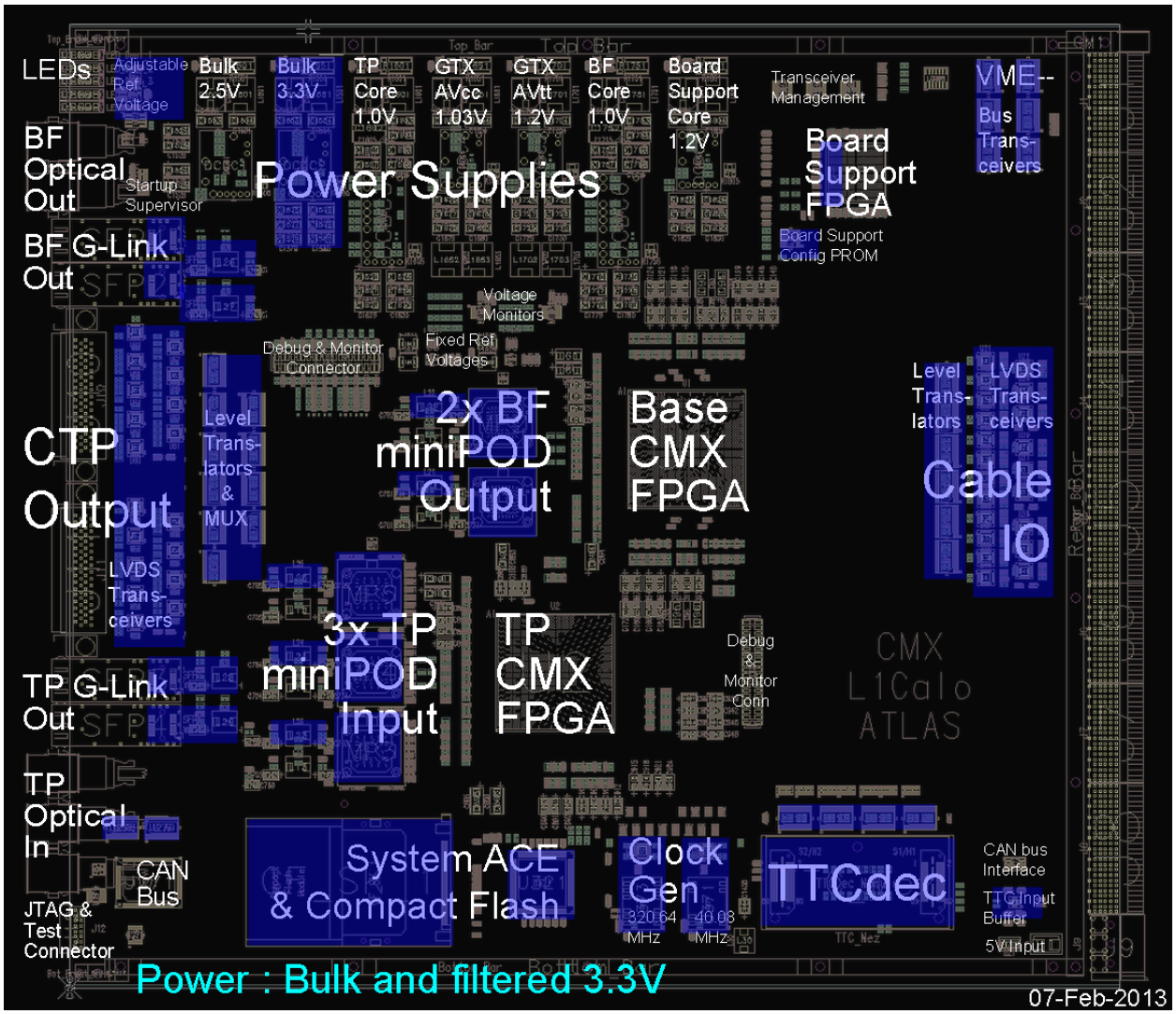

Figure 41 Power: Bulk and Filtered 3.3V

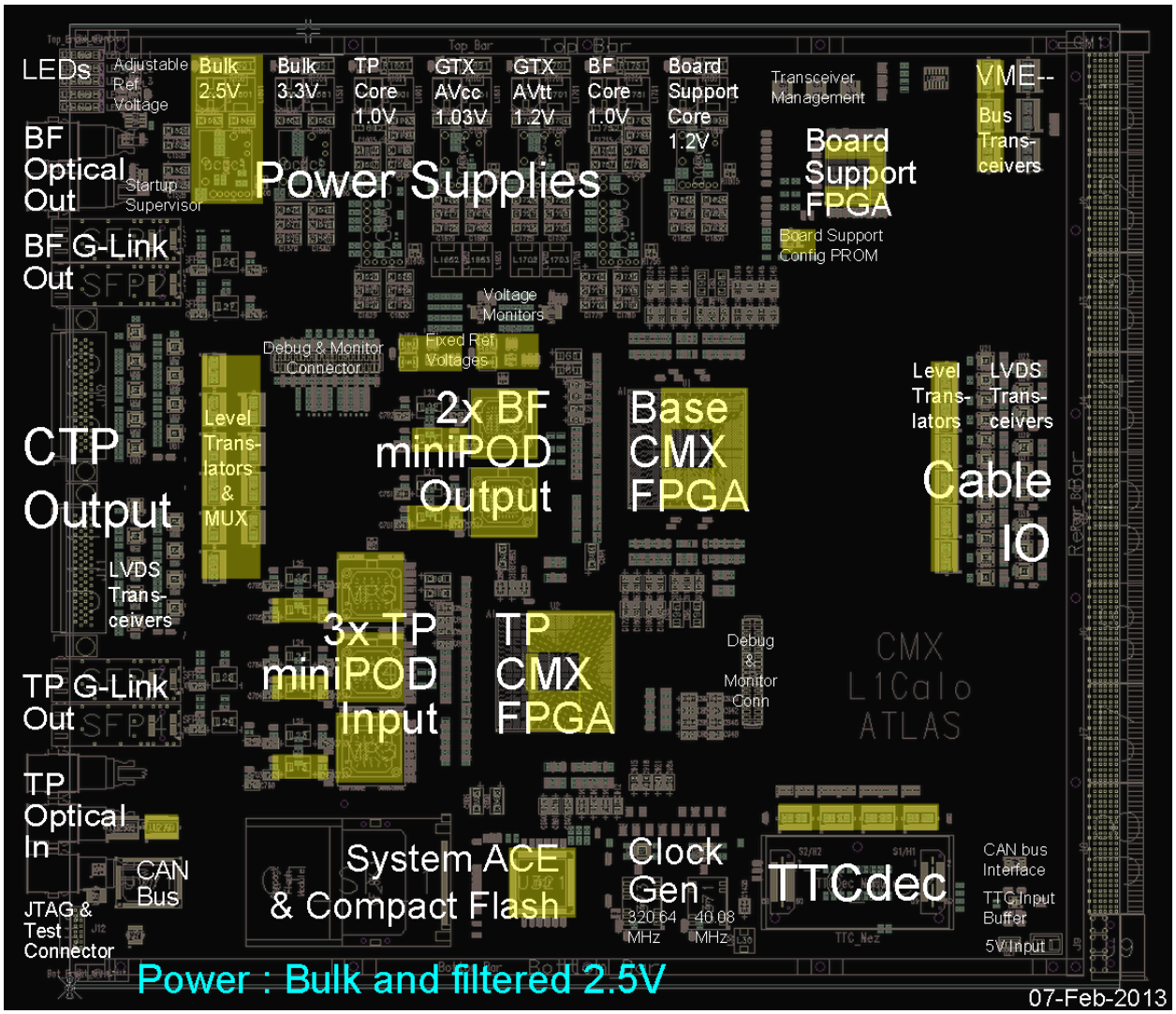

Figure 42 Power: Bulk and Filtered 2.5V

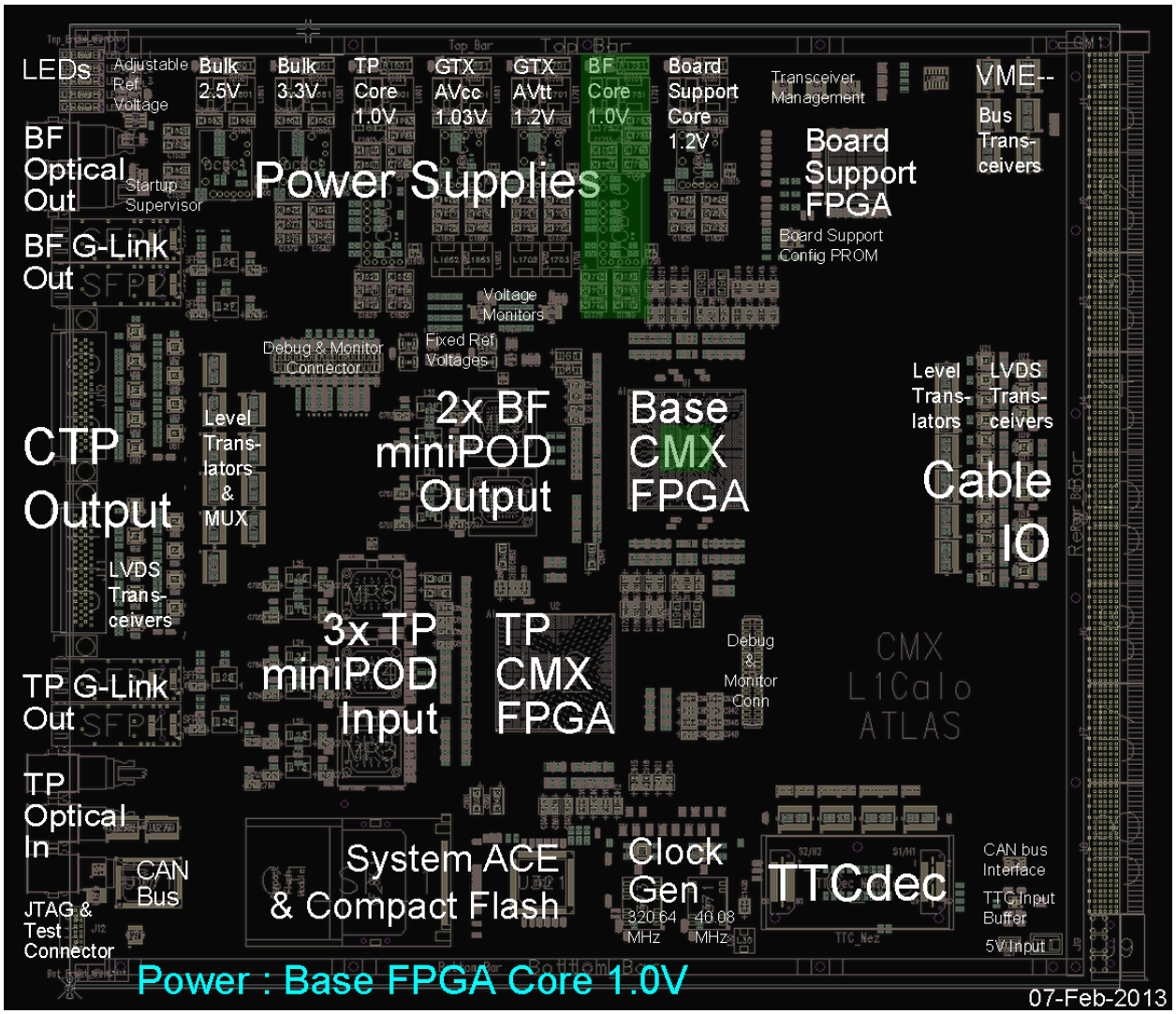

Figure 43 Power: Base FPGA Core 1.0V

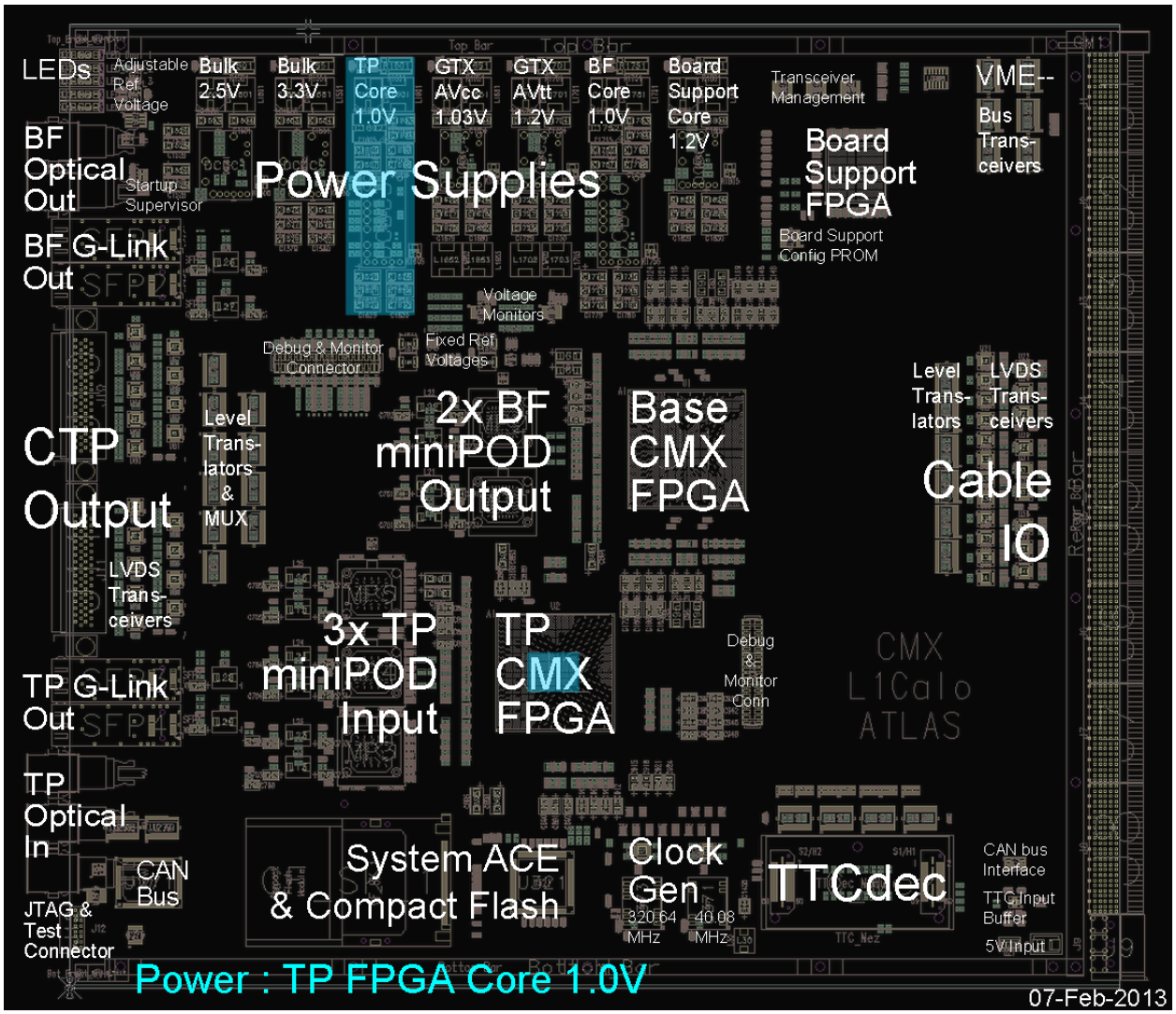

Figure 44 Power: TP FPGA Core 1.0V

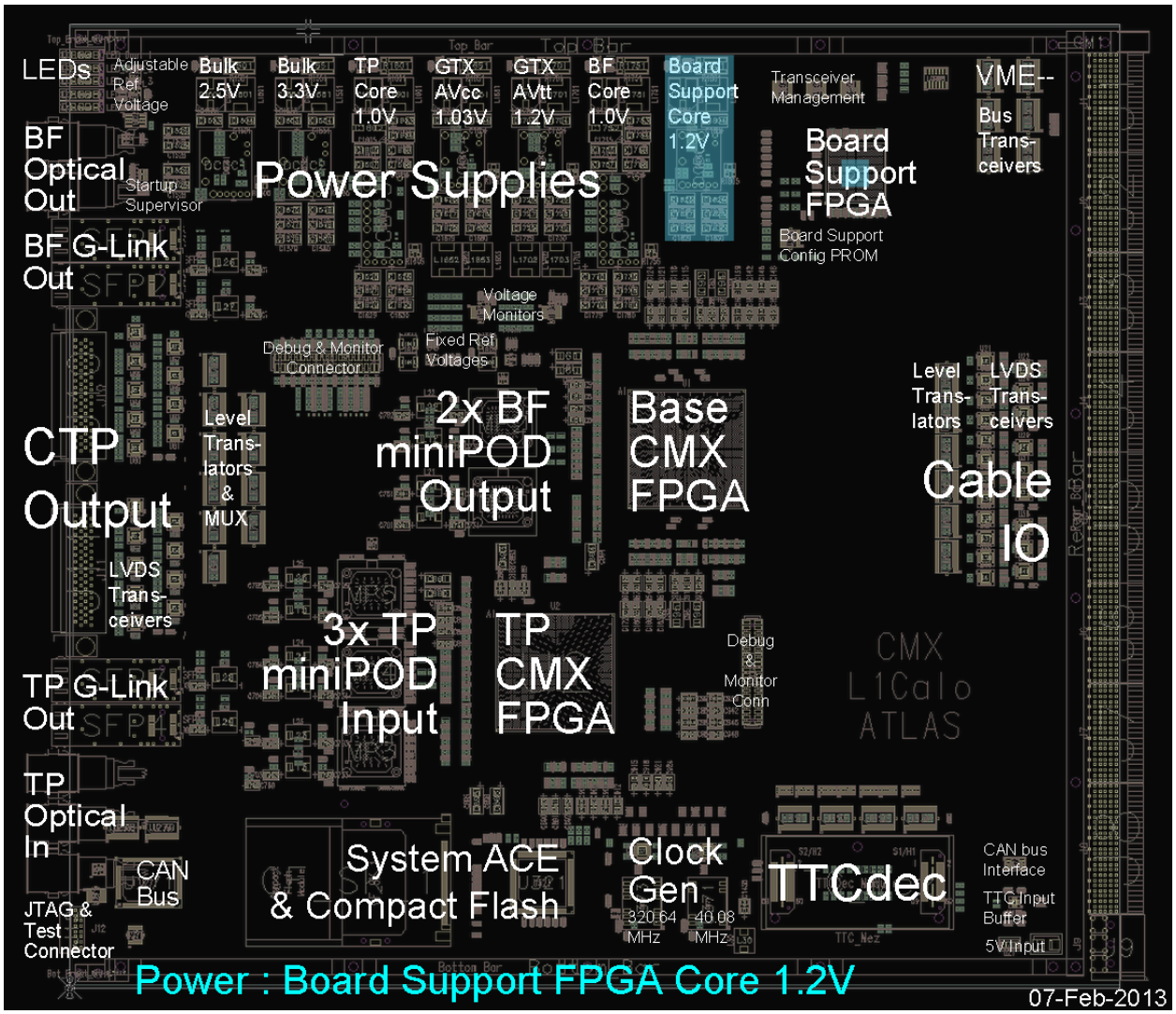

Figure 45 Power: Board Support FPGA Core 1.2V

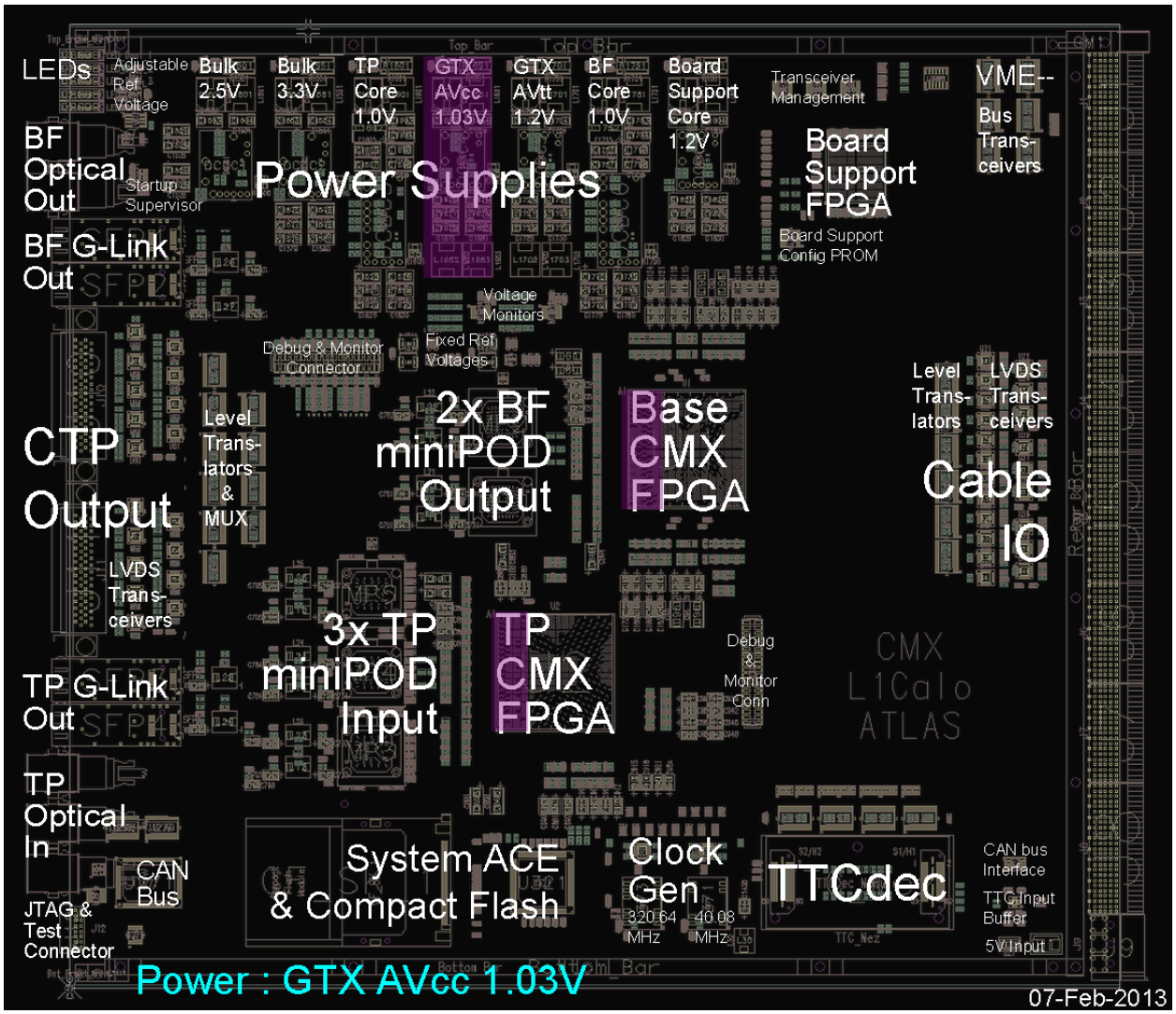

Figure 46 Power: GTX AVcc 1.03V

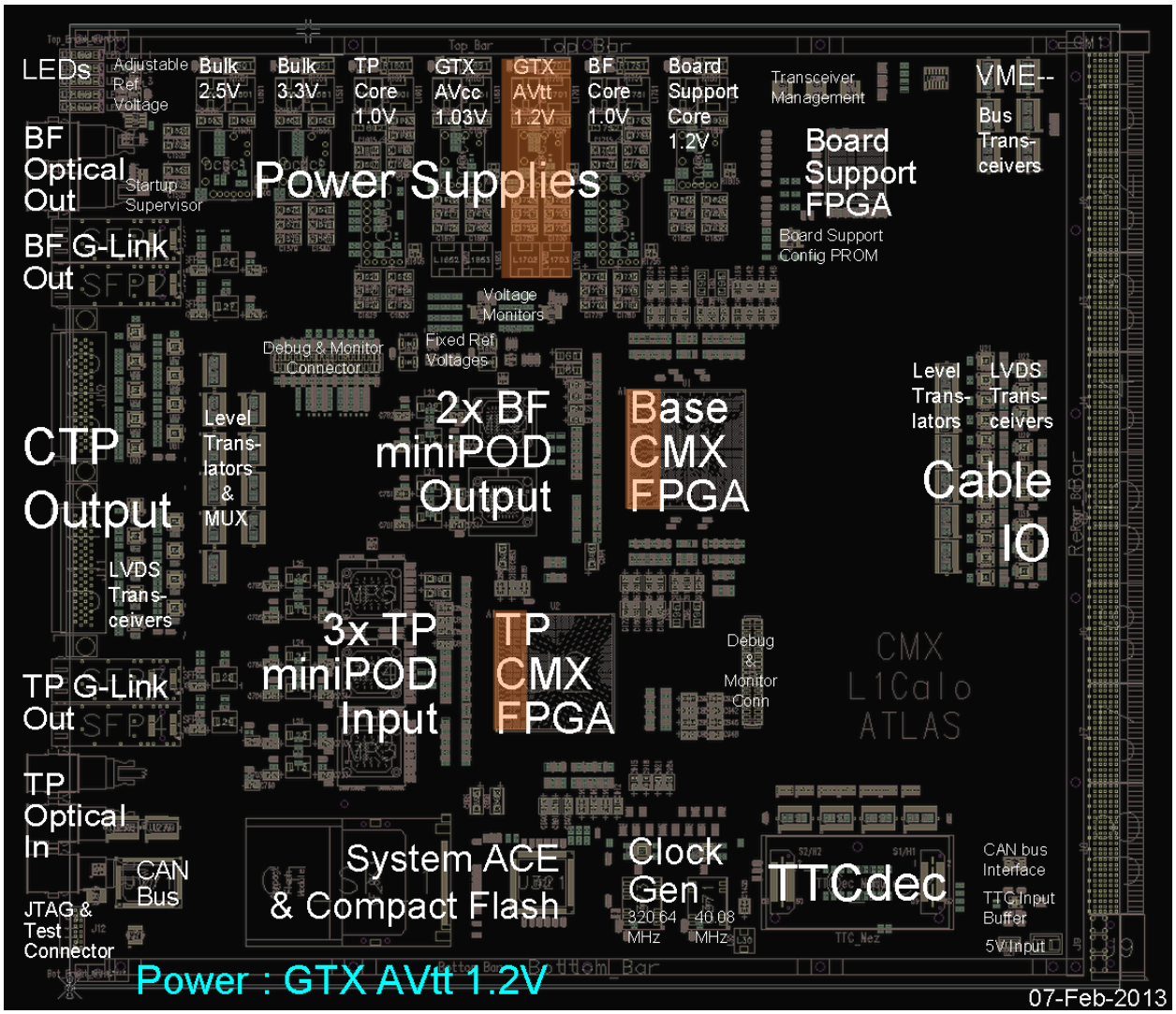

Figure 47 Power: GTX AVtt 1.2V

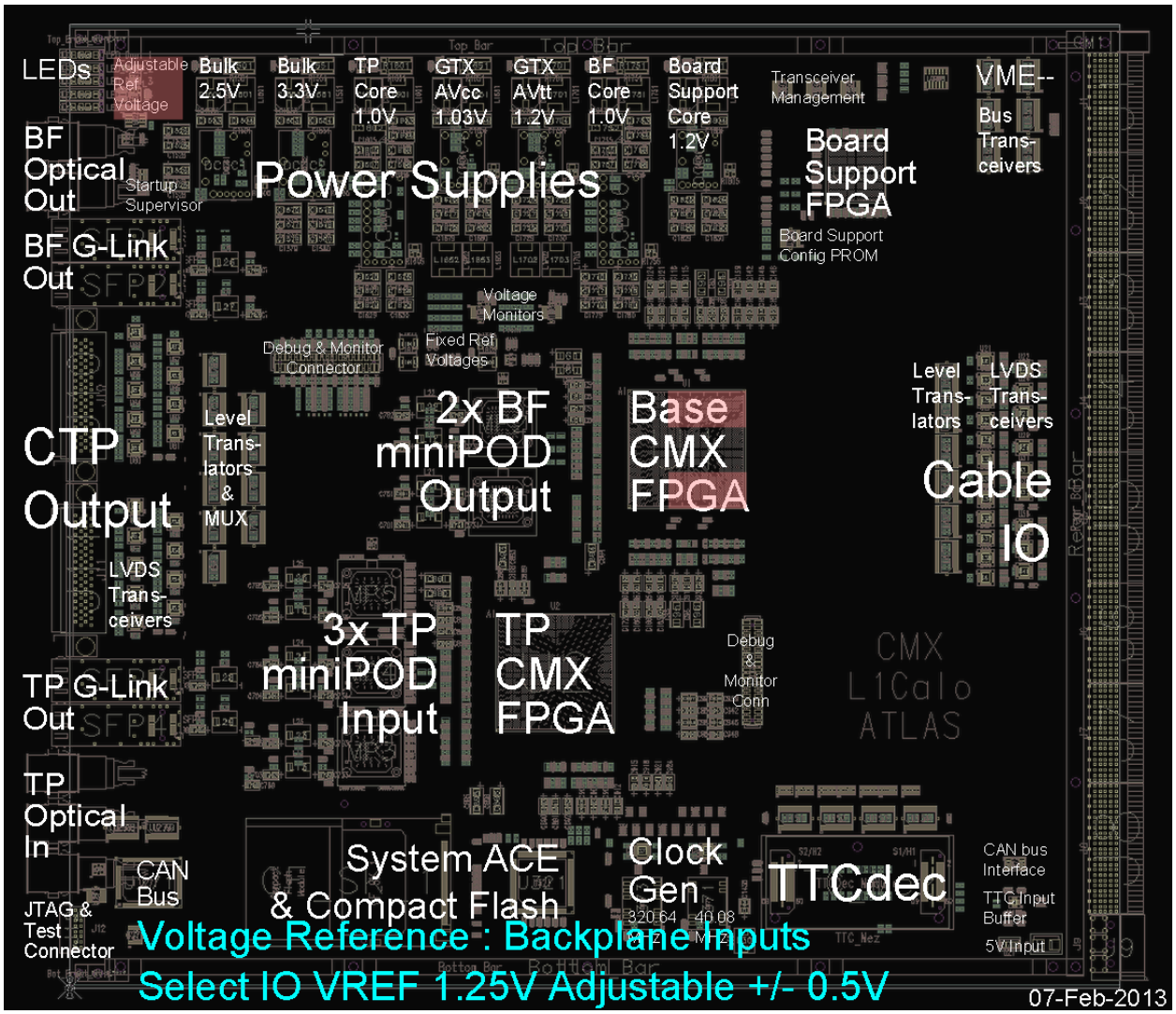

Figure 48 Reference: Select IO VRef 1.25V Adjustable

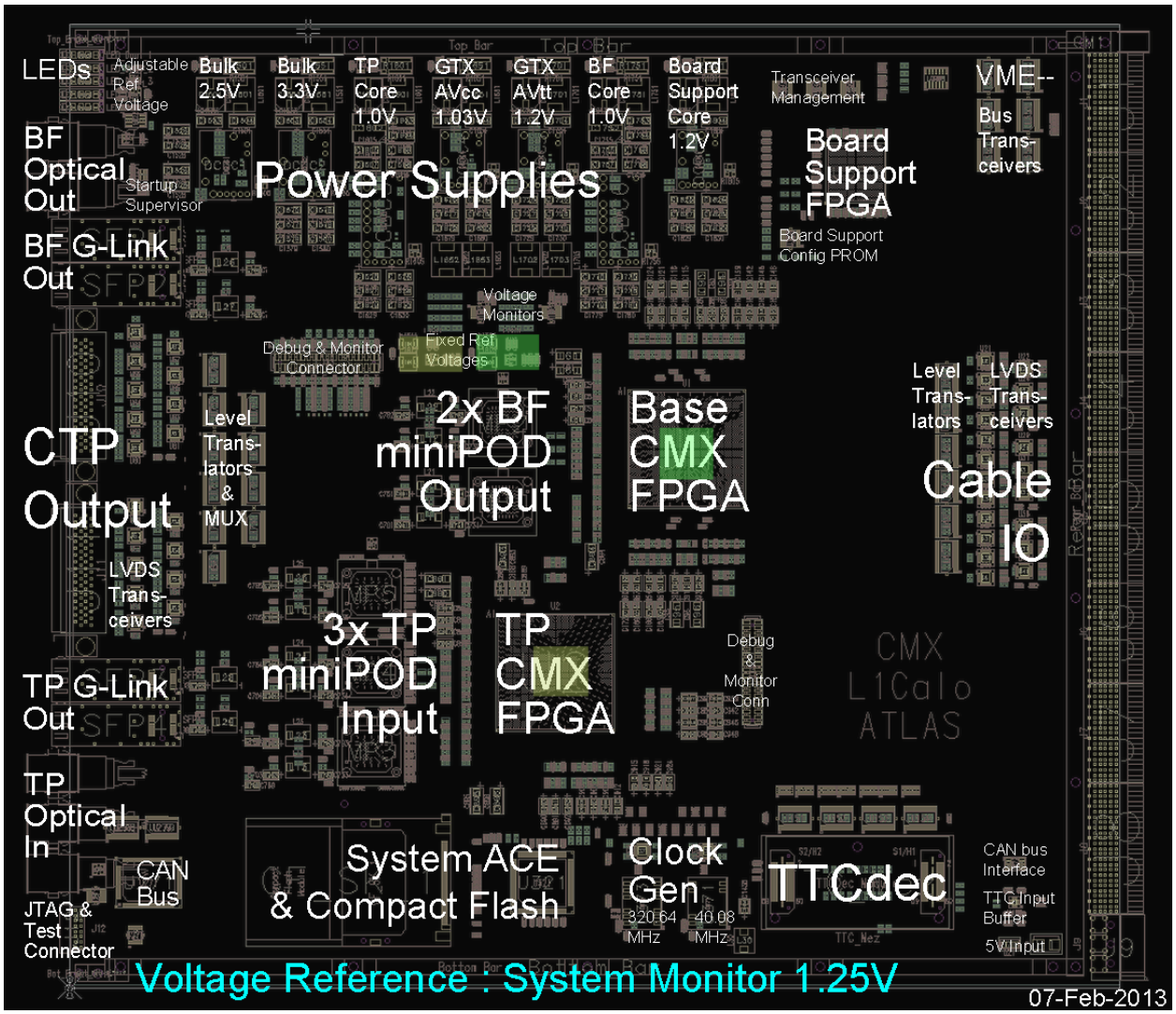

Figure 49 Reference: System Monitor 1.25V

A current snapshot of all the power usage diagrams is included above while future updates to these diagrams will be available as files located in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/block_diagrams/

Appendix P: CMX card layers

A current snapshot is included below while future updates to this description will be in cmx_ab_routing_layer_strategy.txt located in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
                  CMX  Routing Layer Strategy
                 -------------------------------


                                                Current Rev.  12-Feb-2013


This file describes the pcb layer strategy that is used on
the circuit board for the CMX.


CMX Layer Strategy:
-------------------

The word  Layer  means various things:

  - Physical layers in the actual pcb

  - Mentor design Logical layers

  - Thinking about just the Signal Trace layers

  - Recall that a Physical Layer may be used for example
    as a signal trace layer in one part of the CMX card
    and as a power plane in another area of the card.


The design of the 400 backplane inputs and the backplane
LVDS signals thinks in terms of "Signal Layers"  (not in
terms of Physical layers.

  - There are 10 signal layers used in the CMX design.

  - Signal layer number  1 is the   top  surface of the card.
    Signal layer number 10 is the bottom surface of the card.

  - Some of the 10 signal layers can have 65 Ohm traces
    and some can not reach above 50 Ohm Zo.

  - In our technical slang the 65 Ohm layers are called
    the "privileged layers".


Use of the 10 Signal Layers in the 400 Backplane Processor
Input to Base Function FPGA connections.
```

Full Run --> Continuous traces on this layer the whole way from the backplane connector to the BF FPGA pin.

Main Run --> Continuous traces on this layer from the backplane connector to the via array near the BF FPGA.

Last Inch --> Continuous traces on this layer from the via array near the BF FPGA to a BF FPGA pin.

Signal Layer	Use in the 400 Backplane Inputs Connecting to BF-FPGA	Trace Zo
1	Last Inch only CMX Top Physical Layer	
2	Full Run, Main Run or Last Inch	65
3	Full Run, Main Run or Last Inch	65
4	Full Run, Main Run or Last Inch	65
5	Full Run, Main Run or Last Inch	65
6	Last Inch only	50
7	Last Inch only	50
8	24 V_Ref, 8 DCI, 0-2 Last Inch	50
9	Full Run for 14 of the 16 Clks & Full Run or Last Inch for some normal signals	65
10	none CMX Bottom Physical Layer	

Use of the 10 Signal Layers in the Backplane LVDS Cable IO connections to the Base Function.

Conn-TX --> Traces on this layer from the backplane connector to the LVDS<-->3V3CMOS transceiver

Transl-FPGA --> Traces on this layer from the 3V3CMOS<--<2V5CMOS translator to the BF FPGA.

Signal Layer	Use in the Backplane LVDS Cable IO Connection to the BF-FPGA	Trace Zo

1	Transceiver <--> Translator and the last cm to pads for these parts CMX Top Physical Layer			
2	Conn-TX	and	Transl-FPGA	50
3	Conn-TX	and	Transl-FPGA	50
4	Conn-TX	and	Transl-FPGA	50
5	Conn-TX	and	Transl-FPGA	50
6	- none -			
7	- none -			
8	- none -			
9	Conn-TX	and	Transl-FPGA	50
10	- none - CMX Bottom Physical Layer			

Use of Signal Layers #6, #7, #8 in the area between the Base Function FPGA and the Backplane Connectors:

- Signal Layers #6, #7, #8 will carry the vertical mat of traces that involve many non principal signal flow signals and the signals to the front panel LVDS CTP connectors.

Physical Layer Rules:

- Follow exactly the GTX layer rules.
- All power planes must have an immediately adjacent ground plane on at least one side.

Common Sense:

- Ground planes should be contiguous Physical Layers.

Physical Layer Design:

There are 22 Physical Layers in the CMX circuit board.

Physical Layer	High Speed Ser IO FPGA and Optic TX	Rest of BF FPGA	PB 400 & LVDS & TX and Translate
1	50 Ohm Microstrip	Signal Layer #1	Signal Layer #1
2	Ground Plane	Ground Plane	Ground Plane

3	50 Ohm Stripline	Signal Layer #2	Signal Layer #2
4	Ground Plane	Ground Plane	Ground Plane
5	50 Ohm Stripline	Signal Layer #3	Signal Layer #3
6	Ground Plane	Ground Plane	Ground Plane
7	Diff FPGA Clocks	Signal Layer #4	Signal Layer #4
8	Ground Plane	Ground Plane	Ground Plane
9	Diff FPGA Clocks	Signal Layer #5	Signal Layer #5
10	Ground Plane	Ground Plane	Ground Plane
11	AVCC Fill	Bulk_2V5 Fill	Bulk_2V5 Fill
12	AVTT Fill	BF_Core Fill	Bulk_3V3 Fill
13	Ground Plane	Ground Plane	Ground Plane
14		Signal Layer #6	Signal Layer #6
15	Ground Plane	Ground Plane	Ground Plane
16		Signal Layer #7	Signal Layer #7
17	Ground Plane	Ground Plane	Ground Plane
18		Signal Layer #8	Signal Layer #8
19	Ground Plane	Ground Plane	Ground Plane
20		Signal Layer #9	Signal Layer #9
21	Ground Plane	Ground Plane	Ground Plane
22		Signal Layer #10	Signal Layer #10

- The non high speed serial IO area under the TP FPGA is like the non high speed serial IO area under the BF FPGA except that it uses Physical Layer 12 for the TP_Core fill.

- The area under the Board Support FPGA needs: Bulk_3V3, Bulk_2V5, and BSPT_Core 1.2V power.

- The area under the 12 channel high speed optical parts needs Filtered 2.5V and 3.3V power. Each supply is filtered by a capacitor to Gnd, a series inductor, and a final capacitor to Gnd at the component power pin.

- The area under the low speed SFP optical parts needs to have filtered 3.3V supplies, a separate filtered 3.3V supply for that SFP packages transmitter and for its receiver. Each supply is filtered by a capacitor to Gnd, a series inductor, and a final capacitor to Gnd at the component power pin.

- These are all 1/2 oz copper layers except for the main power planes on layers 11 and 12 which are 1 oz. 1/2 oz copper is about 1 mOhm per square. The tolerance on the Virtex Core supply is 50 mV. The tolerance on the 12 channel optical part is 30 mV. The final design may require power fills on multiple layers.