Report of the internal design review

ATLAS L1Calo CMX Prototype

Abstract

An internal design review of the first prototype ATLAS L1Calo CMX module was held on on 7 March, 2013. The Review Committee approved moving forward with the prototype manufacture and testing, with a limited number of minor changes and recommendations.

Prepared by:	*Checked by:*	*Approved by:*
S. Silverstein, Stockholm		

For information, you can contact:	**S. Silverstein**	Tel. +46.8.5537 8693	Fax.	E-Mail silver@physto.se

Distribution: TDAQ upgrade coordination, all participants mentioned in the report.

PURPOSE OF THE REVIEW

This was an informal, comprehensive review of the first CMX prototype, including both the module specification and the module design. The CMX will add topology-related capabilities to the real-time data paths of the L1Calo cluster processor (CP) and Jet/Energy-sum (JEP) processor systems.

MEMBERS OF THE REVIEW COMMITTEE

Review Committee

RAL: I. Brawn, D. Sankey, B. Barnett,
N. Gee, W. Qian
Birmingham: J. Bracinik, R. Staley,
S. Hillier
Mainz: U. SchaeferHeidelberg: V. Andrei
Stockholm: S. Silverstein (Chair)

CMX design team (MSU)

R. Brock, MSU
D. Edmunds, MSU
Y. Ermoline, MSU
P. Laurens, MSU
J. Linnemann, MSU

AGENDA AND DOCUMENTATION

The agenda and materials are linked from the meeting page on Indico:

https://indico.cern.ch/conferenceDisplay.py?confId=228627

REPORT

The Review Committee thanks the CMX design team for the clear and comprehensive documentation provided, and the detailed responses to questions and comments received from the reviewers. The Committee unanimously approved moving ahead with the prototype CMX module pending a small number of required and recommended changes and clarifications described below.

RECOMMENDATIONS AND COMMENTS

1. COMPATIBILITY WITH EXISTING CRATE AND INFRASTRUCTURE

The CMX is designed to be physically compatible with the existing CMM modules, which it replaces. Some of the physical differences between CMM and CMX led to the following concerns:

- The height of the Avago MiniPOD optical transmitter/receivers intrudes by 0.7mm into the space reserved by the neighbouring modules, according to VME specifications. It was felt that this should not present a real physical problem, but further mechanical tests at CERN will be carried out to be sure of this.
- Due to space issues, the CMX prototype layout does not allow front-panel access to the CompactFlash card, so changing this card would require the module to be removed and then re-inserted in the crate. Frequent extraction/insertion of the CMX poses a significant risk of backplane damage, and should be avoided. Alternatives include implementing a reliable alternative method for changing the flash card contents (through VME or JTAG), or moving the CompactFlash to the front panel. A cost-benefit analysis should be performed and applied.

2. INTERFACES WITH CONNECTED SYSTEMS

For the input signals arriving from the JEM/CPM modules:

- Internal FPGA input termination was confirmed to be sufficient. In the interest of power consumption concerns, it was pointed out that only the data clock lines need to be terminated.
- The signal standard for both systems is 2.5V CMOS.
- All single-ended signal lines on the backplane were manufactured and tested to have 60 ohms impedance within 10%.
- The alignment of the 80 MHz data clock signal relative to the data should be the same for CP and JEP systems. It is considered preferable for the edges of the data clock to be aligned with the center of the data. The CPM can provide this timing alignment, and the situation for the JEM is being investigated. If the JEM and CPM cannot both provide data-centered clock edges then both will use edge alignment, with IODELAY settings to adjust the input data timing. It is believed that the CMX can support either scheme.
- CMX may need to receive test patterns from the CPM and JEM for timing and connectivity tests, and possibly to resolve 80 MHz ambiguity. These would require firmware changes in the CPM and JEM, so if such patterns are needed they need to be agreed and specified in good time.

Real-time LVDS input and output cables:

- The existing data merging cables are currently running at 40 Mbit/s, but higher data rates will be needed for merging higher numbers of threshold multiplicities. The CMX is more than capable of providing these.

Output to CTP:

- During the CMX PDR, it was noted verbally (but not written) that the CMX would not be required to provide optical output to the CTP. This should be followed-up and explicitly confirmed with CTP.
- In Phase-0, cable outputs to CTP will be limited to 40 Mbaud. This could potentially be increased later, but there are no current plans to do so.

Readout links:

- The DAQ and RoI outputs from the BF FPGA will be sent to the L1Calo RODs using G-link data formats. For timing compatibility the BF FPGA needs to be provided with a 40.000 MHz crystal clock.
- The L1Topo modules are expected to act as their own RODs, providing readout to DAQ and the ROIB using S-link protocol. To do the same from the TP FPGA, the TP and BF FPGAs would need to be provided with a 100.000 MHz crystal clock, the input links on the two TP SFP cages would need to be brought to spare GTX inputs on the BF FPGA, and two single-ended flow-control signals would need to be routed between the BF and TP FPGAs. Additionally two “BUSY” lemo cables would need to be routed through the front panel.

  Since this implies a significant addition to the CMX specification and potentially significant delays, it has since been confirmed that there is room on existing L1Calo RODs for the TP to provide eventual (limited) topology readout over G-link formats to those RODs. In this case, the TP FPGA must also be provided with a 40.000 MHz crystal clock for compatibility.

  A cost-benefit analysis should guide the choice of solutions.

Output fibers to L1Topo

- Currently the CMX front panel has five MTP/MPO outputs, each supporting one 12-fiber ribbon. If additional space must be freed, condensing the inputs and outputs to two 48-fiber connectors is straightforward.

Interface with the VME-- bus

- Existing boards in the system use 3.3V devices that are 5V tolerant. It is recommended to do the same on CMX.

3. BOARD FUNCTIONALITY

- The required output from the TTCDec to the BF FPGA includes only the two deskew clocks, L1A and the BC reset signal. If the TP FPGA acts as its own ROD, then most or all of the TTCdec outputs should be routed to that device. If not, then the TP FPGA has the same requirements as the BF.
- The CANbus monitoring should also include currents, implying an implementation using an analog multiplexer.
- To save front-panel space, the number of LEDs at the front-panel is decreased to ten. The LEDs are driven by FPGA outputs, so their functionality can be changed over time. Still, suggestions are solicited for which LEDs are most useful, in testing and running conditions.
- The CMM specification included two front-panel outputs for the deskew1 and deskew2 clocks, but these were not included in the production version. These clock outputs were useful during early testing of the CMM, and could be similarly useful for the CMX. It is acceptable for these signals to be made available on a header; lemo connectors are not required. Again, this should be decided on a cost/benefit basis.

4. OTHER ISSUES

- The number of production CMX modules of each time still has to be finalized. Based on the CMM production run of 19 boards, it was suggested to produce 20 CMX boards due to the need for an additional test rig at MSU. Of the 20 production modules, 6 of them would have TP FPGAs installed.

  The approximate breakdown of where the different boards would be located:

  - USA15: 10 non-TP + 2 TP
  - CERN test rig: 1 TP
  - UK test rig: 1 non-TP
  - Mainz test rig: 1 non-TP
  - MSU test rig: 1 TP
  - Spares (CERN): 2 non-TP + 2 TP