CMX – Base function Firmware: device utilization, timing

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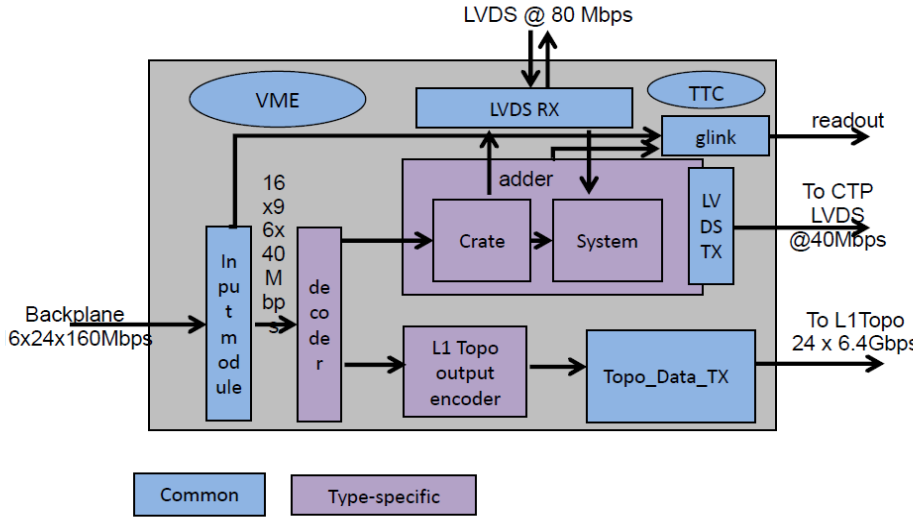
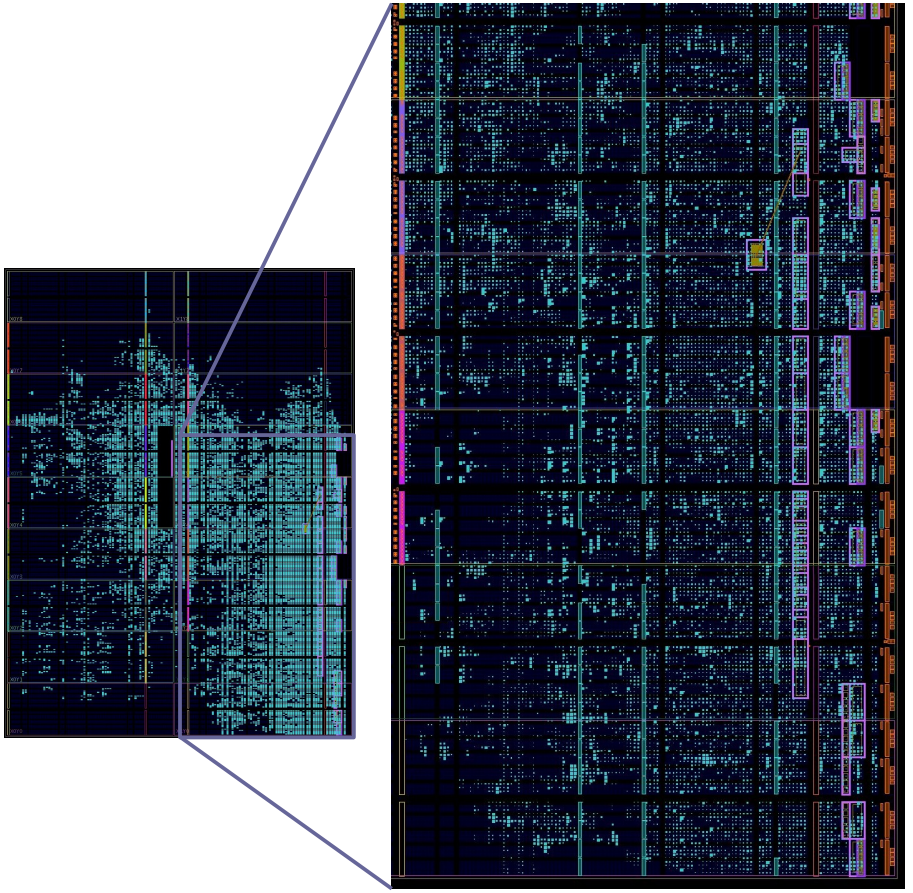
Firmware functionality

- Modular structure to support 3(jet,energy,em)x2(crate,system) flavors
- Work on-going for the Jet-type
- Modules re-used in dedicated FW test configurations over last ~2.5 months
  - Debugged, extended



Will it work on the selected FPGA? Resource use

Resource	Used	Available	%
Registers	44,312	687,360	6
LUTS	24,672	343,680	7
Slices	21,512	85,920	25
RAMB36	195	632	30
RAMB18	59	1264	4
BUFG	7	32	21
BUFR	21	72	29
MMCM	3	18	16



- Full feature set not implemented yet
  - Major RT path present: capture, decoding, Topo TX

Will it work on the selected FPGA? Timing closure

Derived Constraints for TS_CLK_40MHz08_DSKW_2_BF_LOGIC_DIR

Constraint	Period Requirement	Actual Period		Errors		Paths Analyzed	
		Direct	Derivative	Direct	Derivative	Direct	Derivative
TS_CLK_40MHz08_DSKW_2_BF_LOGIC_DIR	24.950ns	10.000ns	24.944ns	0	0	0	9186803030
TS_P_0__24_	12.475ns	10.477ns	N/A	0	0	652	0
TS_P_1__24_	12.475ns	10.665ns	N/A	0	0	652	0
TS_P_2__24_	12.475ns	9.041ns	N/A	0	0	652	0
TS_P_3__24_	12.475ns	10.791ns	N/A	0	0	652	0
TS_P_4__24_	12.475ns	9.527ns	N/A	0	0	652	0
TS_P_5__24_	12.475ns	10.397ns	N/A	0	0	652	0
TS_P_6__24_	12.475ns	10.551ns	N/A	0	0	652	0
TS_P_7__24_	12.475ns	9.821ns	N/A	0	0	652	0
TS_P_8__24_	12.475ns	11.005ns	N/A	0	0	652	0
TS_P_9__24_	12.475ns	10.125ns	N/A	0	0	652	0
TS_P_10__24_	12.475ns	9.359ns	N/A	0	0	652	0
TS_P_11__24_	12.475ns	8.867ns	N/A	0	0	652	0
TS_P_12__24_	12.475ns	10.741ns	N/A	0	0	652	0
TS_P_13__24_	12.475ns	10.811ns	N/A	0	0	652	0
TS_P_14__24_	12.475ns	9.701ns	N/A	0	0	652	0
TS_P_15__24_	12.475ns	8.925ns	N/A	0	0	652	0
TS_D_CBL_25_B	24.950ns	6.370ns	N/A	0	0	32	0
TS_D_CBL_48_B	24.950ns	6.094ns	N/A	0	0	31	0
TS_CMX_clock_manager_1_clk40	24.950ns	23.311ns	N/A	0	0	9186774205	0
TS_CMX_clock_manager_1_clk200	4.990ns	3.225ns	N/A	0	0	93	0
TS_CMX_clock_manager_1_clk320	3.119ns	3.118ns	N/A	0	0	18237	0

Derived Constraints for TS_Topo_Data_TX_1_TXOUTCLK_OUT_0_

Constraint	Period Requirement	Actual Period		Errors		Paths Analyzed	
		Direct	Derivative	Direct	Derivative	Direct	Derivative
TS_Topo_Data_TX_1_TXOUTCLK_OUT_0_	3.118ns	2.000ns	3.058ns	0	0	0	4929
TS_Topo_Data_TX_1_TXUSRCLK2_IN_unbuffered_0_	3.118ns	3.058ns	N/A	0	0	4929	0

Derived Constraints for TS_Topo_Data_TX_1_TXOUTCLK_OUT_12_

Constraint	Period Requirement	Actual Period		Errors		Paths Analyzed	
		Direct	Derivative	Direct	Derivative	Direct	Derivative
TS_Topo_Data_TX_1_TXOUTCLK_OUT_12_	3.118ns	2.000ns	3.110ns	0	0	0	2852
TS_Topo_Data_TX_1_TXUSRCLK2_IN_unbuffered_1_	3.118ns	3.110ns	N/A	0	0	2852	0

- Timing very close:
  - Operating near GTX switching limit (330 MHz)
  - Complex operations performed with minimal latency e.g. CRC

Conclusions

- No problems foreseen due to resource use.
  - High occupancy areas do not need major changes.
- Meeting timing constraints is challenging.
  - Timing analysis shows that high speed logic can work at that operating point.