Atlas Level 1 Calorimeter Trigger

Common Merger eXtended module (CMX)

Hardware Description

Document prepared for the

CMX Production Readiness Review

12-May-2014

Dan Edmunds, Philippe Laurens,

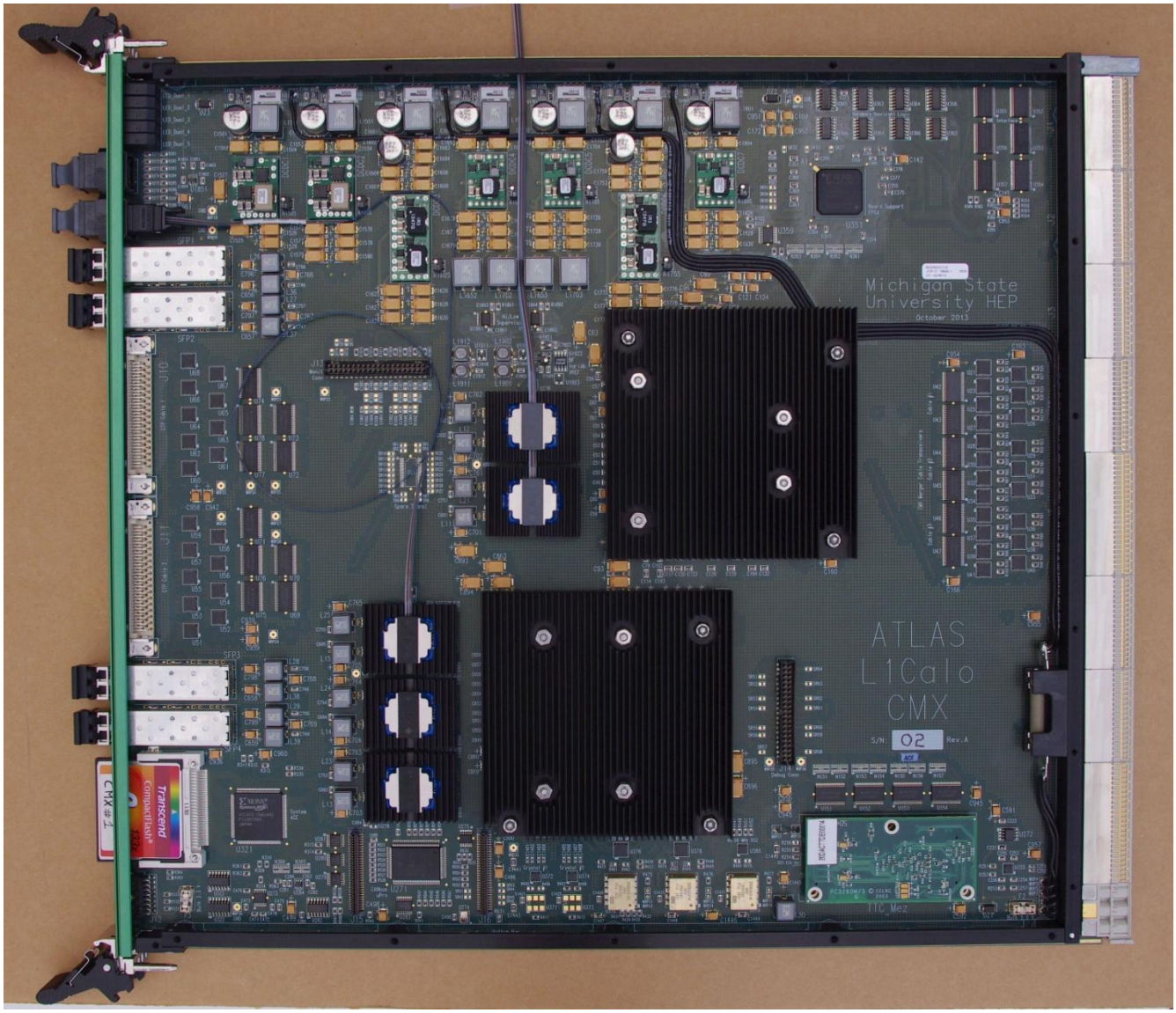
Yuri Ermoline, Chip Brock,

Wojtek Fedorko*

Michigan State University

(*) University of British Columbia

30-Apr-2014



Atlas L1calo CMX

TABLE OF CONTENT

Table of Figures

1 Introduction

1.1 Scope

The CMX project is part of the Phase-0 upgrade of the Atlas Level-1 Calorimeter Trigger system (L1calo). The CMX module is designed as a replacement for the Common Merger Module (CMM). The CMX modules must be able to replace the existing CMM modules, provide an increase in performance and add new functionality as described in this document.

This Introduction (section 1) summarizes the historical evolution of this project and is followed by (section 2) a general description of the CMX card and its main features, (section 3) a description of the real-time data path and usage in L1calo, (section 4) a description of the board control, configuration and monitoring, (section 5) a description of the powering of the components on the card, (section 6) a description of the Card Layout and finally (section 7) a table of the number of CMX cards to be built.

This document also contains appendices which include the circuit diagrams and engineering notes used to design the CMX card.

The use of large FPGAs with well over a thousand pins per device does not make the standard schematic entry methods very practical for the designer or welcoming to the outside reader. The CMX was instead entered in the Mentor CAD system directly as a keyed-in net list, i.e. a text file describing all the connections in the plain ASCII file format used by the CAD system. The overall net list was assembled from a collection of smaller and more easily manageable files including the comments and annotations found useful to design and document the card. Schematic diagrams are still a critical part of the process and circuit diagrams are created using a more flexible format. A circuit diagram was made for each sub-sections of the CMX to help in the detailed design and the documentation of the project. A snapshot of these circuit diagrams contemporary to this document is included in the appendices of this document. The key-in net list is not included here but available via the references below.

The appendices form a snapshot of the current state of all these design documents. Collecting all these sub-documents and organizing them into one common document was intended to help the reviewers and also remain as an archive of this stage of the design. The appendices include references to the locations where the source documents will continue to evolve if necessary as the project continues through the manufacturing of the final production modules.

References:

The main URL for the CMX project is
http://www.pa.msu.edu/hep/atlas/l1calo/

Pictures of the CMX card are in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/photos/
The CMX project specification documents (including previous reviews) are in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/specification/
The CMX block diagrams are in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/block_diagrams/
The circuit diagrams are in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/
Views of the trace layout are in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/pcb_layout_views/
The final key-in net list files are in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/net_lists/
The most recent versions of the engineering notes are in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

The mechanical drawings for the front panel, stiffener bars and heat sinks are in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/front_panel/
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/stiffening_bars/
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/heat_sinks/

Device datasheets and documentation for the parts used on CMX are in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/components/
All manufacturing information is located here
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/manufacturing/

The CMM documentation contains a lot of relevant information not repeated in this document and a copy of the CMM documentation is available here
http://www.pa.msu.edu/hep/atlas/l1calo/reference/l1calo/cmm/

This and other PRR documents plus reviewer comments or recommendations are in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/specification/4_production_design_review/

1.2 Preliminary Design Review

The CMX project was presented to a Preliminary Design Review (PDR) in July 2011 in Stockholm. The PDR specification document and the review report are available in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/specification/1_preliminary_design_review/

1.3 Design Study and Report

A design study phase followed the PDR to determine an optimal choice for implementing the base functionality required to replace the CMM and to explore the feasibility of implementing some topological processing using the CMX as a platform. The results of this study were presented during a workshop at the Rutherford Appleton Laboratory in February 2012.

The main outcome of this study was the decision to separate the topological processing functions on CMX from the base functions on CMX. Instead of using one of the largest Virtex 6 FPGAs (XC6VHX565T) the CMX is implemented on two medium size Virtex 6 devices (both being XC6VHX550T). One FPGA implements the Base Function (BF FPGA) required of all CMX modules, and the other FPGA implements the Topological Processing Function (TP FPGA) optionally required on only one or a few CMX modules. Most CMX cards are built with only the Base Function FPGA installed and only a few cards will have both FPGAs installed.

The recommendations from this workshop also specified that the CMX BF FPGA should provide High Speed outputs for two 12-fiber ribbons and that the TP FPGA should receive High-Speed inputs from three 12-fiber ribbons. All optical links must operate at 6.4 Gbps with a reference clock derived as a multiple of the LHC clock.

The material presented at the workshop, the resulting recommendation and a more detailed study report are available in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/specification/2_design_study/

1.4 Requirements changes since then

One additional requirement which was not explicitly part of the original PDR nor part of the RAL workshop recommendations is the option of operating the CTP output at speeds higher than the current 40 Mbps on CMM. The CMX was designed to support higher CTP output data rates of 80 and 160 Mbps. This option may not be usable in practice as the CTP hardware used during Phase 0 will likely not support these higher transfer rates.

A self-imposed requirement was also added to the CMX hardware such that the BF FPGA is able to operate the three Cable IO ports of the CMX card independently, separately controlling the direction of each cable. This additional capability allows standalone testing of CMX cards to verify proper cable IO connectivity and operation. This option has proven to be useful during initial tests.

In order to reduce the total number of component types used on the CMX card the CTP output circuitry uses the same logic level translators and the same LVDS transceiver devices as the Cable IO circuitry does. The equivalent requirement was also added such that the BF FPGA (or the TP FPGA) is able to operate the two CTP output ports independently, as input or output.

It was noticed that the backplane pinout defines three additional Cable IO signals that were not routed on the CMM card and are not handled by the Rear Transition Module (RTM) cards. There were unused resources in the Cable IO circuitry used on CMX and one signal was thus added to each port. This extra bit or lane of communication between a Crate CMX and a System CMX will not be usable without building new RTM cards.

The merged clock-parity scheme described in the PDR for operation of the backplane input is no longer the intended mode of operation. One dedicated clock signal and one dedicated parity signal are now accompanying the 23 data signals from each processor source. The CMX hardware has been designed to be compatible with both the old and the new scheme.

1.5 Parallel Support Projects

1.5.1 VAT Card

A project was started in parallel to the CMX design as a prototype of some of the aspects of the full CMX card. The VAT card (VME/ACE/TTC) was created to redesign some of the CMM hardware circuitry using new components and replace several discrete components with a single FPGA device which is now called the Board Support FPGA on CMX. The VAT card is a test card in 6U VME form factor which implements the interface to the ACE and TTC sub-sections and includes a small Virtex-6 FPGA device as a target for configuration.

The VAT card has been used to design the VME Interface Firmware and practice controlling the System ACE and configuration of the Virtex-6 FPGA from the Board Support FPGA. It has also been used to practice working with the test stand.

Some of the hardware and firmware details learned from the VAT project have been implemented in the CMX design.

The VAT card design files and details can be found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/vat_card/

1.5.2 Mechanical-Only CMX Card with Stiffener Bars

A Mechanical-Only CMX Card was produced including all backplane components. The purpose of this card was to verify that the CMM Gerber files had been properly interpreted and the measurements properly transferred to the CMX design. It was a verification of the exact placement of the backplane 5-row connectors, the power connector and the metal guide module.

A card the size of CMX with large Ball Grid Array components and with a large number of backplane pins needs to be mechanically stiff to allow proper insertion and to protect the Ball Grid connection. Stiffener bars are thus required along the sides and the back of the card. These bars also help in transferring and distributing the force exerted by the front panel ejector handles during card insertion and card extraction.

The FPGAs and the optical transceivers will generate heat and the stiffener bars must be designed for minimal interference with the airflow across the board. Much of the metal has

been removed from the stiffener bars installed on the top and bottom edges of the card. The posts where the bars attach to the circuit board have been carefully aligned with the mechanical structures of the VME card cage which are already impeding airflow.

This Mechanical-Only CMX Card was fitted with a prototype of the full set of the stiffener bars designed for use on CMX. The stiffener bars are screwed to the board and to a front-panel with the required all-metal handles.

This Mechanical-Only CMX Card was also used to test the height of the MiniPOD components and verify that there would not be any interference with modules in adjacent VME slots.

Pictures of the Mechanical-Only CMX Card installed in the MSU test rack can be found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/manufacturing/1_mechanical_only/

1.5.3 Virtex-6 Evaluation Board Studies

A Xilinx M605 Evaluation Board for the Virtex-6 was used as a test platform for designing and validating the firmware of the Base Function FPGA and for making timing and power usage measurements.

2 General Description

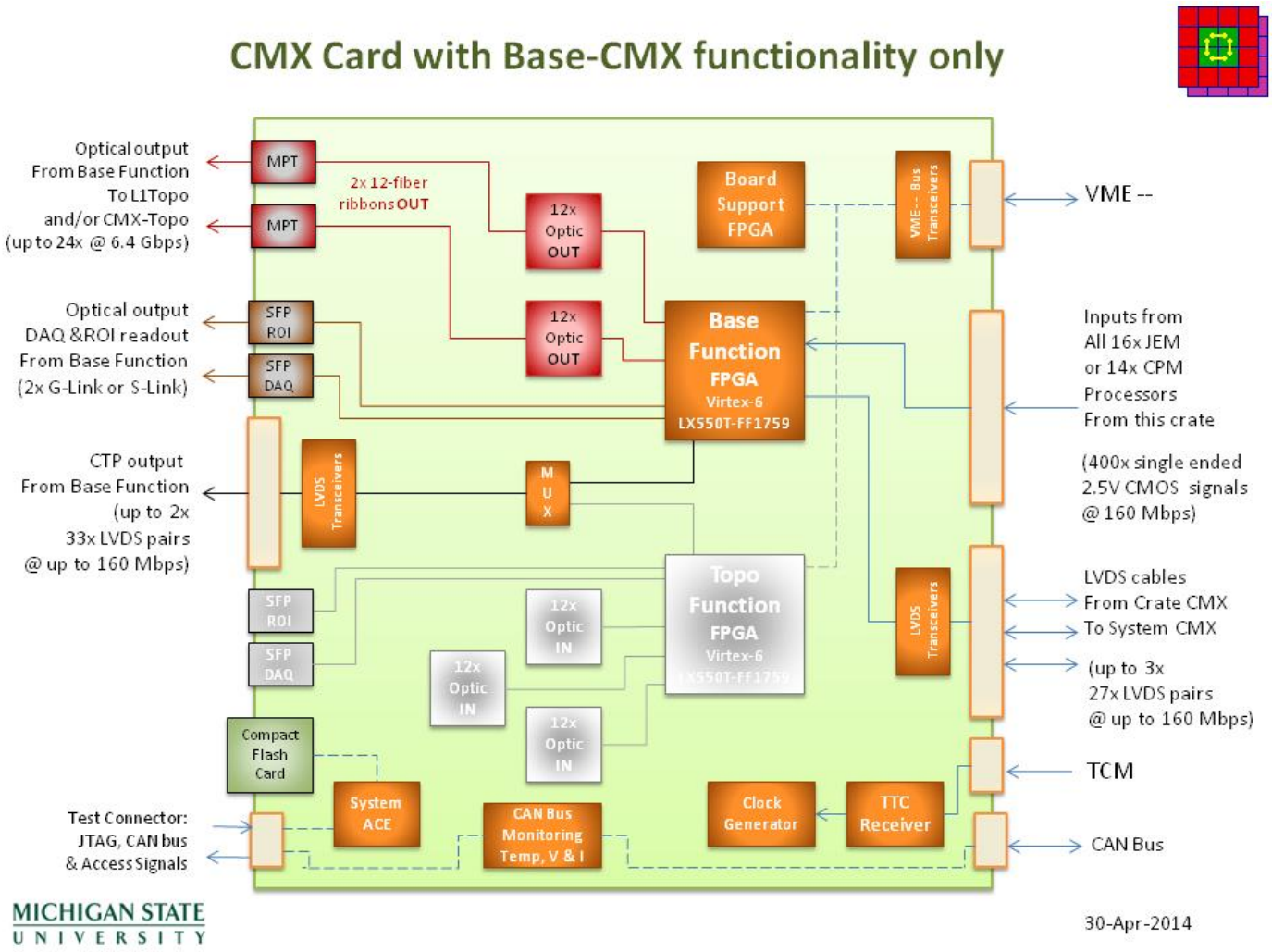


Figure 1: CMX block diagram for Base Function operation

The CMX:

1- is able to perform all tasks previously handled by any CMM.
2- is able to perform these CMM tasks at higher input and output line rates.
3- provides more computing power to support additional algorithms.
4- provides new functionality to send out raw or processed copies of its inputs over optical fibers.
5- provides optional functionality to perform Topological Processing on CMX data.

2.1 CMM Emulation

In order to become a replacement for the CMM card, the CMX module is able to operate in the CMM slots of the L1calo crates. It obeys the same backplane pinout for all its backplane VME--, power, signal, control and monitoring pins. Signal names were carried over from the CMM to the CMX to avoid confusion.

The CMX also provides the same LVDS connectors as CMM for sending its results to the CTP over the existing cable plant.

The CMX is able to provide the same backplane Merger Cable IO capabilities as the CMM and is able to operate as a Crate CMX or System CMX. The set of CMX cards installed in L1calo is thus able to use the existing RTM modules and Crate CMX to System CMX cable plant.

Like the CMM the CMX provides G-link ports for optical DAQ and ROI outputs to the existing RODs over the existing fibers.

Like the CMM the CMX uses System ACE for configuring the Virtex-6 FPGA firmware.

Like the CMM the CMX supports CAN Bus monitoring. Temperatures from several locations on the board and voltages from the on-board power supplies are being monitored on the CMX as on the CMM. In addition to the power supply voltages the CMX monitors their currents.

Because of its additional features, the CMX is not able to present the exact same set of VME control registers as the CMM, and the online software is thus being modified and extended to control and monitor the CMX cards.

2.2 Increased Bandwidth

The CMX is able to run at the speed of the CMM card, if desired, but also supports a new mode of operation with higher line rates for:

1- the backplane signals it receives from the JEM or CPM modules
2- the cable IO connecting a Crate CMX to its corresponding System CMX
3- the CTP output

2.2.1 Inputs from JEM or CPM modules

Over the backplane the CMX receives inputs from up to 16 JEM or 14 CPM processor modules present in the same crate. 25 signals are received from each processor module for a total of 400 (16 x 25) backplane input signals. The CMM mode of operation is based on receiving one bit of information on each backplane input line for each beam crossing, i.e. one bit every 25 ns or 40 Mbps per line. In this mode one bit out of the 25 bits received from each source processor module dedicated to parity.

The CMX is able to receive 4 bits of information on every backplane line for every beam crossing, i.e. one bit every 6.25 ns or 160 Mbps. The bit that was previously used for parity is now dedicated to carry a clock signal, alternating between low and high every 6.25 ns, which is the 80 MHz forwarded clock sent by the processor module.

The characteristic impedance of the 400 processor input lines is 60 Ohms. The CMX tries to maintain a 60 Ohm characteristic impedance over the whole path from the backplane pins to the FPGA input pins. This requirement proved impractical and a compromise had to be made for the last ~ 1cm of signal traces which are described in section 3.

2.2.2 Crate CMX to System CMX Cable IO

The CMX card is able to send or receive parallel LVDS data to or from other CMX cards. The direction of data flow depends on whether the CMX card is used as a Crate CMX or a System CMX as will be described in more details in section 3. Up to three LVDS cables can be connected to a CMX card via a Rear Transition Module (RTM) plugged in the back of the crate that route the cable LVDS signals to the backplane pins.

On the CMM card three sets of 27 LVDS signals are operated together as inputs or as outputs. The CMM operation is based on sending or receiving one bit of information on each Cable IO

LVDS line for each beam crossing, i.e. one bit every 25 ns or 40 Mbps, with one bit out of the 27 bits from each cable being dedicated to parity and one bit being reserved.

The CMX is able to send or receive up to 4 bits of information on every LVDS line for every beam crossing, i.e. one bit every 6.25 ns or 160 Mbps. A bit from each cable which is currently reserved could be used as a clock signal if necessary. The current plan is to operate the Cable IO links at 80 Mbps. The existing RTMs and cable plant are able to support operation at 80Mbps. New RTM modules might be required if operation at 160Mpbs becomes desirable.

The direction of the LVDS transceivers used for each IO Cable is controllable from the Base Function FPGA, and each cable can be controlled independently to operate as input or output. This feature is useful during initial card testing and commissioning.

2.2.3 Output to CTP

The CMX card is able to send parallel LVDS data to the CTP system. Only the System CMX cards send trigger information to the CTP as will be illustrated in more details in section 3. Up to two CTP LVDS cables can be connected to a CMX card via its two front panel connectors.

On the CMM card two sets of 33 LVDS signals are used as outputs. The CMM operation is based on sending one bit of information on each CTP Output LVDS line for each beam crossing, i.e. one bit every 25 ns or 40 Mbps, with one bit out of the 33 bits in each cable being dedicated to parity.

The CMX is able to send up to 4 bits of information on every LVDS line for every beam crossing, i.e. one bit every 6.25 ns or 160 Mbps. The current usage plan is to operate the CTP Outputs at 40 Mbps.

The direction of the LVDS transceivers used for each CTP Output connector is controllable from the BF FPGA (or the TP FPGA when present), and each cable can be controlled independently to operate as input or output. This feature is useful during initial card testing and commissioning. The CMM provides boundary scan for this port, but CMX test firmware and loopback cables can be used to achieve a similar test feature.

2.3 Increased Processing Power

One motivation for redesigning the CMM module using newer FPGA technology is that more logic blocks and thus more processing power is available on the CMX than on CMM by a factor of between 1 and 2 orders of magnitude, depending on what is being considered cf. Figure 2.

This document does not attempt to explore the possible usage of these resources which may include implementing thresholds on CMX in addition to those available on JEM and CPM.

	Part Number	XC6VLX550T
	EasyPath™ FPGA Cost Reduction Solutions(1)	XCE6VLX550T
Logic Resources	Slices(2)	85,920
	Logic Cells(3)	549,888
	CLB Flip-Flops	687,360
Memory Resources	Maximum Distributed RAM (Kb)	6,200
	Block RAM/FIFO w/ECC (36 Kb each)	632
	Total Block RAM (Kb)	22,752
Clock Resources	Mixed-Mode Clock Managers (MMCM)	18
I/O Resources(4,5)	Maximum Single-Ended I/O	1,200
	Maximum Differential I/O Pairs	600
Embedded Hard IP Resources(6)	DSP48E1 Slices	864
	PCI Express® Interface Blocks	2
	10/100/1000 Ethernet MAC Blocks	4
	GTX Low-Power Transceivers	36
	GTH High-Speed Transceivers	—
Speed Grades	Commercial	-L1, -1, -2
	Extended	-2
	Industrial	-L1, -1
Configuration	Configuration Memory (Mb)	144.1

Figure 2: Resources available on the Virtex-6 XC6VLX550T

2.4 Added Functionality

In addition to reproducing and extending the functionality existing on the CMM card, the CMX card provides new functionality. The main motivation for replacing the CMM cards was to send the backplane input information that is received on the CMX card to an external L1 Topological Processor system (L1topo).

A given CMX card only sees information local to its crate and only information of one type (electron, tau, or jets objects, or energy). The key characteristic of a L1topo system is in concentrating the information from all 12 CMX cards (plus other sources as they become available). Using more complex algorithms L1topo is able to compare and combine information including the full geographic coverage (e.g. for invariant masses or angle of

separation) and combining multiple types of information (e.g. electrons and jets). This document does not discuss the operation or usage of any form of L1topo system.

Originally requested as a backup plan and in case a dedicated L1topo system would not be built or would not become available on time, some Topological Processing ability was proposed for the CMX card (CMX-Topo). The design study described in section 1 was carried out to explore the feasibility in terms of cost and architecture and to come up with a plan to implement this desired feature.

Topological Processing on the CMX platform is no longer likely to be used because a dedicated L1topo has been designed and built. The functionality required for supporting a reduced L1topo system on the CMX platform has still been included for future undefined optional usage. This feature provides some attractive flexibility for interconnecting CMX cards and concentrating in one place information from geographically separate sources. It could for example be viewed as an alternate and higher bandwidth method of connecting Crate CMX cards to their System CMX card. This document does not try to explore the operation or usage of the CMX platform as a L1topo system or for another purpose.

2.4.1 Cluster information sent by each CMX to a Topological Processor

Each CMX card is able to drive 24 independent optical outputs arranged as two 12-fiber optical ribbon cables operating at 6.4 Gbps per fiber using a reference clock synchronous to the LHC clock.

One 12-fiber ribbon used with 8b/10b encoding is needed to send all the raw input backplane data to an external L1topo system. There are however several motivations for processing the raw information so that it can be sent on fewer than 12 fibers from each CMX card. For example one could zero-suppress the input data or perhaps re-order the information to send the highest energy objects first.

The 24 output fibers are ganged in two 12-fiber ribbons, but each of the 24 optical outputs can be independently driven to form arbitrary subsets of e.g. 4 or 6 fibers with each set sending identical or different information to multiple destinations. If some subset(s) of the 12 fibers from a given ribbon need to be split and sent to separate destinations, some kind of external splitting and re-bundling patch panel system will need to be devised and built.

The data format and protocols used over the optical links are described elsewhere.

This additional functionality is implemented by the Base Function FPGA.

2.4.2 Optional limited TP capability included

A second Virtex-6 FPGA and additional circuitry were added to the CMX platform so that it can operate in a manner similar to the standalone L1 Topological Processor (L1Topo) but with a reduced input bandwidth and reduced processing power. Such a system is called CMX-Topo to differentiate it from the full dedicated L1Topo system. This means that a CMX card acting as a CMX-Topo is able to receive the information sent out optically by some (or all) of the other CMX cards of the L1calo system.

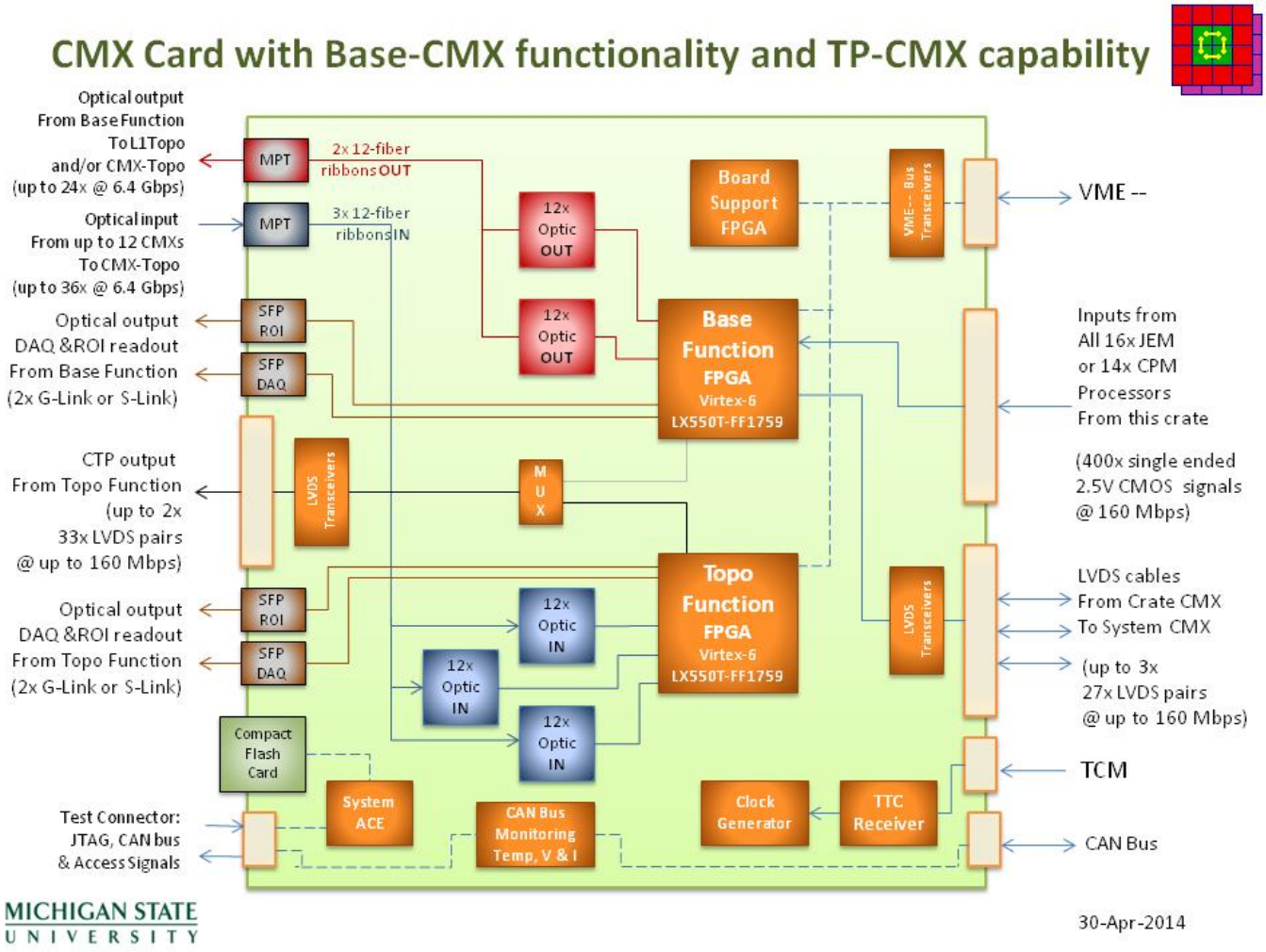


Figure 3: CMX block diagram with TP FPGA installed

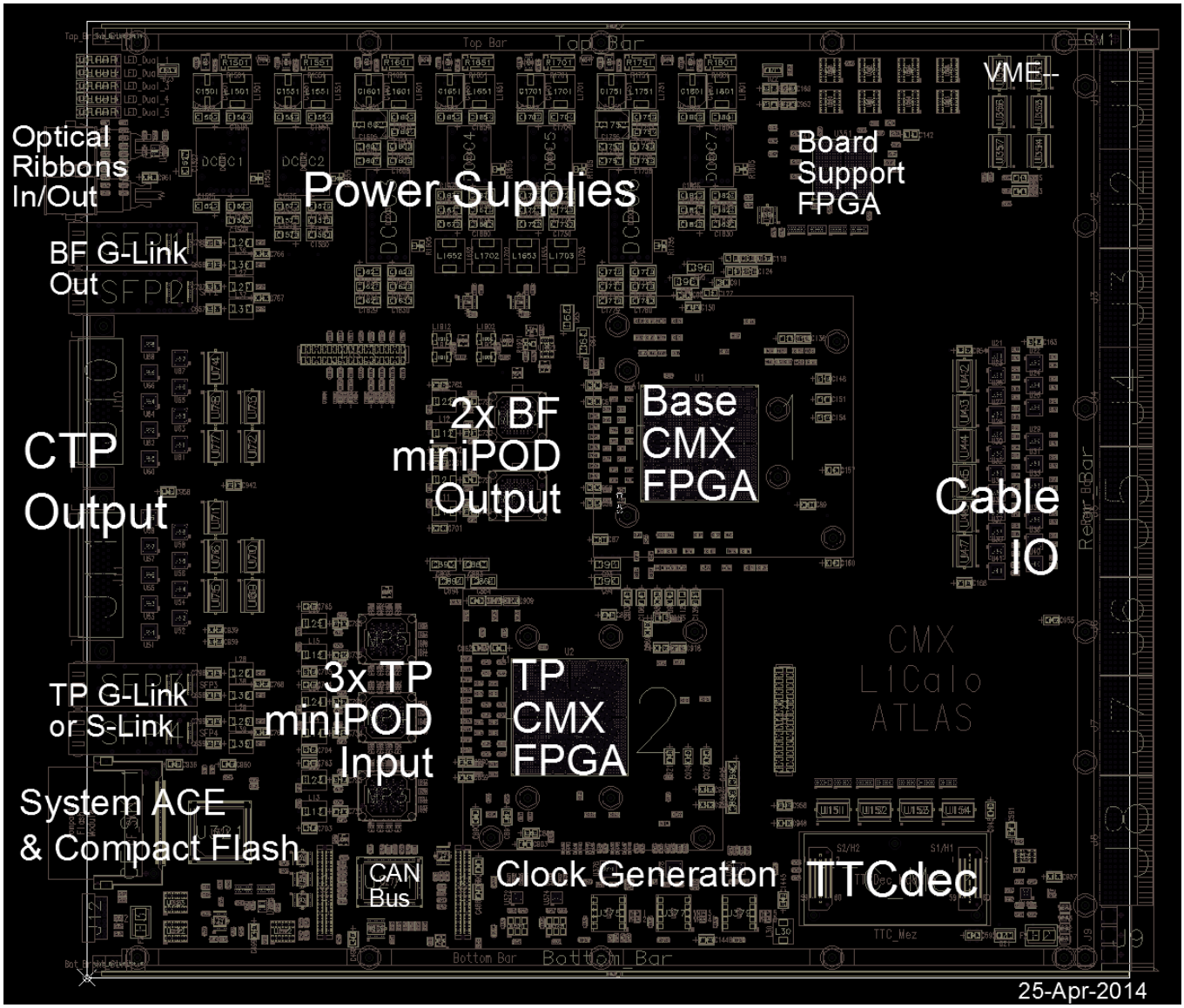


Figure 4: Board Layout view of CMX

The CMX-Topo functionality is implemented in a separate Topological Processing FPGA (Topo FPGA or TP FPGA, cf. Figure 3 and Figure 4). There will be no real-time communication between the BF and TP FPGAs (except for the TP FPGA S-link readout support described in Section 3.7 Optional DAQ and ROI S-link Outputs) and this means that any trigger information from the local BF FPGA that needs to be sent to the TP FPGA on the same card needs to be sent over optical fibers just like the trigger information coming from any other participating CMX card.

Each CMX card acting as a CMX-Topo is able to receive 36 optical inputs arranged as three 12-fiber optical ribbon cables operating at 6.4 Gbps coming from sources that are expected to use a reference clock synchronous to the LHC clock.

The TP FPGA is installed on only a subset of the CMX cards that are being produced (cf. section 7). The absence or presence of the TP FPGA device is the only manufacturing difference between CMX cards providing just Base Function operation and CMX cards providing the additional CMX-Topo capability. All passive sockets for all MiniPOD devices and all passive sockets for SFP transceivers are installed on all CMX cards. This aspect is illustrated in the difference between Figure 1 and Figure 3.

Any CMX card (with or without a TP FPGA) is able to operate as a Crate or System CMX. A CMX card using the CMX-Topo feature in L1calo would most likely need to send information to the CTP system. Atlas could simply elect one of the Crate CMX cards (with otherwise unused CTP output driver resources) for the location of a CMX-Topo system.

2.5 Board Control

Ancillary tasks which are not part of the real-time operation of the CMX card are implemented in a separate smaller FPGA called the Board Support FPGA (BSPT).

The BSPT is responsible for controlling the configuration of the Virtex-6 FPGAs and presents a number of registers on the VME-- Bus to provide control and monitoring of the devices on the board. This function is sometimes referred to as the VME interface, but it is not an interface in the full sense of the word where the VME-- Bus would be on one side and an internal version of the bus would be on the other side. The buffers and level translators form the true physical interface between the VME-- Bus and the On-Card Bus. The BSPT FPGA manages that physical interface. All three FPGAs (BF, TP, and BSPT) are targets for VME-- Bus cycles via the same On-Card Bus and each presents its own set of VME-- addressable registers. More details appear in section 3.

2.6 Additional CMX Features

A number of additional monitor, test and expansion features are available on the CMX card.

1. In addition to CAN Bus monitoring of voltage and currents from the on-board DC-DC power supplies and voltage references, 6 voltage and 6 current test points are routed to 12 of the Virtex 6 System Monitor inputs on the BF FPGA. Cf. Appendix Q: Virtex System Monitor.
2. A complete set of test points for voltages and currents from all on-board DC-DC power supply and Voltage references is accessible on Monitor Connector J13. A test fixture with a rotor switch and a custom cable is used to test prototype and production CMX boards after assembly.
3. 10 spare signals from each of the BSPT, BF and TP FPGA are available on Debug Connector J14. These 30 spare signals can be used with a test probe or even a mezzanine card

4. 2 of the signals routed to connector J14 can be made available as Front-Panel Access Signals. This is described in Appendix T: Front Panel Access Signals.
5. 8 spare signals are routed between the BF FPGA and the BSPT FPGA.
6. 8 spare signals are routed between the TP FPGA and the BSPT FPGA.
7. All signals involved with CAN Bus monitoring are accessible via a pair of connectors suited for a mezzanine board, in case the on-board CAN Bus circuitry needs to be replaced in the future.

3 Real-time Data Path

3.1 Overview and usage in L1calo

There are two separate usages for the CMX cards in the L1calo system. Some CMX cards act as Crate CMX cards and others as System CMX cards. Consequently there are two separate patterns for the real-time data paths possible in the operation of the Base Function tasks performed by the CMX.

There is a total of twelve CMX cards in the full L1calo system inter-connected as 4 groups, with each group handling the trigger information concerning a particular object type: electron, tau, Jet or Energy (cf. Figure 5).

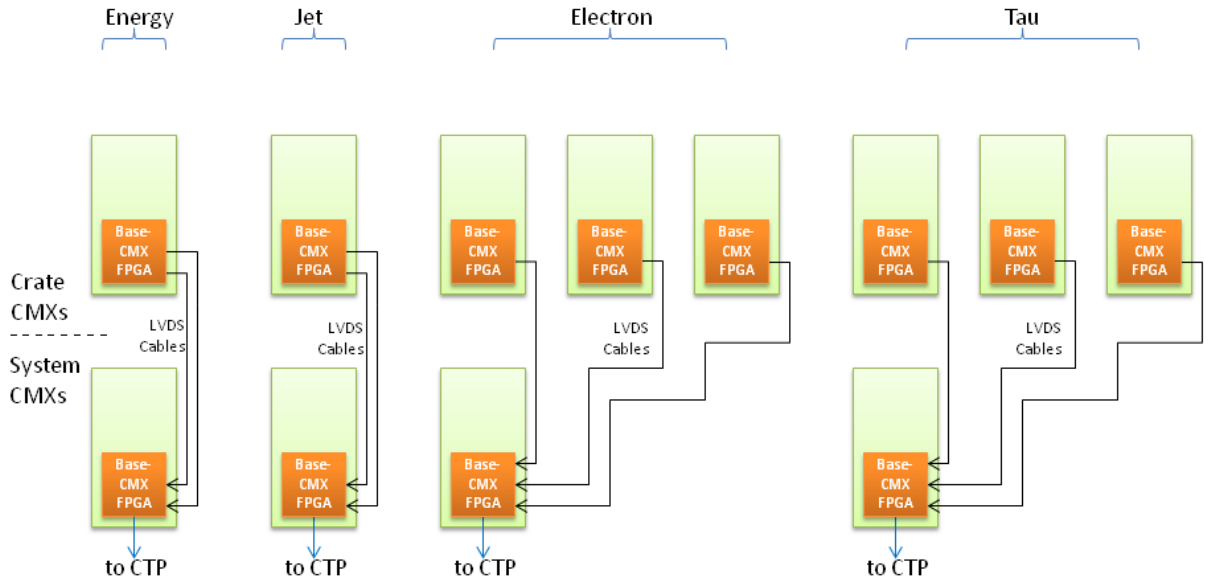


Figure 5: Crate CMX and System CMX arrangement in L1Calo

3.1.1 Crate CMX

A CMX acting as a Crate CMX receives the 400 backplane inputs coming from the 16 processor modules slots in that crate (yellow in Figure 6) and computes local counts of objects before sending that information out through the backplane over one or two LVDS cables to a System CMX (blue in Figure 6).

A Crate CMX (as every CMX card in the L1calo system) also sends this local trigger information out optically to L1topo (green path in Figure 6). Information going to the L1topo is serialized by the Base Function FPGA which drives two Avago MiniPOD optical transmitters. Two 12-fiber ribbon "pigtails" connect the MiniPODs to two MTP feed-through connectors on the front-panel.

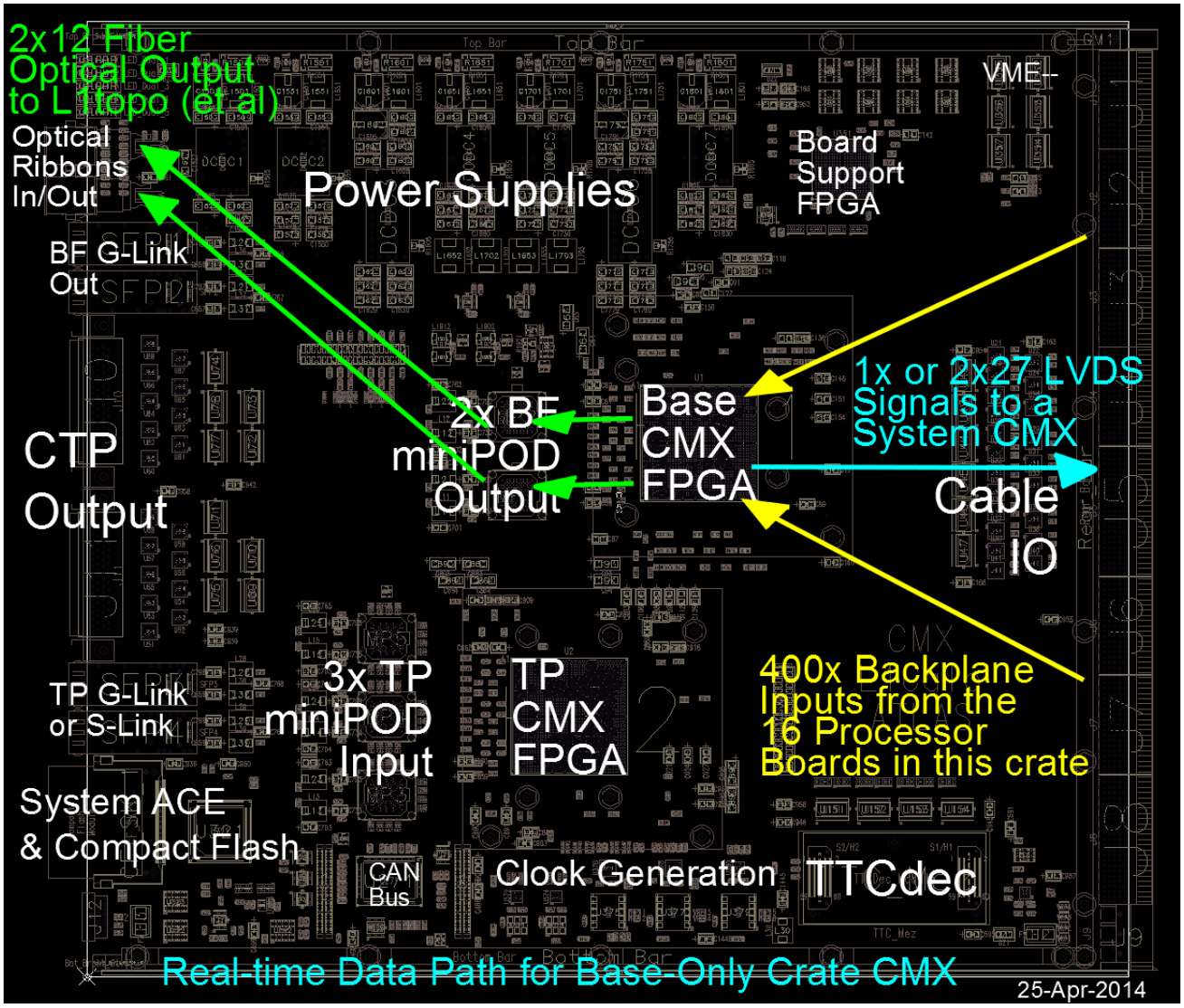


Figure 6: Real-time Data Path for the Base Function on a Crate CMX

3.1.2 System CMX

A CMX acting as a System CMX receives the 400 backplane inputs coming from the processor modules in the crate (yellow in Figure 7) and sends this local trigger information out optically to L1topo (green in Figure 7) exactly like a Crate CMX does.

A System CMX computes its counts of local objects as well but does not send that information out. Rather it merges its own count information with the count information it receives through the backplane over 2 or 3 LVDS cables (cf. Figure 5) coming from all the Crate CMXs handling the same type of information (blue in Figure 7).

A System CMX forms the final trigger information for the object type it handles and sends it to the CTP over 1 or 2 LVDS cables attached to the front panel (red in Figure 7).

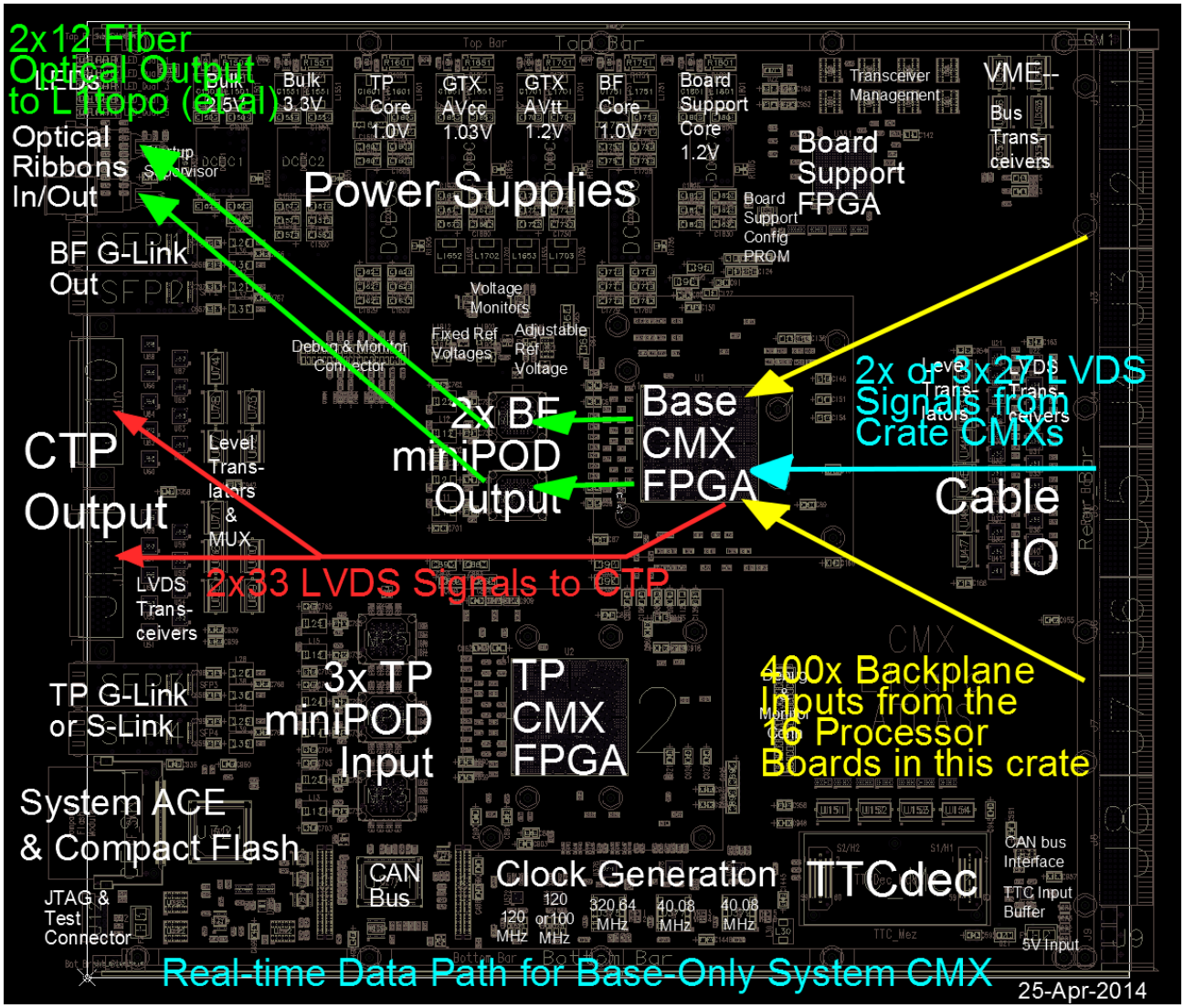


Figure 7: Real-time Data Path for the Base Function on a System CMX

All twelve CMX cards in the full L1calo system send optical information to the external L1topo (green in Figure 6 and Figure 7). This connection could be direct, using one full 12-fiber ribbon from each CMX card. If fewer than 12 fibers are needed from each CMX card (6 fibers as currently planned) a patch panel will be necessary for splitting and re-bundling the 12-fiber ribbons as shown in Figure 8.

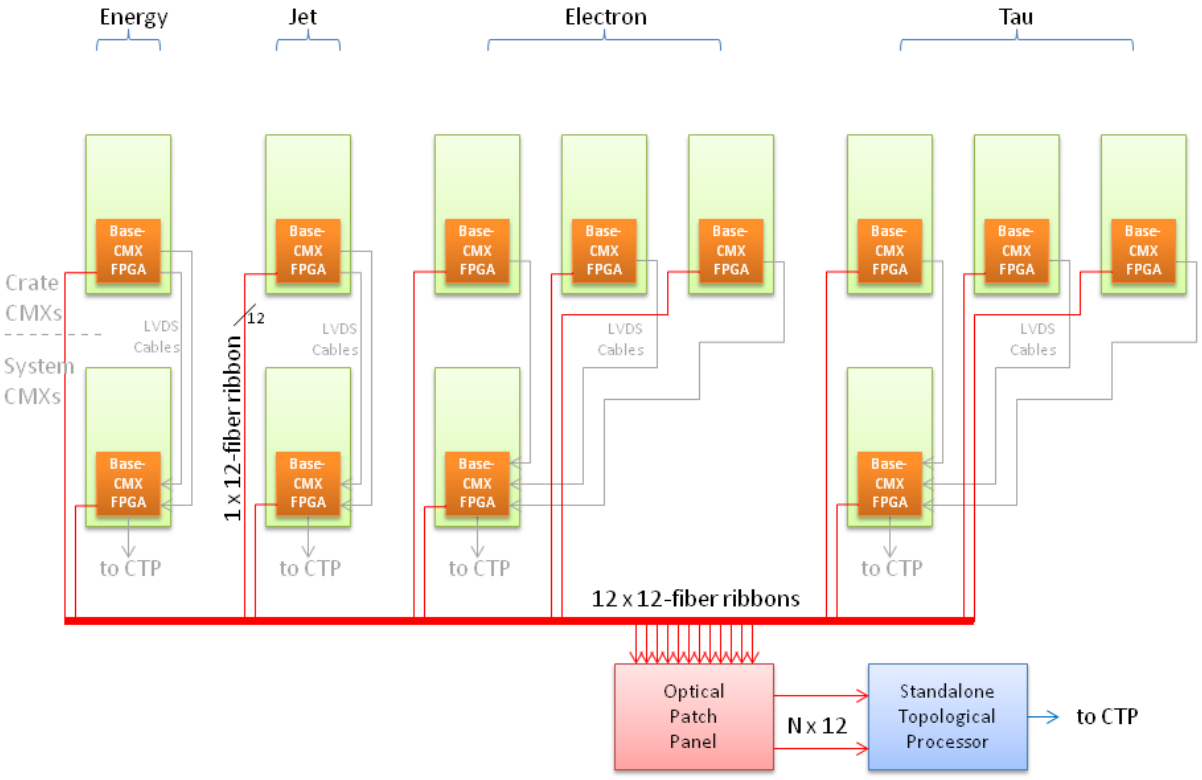


Figure 8: Twelve CMX sending information to L1topo via an optional patch panel

3.1.3 CMX-Topo CMX

A CMX equipped with a TP FPGA can be used as a CMX-Topo system. The Topological Processing functionality is independent from and in addition to the Base functionality but requires sending output to CTP and thus should be used on a Crate CMX card (as opposed to a System CMX card), i.e. on a CMX cards whose Base Function does not already need to use the CTP Output LVDS resources.

The CMX-Topo input information is received over up to three 12-fiber ribbons, translated to electrical signals by three Avago MiniPOD Receivers connected to the TP FPGA (orange in Figure 9). The TP FPGA de-serializes this trigger information, performs all sorting and processing

needed to implement the desired trigger algorithms and sends its results to the CTP over 1 or 2 LVDS cables attached to the front panel connectors (red in Figure 9).

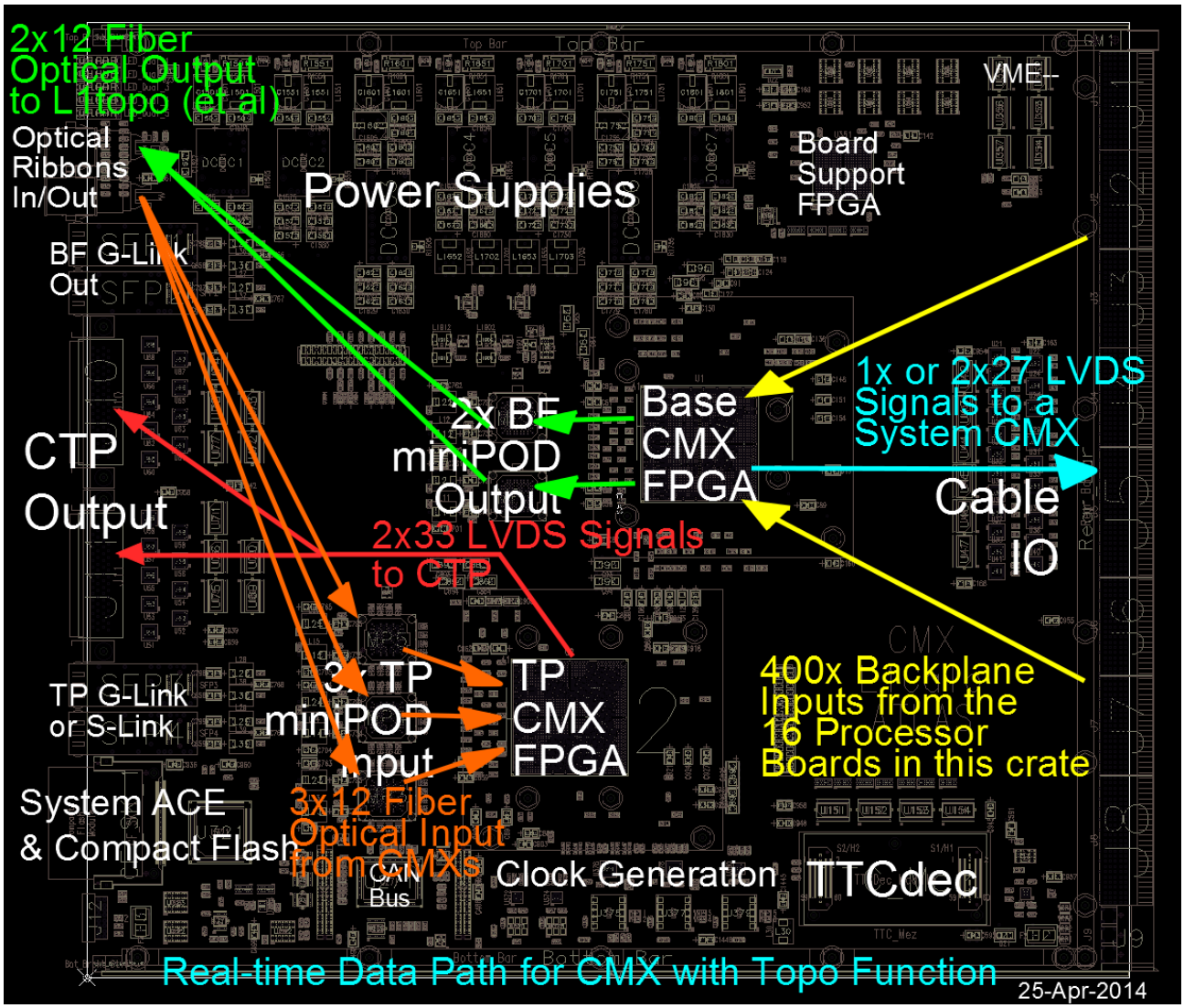


Figure 9: Real-time Data Path for a Crate CMX also using its TP Function

All or a subset of the twelve CMX cards in the L1calo system may send input information to the CMX-Topo. A source CMX card sends its information out on a 12-fiber ribbon and a patch panel would presumably be required to split a subset of the 12 fibers from each source CMX and re-bundle the resulting set of fibers in up to three 12-fiber ribbons that can then be connected to a CMX-Topo.

More than one CMX-Topo instances could operate independently and in parallel if desired, as illustrated in Figure 10.

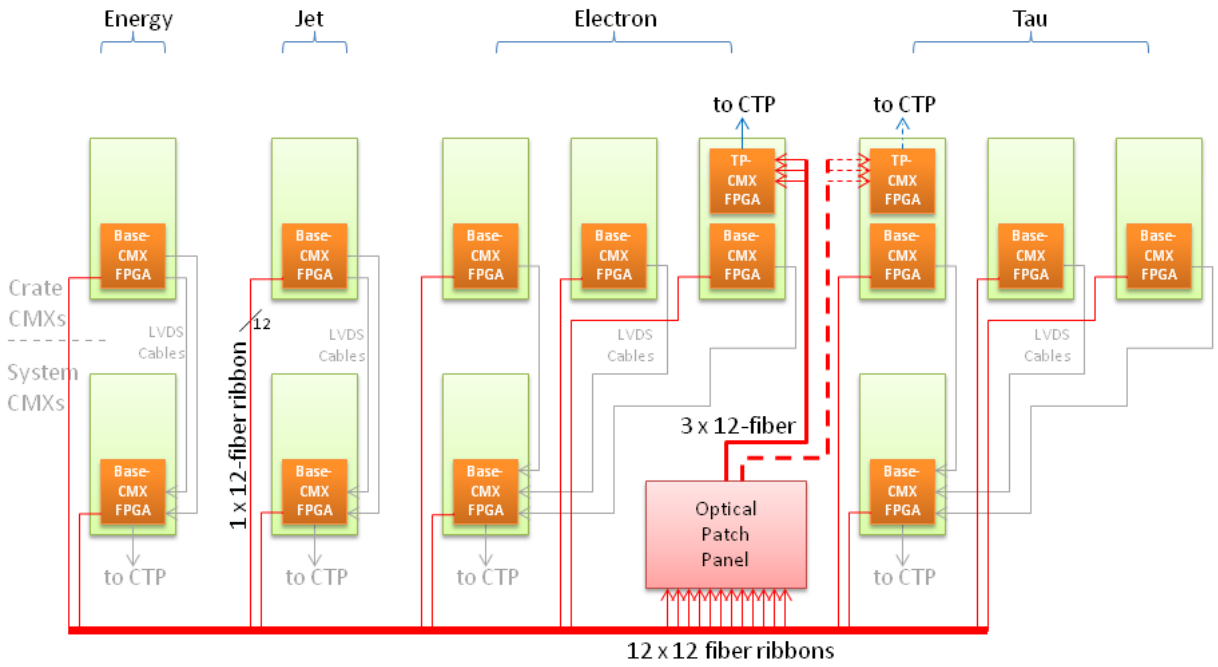


Figure 10: Twelve CMX cards sending TP information to one (or more) CMX-Topo

The standalone L1topo and a CMX-Topo could also be used at the same time, as illustrated in Figure 11.

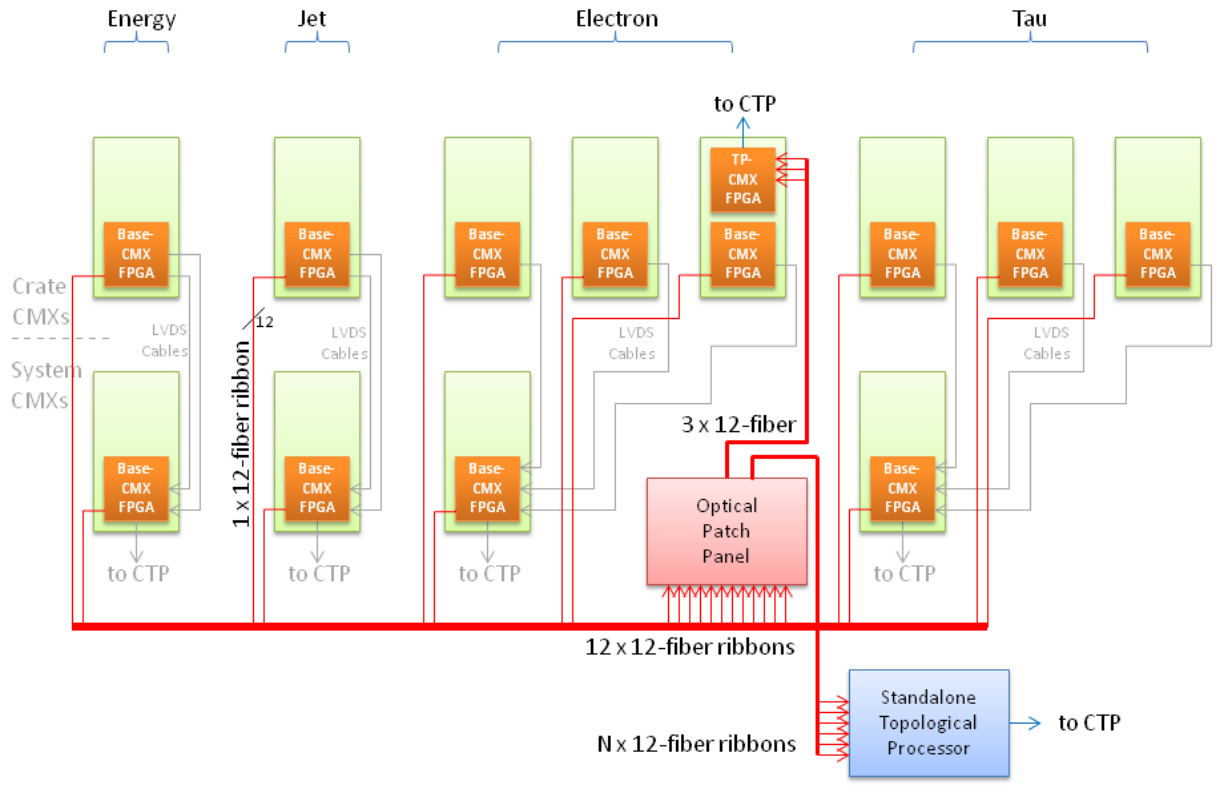


Figure 11: Twelve CMX cards sending TP information to a Standalone L1topo and a CMX-Topo

3.2 Backplane Inputs

The CMX card receives 400 (25 from each of the 16 Processor modules in the crate) source terminated single-ended signals with a line impedance nominally specified as 60 Ohms. The Phase 0 upgrade involves an increase in line rate on these 400 lines from the current 40 Mbps to 160 Mbps, i.e. 6.25 ns per bit of information transferred.

These signals are routed directly from the backplane to the Base Function FPGA. Every known precaution has been taken to maintain signal integrity and insure signal recovery for all 400 inputs.

In each group of contiguous IO banks handling one set of Processor inputs, one pair of VRN and VRP IO pins has been connected to a pair of external resistors to provide the reference impedance for the line termination implemented by the Virtex-6 Digitally Control Impedance (DCI) technology. This feature was implemented and is available as needed to help with the reception of the 400 Processor input signals.

For all IO banks handling Processor inputs the VREF pins are connected to an adjustable power supply on the card which provides a reference voltage of 1.25 V +/- 0.5 V. This feature allows for fine control of the threshold voltage used with the differential input receiver of the Select IO pins used for the 400 backplane inputs. This adjustable reference voltage lets us adjust the threshold to something other than the middle of the 0-2.5 V logic range if difficulties are encountered at the 160 Mbps line rate.

The PDR document specified that one signal from each set of 25 input signals is to be used as a combined clock and parity signal and that the incoming clock and timing information should be recovered from this clock/parity signal. This protocol had the advantage of dedicating only one of the 25 lines for a purpose other than carrying trigger information thus leaving 4*24 bits (for a 160 Mbps line rate) of information available from each source for each beam crossing. Implementing this clock/parity communication protocol would require using one Mixed-Mode Clock Manager (MMCM) per source Processor Module.

After extensive firmware studies it became apparent that (1) the MMCM used had to be on the same horizontal row of the FPGA logic architecture as the clock/parity line it serves, (2) the IO banks used to receive all backplane inputs had to be on the inner vertical rows of logic inside the FPGA and (3) the clock/parity lines had to be connected to regional clock inputs to be compatible with all proposed clocking schemes. After several iterations a satisfactory allocation of the IO banks and IO pins was found that satisfied board layout constraints while only using the inner columns of IO banks for the processor inputs and while requiring only two Regional

Clocks per horizontal row to match the distribution of MMCMs per horizontal row, as illustrated in Figure 12.

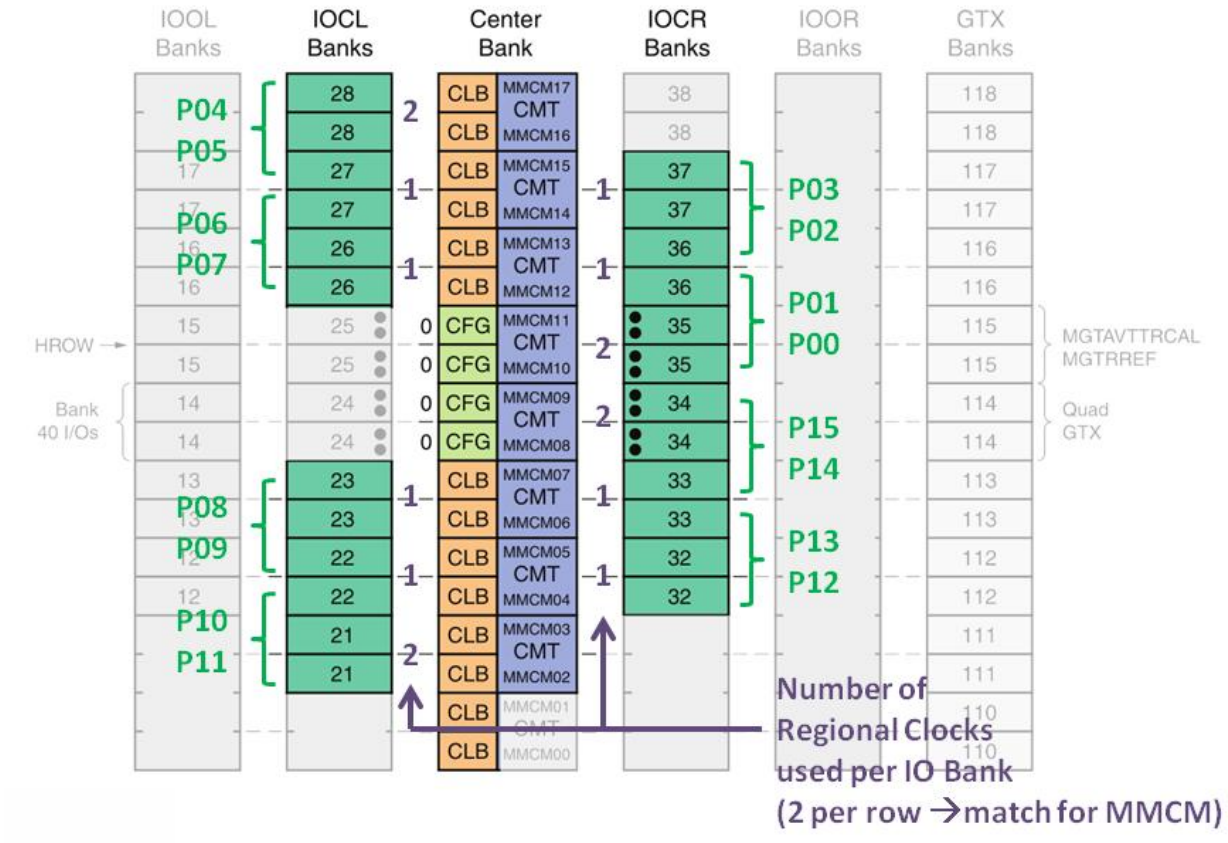


Figure 12: IO Banks Allocation for the 16 sets of Processor inputs

Using this merged clock/parity scheme would use 16 of the 18 MMCM resources of the Virtex-6 leaving two MMCMs for all logic processing and MGT operation on the Base Function FPGA. The merged clock/parity scheme is no longer expected to be used in L1calo but the CMX card has been designed to be compatible with this protocol as defined in the PDR.

The current protocol uses 23 lines to carry data, one line to carry parity and uses the 25th line as a dedicated clock signal switching at 160 Mbps, i.e. an 80 MHz clock. The input data will be latched according to both the rising and falling edges of this clock signal. The input data comes from each source module with some fixed timing skew among the data and parity lines with respect to the clock edges. With an input signal switching every 6.25 ns the valid window for latching the information might only be 1-2 ns wide. If necessary we can use the IODELAY technology available on the Virtex-6 FPGA and individually adjust the time when each input line is being latched with respect to the clock edges. Offline measurements can be done to seek the optimum IODELAY for each of the 400 backplane signals. These values will likely need to be

determined in situ for each crate, but are expected to remain stable until the CMX or one of the Processor Modules in the crate needs to be replaced.

Maintaining the 60 Ohm line impedance over the full signal trace path turned out not to be practical. In order to maximize signal integrity, the original intention was to route all 400 trace signals on internal layers straight from the backplane pin to a via located under the FPGA select IO pin receiving that signal without any additional via in-between. A solution was found that solved the topological requirements and used 10 internal signal layers. It was however not possible to build a card with that many signal layers and still able to support 60 Ohm traces of reasonable width. The higher thickness of dielectric required and number of trace layers would have lead to a total board thickness not practical for a VME card.

The next best strategy was chosen which uses fewer trace layers in general and fewer 60 Ohm trace layers in particular. For all 400 backplane signals either **all** of the trace path to the Select IO pin or **most** of the trace path from the backplane pin to within about 1 cm of the Select IO pin is routed with a 60 Ohm trace. A fraction of the backplane signal traces switch from the carefully controlled 60 Ohm environment for the last ~1cm of the run. This method requires careful management of the resulting "ring of vias" required near the FPGA so that they can be located close to the FPGA perimeter without impeding the path of the majority of the traces routed directly under their target Select IO pins. Short and angled rows of 6 to 8 vias provide these internal access channels.

The CMX card has 7 internal signal layers and 3 power plane layers in addition to the top and bottom signal layers. 5 of the internal layers are compatible with 60 Ohm traces while the top, bottom and the other 3 layers don't need to be.

In summary:

- All backplane input signal traces are routed from their backplane pin to within 1 cm of the FPGA perimeter on 60 Ohm traces located on internal signal layers situated between two ground planes.
- 265 traces (66%) reach all the way to the via located next to the FPGA pin
- 136 traces (34%) need to switch layers near the FPGA.
- 113 traces (28%) include a short ~1cm segment not matching 60 Ohm.
- All forwarded clock lines remain on 60 Ohm traces and do not switch layer

A spice model of a complete transmission line was created to verify that a an impedance bump on the last 2 cm of the 60 Ohm line had very little impact on signal integrity.

Section 6 provides more details on the CMX card layers and further details concerning routing of signals on CMX are available in Appendix V: Layout Details.

3.3 Cable IO

A Crate CMX needs to send its local counts information to a System CMX for merging into global counts.

This communication if performed over 34 pair LVDS cables connected to Rear Transmission Modules (RTM) plugged in the back of the crate. Only 27 of the 34 signal pairs from each cable are currently accessible to the BF FPGA for a total of 81 differential signals passing through the backplane which are named in the same way as on the CMM card i.e. M_<N>+ and M<N>- with <n>=0 to 80.

The CMX uses National Semiconductor DS91M040 LVDS transceivers which are 3.3V devices rated at 250 Mbps. The Virtex-6 IO banks cannot provide 3.3V logic levels so Texas Instrument 74AVCAH164245 level translators are used as an interface between the 2.5V logic levels of the FPGA and the LVDS transceivers. The bidirectional level translators and LVDS transceivers for each cable are managed separately. Even though the operation of any CMX cards in L1calo requires that all cables being used (1, 2 or 3 cables being used on different CMX cards) be operated in one common direction, the CMX provides independent direction control from the Base Function FPGA. This feature is used for test and maintenance of individual boards. Short 100 Ohm differential traces are routed between the transceivers and the backplane pins on internal layers sandwiched between ground planes. The CMX provides a 100 Ohm differential termination on each line while the DS91M040 drivers provide twice the normal LVDS output current to be able to drive these doubly-terminated CMX to CMX transmission lines.

The RTM schematic shows the LVDS signals names with their assignments to the three cable connectors:

Connector 1		Connector 2		Connector 3	
pair	signal	pair	signal	pair	signal
01	M_00	01	M_27	01	M_54
02	M_01	02	M_28	02	M_55
03	M_02	03	M_29	03	M_56
04	M_03	04	M_30	04	M_57
05	M_04	05	M_31	05	M_58
06	M_05	06	M_32	06	M_59
07	M_06	06	M_33	06	M_60
08	M_07	08	M_34	08	M_61
09	M_08	09	M_35	09	M_62
10	M_09	10	M_36	10	M_63
11	M_10	11	M_37	11	M_64
12	M_11	12	M_38	12	M_65
13	M_12	13	M_39	13	M_66
14	M_13	14	M_40	14	M_67
15	M_14	15	M_41	15	M_68
16	M_15	16	M_42	16	M_69

```
17    M_16        16    M_43        16    M_70
18    M_17        18    M_44        18    M_71
19    M_18        19    M_45        19    M_72
20    M_19        20    M_46        20    M_73
21    M_20        21    M_47        21    M_74
22    M_21        22    M_50 *      22    M_75
23    M_22        23    M_51        23    M_76
24    M_23        24    M_52        24    M_77
25    M_24        25    M_53        25    M_80 *
26    term        26    term        26    term
27    term        26    term        26    term
28    term        28    term        28    term
29    term        29    term        29    term
30    term        30    term        30    term
31    term        31    term        31    term
32    M_25        32    M_48        32    M_78  <-- reserved for use as clock signal
33    M_26        33    M_49        33    M_79  <-- used for parity on all 3 cables
34    GND         34    GND         34    GND

term = 100 ohm termination across the differential pair on the RTM
*    = numbering discontinuities (for some historical cause unknown to us)
```

The L1calo backplane defines three more LVDS IO signals (namely M_81+, M_81-, M_82+, M_82-, M_83+, and M_83-) which are not routed on the CMM card and not routed on the RTM card. All three of these differential signals are routed on the CMX card with one bit assigned to each LVDS Cable. These additional bits could be made available for communication between Crate and System CMX if necessary, but taking advantage of these additional signals would require that new RTM modules be produced. The LVDS transceivers used (National Semiconductor DS91M040) are able to safely default to a defined state when no input signal is present.

The circuit diagram for this part of the circuitry and further details regarding the LVDS connections is found in Appendix D: LVDS Connections.

3.4 CTP Output

A System CMX or a CMX acting as CMX-Topo needs to send information to the Central Trigger Processor (CTP). This output is available on two 33-pair LVDS ports accessible on the front panel. This access port uses two 68-pin 3M MDR connectors. The 34th pair on each connector and connected cable can be left unused or grounded on the CMX.

Although normally used as an output, each CTP connector can be independently operated as input or output communicating with either the BF or TP FPGA. This features is used for testing and diagnostics. The same LVDS transceivers and level translator parts used for the cable IO described above are used for the CTP output.

Two sets of 33 LVDS signals (i.e. 66 differential signals named CN_CTP_<NN>P and CN_CTP_<NN>N on CMM but CN_CTP_<NN>_POS and CN_CTP_<NN>_NEG on CMX, with <NN>=00 to 65) are currently used. One bit on each cable is used for parity (namely <NN>=32 and 64). On CMX one bit from each cable (namely <NN> = 31 and 63) has been routed to a regional clock pin of the FPGA so that it can be used as a forwarded clock signal if needed.

On a System CMX the BF FPGA needs to drive the CTP Output while on a Crate CMX also acting as a CMX-Topo CMX the TP FPGA needs to drive the CTP Output. The required multiplexing is performed by the same 74AVCAH164245 ICs already providing the logic level translation.

The circuit diagram for this part of the circuitry and further details regarding the LVDS connections are found in Appendix D: LVDS Connections.

3.5 High Speed optical

All CMX cards used in L1calo need to send high-speed (6.4 Gbps) optical information out to the standalone L1topo (and optionally to a CMX-Topo). Two AFBR-821FH1Z Avago MiniPOD transmitter devices connected to the BF FPGA can drive up to 24 optical fibers arranged as two 12-fiber ribbons.

A CMX card acting as a CMX-Topo needs to receive high-speed (6.4 Gbps) optical information from (presumably) other CMX cards. Three AFBR-811FH1Z Avago MiniPOD receiver devices connected to the TP FPGA can receive up to 36 optical fibers arranged as three 12-fiber ribbons.

Two USCONEC MTP feed-through connectors mounted on the front-panel provide access to all optical inputs and outputs. The connection between the MiniPODs and the front-panel MTP feed-through connector is made with short “pigtail” cables with a Prizm connector at the MiniPOD end and an male MTP connector for the front-panel end. If the CMX card is not using its optional TP functionality then each 12-fiber output ribbon is simply connected to one of the two available front-panel MTP feed-through connectors. If a particular CMX card is required to use its TP functionality in L1calo then both output 12-fiber ribbons will need to be connected to one of the front-panel MTP feed-through connectors and all three input 12-fiber ribbons will need to be connected to the other MTP feed-through connector, using custom “octopus” Prizm cables with 24 and 36 fiber MTP connectors. There is no current plan for using the CMX TP functionality in L1calo and no octopus cable has thus been purchased. In all use cases, the CMX card is equipped with male MTP connectors.

The 14.5mm height of the MiniPOD devices was a potential issue for use in the VME environment. The mechanical-only CMX prototype was fitted with MiniPOD devices and inserted in the test stand of CERN Building 104 to verify that proper clearance was indeed

available with respect to all modules that can be neighbors to CMX modules. The height of the MiniPOD also precludes using the standard type of heat sink sold by Avago because it is designed to be clipped onto the top of the MiniPOD. A custom heat sink was designed for the MiniPODs forming a crown surrounding the device without adding any height to it.

The circuit diagram for this part of the circuitry and further details regarding the high-speed connections is found in Appendix E: High-Speed Optical.

3.6 DAQ and ROI G-link Outputs

All CMX cards need to send their DAQ readout information to a DAQ ROD and a System CMX additionally needs to send ROI readout information to an ROI ROD. These connections use the G-link protocol and two SFP optical transceivers are connected to the BF FPGA for that purpose. The Virtex-6 performs the G-link encoding of the data sent to the transmitter sections of the SFP transceiver modules.

A CMX card acting as a CMX-Topo also needs to send DAQ and ROI information to ROD cards. A separate pair of SFP transceivers is connected to the TP FPGA for that purpose.

The 40.08 MHz clock locked to the LHC frequency cannot be used to drive the G-link connection and the CMX card is equipped with a separate crystal with a fixed clock frequency of 120.00 MHz distributed to the necessary BF and TP MGT quads for that specific purpose.

The circuit diagram for this part of the circuitry and further details regarding the low-speed connections is found in Appendix F: Low-Speed Optical.

3.7 Optional DAQ and ROI S-link Outputs

If a CMX-Topo system is needed in L1Calo but no ROD channel is available for DAQ and ROI readout, then the CMX-Topo CMX will need act as its own ROD. This means that the CMX TP FPGA must support the S-link protocol for DAQ and ROI readout. This requirement added the following specifications:

- All the TTCdec signals needed for ROD functionality are made available to the TP FPGA
- To handle the S-link Return Channel the receiver channels all SFP modules are connected to Virtex-6 MGT receivers, with the added complexity described below.
- A separate fixed frequency of 100.00 MHz must be sent to the appropriate BF and TP FPGA MGT transceiver Quads to support the S-link protocol for the TP FPGA even while the BF FPGA readout is using the G-link protocol.

There are no spare MGT receiver channels available on the TP FPGA. All 36 MGT receiver channels from the TP FPGA are used for the 3 MiniPOD receivers. The BF FPGA, on the other hand, has many spare MGT receiver channels as at it is mostly acting as an MGT data source. The SFP receiver channels from the DAQ and ROI SFP modules associated with the TP function must thus be connected to MGT receivers on the BF FPGA, and furthermore all SFP receiver channels are connected to MGT receivers on the BF FPGA. This constraint adds a level of complexity as it is the TP FPGA that may need to act as its own ROD and thus listen to the S-Link Return Channel information. Two differential signals were connected for that purpose between the BF FPGA and the TP FPGA. These two high speed signals can be used to forward the raw or decoded S-link Return Channel data from the BF FPGA to the TP FPGA.

S-link operation has not been tested. Such test would require extensive firmware effort while there are no current plans to use S-link reaodut.

3.8 Topological Processing on CMX

A CMX acting as a CMX-Topo includes a TP FPGA, three MiniPOD receivers, and two SFP transceivers which are otherwise not installed on the vast majority of the CMX cards. The TP FPGA receives its inputs over (up to) three 12-fiber optical ribbons and has access to the CTP Output LVDS connectors. The TP FPGA is accessible from VME-- over the On-Card Bus (cf. below) for programming and monitoring purposes.

Note that no triggering information can be exchanged electrically between the BF and TP FPGAs on a CMX card. Any exchange of per event triggering information must happen through optical outputs from the BF FPGA connected to optical inputs to the TP FPGA.

Topological Processing on CMX and TP algorithms for CMX-Topo are not described in this hardware description document. The IO bank assignment for the TP FPGA is shown in Appendix C: IO Banks Assignments for BF and TP FPGA.

4 Board Control, Configuration and Monitoring

4.1 Clocks

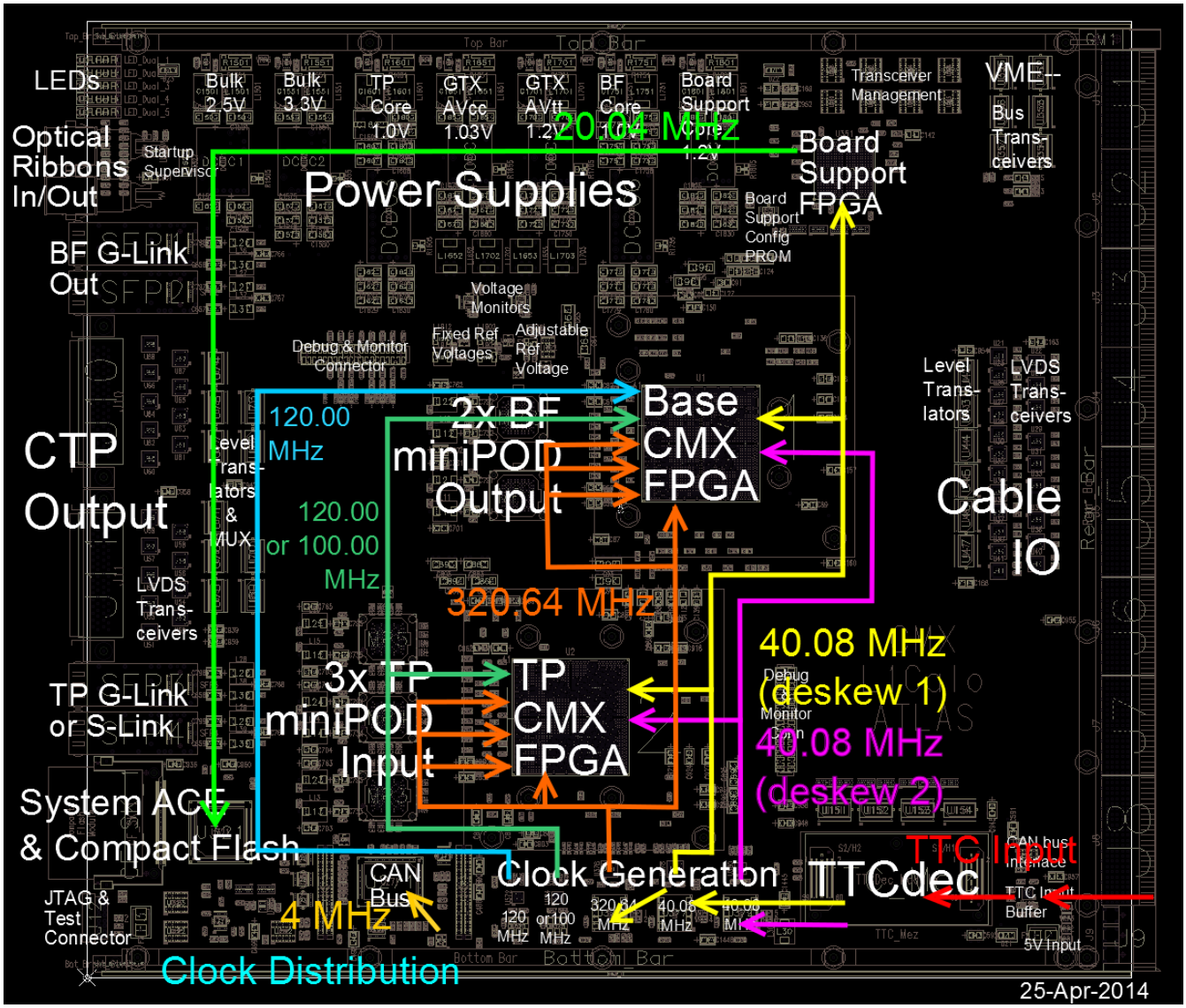


Figure 13: CMX Clock generation and distribution

The CMX card is designed to be equipped with a TTCDec mezzanine card. The CMX uses two custom narrow-range Connor-Winfield PLL Clocks to generate clean copies of both versions of the 40.08 MHz accelerator clock available as outputs from the TTCDec. These TTCDec clock

signals Clock40Des1 and Clock40Des2 track the LHC clock with programmable and controlled phases. Clock fanout buffers distribute these two 40.08 MHz clocks. The BSPT FPGA receives one copy of only Clock40Des1 while the BF and TP FPGAs receive copies of both Clock40Des1 and Clock40Des2. The Clock40Des1 clock is also used to drive a third custom narrow-range Connor-Winfield PLL Clock generating a 320.64 MHz LHC-locked clock. This 320.64 MHz is buffered and distributed to the BF and TP FPGAs as a logic clock and also made available to the MGT quads driving or receiving the MiniPOD channels. One copy is sent to the middle Quad of every group of three Quads handling each set of 12 MGT channels connected to a MiniPOD, i.e. 2 copies are sent to BF FPGA MGT Quads and 3 copies to TP FPGA MGT Quads.

In addition to the three LHC-tracking clocks above, the CMX is also equipped with three fixed frequency crystal oscillators:

- One fixed 120.00 MHz clock is sent to one BF FPGA MGT Quad to support the G-link protocol on the SFP DAQ and ROI outputs from the BF FPGA.
- A second site is equipped with either a fixed 120.00 MHz or 100.00 MHz clock depending on the protocol that needs to be supported for the SFP DAQ and ROI outputs from the TP FPGA, cf. section 3.7 Optional DAQ and ROI S-link Outputs for more details. This clock is sent to one MGT Quad from each of the BF and TP FPGAs.
- One fixed 4 MHz crystal used with the CAN Bus processor.

All control and output lines of the TTCDec mezzanine card are connected to the BSPT FPGA which manages the TTCDec operation. On the CMM only the Bunch Counter Reset and the L1accept signal from the TTCDec are connected to its FPGAs. The CMX connects only these same two lines to the BF FPGA, but provides all the TTCDec signals to the TP FPGA in case they are needed to support S-Link operation. Level Translators are used to interface the TTCDec module to the 2.5V logic levels used at the three FPGAs on CMX.

The System ACE also requires a clock to operate. This clock is provided by the BSPT FPGA in order to allow proper synchronous access to the System ACE Microprocessor Interface by the BSPT firmware. The BSPT firmware uses its input clock (the copy of the Clock40Des1 LHC clock listed above) to derive the 20.04 MHz sent to the System ACE.

The circuit diagram for the TTCDec mezzanine connections and further details regarding the usage of the TTCDec are found in Appendix G: TTCDec data distribution.

The circuit diagram for the clock generation and further details regarding this section of the CMX are found in Appendix H: Clock Generation and Distribution.

4.2 Board Support FPGA

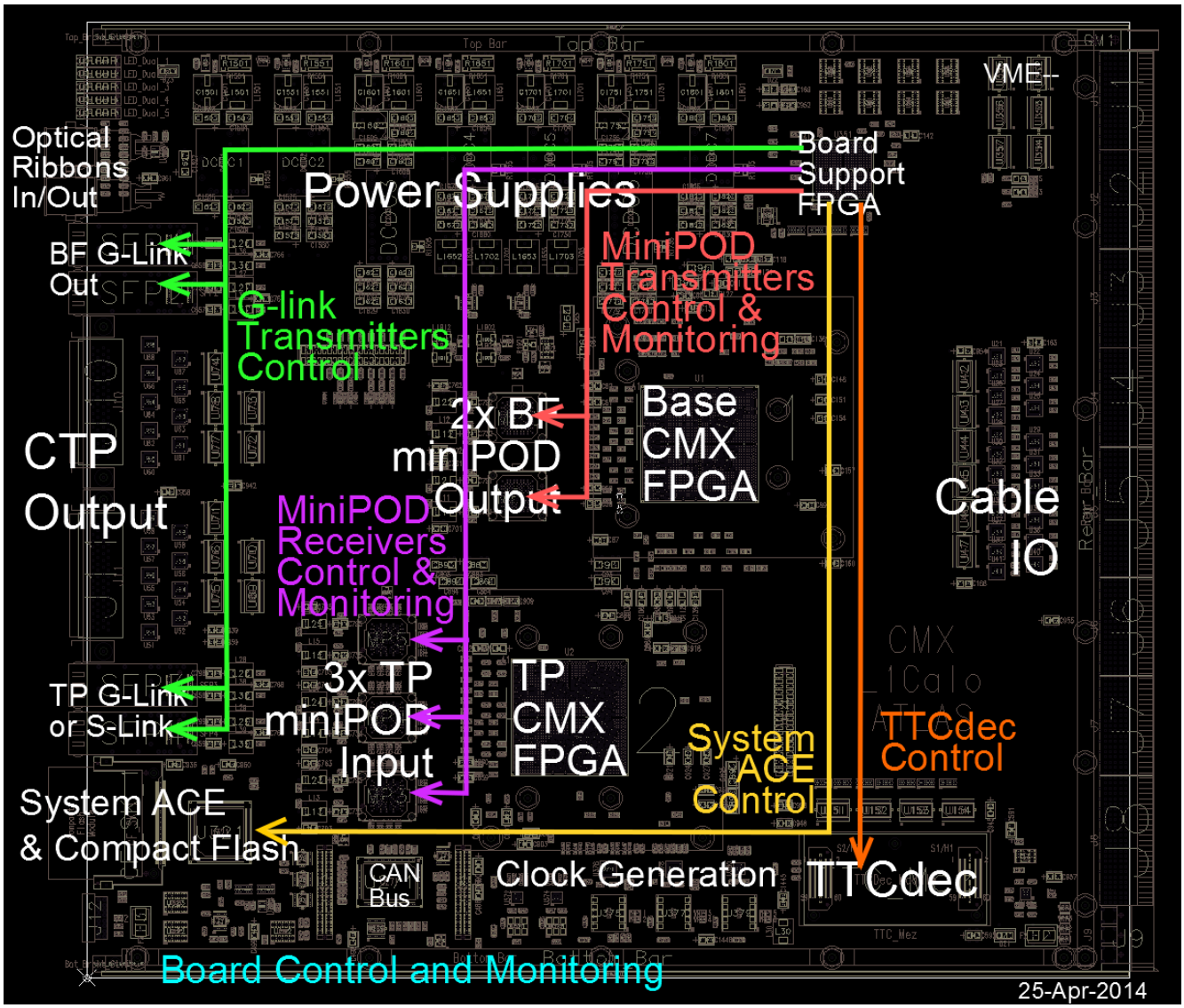


Figure 14: CMX Board Control and Monitoring

The device chosen for the Board Support FPGA (BSPT) is a Xilinx Spartan-3A XC3S400A in the 400 pin FG400 package. It is a larger version of the same device used for the VAT prototype support project.

The Board Control FPGA is responsible for

1. controlling the operation of the System ACE and thus configuration of the main FPGAs
2. controlling and monitoring the operation of the TTCDec
3. controlling and monitoring the MiniPOD transmitters and receivers
4. controlling and monitoring the SFP optical modules

5. presenting registers in VME-- space to access all above control and monitoring features
6. controlling the data bus transceivers to the VME-- bus
7. generating DTACK_B during VME-- Cycles
8. detecting the presence of and configuration of the BF and TP FPGA
9. provide logic as part of the hardwired Transceiver Control Oversight (below)
10. controlling all the front-panel LEDs except one (power)

System ACE Configuration is described below and in Appendix J: JTAG Chains and FPGA Configuration.

The TTCDec data connections are described in Appendix G: TTCDec data distribution.

The MiniPOD control and monitoring aspects are described in Appendix E: High-Speed Optical.

The G-Link control and monitoring aspects are described in Appendix F: Low-Speed Optical

The On-Card Bus is described in section 4.3 VME-- Bus and On-Card Busand in Appendix I: VME-- and On-Card Bus.

The transceiver control oversight is described in section 4.6 Transceiver Control.

The CMX Card offers fewer LEDs than CMM because of the limited front-panel space left for that purpose. Two rows of 5 LEDs are available on the CMX front-panel. In order to maximize flexibility during testing and online operation and to postpone the hard choices to be made, all but one of the front-panel LEDs are “firmware-defined” by the BSPT FPGA. The BF and TP FPGAs send request signals (nominally 5 LED request signals from each FPGA) to the BSPT FPGA.

One front-panel green LED is hardwired to show when the CMX has determined that all its on-board power supplies are operating properly. The rest of the front-panel LEDs are all firmware-controlled:

- 3 green LEDs
- 6 dual color Green/Red LEDs

The LED support circuitry is described in Appendix S: Front Panel.

4.3 VME-- Bus and On-Card Bus

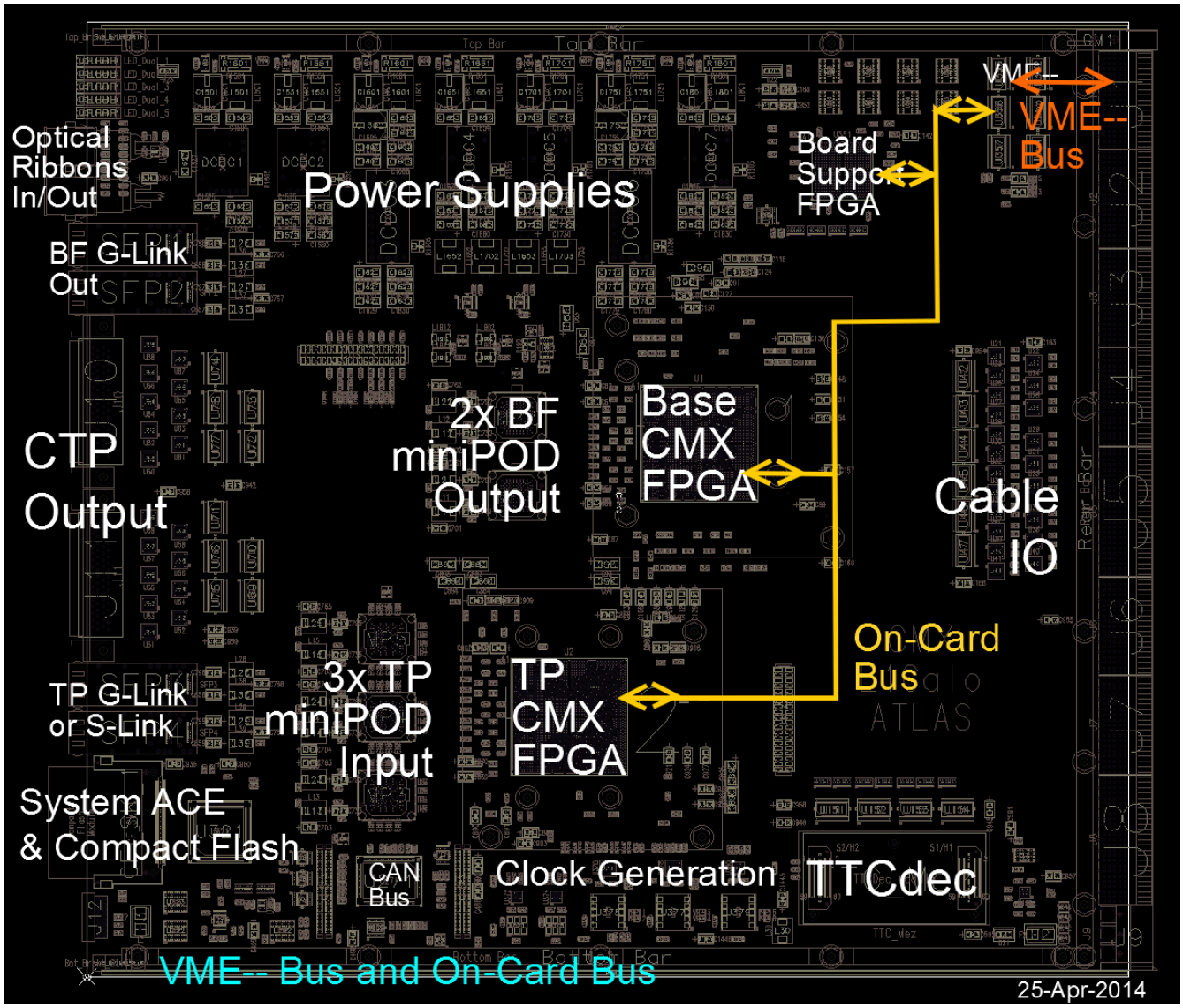


Figure 15: CMX On-Card Bus

The VME-- Bus to On-Card Bus interface is implemented in two steps with VME buffers and level translators. The level translators are used to connect the 2.5V On-Card bus to the 3.3V signals required by the VME drivers and receivers.

All three FPGAs are targets on the On-Card Bus (as illustrated in Figure 15) making them able to implement VME-- addressable registers.

Geographic Addresses #0, 4, 5 and 6 are provided through the backplane while Geographic Addresses #1, 2, and 3 are controlled by 3 jumpers on the card. All Geographic Address signals are available to all three FPGAs and to the TTCDec module.

The circuit diagram for the On-Card Bus and further details regarding this section of the CMX are found in Appendix I: VME-- and On-Card Bus.

4.4 JTAG Chains and FPGA Configuration

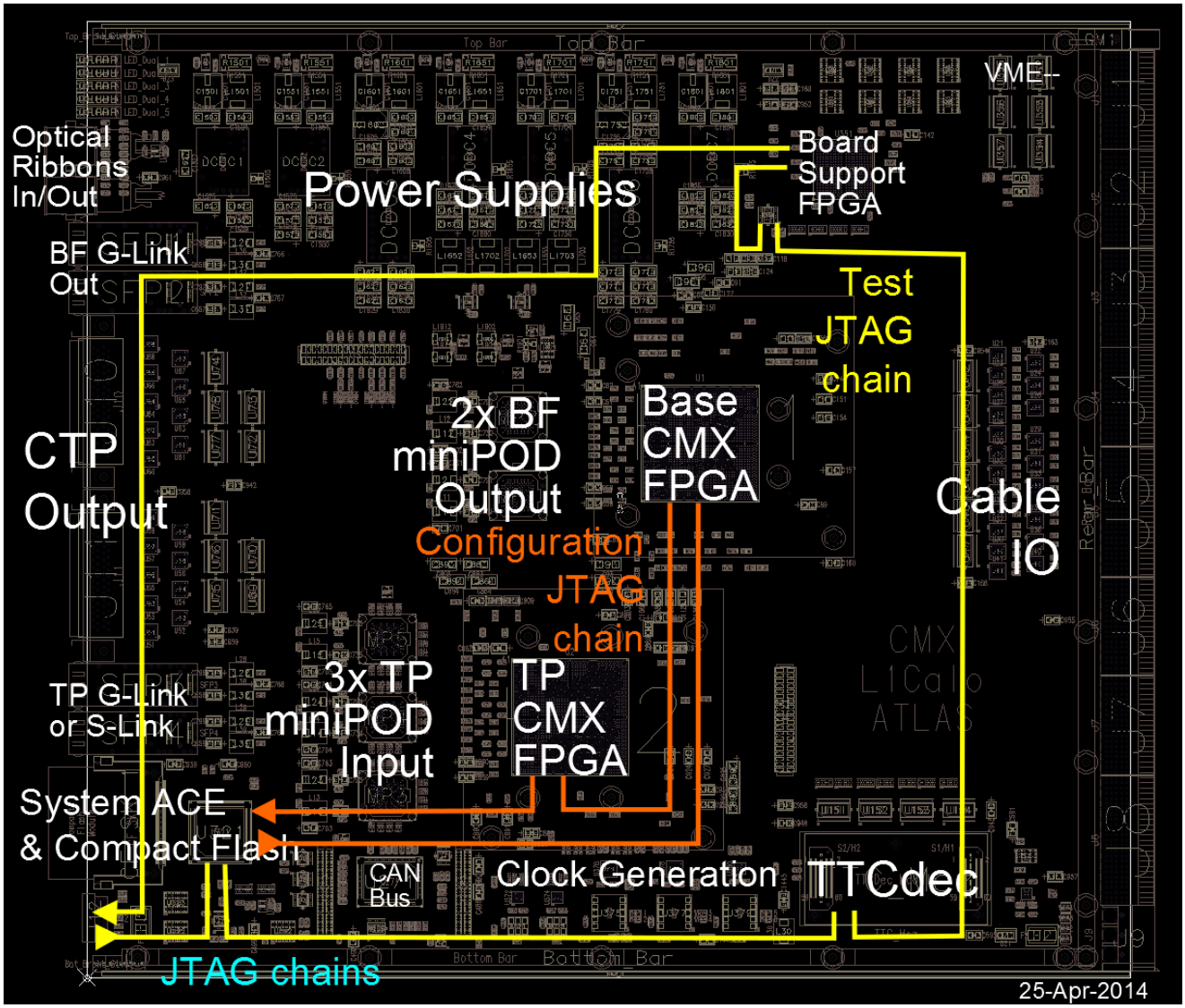


Figure 16: CMX JTAG Chains

The CMX includes two JTAG Chains: a test chain and a configuration chain as shown in Figure 16: CMX JTAG Chains.

The Test JTAG Chain is accessible through the front-panel test connector. The Test JTAG Chain connects the System ACE test port, the TTCDec, the Serial PROM for configuring the BSPT FPGA, and the BSPT FPGA itself. Jumpers are available to individually skip each of these devices along the chain.

The configuration JTAG Chain connects the configuration JTAG port of the System ACE to the BF and TP FPGAs. Jumpers are available to skip each of these devices along the chain; including the case where the TP FPGA is not installed.

Normal CMX firmware configuration after power up starts with the Power Supply Monitor detecting nominal power on the card and allowing the BSPT FPGA to configure itself using its attached serial configuration PROM. The System ACE also waits for the CMX power monitoring circuitry to determine that on-board power is stable before it reads the default configuration files from the Compact Flash card to configure the BF FPGA and (if present) the TP FPGA. The BSPT FPGA can also direct the System ACE to (re-)configure the main FPGAs using any of the configuration files from the Compact Flash card.

Updating the BSPT firmware requires using the Test JTAG Chain to load the new firmware into the Board Support FPGA serial configuration PROM device.

The BSPT FPGA firmware is developed during the test and commissioning period and is then expected to remain stable during normal operation. All flavors of CMX usage (Crate, System, CMX-Topo) will use the same BSPT FPGA firmware. No BSPT configuration problem has been encountered from using the serial PROM configuration method on CMX, matching the experience gained with all previous MSU projects with respect to the management of VME interface firmware.

The Board Support FPGA presents registers visible from the VME-- bus for the control and monitoring of the System ACE by the online software.

The Compact Flash card is accessible and swappable through the front-panel (like on CMM). The content of the Compact Flash card is also accessible from the BSPT FPGA via the System ACE. BSPT firmware and the control software can be developed to support updating the files on the Compact Flash card via the VME-- bus and thus updating the BF and TP FPGA firmware loaded at power-up.

The circuit diagram for the JTAG Test and Configuration Chains and further details regarding this section of the CMX are found in Appendix J: JTAG Chains and FPGA Configuration.

The details regarding all jumpers available on the CMX including the jumpers available to control the JTAG Chains are found in Appendix L: CMX Jumpers.

4.5 CAN Bus

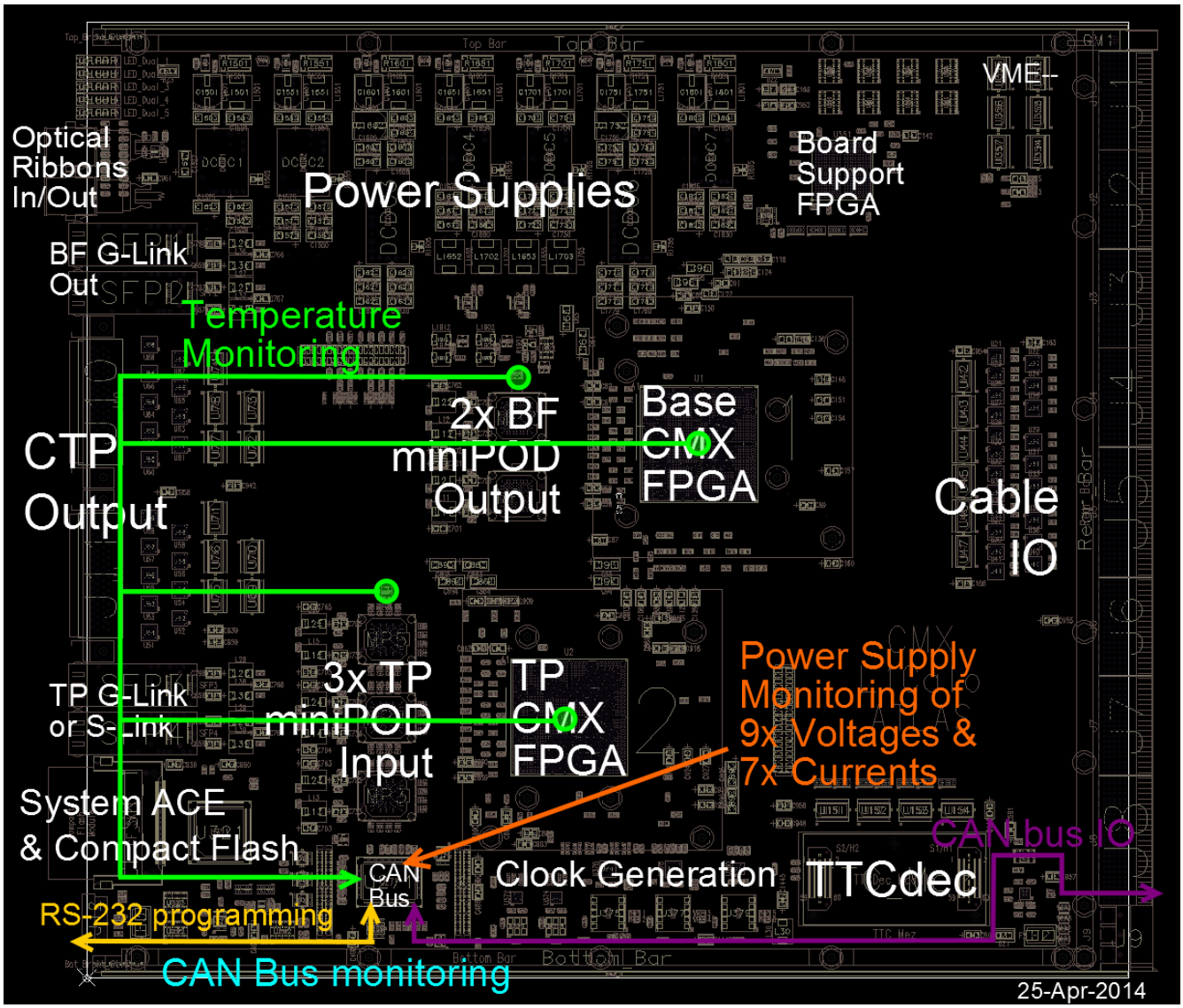


Figure 17: CMX CAN Bus monitoring

The CMX implements monitoring via CAN Bus of:

1. The silicon temperature of the BF and TP FPGA as well as the air temperature past the MiniPOD transmitters and receivers.

2. All eight power supply voltages used on the card (5V raw input and seven on-board DC-DC converters) and the reference voltage (VREF) optionally used with the 400 backplane inputs
3. All currents from the seven on-board DC-DC converters

The circuit diagram for the CAN Bus circuitry and further details regarding this section of the CMX are found in Appendix K: CAN Bus.

Power Supply Monitoring is described within the context of the Virtex 6 System Monitor resources in Appendix Q: Virtex System Monitor.

4.6 Transceiver Control Oversight

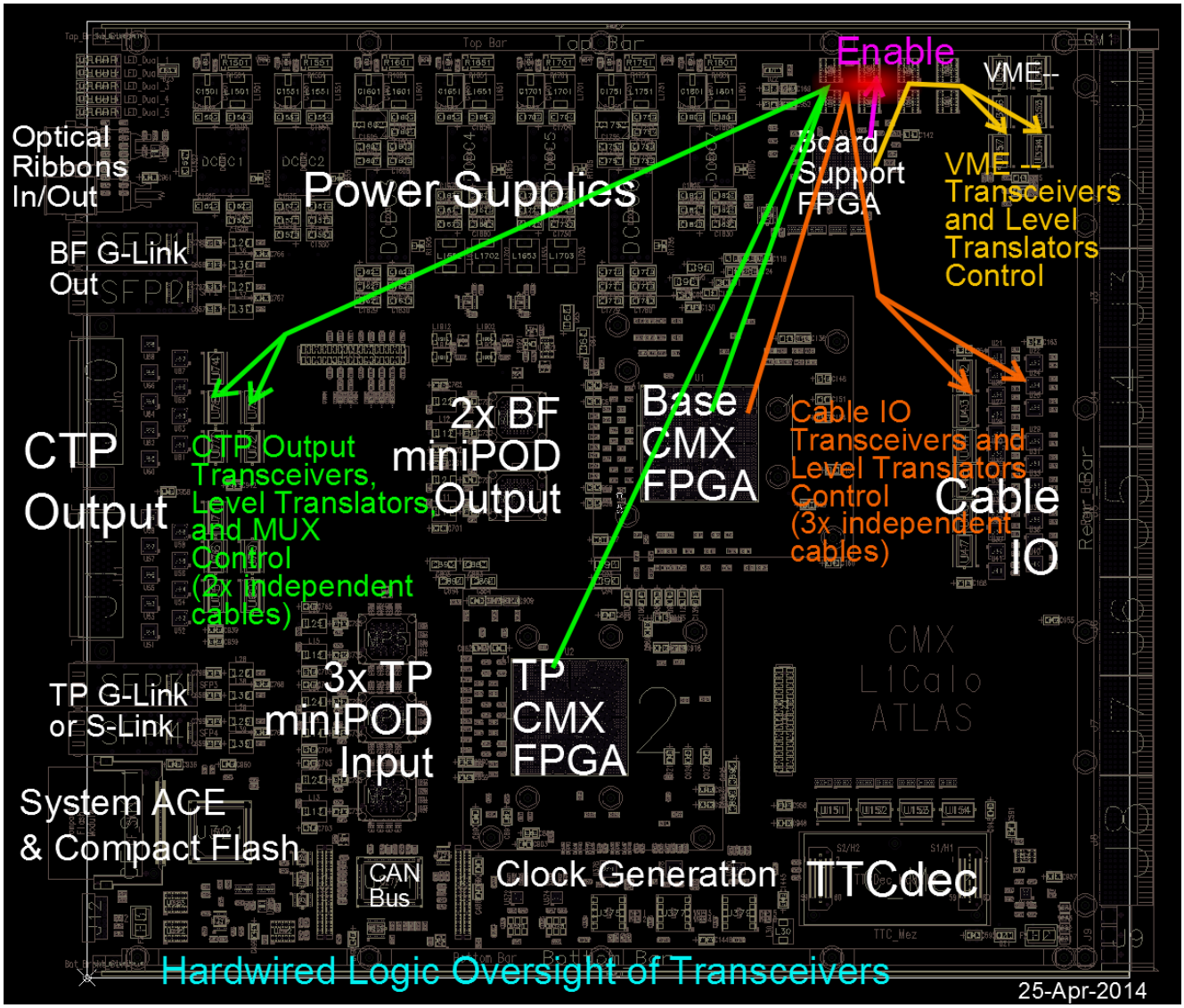


Figure 18: Transceiver management and oversight

Three sets of transceivers on the CMX need to be safely managed:

1. The VME-- bus buffers and level translators
2. The Cable IO LVDS transceivers and level translators
3. The CTP Output LVDS transceivers and level translators

Hardwired logic protects the VME bus interface. The VME-- bus transceivers will not be enabled until the Board Support FPGA is configured and able to manage the operation of these transceivers. This is to help prevent hardware or firmware configuration problems on CMX from making the VME bus unavailable to other cards in the crate (.e.g. by driving VME-- data bus lines with random states). DTACK_B generation is also suppressed until the BSPT FPGA has been configured.

A combination of hardwired logic and BSPT firmware provides the assistance and oversight of the management transceivers. This oversight prevents bus conflict.

The BSPT FPGA first needs to provides a confirmation (called “enable” in Figure 18) that it has detected that the BF FPGA (and TP, if present) have been successfully configured and are operating before this oversight circuitry will release control of the transceivers to the BF and TP FPGA. Then the direction and output enable pins of the multiple transceiver ICs implementing a given IO port (e.g. the 7 LVDS transceivers plus the 2 level translators for one backplane Merger Cable) is managed and controlled via the BSPT FPGA which needs to follow the requests from the BF or TP FPGA needing access and control of a particular IO port (e.g. the BF FPGA requesting the direction of a backplane Merger Cable).

Circuit Diagrams for the Hardware Oversight Logic are in Appendix R: Hardware Oversight Logic.

4.7 Jumpers

Many jumpers are available on CMX to configure particular operational or test features, including to:

1. Set Geographic Address bits 1, 2 and 3
2. Allow the Board Support FPGA to configure from its serial PROM
3. Control the mode for the LVDS receiver thresholds (to handle missing inputs)
4. Force the transceiver oversight circuitry to a failsafe mode during initial tests
5. Set the TTCDec Chip ID and Master Mode bits
6. Select the TTCDec Clock used on CMX
7. Set the BF, TP and BSPT FPGA configuration mode pins
8. Specify if the TP FPGA is expected to be present on the board
9. Skip individual devices on the Test and Configuration JTAG Chains
10. Control if the BF and /or TP FPGA are configured by System ACE
11. Disable the DC/DC converter for Core Power to the TP FPGA (when not installed)
12. Bypass the CAN Bus monitoring analog multiplexer to resemble the CMM environment
13. Send the 3 PLL lock detect signals to the BSPT FPGA for monitoring purpose
14. Select 2 of the BSPT, BF or TP debug signals to copy to the front-panel test connector
15. Control grounding of the SFP cages, connectors, heat sinks
16. Set a unique CMX Card Serial Number

A description of all jumpers available on the CMX is found in Appendix L: CMX Jumpers.

5 Power

The CMX only uses the 5.0V input power available from the backplane. The 3.3V backplane pin is not connected on CMX.

In addition to the DC-DC converters only a few sections of the CMX are using the 5V input voltage directly, namely the CAN Bus circuitry, the startup supervisor and the voltage monitors.

A 20A fuse sets the maximum 5V power consumption from the DC-DC converters and their management. A separate 3A fuse protects the rest of the 5V power usage on CMX.

The CMX needs to generate 7 additional power voltages on the card:

1. Bulk 2.5V
2. Bulk 3.3V
3. 1.0V core power to the BF FPGA

4. 1.0V core power to the TP FPGA
5. 1.2V core power to the BSPT FPGA
6. 1.03V AVcc power to the GTX IO Banks of the BF and TP FPGAs
7. 1.2V AVtt power to the GTX IO Banks of the BF and TP FPGAs

The CMX also needs to generate 4 reference voltages on the card:

1. 1.25V fixed reference for the System Monitor of the BF FPGA
2. 1.25V fixed reference for the System Monitor of the TP FPGA
3. 4.096V fixed reference to the CAN Bus micro-processor ADC
4. 1.25V +/- 0.5V adjustable reference for the Select IO VREF pins of the BF FPGA IO Banks used for the Backplane Processor Input signals

The 1.0V Power Supplies for Core Power to the BF and TP FPGAs are 30A supplies.

The 3.3V and 2.5V bulk power are further filtered before usage with the MiniPOD devices. The 3.3V bulk power is also further filtered before usage with the SFP optical devices. The AVcc and AVtt power are further filtered to provide separate feeds to the BF and TP FPGAs IO Banks.

A short delay after 5V power is applied to the card all on-board power supplies ramp up together until they reach their design voltage with a ramping rate suitable to the Xilinx FPGAs.

Custom heat sinks were designed and manufactured for each Virtex-6 FPGAs and for the MiniPODs with a low profile compatible with the VME standards specification.

The circuit diagram for the power supplies and further details regarding this section of the CMX are found in Appendix M: CMX Power Supplies and Voltage References.

The Virtex-6 FPGA bypass capacitor design details for the CMX are found in Appendix N: Virtex-6 Bypass Capacitors.

Grounding of the front-panel, connector shells and heat sinks is discussed in Appendix U: Ground Connections.

The geographical usage of each power supply and voltage reference on the board is illustrated in Appendix O: Geographical View of Power Usage.

The design of the Heat Sinks for the BF and TP FPGA and for the MiniPODs is described in Appendix W: Heat Sinks.

6 Card Layout

The CMX is a 22 layer cards.

Nine signal layers are used: seven internal signal layers plus the top and bottom layers. All internal signal layers are located between two ground planes. Three power fill planes are used to distribute the eight power voltages and the adjustable VREF voltage reference under the BF FPGA.

All signal layers support 50 Ohm traces but only five of the internal signal layers support traces with 60 Ohm characteristic impedance. All of the 400 backplane inputs are routed on the internal 60 Ohm layers either all the way to or within ~1cm of the via under their target Base FPGA IO pin.

More details concerning the circuit board layers can be found in Appendix P: CMX card layers.

Extensive details concerning the layout and routing of signals on CMX are available in Appendix V: Layout Details.

7 Build Count by CMX Card Type

The table below shows the number of prototype and production CMX cards of each type.

CMX Card Count	Prototype	Production	Total
With TP FPGA	2	2	4
Without TP FPGA (Base-Only)	1	18	19
With no Virtex-6 FPGA	1 (*)	0	1
Total	4	20	24

(*) One prototype was built with neither BF nor TP FPGA and is used to study power supplies, clock distribution and develop BSPT firmware.

Appendices

Appendix A: Glossary

CMX Glossary

Original Rev. 13-Dec-2012
Current Rev. 30-Apr-2014

A number of acronyms and abbreviations have been used in the design of the CMX card. This file contains the definitions of these terms.

The net_names used in the design of the CMX have been written in all capital letters to prevent the chance of confusion by downstream tools.

ACE
: System ACE (Advanced Configuration Environment) is a Xilinx product designed to configure Xilinx FPGAs from the content of a Compact Flash memory card.

BF FPGA
: Base Function FPGA. The CMX FPGA which implements and extends the original CMM functions and additionnally sends data to the L1Topo or CMX-Topo.

BSPT
: the Board Support FPGA

CAN
: CAN bus (Controller Area Network) is a bus standard which originated in the automobile industry and designed to allow microcontrollers and devices to communicate with each other. It is used to report voltage and temperature monitoring on CMX

CMM
: Common Merger Module

CMX
: Common Merger Extended module

CMX-Topo
: An optional mode of operation for a CMX card to act as a limited Topological Processor system in place of or parallel to the L1calo L1Topo system.

CPM
: Cluster Processor Module. One of two types of modules sending real-time trigger information to the CMX through the backplane.

CP
: Cluster Processor sub-system of the Calorimeter Trigger

CTP Central Trigger Processor

DAQ Data Acquisition. Used to identify one of the two types of G-link output ports on CMX by the information they send to a ROD

DCS Distributed Control System. This is a generic term. CAN bus is a DCS

DTACK_B Data Transmission Acknowledge (the "_B" postfix denotes that a logic low is used to assert the signal). One of the VME bus lines used by slave devices to convey their current status to the master during a bus cycle.

FPGA Field Programmable Gate Array. An integrated circuit designed to be configured with specific firmware at run-time.

G-link A 1Gbps protocol used by CMX to send out information to one or more RODs after every L1Accept.

GTX (not an acronym) The MGT resource type available on the Virtex-6 FPGA used on CMX (XC6VLX550T), and capable of serial IO up to 6.6 Gbps.

I2C Inter-Integrated Circuit (pronounced "eye-squared cee" or "eye-two-cee") is a "two-wire interface" multi-master serial single-ended computer bus used to attach low-speed peripherals. It is used to control the TTCrx chip of the TTCdec module.

JEM Jet/Energy processor Module. One of two types of modules sending real-time trigger information to the CMX through the backplane.

JEP Jet/Energy Processor sub-system of the Calorimeter Trigger

JTAG Joint Test Action Group. A Standard for the Test Access Port and Boundary-Scan Architecture.

L1A Level-1 Accept signal distributed via the TTC system.

L1Calo Atlas Level 1 Calorimeter Trigger

L1Topo Level 1 Trigger Topological Processor. This term generally refers to a standalone system being built for the Phase 0 upgrade of L1calo. The CMX platform is also designed to operate like a limited L1topo system using inputs from all CMX cards which is then called a CMX-Topo system.

LVDS Low-Voltage Differential Signaling. A signaling standard used for the CMX to CMX Cable IO and for the output to CTP.

MGT Multi-Gigabit Transceiver. A special type of IO pin on Virtex-6 for multi-gigabit serial IO (as opposed to Select IO pins). All MGT resources on the Virtex-6 FPGA used on CMX are GTX transceivers.

MiniPOD The name of a family of optical transmitters and receivers manufactured by Avago (formerly Agilent, formerly HP).

MMCM Mixed-Mode Clock Manager. A clock management resource on Virtex-6.

MP MiniPOD the Avago optical transmitters and receivers used for the 6.4 Gb/s "high speed" optical links from the Base Function FPGA and to TP Function FPGA

MPO/MTP Multiple-Fiber Push-On. A multi-fiber connector standard.

ROD Read-Out Driver module. CMX sends information a every L1 Accept to a DAQ ROD and some CMX cards also send information to an ROI ROD.

ROI Region of Interest. Used to identify one of the two types of G-link output ports on CMX by the information they send to a ROD

RS-232 A serial communication standard commonly used for computer ports.

RTM Rear Transition Module. A Card plugging in the back of CMX with connectors to plug up to 3 LVDS cables for Crate CMX to System CMX communication

Select IO
The standard type of IO pins on Virtex-6 (as opposed to MGT IO pins)

S-LINK Simple Link Interface. The CERN specification for readout of front-end electronics used in ATLAS L1calo.

SFP Small Form-factor Pluggable the optical transmitters that send out the 1 Gb/s "low speed" optical data from the BF and TP functions on the CMX to the ROI and DAQ systems

TCM Timing and Control Module.
One of the modules in the L1calo crates.

TP FPGA
Topological Processor FPGA on the CMX card

TTC Timing, Trigger and Control. The centralized timing and control distribution system common to LHC experiments. It is distributed by a fibre distribution tree, with all information multiplexed onto a single optical signal.

TTCDec TTC Decoder mezzanine card which recovers the 40.08 MHz LHC clock, the L1 Accept, the Bunch and Event identification information, as well as broadcast or targeted commands. It also includes a 40.00 MHz crystal for tests purposes.

TTCrx The CERN custom IC used to receive the TTC signal.
This chip provides is the core of the TTCDec.

VAT The VAT card (VME/ACE/TTC) is a parallel prototype project to practice System ACE control and test Board Support FPGA firmware

VME Versa Module Eurocard. A computer bus standard popular in HEP.

VME-- A subset of the VME signals used for communication within L1calo crates. This bus is used on the custom backplane for the L1calo CP and JEP crates.

VREF The name for the usage of some Virtex-6 Select IO pins with an external voltage reference. VREF can be used by an IO Bank as an input threshold voltage with a differential amplifier input buffer. Using an external VREF is a backup feature of CMX to recieve the 400 backplane inputs, as the nominal plan is to use the built-in 2.5V CMOS input standard.

VRP,VRN The names of the two Virtex-6 Select IO pins used with a pair of external resistors to be optionally used with the Digitally Controlled Impedance technology to set the input impedance of the 400 backplane inputs. This is a backup feature of CMX as the nominal plan is to NOT terminate the 400 processor input signals.

Appendix B: CMX component placement

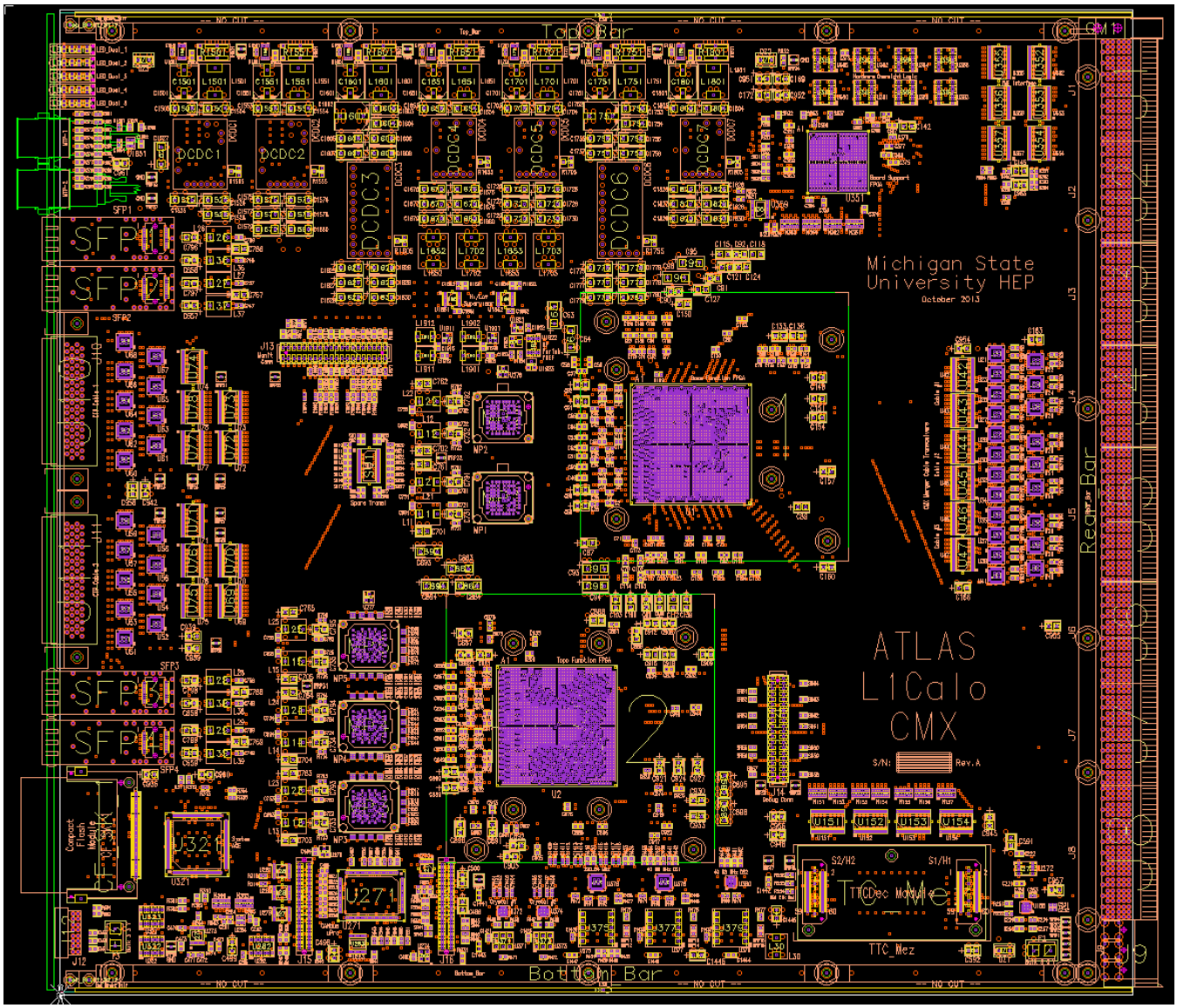


Figure 19: CMX top side component view

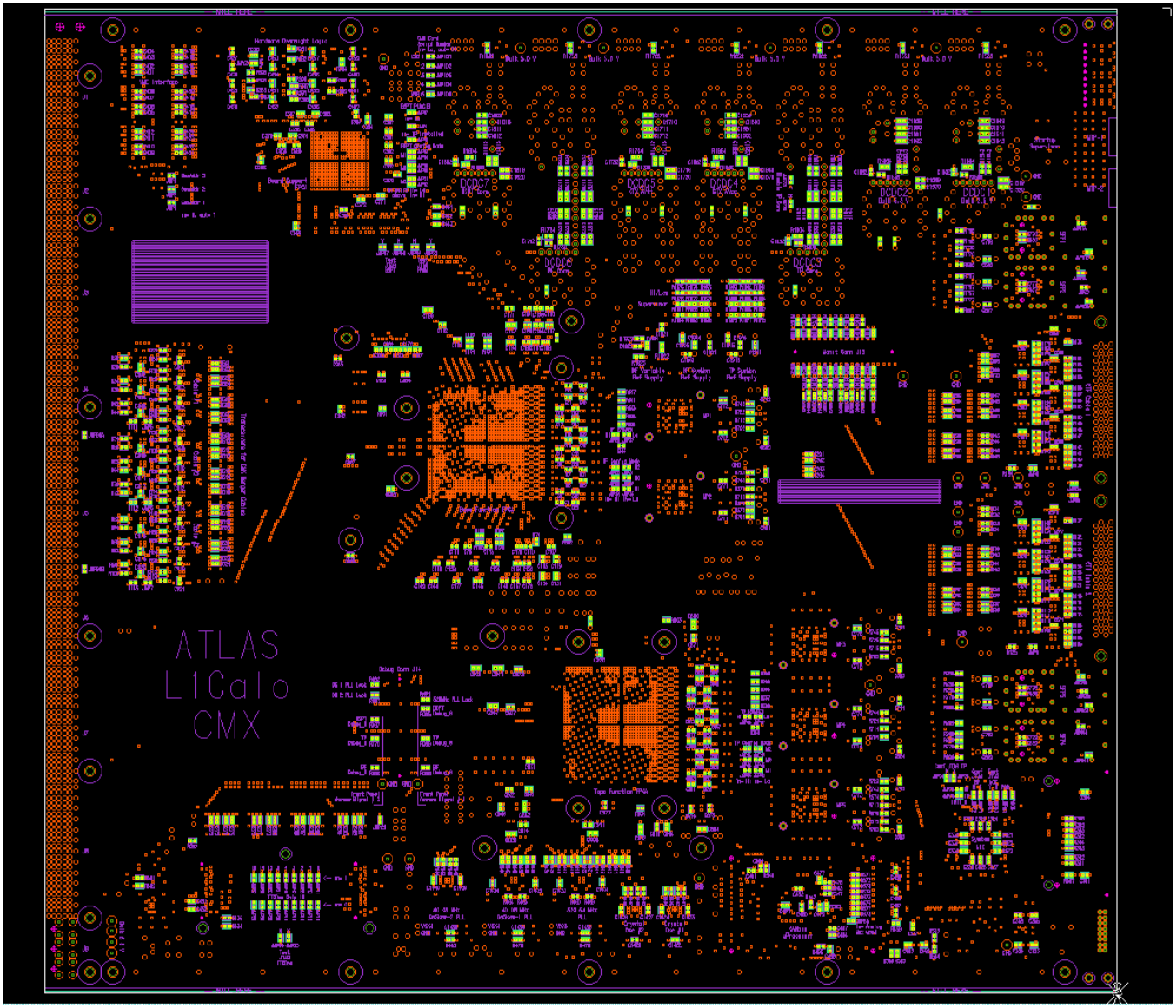


Figure 20: CMX bottom side component view

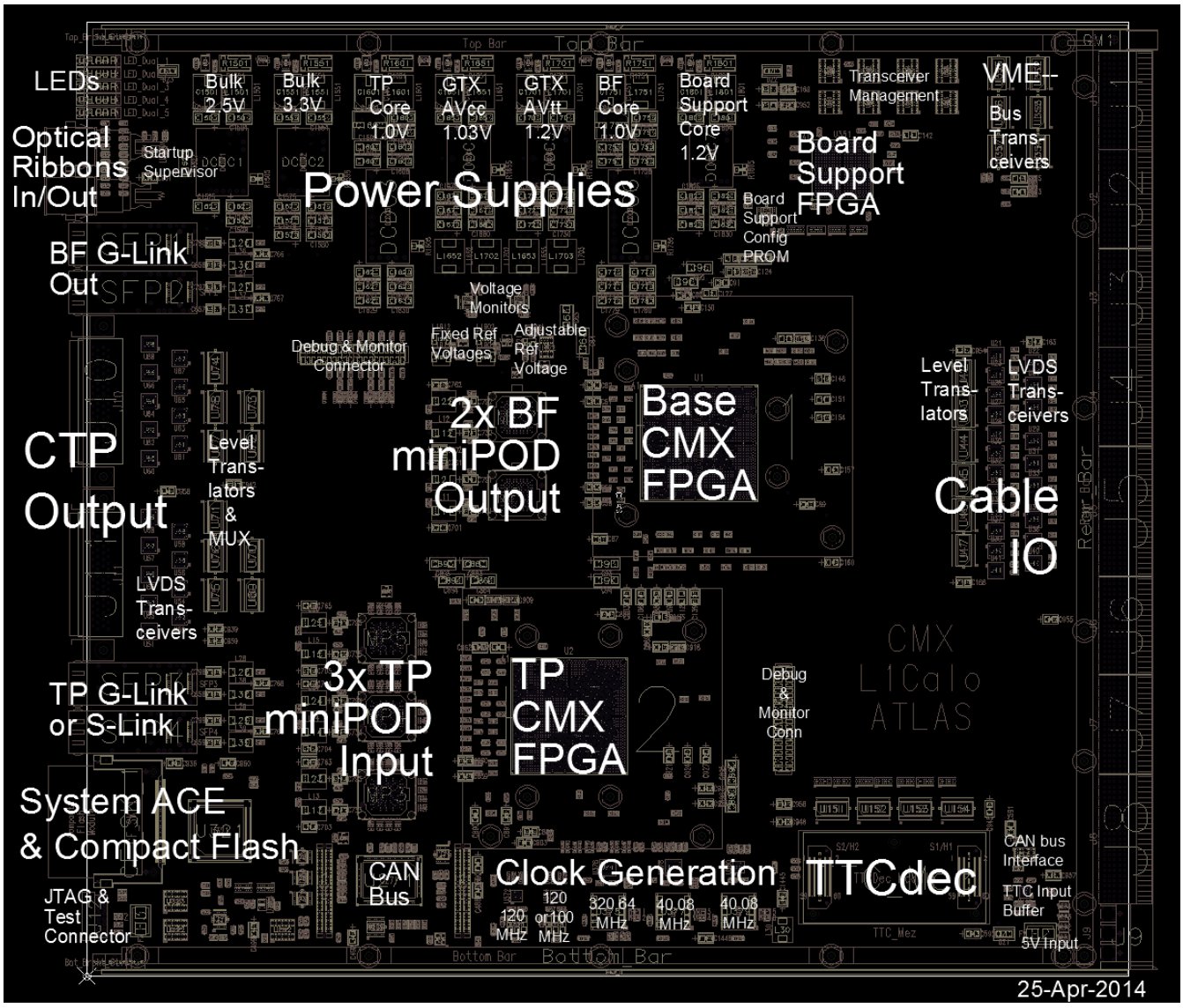


Figure 21: Annotated CMX component placement

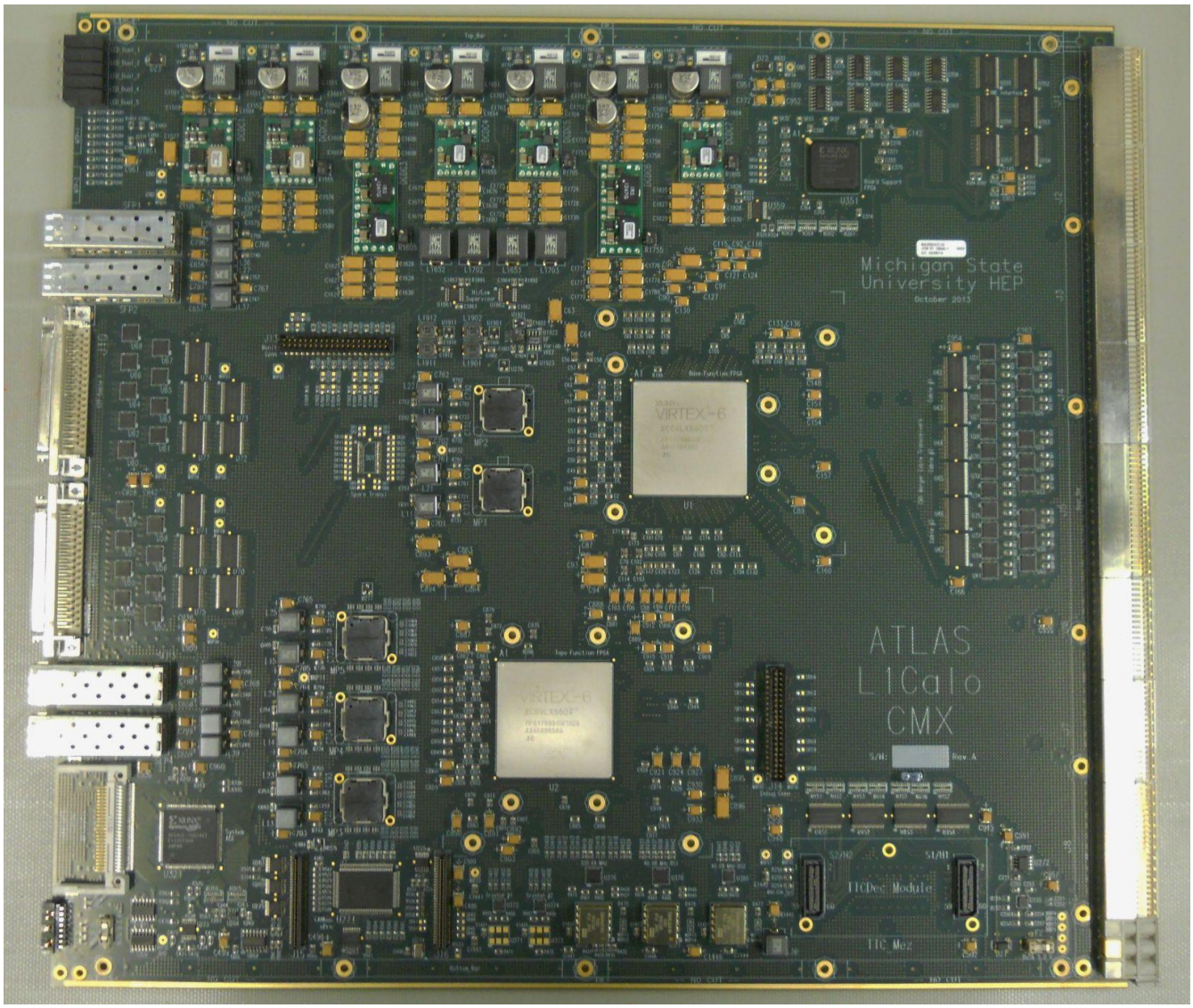


Figure 22: CMX top side before final assembly

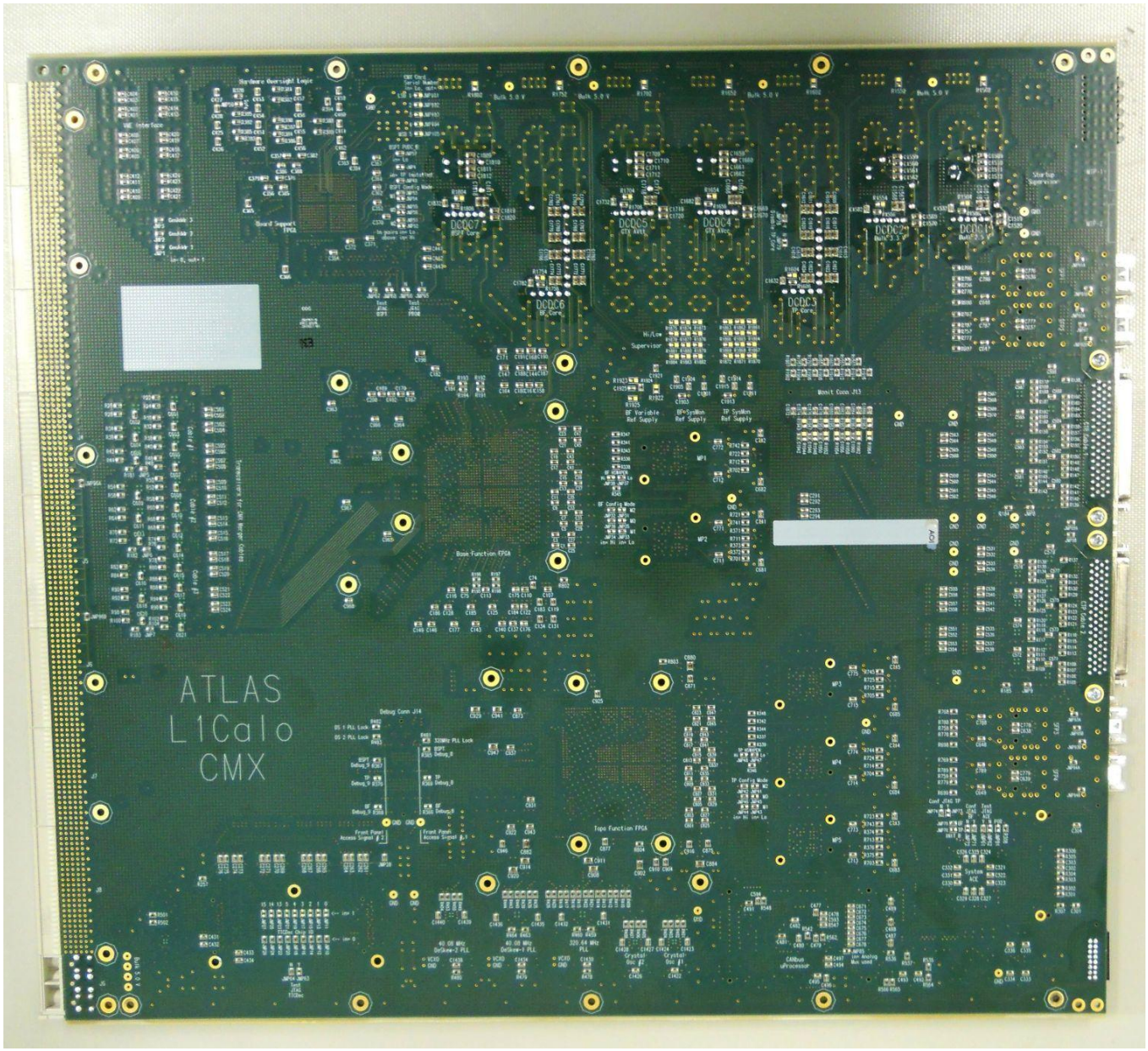


Figure 23: CMX bottom side before final assembly

Additional views and photos are available

http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/pcb_layout_views/

http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/block_diagrams/

http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/photos/

Appendix C: IO Banks Assignments for BF and TP FPGA

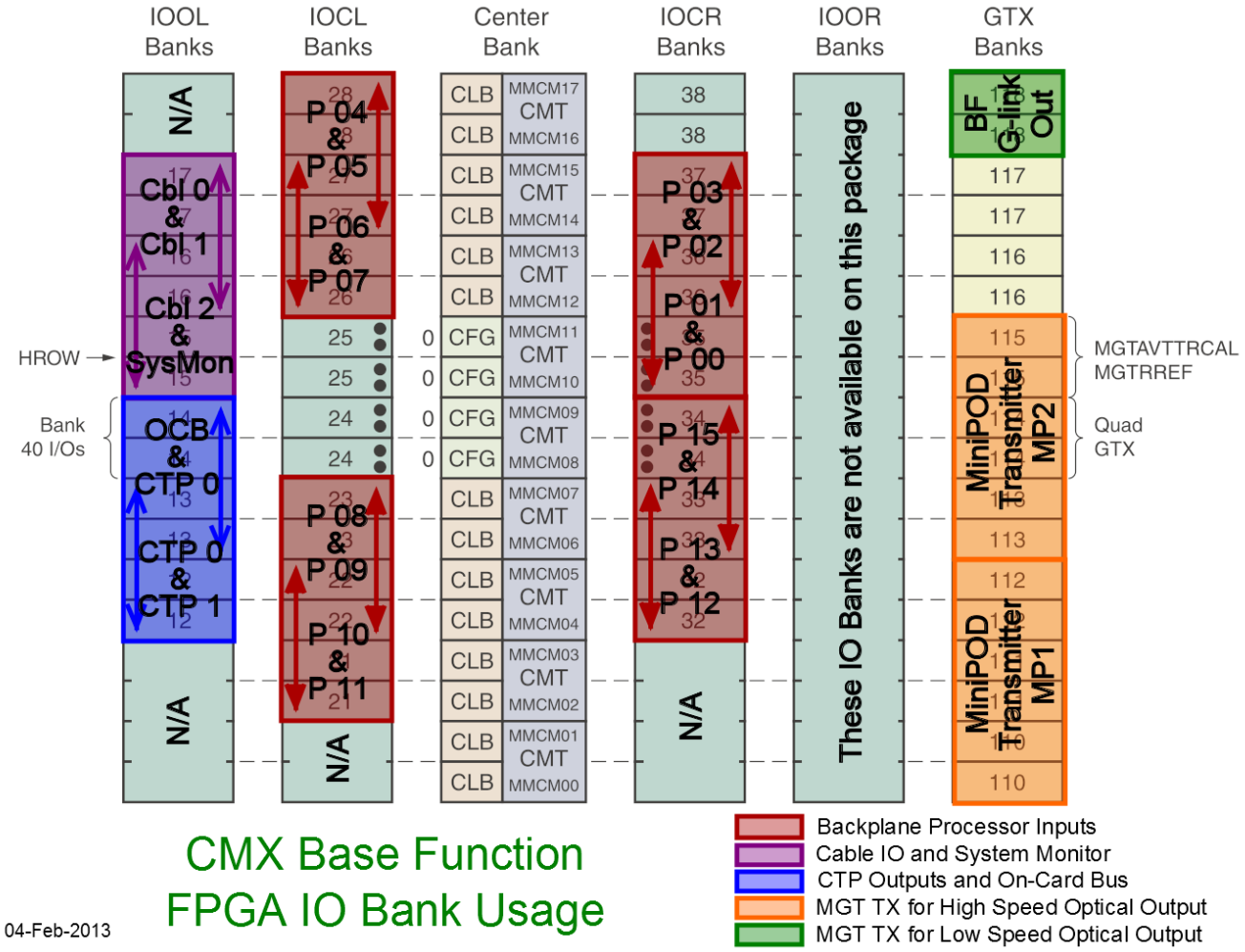


Figure 24: BF FPGA IO Banks Assignments

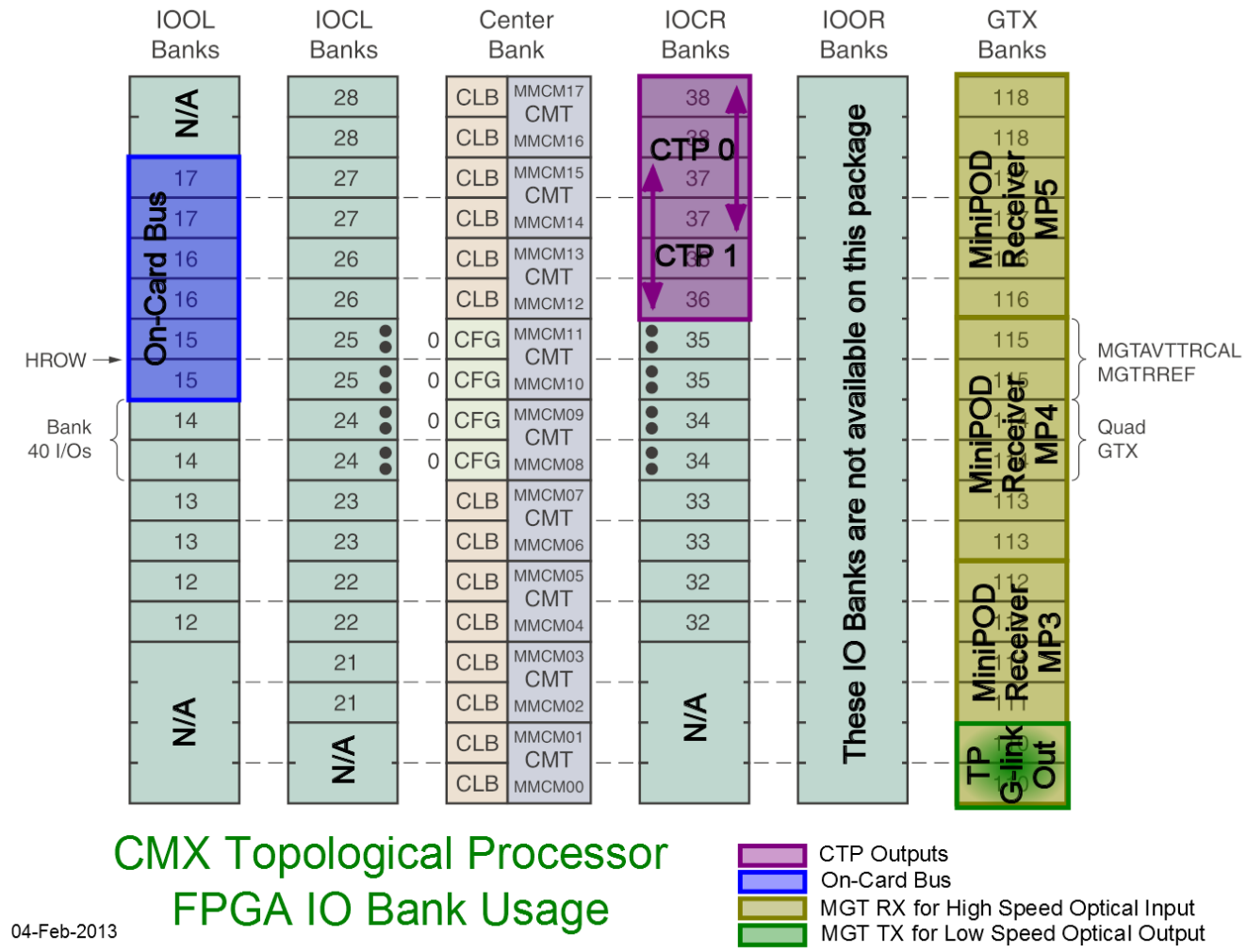


Figure 25: TP FPGA IO Banks Assignment

These diagrams are available in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/block_diagrams/

Appendix D: LVDS Connections

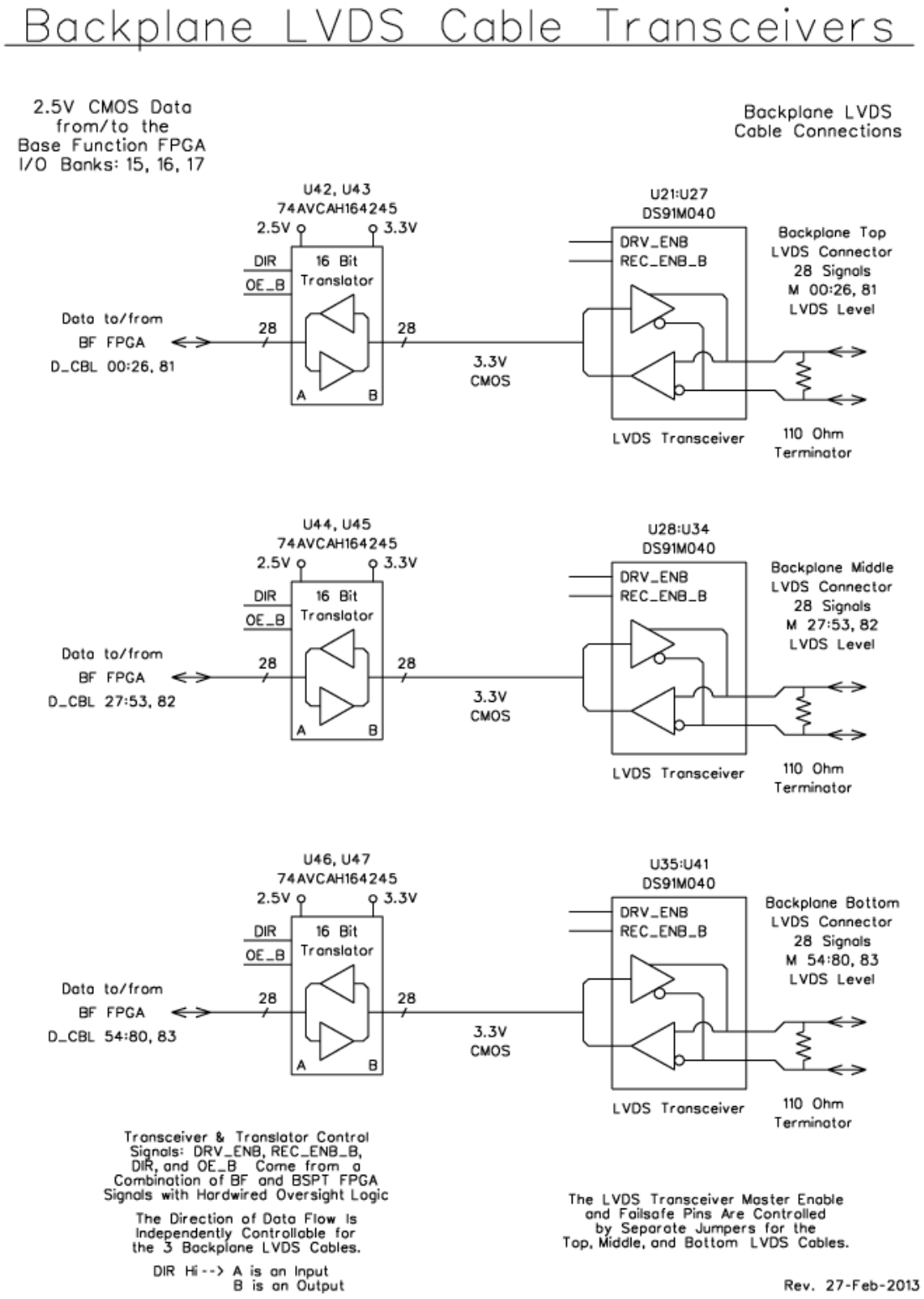


Figure 26: Circuit Diagram for the LVDS Cable IO

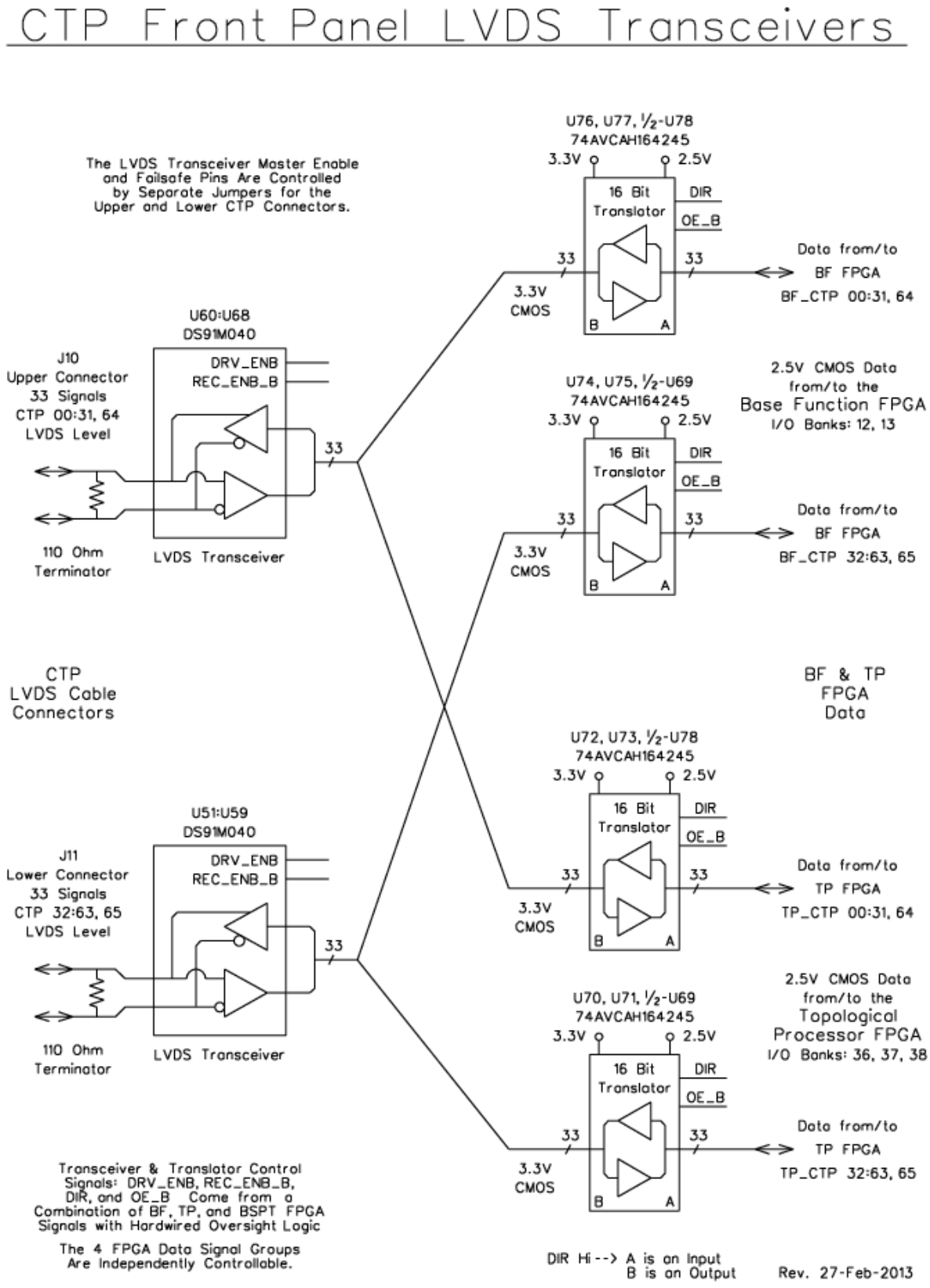


Figure 27: Circuit Diagram for the LVDS CTP Output

A current snapshot of the circuit diagrams is included above while the source material is in

- 10_lvds_backplane_cables.pdf
- 09_lvds_ctp_output.pdf

found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot of the detailed description is included below while the source material is in cmx_ab_lvds_connections.txt found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
                  CMX  LVDS Connections
                 -------------------------


                                      Original Rev.  13-Dec-2012
                                       Current Rev.  28-Apr-2014


This file describes the LVDS connections to and from the CMX
circuit board.

 - The backplane of the CMX card contains 3 "LVDS Cable
   Connections" of 27 bits each.  All of these signals
   are routed to the Base Function FPGA.  The backplane
   LVDS Cable connections on the CMX card are shown in
   the following circuit diagram on the web:

     10_lvds_backplane_cables.pdf


 - The front panel of the CMX card contains 2 "CTP LVDS
   Cable Connections"  of 33 bits each.  All of these
   signals are routed to both the Base Function FPGA and
   to the Topological Processor FPGA.  The front panel CTP
   LVDS connections to the CMX card are shown in the
   following circuit diagram on the web:

     09_lvds_ctp_output.pdf


Note that in some cases the connector pinout signal numbering
scheme that is used in these LVDS connections is not
continuous and skips around a bit.

The CMX card implements both the backplane and the front
panel LVDS connections in the same way.  Specifically:

 - Each LVDS signal is received or transmitted by one channel
   of a quad National  DS91M040  LVDS Transceiver.  This is a
   high speed "M" type LVDS transceiver that provides double
   the normal drive current  (for cables that are terminated
   at both ends)  and has a receiver with wide common mode
   input range for use with cables.
```

- The CMX circuit board provides a 100 Ohm differential termination resistor on each channel. In this way the LVDS circuits can be used as either transmitters or as receivers without making any changes to the card.

- The DS91M040 LVDS transceivers have 3.3V CMOS single ended data and control signals. These 3.3V signals can not be used directly with the Virtex-6 BF and TP FPGAs.

- Between the Virtex-6 FPGAs and the 3.3V CMOS data pins on the DS91M040 LVDS transceivers there are bi-directional 2.5V <-> 3.3V level translators. These parts are TI 74AVCAH164245. These translators include hold circuits to avoid the problem of floating CMOS inputs.

- These 74AVCAH164245 translators are also used to provide the multiplexing function that allows either the Base Function FPGA or the Topological Processor FPGA to be connected to the front panel CTP LVDS signals.

  Note that this multiplexing of the front panel CTP LVDS signals is done on a per connector basis. Thus for example the BF FPGA can be sending or receiving LVDS signals on the upper front panel CTP LVDS connector while the TP FPGA is using the lower front panel CTP LVDS connector.

Management of the National DS91M040 LVDS transceivers:

- Management of the DRIVER_ENB and RECEIVER_ENB_B control signals to the LVDS transceivers comes from the BSPT FPGA. In turn the BSPT FPGA listens to signals from the BF and TP FPGAs to learn how they want the various LVDS transceivers configured, i.e. as inputs or as outputs. Once everything is running the BF and TP FPGAs have control over the direction of all of the LVDS transceivers with logic in the BSPT enforcing rules to prevent conflicts, e.g. aiming the transceiver and translator in different directions.

- The National DS91M040 LVDS transceivers include control pins for their Failsafe and Master Enable functions. We do not anticipated that we will frequently need to change these control signals and thus their state is set in groups by jumpers which are described in detail in the file on the web:

  cmx_ab_board_jumpers.txt

Management of the TI 74AVCAH164245 level translators:

Management of the DIRECTION and OUTPUT_ENABLE_B control signals to the level translators comes from the BSPT FPGA and includes Hardwired Oversight Logic to prevent enabling the output of these translators before the BSPT FPGA is configured. In turn the BSPT listens to signals from the BF and TP FPGAs to learn how they want the level translators configured. Thus once everything is running the BF and TP FPGAs have control over these devices with logic in the BSPT enforcing rules to prevent conflicts, e.g. enabling two drivers on the same line at the same time.

BSPT FPGA Firmware Management and Hardwired Oversight Logic Management of the LVDS Transceivers and Translators:

- Management of the Backplane LVDS Cable Transceivers and Translators is shown in the following circuit diagram:

  21_backplane_cable_management.pdf

  The Hardwired Oversight component of this management is shown in the upper left-hand corner of this drawing. The Hardwired Oversight Logic makes the ALLOW_BUSSED_IO signal which must be asserted Hi to enable the output buffers on any of the level translators in the Backplane LVDS Cable circuits. With all of the level translator outputs disabled there can not be any logic level conflicts at either the BF FPGA pins or at the LVDS transceiver pins of the Backplane LVDS Cable circuits.

  The BSPT FPGA Firmware component of this management is shown on the upper right-hand corner of the drawing noted above. This BSPT firmware generates the 9 control signals: CABLE_x_TRNCVR_DIR, CABLE_x_TRNSLT_DIR, and BSPT_CABLE_x_TRNSLT_OE_B where x is 1, 2, or 3 to manage the direction of the 3 Backplane LVDS Cables.

  The BSPT FPGA Firmware component of the management of the Backplane LVDS Cable Transceivers and Translators listens to the 3 BF_REQ_CABLE_x_INPUT signals that come from the Base Function FPGA to learn if the BF wants a given Backplane LVDS Cable to be an input or an output. This BSPT firmware then sets the control signals listed above to put the translator and LVDS transceiver circuits in the desired direction. Note that this needs to be coordinated with putting the BF FPGA pins that receive or send the Backplane LVDS Cable signals in the matching direction.

- Management of the Front Panel CTP LVDS Transceivers and Translators is shown in the following circuit diagrams:

  22_ctp_connector_management.pdf
  23_ctp_connector_bstp_logic.pdf

  The Hardwired Oversight component of this management is shown in the top center of drawing 22. The Hardwired Oversight Logic makes the ALLOW_BUSSED_IO signal which must be asserted Hi to enable the output buffers on any of the level translators in the CTP LVDS circuits. With all of the level translator outputs disabled there can not be any logic level conflicts at either the BF or TP FPGA pins or at the LVDS transceiver pins of the CTP LVDS circuits.

  The BSPT FPGA Firmware component of this management is shown in drawing 23. This management firmware for the CTP Transceivers and Translators must separately manage the upper and lower CTP connectors and prevent conflicts between how the BF and TP FPGAs want to use these bi-directional LVDS circuits.

  This management firmware listens to the following signals: ALLOW_BUSSED_IO, BF_CONFIG_DONE, BF_REQ_CTP_x_INPUT, TP_FPGA_INSTALLED_B, TP_CONFIG_DONE, TP_REQ_CTP_x_INPUT, where x = 1 or 2 for the upper or lower CTP connectors. This firmware generates the 10 control signals to manage the transceivers and translators for the two CTP LVDS connectors. Note that this needs to be coordinated with putting the BF and TP FPGA pins that receive or send the CTP LVDS signals in the matching direction.

- Overall Hardwired Oversight Logic:

  An overall drawing of the Hardwired Oversight Logic is given in circuit diagram:

  24_hardwired_oversight_logic.pdf

  The main purpose of the Hardwired Oversight Logic is to prevent enable type signals from turning on various buffers, translators, and drivers before the BSPT FPGA that manages them is configured and running normally. The purpose of this is to prevent bus conflicts and to prevent problems like the CMX from asserting the VME_DTACK_B line before the BSPT FPGA is configured. The BSPT FPGA manages VME_DTACK_B once it is running.

  The Hardwired Oversight Logic consists of generating the ALLOW_BUSSED_IO signal and then using that signal to force the 12 control signal that pass through the Hardwired Oversight Logic to a benign state whenever ALLOW_BUSSED_IO is not asserted.

The top of drawing 24 shows the signals that are used to generate the ALLOW_BUSSED_IO signal.

The Hardwired Oversight Logic qualifies the following 12 enable type control signals with the ALLOW_BUSSED_IO signal:

BSPT_CABLE_1_TRNSLT_OE_B BSPT_CABLE_2_TRNSLT_OE_B BSPT_CABLE_3_TRNSLT_OE_B	Protect against Backplane LVDS Cable conflicts
BSPT_CTP_1_BF_TRNSLT_OE_B BSPT_CTP_2_BF_TRNSLT_OE_B BSPT_CTP_1_TP_TRNSLT_OE_B BSPT_CTP_2_TP_TRNSLT_OE_B	Protect against Front Panel CTP LVDS Connector conflicts
BSPT_SEND_VME_DTACK_B BSPT_VME_BUS_TRNCVR_OE_B BSPT_OCB_ADRS_AND_CTRL_TRNSLT_OE_B	Protect against hanging the crate's VME Bus
BSPT_TTC_TRNSLT_OE_B BSPT_TTC_RESET_TRNSLT_OE_B	Protect against TCCDec translator output conflicts

Appendix E: High-Speed Optical

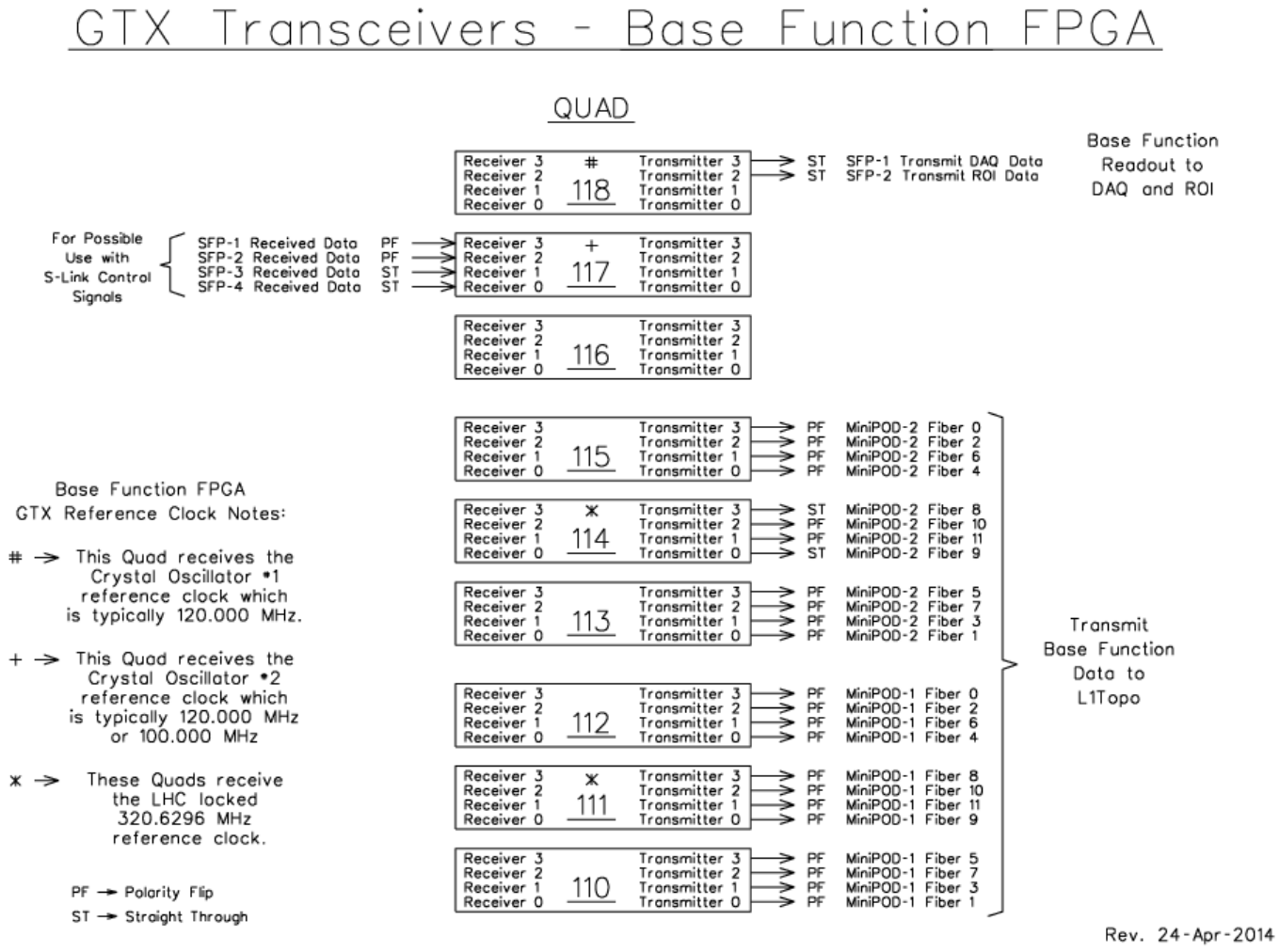


Figure 28: Base Function FPGA GTX transceiver usage

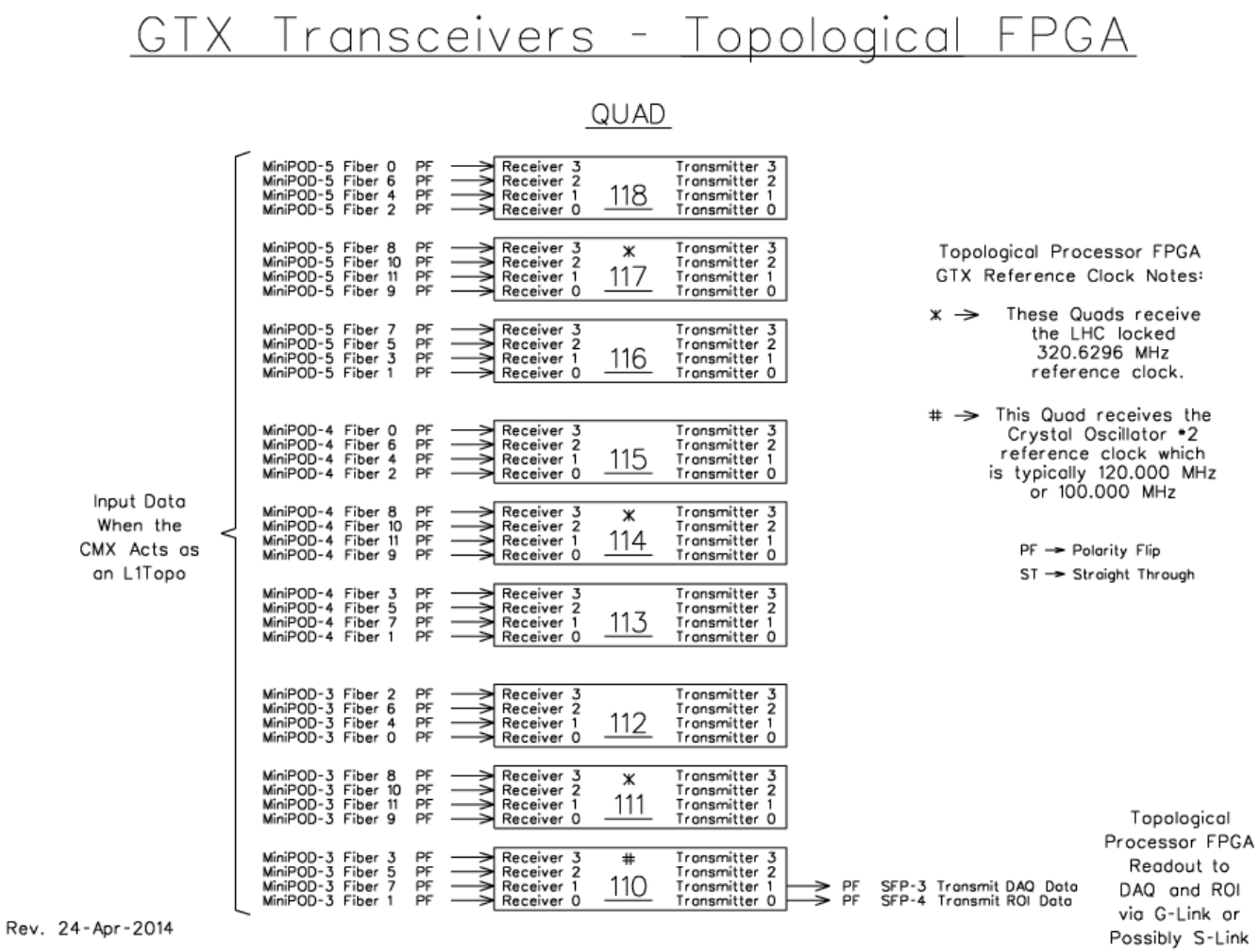


Figure 29: Topo Function FPGA GTX transceiver usage

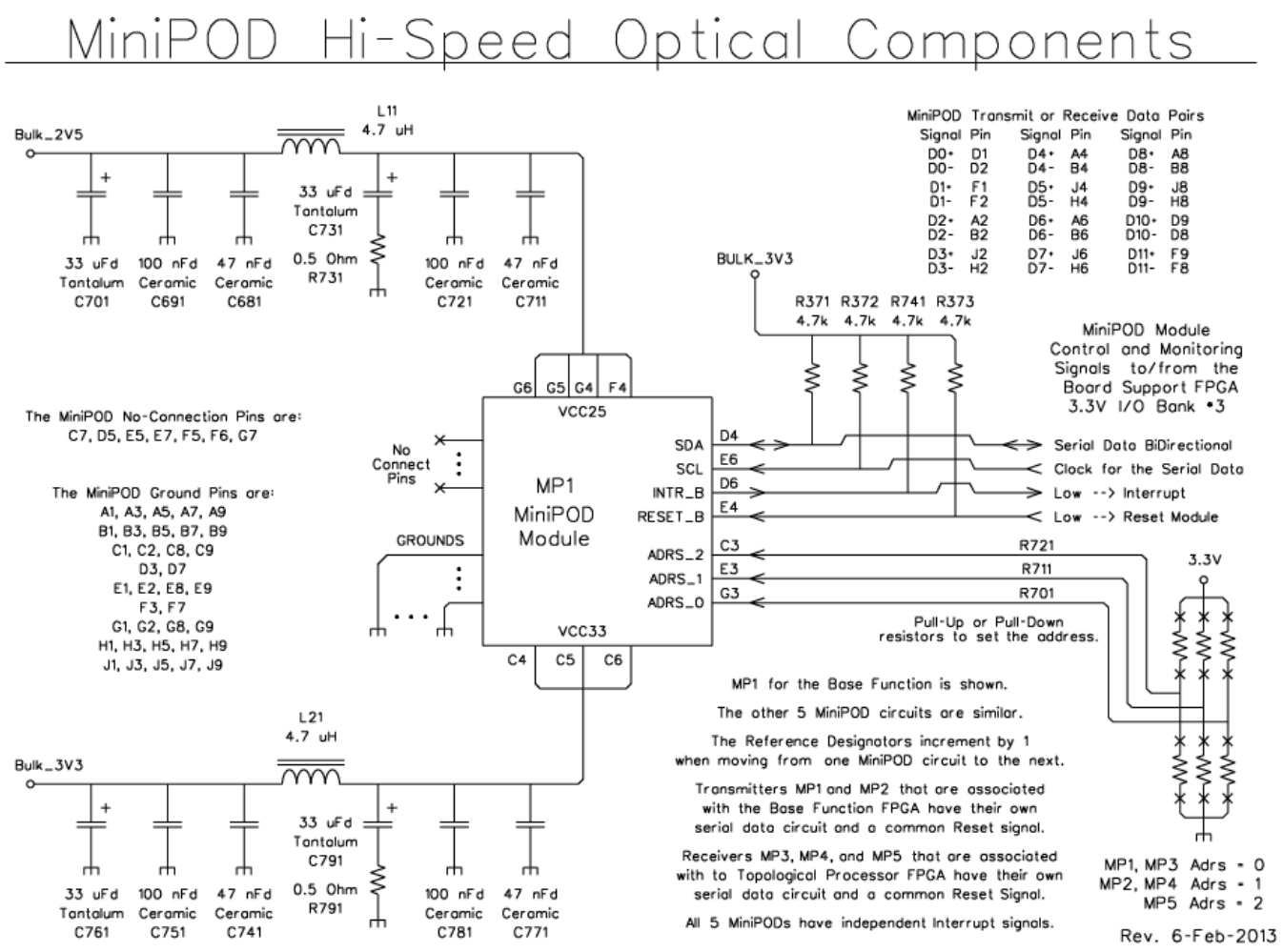


Figure 30: Circuit Diagram for high-speed optical connections

A current snapshot of the circuit diagrams is included above while the source material is in

- 27_gtx_transceivers_base_function.pdf
- 28_gtx_transceivers_topological.pdf
- 14_high_speed_minipod_optical.pdf

found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot of the detailed description is included below while the source material is in cmx_ab_high_speed_optical.txt found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

CMX As Built High Speed Optical

Original Rev. 29-Nov-2012
Current Rev. 25-Apr-2014

This intent of this note is to record the engineering information about the high speed MiniPOD optical components on the CMX card.

- A overall drawing of the connections to the MiniPODs on the CMX circuit board is shown in:

  14_high_speed_minipod_optical.pdf

- MiniPOD Optical Part Numbers:

  The high speed optical parts that are used on the CMX card are the following:

  Transmitter is a 12 channel Avago "MiniPOD" type Avago Part No. AFBR-811FN1Z which translates into: 10 Gbps per lane, Flat ribbon jumper cable, without clip-on heat sink, 100m.

  Receiver is a 12 channel Avago "MiniPOD" type Avago Part No. AFBR-821FN1Z which translates into: 10 Gbps per lane, Flat ribbon jumper cable, without clip-on heat sink, 100m.

  These are high speed short range parallel devices designed for multimode fiber systems at a nominal 850 nm wavelength.

- Module Pinout:

  The actual module pinout is common to the transmitter and receiver. There is a separate mechanical identification pin hole. There are 2 holes for screws M1.6 to hold the MiniPOD package down again the supporting circuit board. CMX is using M1.6 x 8mm screws.

- Power Filters:

  Power filters are used for both the 2.5V and 3.3V supplies. Avago recommends 100 nFd to Gnd, 4.7 uH series, 100 nFd to Gnd and 22 uFd to Gnd through a 0.5 Ohm resistor.

The MiniPOD power filters on CMX use:

100 nFd and 47 nFd 0603 ceramic capacitors

33 uFd 10 Volt Tantalum capacitors B case with a

0.47 Ohm 0603 resistor ERJ-3RQFR47V

4.7 uH 12.4 mOhm, 7.5 Amp 45 Mhz Wurth No. 7443340470

- MEG-Array PCB Mount Socket:

The CMX needs to have a connector from the FCI series 55714 for the MiniPOD optical components to plug into.

The CMX is built with a lead free process. The FCI series 55714 socket specification clearly calls out that they do not want you to use their lead free solder ball parts on a leaded assembly process. This is Note #4. See also FCI Specification: GS-20-033.

On CMX we use the FCI Part Number: 55714-002LF connector.

Note that FCI calls for a 0.58 to 0.64mm pad diameter. Copper defined pads with a solder mask that gives 0.15mm minimum clearance all around the pad. Via not in pad. Tented via. Keep out area of 5.1mm from the perimeter of the part. 0.25mm trace from pad to via. 0.64mm via land. 0.30mm via drill plated. FCI does mark pin A1 on their connectors and on the second page of drawings in the drawing file for the 55714 series of connectors.

- High-Speed Differential Signal Routing on the PCB:

Between the output of the receivers and the Xilinx GTX serial inputs we need to have DC-Blocking capacitors. They specify 100 nFd capacitors but say that smaller values may work with 8b10b encoding. 100 nFd x 50 Ohms = 5 usec. A bit length is about 0.15 nsec. Why such a big capacitor ? For these Receiver DC Blocking capacitors CMX uses 100 nFd 6.3 Volt X5R Ceramic 0201 Size Kemet Part No. C0201C104K9PACTU.

All of the GTX to/from MiniPOD differential traces are routed without any cross overs. Where this non cross over trace routing flips the sign then it can be flipped back on the MiniPOD devices by:

Receiver "polarity flip" is controlled from the Receiver Memory Map 01h Upper Page Addresses 226 and 227

Transmitter "polarity flip" is controlled from the Transmitter Memory Map 01h Upper Page Addresses 226 and 227

The GTX transceivers can also flip the sign of their differential signals. In the GTX user manual see page 167 for the transmitter flip and page 216 for the receiver sign flip.

Trace length matching: Have 6.4 Gb/s data rate but also need corners so we need the 3rd and hopefully the 5th harmonics, i.e. 19.2 or 32.0 GHz. This is a free space wavelength of 15.6mm or 9.4mm. But for a good transmission line we care about stuff at the scale of one tenth wave length (or smaller). One tenth wavelength is 1.56mm or 0.94mm. But the transmission velocity is only about 50% the speed of light so we care about the physical layout of the traces at the scale of 0.78mm or 0.47mm or smaller. The GTX to/from MiniPOD differential traces were length matched to 0.39mm worst case 0.25mm or better typical.

- Physical Mounting:

The Flat Ribbon optical cables version of the MiniPOD module has a height of at least 14.50mm above the supporting pcb. With a 14.50mm height it means that there will only be 1.75mm clearance between the top of the MiniPOD module and the inter-board separation plane.

Clearance from the MiniPODs to the adjacent L1Calo cards was checked in the "mechanical only" CMX card.

As Avago suggests, the MiniPOD external case is connected to the CMX ground via the pcb pads for the M1.6 screws that run into the threaded bosses on the MiniPOD case

.

- Optical Connection to the MiniPOD:

For the optical run from the MiniPOD PRIZM connector to the front panel MTP feedthrough connector the CMX card uses Molex Part No. 106267-2011 cables. The MTP connector on these stub cables has male pins.

- MiniPOD TWS Interface with the CMX BSPT FPGA:

This is based on Atmel Two Wire Serial EEPROM e.g. AT24C01A but note the difference in the write timing. The MiniPOD module is a "slave" on this bus.

There serial bus between the BSPT FPGA an the two transmitter MiniPODs MP1, MP2. There is a separate serial bus between the BSPT FPGA and the three receiver MiniPODs MP3, MP4, MP5.

- TWS Management and Monitoring:

  All Management and Monitoring of the MiniPOD High Speed optical components is handled through the BSPT FPGA.

  There are separate TWS serial string for the Base Function FPGA transmitters and for the Topological FPGA receivers.

  There are separate Reset_B signals from the BSPT FPGA to the Base Function transmitter MiniPODs and to the Topological receiver MiniPODs.

  There is a separate Interrupt_B line from each of the 5 MiniPOD optical components to the Board Support FPGA.

  The 3 address lines to each of the 5 MiniPOD optical components are brought out to jumpers so that in an emergency the addresses can be changes. There will be only one jumper per address bit, i.e. there is an expected default configuration that will be used - but this allows any address setup in an emergency. The default address configuration is:

MiniPOD Device	ADR_2	ADR_1	ADR_0	Function
MP1	low	low	low	Base Function Transmitter
MP2	low	low	hi	Base Function Transmitter
MP3	low	low	low	Topological Receiver
MP4	low	low	hi	Topological Receiver
MP5	low	hi	low	Topological Receiver

- Transmitter:

  The Transmitter has 100 Ohm differential inputs, CML signal level, and does not require DC blocking capacitors. VCSEL, Vertical Cavity Surface Emitting Laser. Management and monitoring are through a Two Wire Serial interface TWS. Can measure light output power LOP and elapsed operating time. The signals or pins involved with the transmitter:

12x	high speed differential CML transmit data
	SCL and SDA for the Two Wire Serial interface
1x	Interrupt
3x	Address allow you to set the TWS address
1x	Reset_B
7x	DNC Reserved Do Not Connect
33x	Ground
3x	3.3V power
4x	2.5V power

The transmitter's maximum current draws are 400 mA from 2.5V and 160 mA from 3.3V. Loss of input signal is typically detected at 120 mVpp differential input. TWS clock rate is 400 kHz maximum.

- Receiver:

The Receiver has 100 Ohm differential CML level outputs that may require AC coupling capacitors. The receivers use PIN diodes. Management and monitoring are through a Two Wire Serial interface TWS. It can measure: optical input power, temperature, both supply voltages, elapsed operating time.

12x	high speed differential CML received data
	SCL and SDA for the Two Wire Serial interface
1x	Interrupt
3x	Address allow you to set the TWS address
1x	Reset_B
7x	DNC Reserved Do Not Connect
33x	Ground
3x	3.3V power
4x	2.5V power

The receiver's maximum current draws are 525 mA from 2.5V and 90 mA from 3.3V. The differential output voltage from the receiver is controllable over the 100 mVpp to 800 mV range. Common Mode output voltage 2.00 V min 2.54 V max.

Note that the differential input to the GTX receiver has a common mode of 2/3 GTX AVTT where AVTT is typically 1.2 Volts --> We must use the AC coupling.

Note that the receiver's data outputs can appear as 2.5V through 50 Ohms anytime that the receiver is powered.

- Power:

No power up sequencing is required. Note that the Power Down must be to <50mV for both 2.5V and 3.3V supplies or the module may not start up correctly next time.

- Front-Panel MTP Connectors:

Short 12-fiber optical ribbon cables are used to make the MiniPOD inputs and outputs accessible from the CMX card front panel. Two MTP feedthrough connectors are mounted on the card's front panel.

In its standard configuration both of the CMX front panel MTP feedthrough connectors will be used for a 12 fiber ribbon cable that runs to a MiniPOD transmitter. This

applies to Crate CMX and to System CMX cards processing any data type (EM, jets, etc). The MTP connectors on the CMX stub cables have male pins.

If the MiniPOD receivers are required for some application of the CMX card then a specialized optical cables setup will be required. If the MiniPOD receivers are used then it is assumed that one MTP feedthrough will have two 12 fiber ribbons running to the two MiniPOD transmitters and that the other MTP feedthrough will have three 12 fiber ribbons running to the three MiniPOD receivers.

These two use cases are illustrated in block diagrams found in:

http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/block_diagrams/

<rev_date>_CMX_Layout_DataPath_Base_Only_Crate.png
<rev_date>_CMX_Layout_DataPath_Base_Only_System.png
<rev_date>_CMX_Layout_DataPath_with_Topo.png

Appendix F: Low-Speed Optical

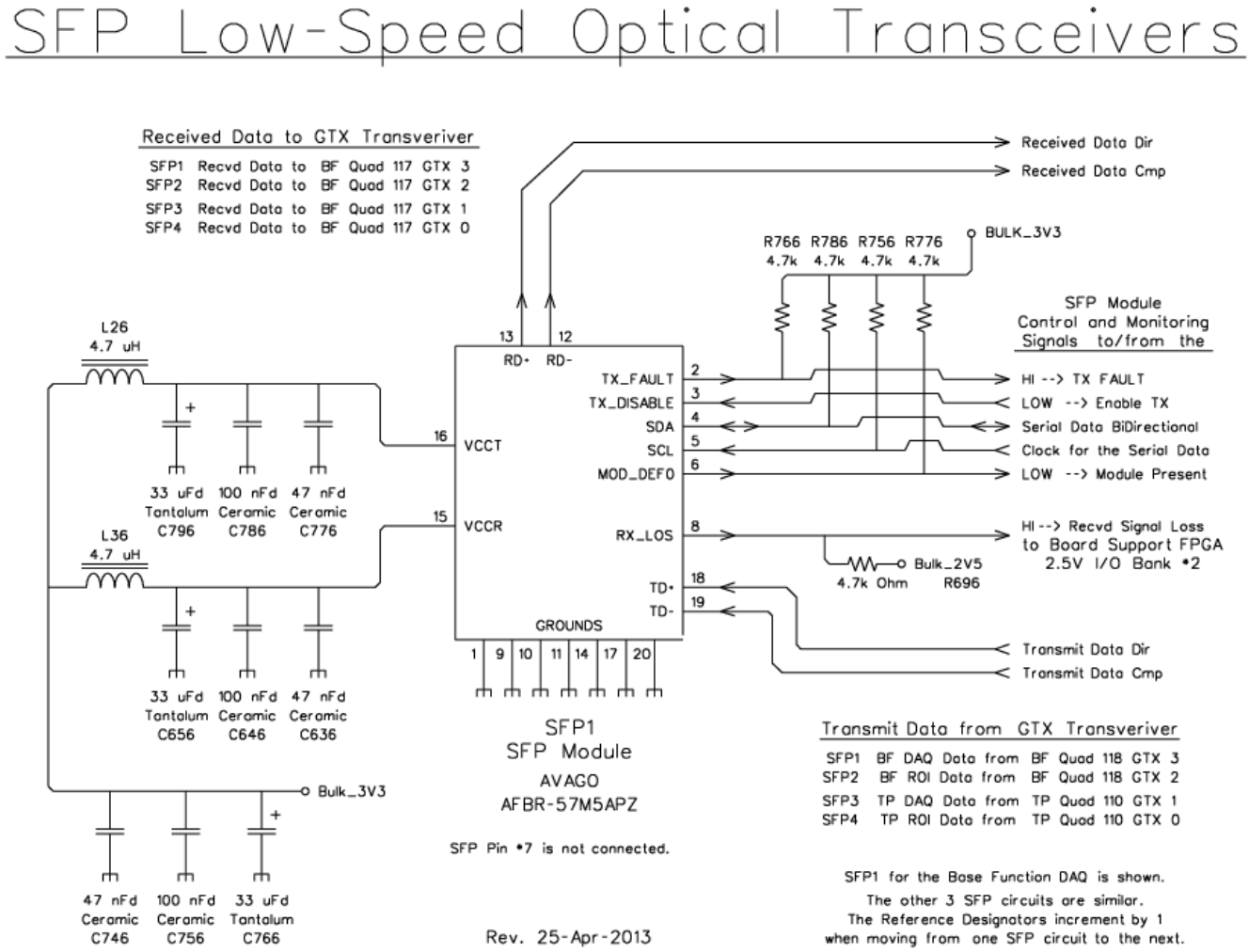


Figure 31: Circuit Diagram for the low-speed optical connections

A current snapshot of the circuit diagrams is included above while the source material is in 13_low_speed_optical.pdf found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot of the detailed description is included below while the source material is in cmx_ab_low_speed_optical.txt found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

CMX Low Speed Optical Components

Current Rev. 28-Apr-2014

This file describes the Low Speed Optical components that are used on the CMX card to send out DAQ and RIO information from the Base Function and Topological Processor FPGAs. On the CMX card these are components SFP1 through SFP4. These parts are located on the front panel of the CMX card right above and below the cable connectors for the CTP output. A circuit diagram of the Low Speed Optical components on the CMX card is given in:

13_low_speed_sfp_optical.pdf

- The actual SFP fiber optic module that is used on the CMX card is the Avago AFBR-57M5APZ optical transceiver. This Avago part is being used on the CMX card because the original Infineon part that was used on the CMM card is no longer available.

  The AFBR-57M5APZ is a Small Formfactor Pluggable transceiver. The SFP specification covers most of its operation. Only the transmitter section of this device is being used in the normal mode of operation with G-Link format output from the CMX cards. The CMX card was designed so that the option of using S-Link output was also possible. In the S-Link operation both the transmitter and receiver sections of the Avago SFP transceivers will be used.

- The monitoring and control of the 4 low speed SFP optical parts is done through the Board Support FPGA. 6 control pins from each SFP package are routed to pins in the 3.3V I/O bank of the BSPT FPGA. These 6 control pins are: TX_FAULT, TX_DISABLE, RX_LOS, MOD_DEF0, SDA, and SCL.

  The TX_FAULT signal allows the BSPT FPGA to know if there are problems with the laser transmitter. TX_DISABLE allows the BSPT to turn off the laser in the transmitter. RX_LOS indicates that the optical input is absent or unusable. The MOD_DEF0 signal tells the BSPT whether or not a component is plugged into the SFP socket. The SDA and SCL lines provide serial communication between the BSPT FPGA and the many registers in the AFBR-57M5APZ optical component.

- Power is supplied individually to each SFP socket through a filter circuit. Both the receiver and transmitter sections of the AFBR-57M5APZ transceiver will be powered. The standard l1calo G-link usage of the SFP transceivers only uses the transmitter half of the SFP transceivers, but CMX needs to allow the TP FPGA to act as its own ROD and thus instrument the SFP receiver to listen to the S-link Return Channel.

It is possible that the BF FPGA might also need to use S-link, thus all SFP receivers are wired up. All 4 SFP receivers are connected to BF GTX inputs. See below for more details on supporting a ROD functionality.

It is also not clear in the AFBR-57M5APZ data-sheet whether or not the monitoring and control functions in this device would operate normally if only its transmitter is powered.

- The CMX card does not use HP G-Link chips to encode its RIO and DAQ output data. Rather the function of the HP G-Link chip will be implemented by a combination of Virtex FPGA logic and a GTX transmitter. The reference clock to these GTX transmitters is a dedicated 120.00 MHz crystal for G-link operation. The CMX G-Link reference frequency is intentionally NOT tracking the 40.08 MHz LHC clock as required in l1calo receiver of this G-Link data.

- One reference crystal oscillator is used with the pair of SFP GTX transceivers associated with the BF function of CMX and a separate oscillator is used for the transceiver pair associated with the TP function of CMX. This is to allow the TP FPGA to implement its own ROD functionality as detailed below. If this ROD functionality and S-link protocol are needed, the crystal oscillator feeding the two SFP GTX transceivers in the TP FPGA will probably need to be a frequency of 100.00 MHz.

- The longest 100 Ohm differential traces from the BF or TP FPGAs to their SFP optical transmitters are about 185 mm long. This trace length is not be a problem at 1 GHz data rate with the pcb laminate that is used for the CMX pcb. This routing is made simpler because the AFBR-57M5APZ transceiver do not require AC coupling capacitors in their differential data lines.

Hardware Support for the TP Function to Act as Its Own ROD:

The February 2013 CMX review added a new requirement for the CMX card design to provide the hardware support necessary for the Topological Processor on CMX to be able to act as its own ROD for readout purposes. This is an alternative to the standard G-link readout of the CMM card and of the CMX Base Function DAQ and ROI outputs.

Note: It is clear that a large amount of firmware work would be required to implement ROD functionality on the CMX card and that no one is currently working on or even planning to work on this firmware. This ROD S-Link readout requirement for CMX is thus a form of insurance.

Providing ROD functionality implies using an S-link protocol instead of the G-link protocol which is used by the CMM card and the Base Function of the CMX card. The TP Function acting

as a ROD would then become a Link Source Card (LSC) with respect to the S-link protocol.

The TP function needs to be able to readout as either a G-link source (a ROD input) or as a S-link source (a ROD output). The BF function is only required to readout as a G-link source that will be connected to the existing RODs currently reading out the CMM cards that are being replaced.

The same SFP optical module is used for G-Link or S-link outputs. Only one of these two protocols can be supported at a given time and this choice applies to both DAQ and ROI outputs from the TP function.

This ROD-capable requirement has several direct implications for the CMX card design which are listed below.

GTX Reference Clocks for SFP links:

- The reference clock frequency that the CMX card supplies to the GTX transceivers driving and receiving the serial data from the two (DAQ and ROI output) TP SFP transceivers needs to be independent from the reference clock frequency supplied to the GTX transceivers driving and receiving the serial data from the two (DAQ and ROI output) BF SFP transceivers. The CMX card thus uses two separate crystals.

- If both BF and TP functions use G-link outputs, then both of these reference clocks are generated by installing two 120.00 MHz crystal oscillators.

- If the TP function needs to provide an S-link output, then its clock generator will be fitted with a 100.00 MHz crystal oscillator (or whichever frequency is appropriate for GTX channels to handle the S-link serial data).

- Views of the clock distribution to the GTX transceivers for the DAQ and ROI readout are available in circuit diagrams:

  11d_clock_generation_and_distribution_d.pdf
  26_clocks_overall_view.pdf
  27_gtx_transceivers_base_function.pdf
  28_gtx_transceivers_topological.pdf

- The clock distribution is also illustrated in block diagram found in:

  <revision_date>_CMX_Layout_Clocks.png

S-link Return Channels:

- The G-link protocol only uses the transmitter half of each SFP transceiver, but the ROD application of the S-link protocol uses both the transmitter and receiver in each SFP transceiver. The SFP transmitter carries the S-Link "Forward Channel" and the SFP receiver carries the S-link "Return Channel".

- All of the 36 GTX receiver channels available on the TP FPGA have been allocated to receive the 3 sets of 12-fiber ribbons connected to the three Avago MiniPOD receivers. The two (DAQ and ROI) TP SFP receivers must thus be connected to GTX receivers located on the BF FPGA.

- The reference clock associated with the TP SFP outputs must thus also be connected to the BF GTX channels that handle the S-link return channels.

- Two differential pairs of Select IO pins on the BF FPGA are connected to two differential pairs of Select IO pins on the TP FPGA. These two differential pairs may be used to forward the raw serial or decoded content of the S-link Return Channel information from the BF FPGA GTX receivers to the TP FPGA logic.

- The signals for these two differential pairs are in the net list files:

  Base_Fpga_Assign/base_function_24_to_tp_fpga_n2r.txt
  TP_Fpga_Assign/tp_function_24_from_bf_fpga_n2r.txt

Busy Signal:

- The requested ROD functionality in the TP FPGA needs to be able to send a Busy signal to the Central Trigger Processor (via a ROD busy module). It is not clear whether the DAQ and ROI outputs from TP would need to provide one common or two individual Busy signals. It is more likely to be one common signal as the current ROD card seem to have only one BUSY output.

- On the front panel of the CMX card there are two Access Signals (back terminated 3.3V CMOS signal) that can be driven by either the BSPT, BF, or TP FPGAs. If needed, the ROD Busy signal(s) would be made available via a custom adapter cable plugged into the CMX front panel J12 connector. The adapter cable would present the BUSY signal(s) on LEMO connectors or whatever connector type is required for this application.

- The Circuit Diagrams of the Front Panel Access signals:

    29_front_panel_access_signals.pdf
    34_front_panel_j12_connector_and_cables.pdf

- The signals for these optional front-panel Busy signals are in the net list files:

    Everything_Else/debug_connector_nets_n2p.txt
    TP_Fpga_Assign/tp_function_26_debug_connections_n2r.txt

TCM Control Information:

- The buffer management required by the ROD function is driven by control information provided by the TCM. This control information is received and decoded by the TTCDec mezzanine on the CMX card.

- To avoid any chance of omission or misunderstanding all of the TTCDec outputs are made available to the TP FPGA.

Appendix G: TTCDec data distribution

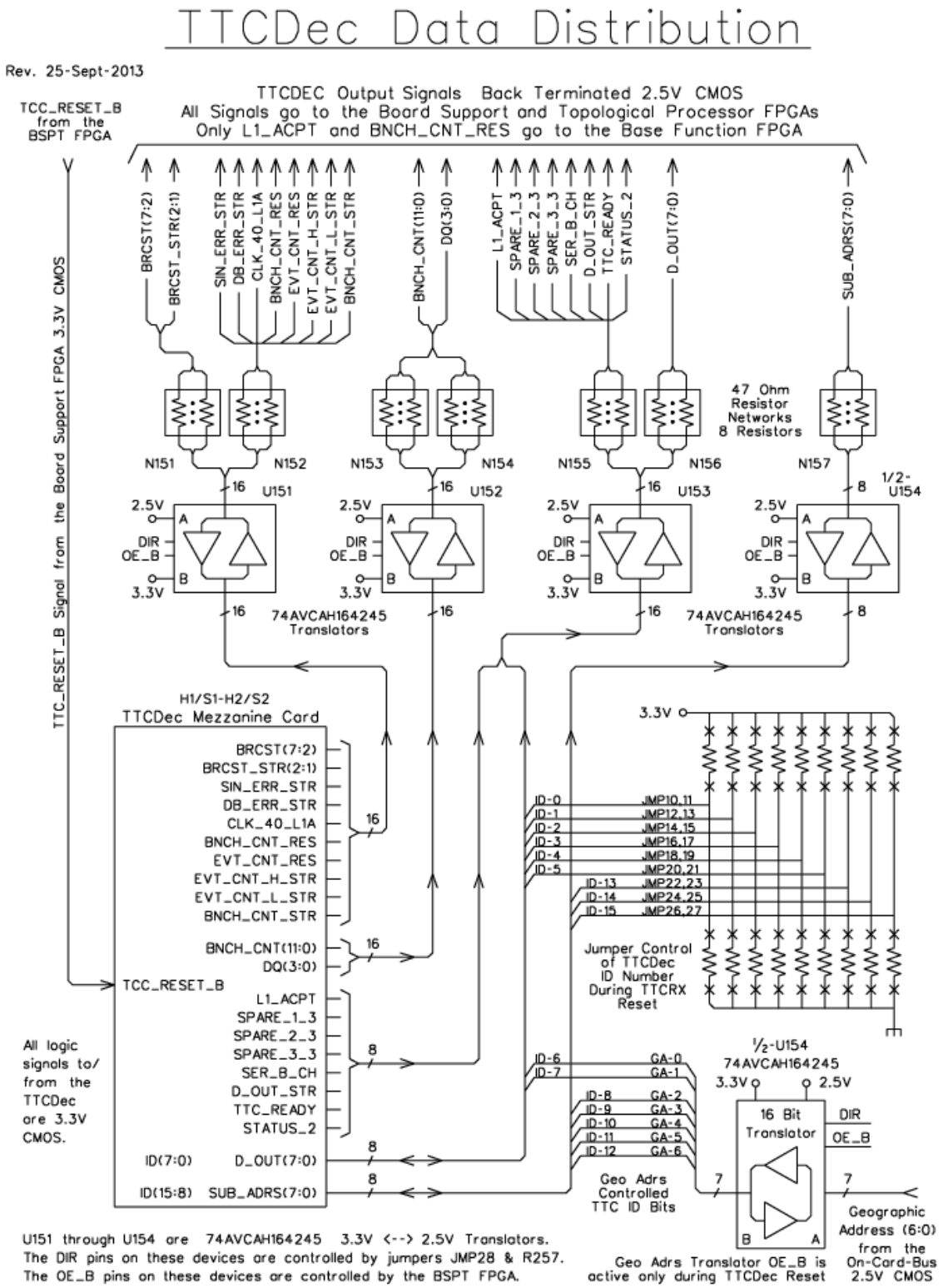


Figure 32: Circuit Diagram for TTCDec data distribution

A current snapshot of the circuit diagrams is included above while the source material is in 12_ttcdec_data_distribution.pdf found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot of the detailed description is included below while the source material is in cmx_ab_ttcdec_connections.txt found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
                CMX  TTCDec Signal Connections
               --------------------------------


                                        Current Rev. 27-Apr-2014


This file describes the connections to the TTCDec mezzanine
card on the CMX circuit board.  The TTCDec mezzanine card is
located in the lower right-hand corner of the card where it
is close to its input "clock" and were its outputs can run
directly up on the right hand side of the 3 FPGAs that use
the TTCDec output signals.


The TTCDec "input clock" enters the CMX card via backplane
pins and is immediately received by the differential buffer
chip U155.  The input to the U155 buffer is AC coupled with
10 nFd capacitors to help reduce out of band noise.  This
OnSemi NB6L611 buffer provides an internal input termination.
From the output of this buffer there is a short direct
connection to the clock input on the TTCDec mezzanine.

The DeSkew_1 and DeSkew_2 clock outputs from the TTCDec
provide the time-base for the CMX card.  These TTCDec
clock connections are shown in the following drawings:

  26_clocks_overall_view.pdf
  11a_clock_generation_and_distribution_a.pdf
  11b_clock_generation_and_distribution_b.pdf


Installation of either jumper R254 or R256 selects either
the TTCDec:  CLK_40_DES_1_PLL_2  or the  CLK_40_DES_1  signal
as the source of the DeSkew_1 timing on the CMX card.
Jumper R255 is always installed to select the TTCDec signal
CLK_40_DES_2_PLL_2  as the source of DeSkew_2 timing on the
CMX circuit board.

These TTCDec clock outputs are right next to the Clock
Generation and Distribution section of the CMX card.  With
this close physical location of the TTCDec and the Clock
Generation and Distribution components the interconnecting
traces are kept short and direct and are located in a quiet
section of the CMX circuit board.
```

A drawing showing the output signals from the TTCDec mezzanine card and the reset signals to the TTCDec is on the web at:

12_ttcdec_data_distribution.pdf

All of the non-clock type TTCDec output signals are buffered by 3.3V to 2.5V translators (74AVCAH164245s) and then back terminated by 47 Ohm resistor packs. These buffered TTCDec outputs run up the right-hand side of the 3 FPGAs on the CMX card. All of the TTCDec output signals are routed to both the BSPT FPGA and to the Topological Processor FPGA.

Only the TTCDec signals: L1_ACCEPT and BNCH_CNT_RESET are routed to the Base Function FPGA. Routing only these two TTCDec output signals to the BF FPGA matches the functionality on the CMM card. Because of the high density of traces in the break-out region of the BF FPGA the intent is to not route TTCDec signals to the BF that will clearly never be used by it. The full list of TTCDec output signals is given for reference at the end of this note.

The TTCDec can be reset by the BSPT FPGA. The TTCDec_Reset_B signal comes directly from a pin in the 3.3V I/O Bank of the BSPT FPGA. The process of resetting the TTCDec includes sending ID bits 13:0 and the 2 Master Mode bits to the TTCDec. In some ATLAS documents the 2 Master_Mode bits are referred to as ID bits 14 and 15 probably because this makes a nice round 16 bit quantity.

CMX uses the same basic method of providing the ID and Master Mode bits to the TTCDec during its Reset process as the CMM card does. Considering the ID plus Master Mode information as one 16 bit quantity, bits 15, 14, 13, and bits 5:0 come from a set of resistor "jumpers": JMP27 through JMP10. During Reset the pins in the TTCDec that receive this information become inputs and their logic level is determined by which of these resistor jumpers have been installed. After the Reset process is complete these same pins are outputs with sufficient drive to over come the bias of the installed 4.7k Ohm resistor jumpers.

ID bits 12:6 are handled in basically the same way except that during the Reset process these 7 ID bits come from the output of one half of U154 a 2.5V to 3.3V translator chip. The input to this translator is the 7 bit Geographic Address of the CMX card that comes from the 2.5V On-Card_Bus. During the TTCDec Reset process the BSPT FPGA coordinates enabling the output drivers on this half of the U154 translator in time with the TTCDec_Reset_B signal. After the Reset process the output of this half of the U154 translator is disabled and the TTCDec pins that received ID bits 12:6 return to being outputs.

On the CMX card the BSPT FPGA provides connections to the SDA and SCL pins on the TTCDec. These signals come from the 3.3V I/O Bank on the BSPT FPGA and are back terminated by resistors R324 and R325. These signals are the I2C serial bus connection to the TTCDec mezzanine card.

The 3.3V I/O bank on the BSPT FPGA also provides direct connections to the CLK_SEL and P/D pins on the TTCDec. These signals select either a 40.000 MHz crystal on the TTCDec mezzanine or the TTCrx ASIC Clk40Des1 and Clk40Des_2 signals in either a Normal mode or a Protected mode as the source of the clock outputs from the TTCDec. Recall that the CMX cards Clock Generation and Distribution circuits can only operate with a real LHC frequency clock reference, i.e. they will not operate correctly with a 40.000 Mhz reference clock.

The CMX card also provides a JTAG connection to the TTCDec mezzanine on its 3.3V Test JTAG chain. No JTAG management of TTCDec is required that I know of. Jumpers are normally installed to jump the Test JTAG chain around the TTCDec. The only required management of the TTCDec that I know of is to Reset it.

The 2.5V buffered TTCDec output signals that are available to the 3 FPGAs on the CMX card are the following:

BRCST(7:2), BRCST_STR(2:1)	from one section of U151
SIN_ERR_STR, DB_ERR_STR, CLK_40_L1A, BNCH_CNT_RES, EVT_CNT_RES, EVT_CNT_H_STR, EVT_CNT_L_STR, BNCH_CNT_STR	from other section of U151
BNCH_CNT(11:0), DQ(3:0)	from U152
L1_ACPT, SPARE_1_3, SPARE_2_3, SPARE_3_3, SER_B_CH, D_OUT_STR, TTC_READY, STATUS_2	from one section of U153
D_OUT(7:0) - ID(7:0)	from other secion of U153
SUB_ADRS(7:0) - ID(15:8)	from one section of U154

Note that if it ends up that only the TTCDec signals: L1_ACCEPT and BNCH_CNT_RESET are ever needed for the operation of the Base Function, Topological, and BSPT FPGAs then to reduce the amount of digital noise on the CMX card one could turn off the 2.5 V outputs on: one section of U151, both sections of U152, one section of U153, and the section of U154 that is used to drive the 2.5V TTCDec signals to the FPGAs.

Appendix H: Clock Generation and Distribution

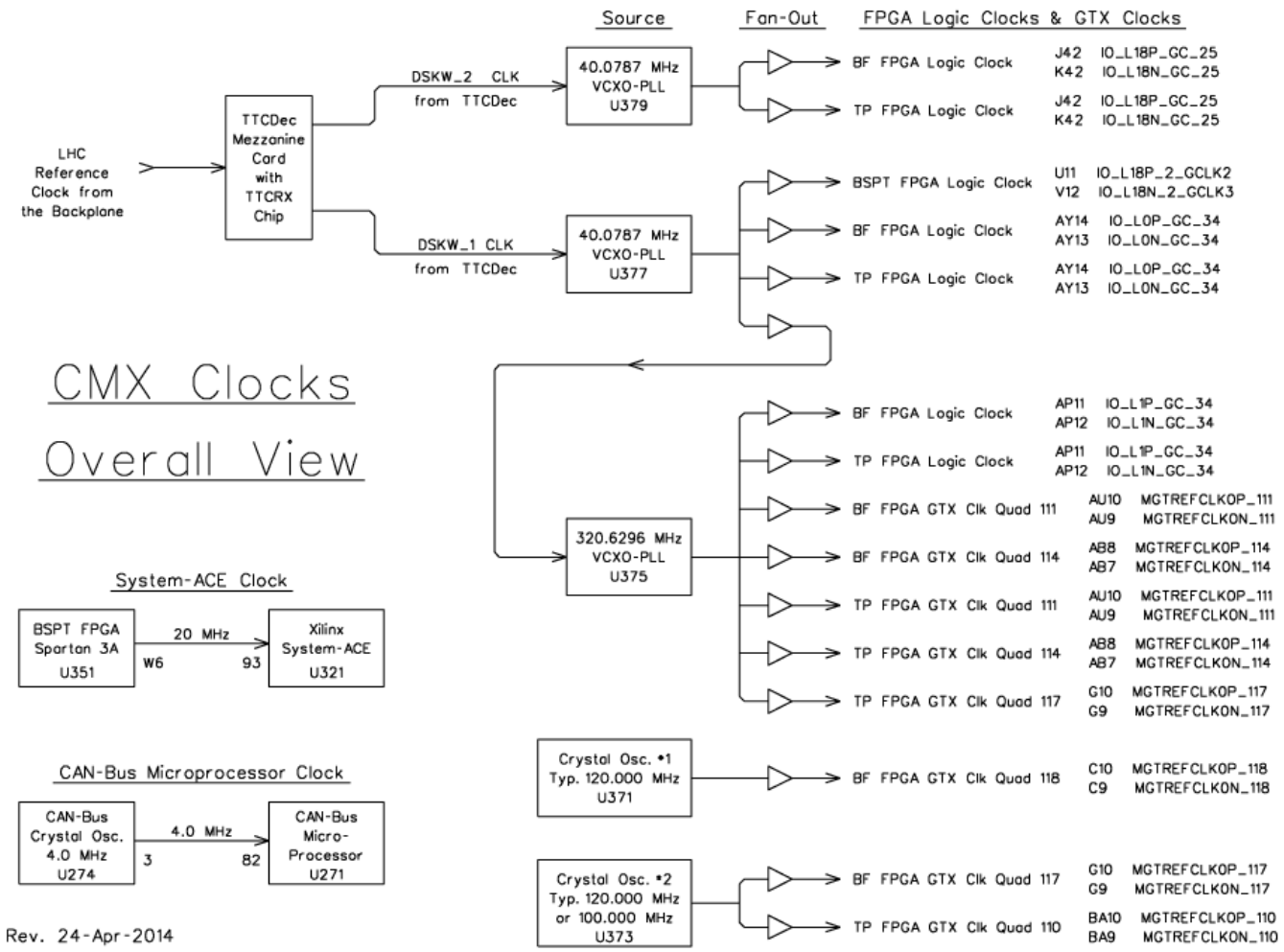


Figure 33: Overall Diagram of CMX Clock generation and distribution

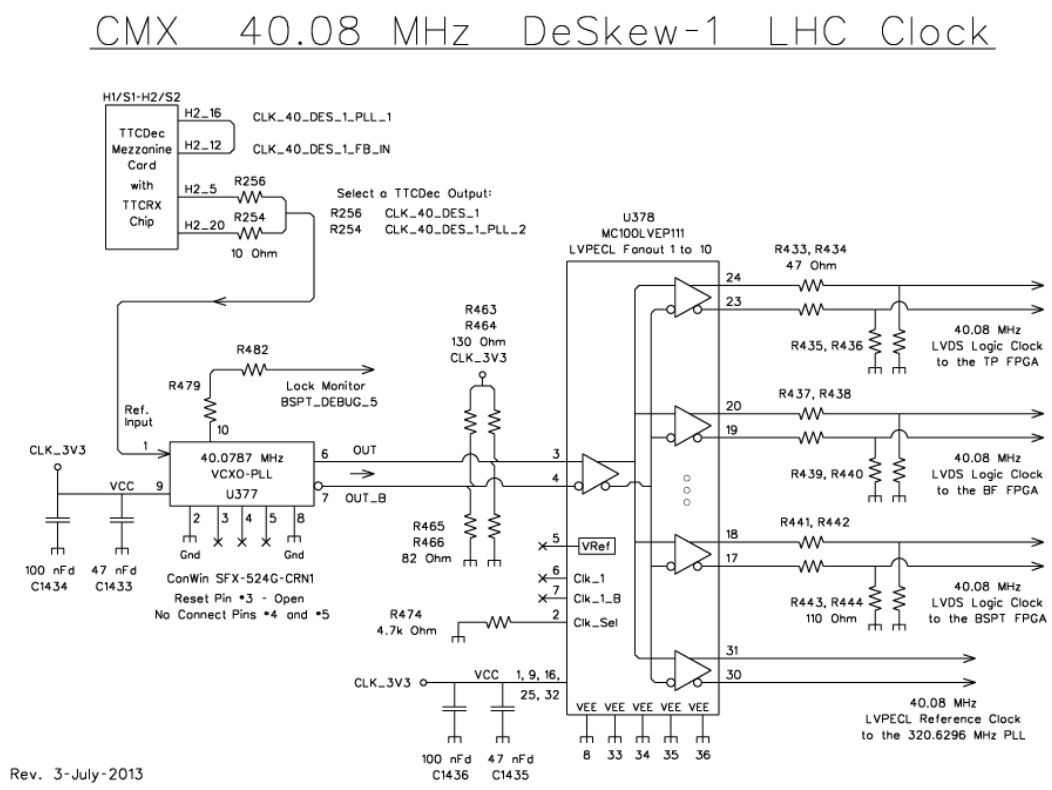


Figure 34: Circuit Diagram for 40.08 MHz DeSkew1 clock generation and distribution

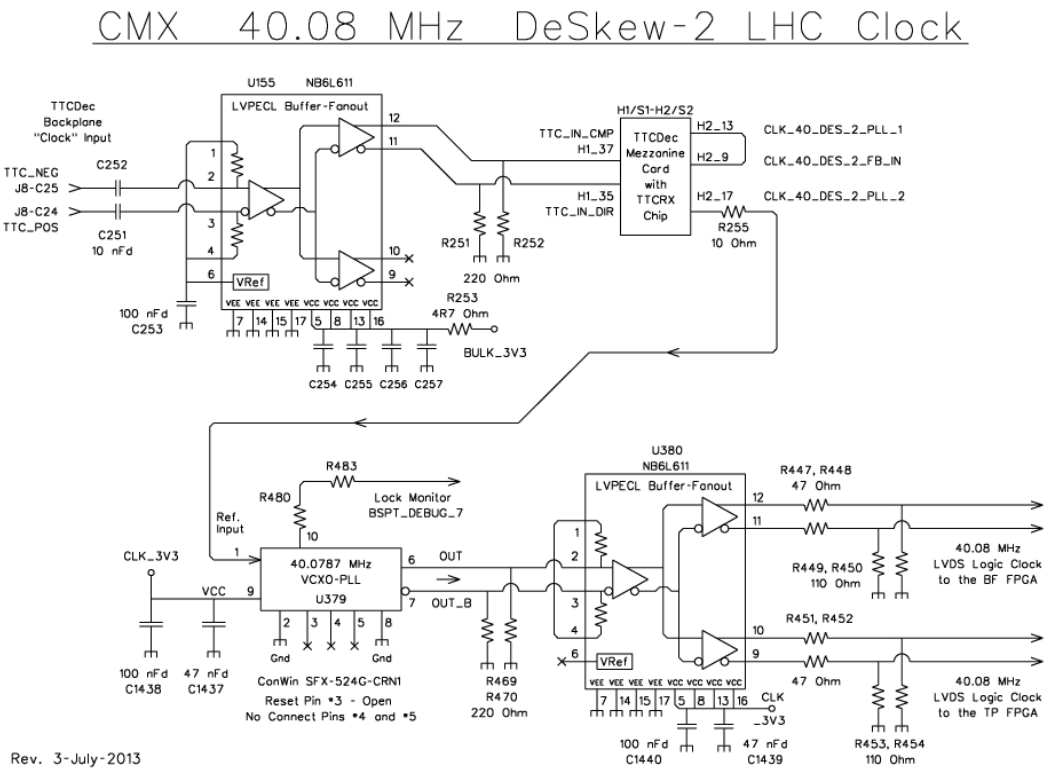


Figure 35: Circuit Diagram for 40.08 MHz DeSkew2 clock generation and distribution

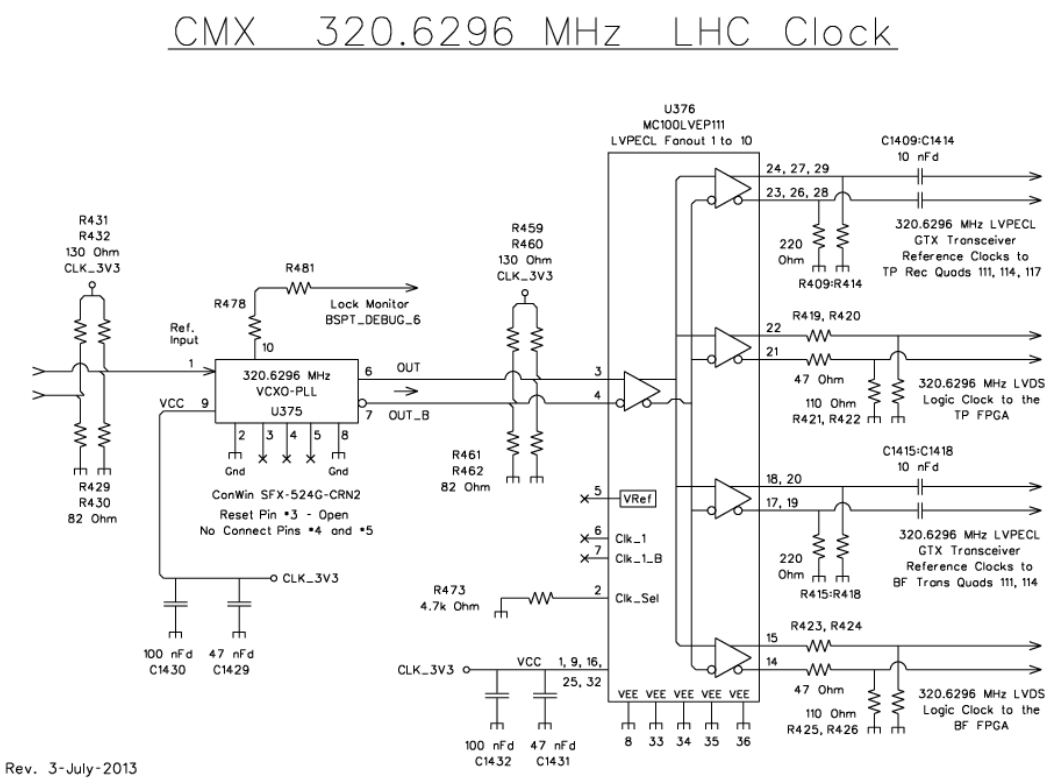


Figure 36: Circuit Diagram for 320.6 MHz clock generation and distribution

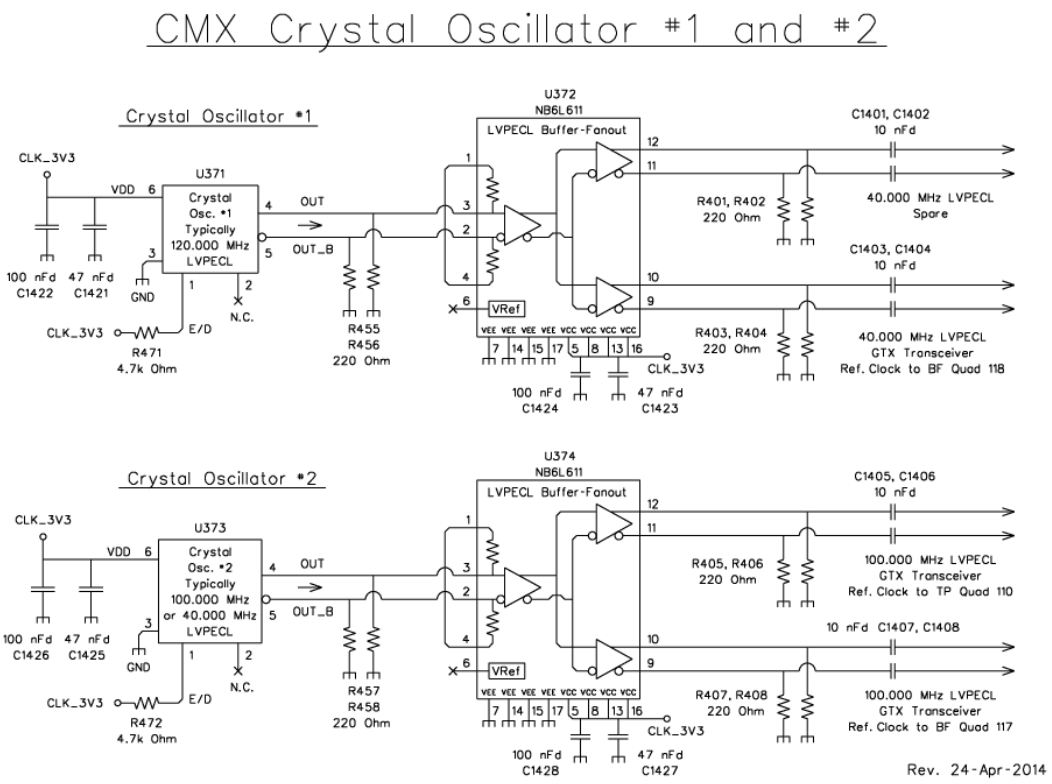


Figure 37: Circuit Diagram for fixed frequency clocks generation and distribution

A current snapshot of the circuit diagrams is included above while the source material is in

- 26_clocks_overall_view.pdf
- 11a_clock_generation_and_distribution_a.pdf
- 11b_clock_generation_and_distribution_b.pdf
- 11c_clock_generation_and_distribution_c.pdf
- 11d_clock_generation_and_distribution_d.pdf

found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot of the detailed description is included below while the source material is in cmx_ab_clock_gen_and_dist.txt found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
            CMX  Clock Generation and Distribution
          ----------------------------------------


                                          Original Rev.  20-Nov-2012
                                           Current Rev.  30-Apr-2014


This file describes the generation and distribution of the
clocks on the CMX circuit board.  The main focus of this
file is the LHC locked 40.08 MHz and 320.64 MHz clocks for
the Logic and GTX Transceiver functions in the 3 FPGAs on
the CMX card.

In addition to these LHC locked clocks the CMX circuit board
includes:  GTX Quad reference clocks of 40.000 and 100.000 MHz
to the BF and TP FPGAs for G-Link and possibly for S-Link
operation of GTX Transceivers,  a 20 MHz clock to the Xilinx
System ACE, and a 4 MHz clock to the CAN-Bus microprocessor.

An overall view of the clocks on the CMX card is shown in the
following drawing in the circuit diagrams section of the MSU
CMX web site:

   26_clocks_overall_view.pdf


The generation and distribution of the LHC locked 40.08 MHz
and 320.64 MHz clocks is shown in the following 3 drawings:

   11a_clock_generation_and_distribution_a.pdf
   11b_clock_generation_and_distribution_b.pdf
   11c_clock_generation_and_distribution_c.pdf
```

The generation of the 40.000 MHz and 100.000 MHz crystal oscillator based clocks is shown in the drawing:

11d_clock_generation_and_distribution_d.pdf

The distribution of reference clocks into the Base Function and Topological Processor GTX Quads is shown in the drawings:

27_gtx_transceivers_base_function.pdf
28_gtx_transceivers_topological.pdf

Basic Design of the LHC Locked Clocks:

- On the CMX circuit board the LHC reference for the LHC locked clocks comes from a TTCDec mezzanine.
- The CMX card provides a TTCDec DSKW-1 locked 40.08 MHz Logic clock to all 3 FPGAs.
- The CMX card provides a TTCDec DSKW-2 locked 40.08 MHz Logic clock to just the BF and TP FPGAs.
- The 320.64 MHz clock that is generated on the CMX card is locked to the TTCDec DSKW-1 output. This 320.64 MHz clock is provided as both a Logic clock and as a GTX Reference clock to both the BF and TP FPGAs.
- The CMX card uses a narrow band PLL-VCXOs to generate its clean LHC phase locked 40.08 and 320.64 MHz clocks.
- The PECL outputs from the three narrow band PLL-VCXOs are fanned out using low noise PECL clock distribution chips.
- Signals from these clock distribution chips are routed as either LVDS level signals to differential Global Clock inputs on the FPGAs and as AC coupled LVPECL level signals to differential GTX Reference clock inputs on the GTX Transceiver Quads.

Virtex-6 Clock Input Signal Levels:

- The signal level requirement for the GTX Transceiver reference clocks is clearly given in the chapter 5 of the GTX User Guide and in the Virtex-6 DC and Switching Data Sheet. The GTX reference clock input is clearly aimed at AC coupled Differential LVPECL signal levels. In the GTH User Guide AC coupled Differential LVPECL reference clocks are specifically recommended.

- The Global Clock inputs for the Base Function and Topological Processor logic clocks can be any signal level that is supported by the Virtex-6 Select I/O inputs. It does not appear that the Select I/O inputs will directly accept Differential LVPECL with internal termination. The cleanest solution appears to be to use LVDS_25 signal levels to send the logic clocks to the Virtex-6 global clock inputs (and to the Board Support Spartan 3A FPGA). In all cases internal 100 Ohm internal termination can be used with these LVDS_25 signals.

- The 40.08 MHz and 320.64 MHz clock fanout is all done with Differential LVPECL chips and the logic clocks to the Virtex-6 Global Clock inputs may be scaled to LVDS_25 levels with simple resistor networks at the sending end and internally differential terminated at the receiving FPGA end.

- The relevant signal specifications are:

  Virtex-6 LVDS_25 Input:

V Input Diff:	100 mV min,	350 mV Typ,	600 mV max
V Input CM:	0.30 V min,	1.25 V Typ,	2.20 V max

  MC100LVEP111 Differential LVPECL Output:

Vout HI:	2.155 V min,	2.280 V Typ,	2.405 V max
Vout LOW:	1.355 V min,	1.530 V Typ,	1.700 V max

Scaling Differential LVPECL to LVDS_25:

- Scaling both the Direct and Complement LVPECL outputs at the sending end by makes both the differential and common mode voltages in the correct range for reception by the Xilinx LVDS_25 receivers.

- The resistor network to scale the Differential LVPECL signals can be 47 Ohm series then 110 Ohm to ground.

- At the Virtex input:
  The expected differential voltage will be 317 mV.
  The expected common mode voltage will be 1.349 V.

- This will result in about 16.9 mA of emitter current to the HI side of the Diff LVPECL driver and 7.6 mA to the LOW side. These emitter currents are right in the normal operating range for these parts.

- The internal Xilinx 100 Ohm differential LVDS terminator can be used with these LVDS level clock lines.

- Average heat in the 47 Ohm resistor is 8.1 mW
  Average heat in the 110 Ohm resistor is 16.7 mW
  So 0603 size resistors may be used in this application.

Base Function and TP GTX Transceiver Reference Clock:

- The GTX transceiver PLLs can multiply up their reference clock by a factor in the range from 4 to 25.

- The GTX transceiver PLL output is 1/2 the transceivers line bit rate, e.g. 3.3 GHz PLL output gives 6.6 Gb/s data rate.

- The GTX transceiver PLL's reference must be in the range from 62.5 MHz to 650 MHz, 50/50 duty cycle, 200 ps edge speed, AC coupled, 800 mV typical differential amplitude with range of from 210 to 2000 mV differential, 100 Ohm input resistance. Note the somewhat special way that Xilinx defines differential amplitude for the Transceiver Reference Clocks.

- The GTX transceivers can operate over the data rate range from 480 Mb/s up to 6.6 Gb/s. What internal PLL ratios do they use ?

  At the low end:
  480 Mb/s --> 240 MHz PLL output
  240 MHz divided by 62.5 MHz Ref --> 3.84 ratio

  At the Hi end:
  6.6 Gb/s --> 3.3 GHz PLL output
  3.3 GHz divided by 62.5 MHz Ref --> 52.80 ratio
  3.3 GHz divided by 650 MHz Ref --> 5.08 ratio

- GTX PLL Control Values:

  The reference clock is divided by "M"
  before going into the PLL M = 1 or 2

  The feedback divider is N1 x N2
  where N1 = 4 or 5
  where N2 = 2 or 4 or 5
  and where N1 x N2 must not equal 4 or 5

  There is a final divider "D" between the PLL output and the transceiver where D is either 1 or 2 or 4

  Recall that the line rate is 2x the PLL output frequency.

  GTX User Guide 2v6 pg 117 shows typical reference clocks in the range of about 200 to 325 MHz for line rates of about 4 to 6 Gb/s.

We know that for a 6.4 Gb/s line data rate we want/need
M = 1 and D = 1.

- The actual line rate that we want is 6.4 Gb/s
--> 3.2 GHz PLL output which is 80 times the "40 MHz"
LHC frequency. 80 is 2 x 2 x 2 x 2 x 5

- Example setups from 40 MHz LHC to 6.4 Gb/s:

  40 MHz times 8 external gives 320 MHz reference
  320 MHz reference with N1=5 and N2=2 give 3.2 GHz

G-Link GTX Transceiver Reference Clock:

- Reference Clock for the "Slow Optical" RIO and DAQ Outputs

  On the CMX card the G-Link for the ROI and DAQ outputs
  will be implemented with GTX transceivers. This GTX
  implementation of the G-Link will need a 120.000 MHz
  non LHC locked reference clock. This is provided by
  a separate 120.000 MHz LVPECL crystal oscillator and
  PECL fanout chip. This is CMX Crystal Oscillator #1
  reference designator U371. This 120.000 MHz PECL clock
  signal is AC coupled to the GTX Quad 118 Reference
  Input on the Base Function FPGA.

Board Support FPGA Clock:

- The Spartan 3A Board Support FPGA will receive just one
clock - the LHC locked 40.08 MHz clock referenced to the
TTCDec DSKW-1 output.

- The Spartan 3A part can receive this clock as an LVDS
signal with internal 100 Ohm termination.

- The LVDS input specifications for the Spartan 3A are:
  V Input Differential: 100 mV min, 350 mV Typ, 600 mV max
  V Input Common Mode: 0.30 V min, 1.25 V Typ, 2.35 V max

- This is really a Xilinx LVDS_25 signal going to an
I/O Bank with VCCO of 2.5 Volts.

- The same resistor network as described above will be
used to connect the LVPECL fanout signal to this Spartan 3A
LVDS_25 global clock input.

System-ACE Clock:

- The System-Ace typically runs from a 20 MHz clock.

- The 20 MHz clock for the System-ACE needs to be the same as the clock that is running whatever device is connected to the System-ACE Microprocessor port, i.e. its MPU port.

- On the CMX card it is the Board Support FPGA that provides the connection to the ACE MPU port. The BSPT FPGA runs from the 40.08 MHz clock and it will provide a 20.04 MHz clock to the System-ACE. In this way the cycles in the MPU port of the System-ACE will be synchronous with activities in the BSPT FPGA.

- The clock input to the System-ACE is referenced to its VCCL power bus. On the CMX card the System-ACE VCCL bus will be supplied with 2.5 Volts. Thus the pin #93 clock input to the System-ACE must be a 2.5V CMOS level clock signal.

- The System-ACE clock trace will be back terminated at the BSPT FPGA. The source of the ACE clock is pin V14 on the BSPT FPGA.

CAN-Bus Microprocessor Clock:

- The clock to the MB90F594 CAN-Bus microprocessor can be either a 4 MHz quartz crystal with associated capacitors connected to the X0 and X1 pins or it can be a clock signal connected to only the X0 pin with pin X1 floating.

- Table 3 DC Characteristics page 39 hints that this device has strange input voltage levels, i.e. Vish min of 0.8 x Vcc and Vils max of 0.5 x Vcc. The diagram on page 41 hints that the X0 clock input runs between 0.2 x Vcc and 0.8 x Vcc. Other diagrams e.g. pg 45 indicate TTL type levels of 0.8V and 2.4V.

- CMX will provide a real 5V CMOS 4 MHz clock to the X0 pin (pin No. 82) of the MB90F594 CAN-Bus microprocessor and it will float its X1 pin (pin No. 83). This is the setup shown on page 13 of the MB90F594 data sheet.

```
LHC Locked Clock Frequency:
---------------------------

 - The LHC RF frequency is about:         400.8       MHz

 - The LHC BX frequency is really:
    At 450 GeV Proton Injection:           40.0788790 MHz
    At   7 TeV Proton Physics:             40.0789658 MHz
    At 450 GeV Ion Injection:              40.0784139 MHz
    At   7 TeV Ion Physics:                40.0789639 MHz

 - Round to the nearest 1 Hz:
    At 450 GeV Proton Injection:           40.078,879  MHz
    At   7 TeV Proton Physics:             40.078,966  MHz
    At 450 GeV Ion Injection:              40.078,414  MHz
    At   7 TeV Ion Physics:                40.078,964  MHz

 - For all modes the biggest pulls at 40.08 MHz are +- 276 Hz

 - For all modes the fastest slew rates at 40.08 MHz are 22 Hz/sec
   The ramp up/down slews are much slower  < 1 Hz/sec

 - The center for Protons is:  40.078,922  MHz   +-  43 Hz

 - The center for Ions is:     40.078,689  MHz   +- 275 Hz

 - The center for both is:     40.078,690  Mhz   +- 276 Hz

 - Order symmetric pull center frequency of:   40.078 700 MHz
     This will require a pull of +266 Hz  - 286 Hz
     This is a pull of about 7.2 ppm

 - Order symmetric pull center frequency of:  320.629 600 MHz
     This is a pull of about 7.2 ppm



Components Used:
----------------

 - 40.0787 MHz input, 40.0787 MHz output VCXO PLL
   3.3V CMOS or AC PECL reference input signal level
   Differential LVPECL output signal level
   50 Hz PLL loop bandwidth
   Custom 40.0787 MHz PLL Clock
   6 x 5 mm  10 pin   SMD
   Connor-Winfield Part No.  SFX-524G-CRN1

 - 40.0787 MHz input, 320.6296 MHz output VCXO PLL
   3.3V CMOS or AC PECL reference input signal level
   Differential LVPECL output signal level
   200 Hz PLL loop bandwidth
   Custom 320.6296 MHz PLL Clock
   6 x 5 mm  10 pin   SMD
   Connor-Winfield Part No.  SFX-524G-CRN2
```

- Clock 1 to 10 Fanout OnSemi MC100LVEP111MNG
  Differential LVPECL inputs and outputs
  3.3 Volt power 5mm x 5mm LLP-32 QFN-32

- Clock 1 to 2 Fanout OnSemi NB6L611MNG
  Differential LVPECL inputs and outputs
  3.3 Volt power 3mm x 3mm 6-VFQFN 16-QFN

- 100.000 MHz PECL Crystal Oscillator
  7 x 5 mm 6 pin 3.3 Volt SMD
  Connor-Win Part Number: P143-100.0M

- 120.000 MHz LVPECL Crystal Oscillator
  7 x 5 mm 6 pin 3.3 Volt SMD
  Connor-Win Part Number: PGF123-120.0M

- 4 MHz 5 Volt CMOS Crystal Oscillator
  5.0mm x 3.2mm 4 pin package SMD
  ECS Inc. Part No. ECS-3961-040-AU-TR

Monitoring of the PLL Based Clock Signals:

- The narrow band PLL-VCXO components that are used to generate the LHC locked 40.08 and 320.64 MHz clock signals provide an output signal that indicates whether or not they are locked to their reference input.

- This "Lock Detect" signal from the three PLLs on the CMX card has been routed so that these signal can be inputs to the BSPT FPGA. I assume that these signals will be bits in a status register which will indicate whether or not the PLLs are locked onto the reference signals from the TTCDec.

- Logic can be placed in the BSPT to detect even isolated momentary drop out of a Lock Detect signal.

Layout of the Clock Generator Section of the CMX Card:

- The TTCDec reference clock enters the CMX card at its lower right-hand corner. This input is buffered and sent to the TTCDec input.

- The TTCDec mezzanine is located immediately to the West of its reference input buffer chip. The standard pair of SamTec QSH connectors is provided for mounting the TTCDec mezzanine card.

- All ground connections to the TTCDec have been connected and locally bypassed 3.3V power is provided to the TTCDec via its QSH connectors.

- The CLK_40_DES_2_PLL_2 output and either the CLK_40_DES_1 or the CLK_40_DES_1_PLL_2 output may be selected as the DSKW-2 and DSKW-1 references that are used by the CMX card.

- The Clock Generator section of the CMX card is immediately West of the TTCDec mezzanine card.

- All components within the CMX Clock Generator run from an isolated filtered 3.3V power plane that services just the Clock Generator section of the CMX card. This power is distributed on a separate "fill" within the CMX pcb.

Appendix I: VME-- and On-Card Bus

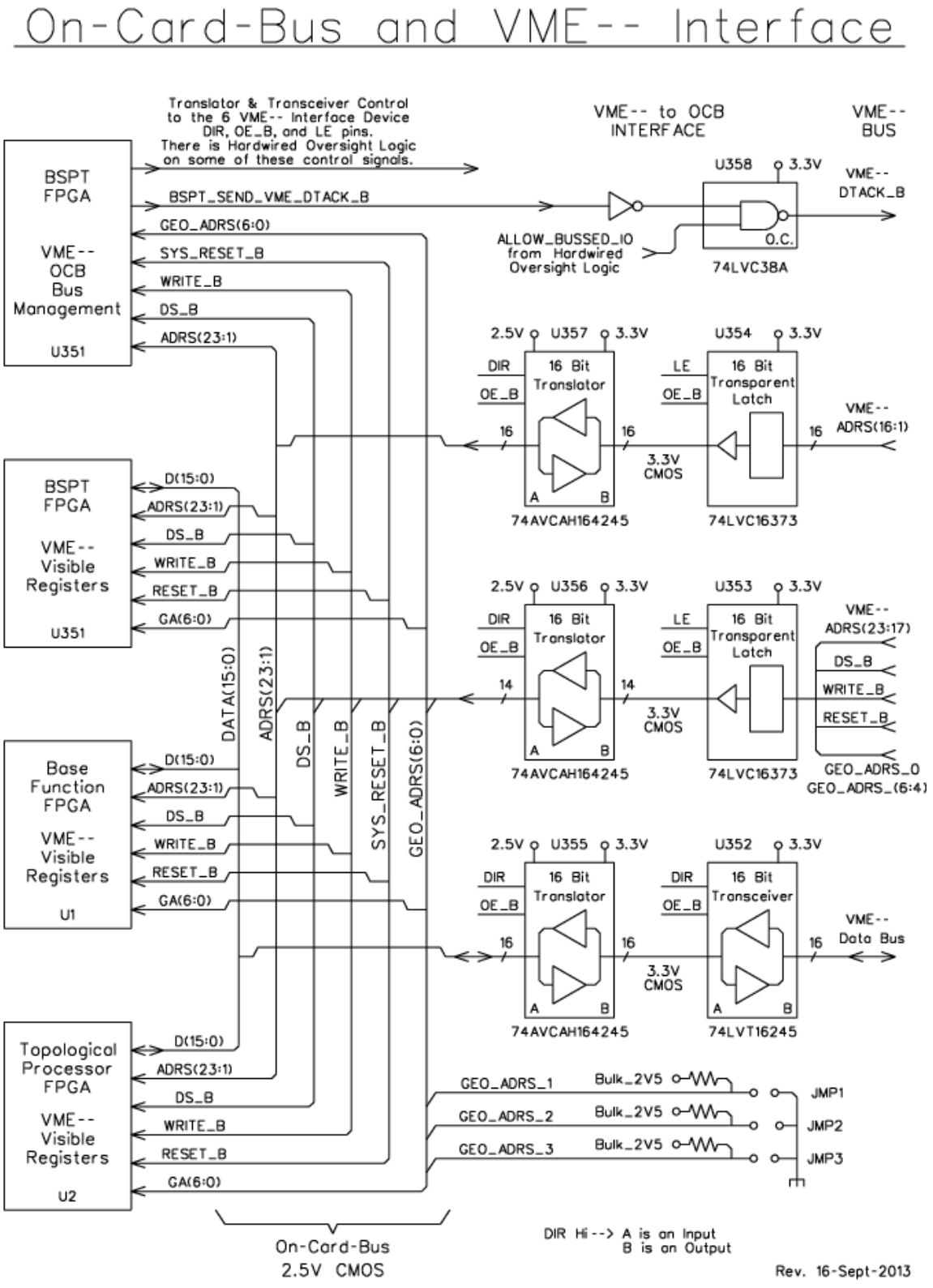


Figure 38: Circuit Diagram for the On-Card Bus Distribution

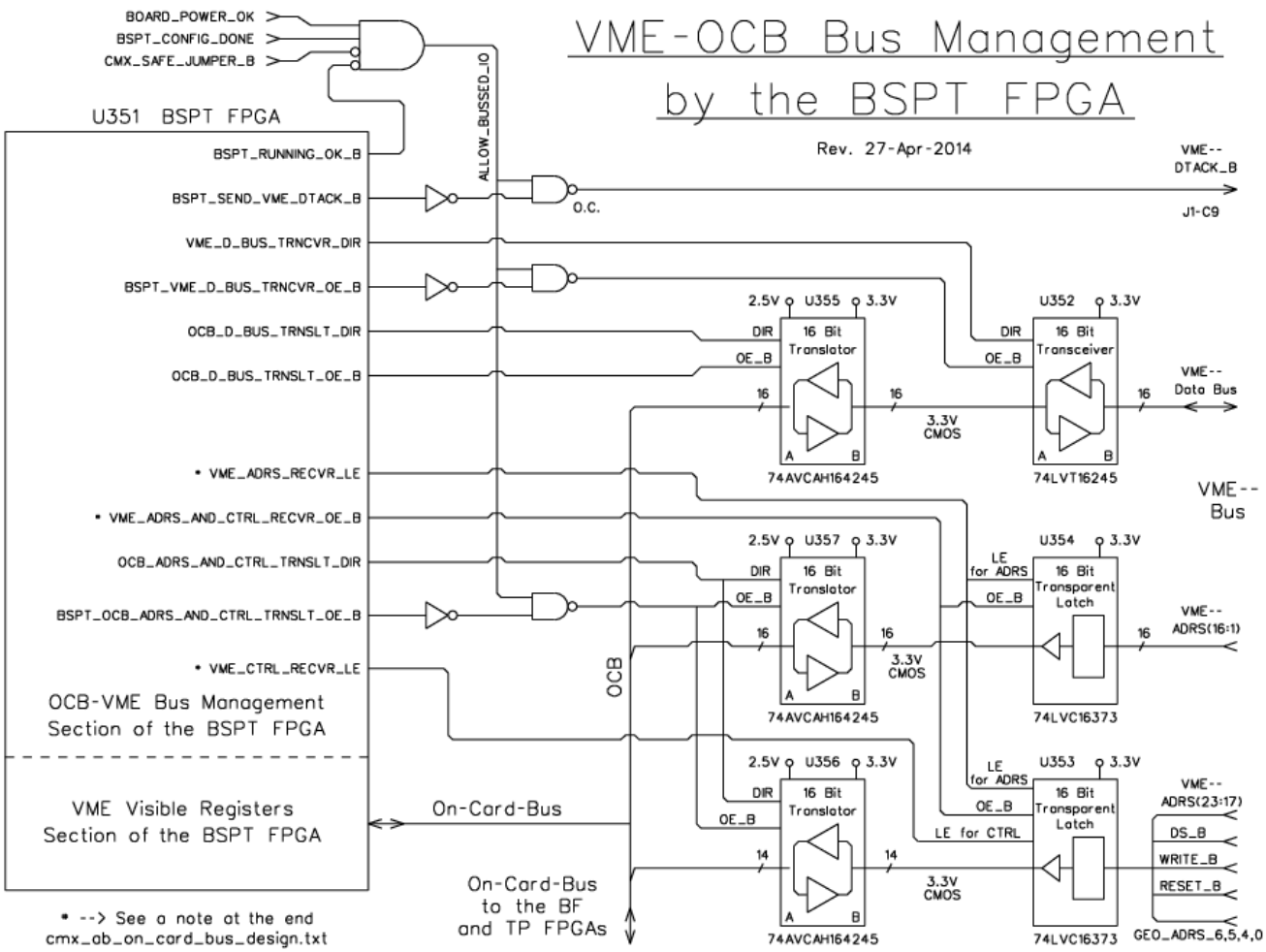


Figure 39: Circuit Diagram for the On-Card Bus Management

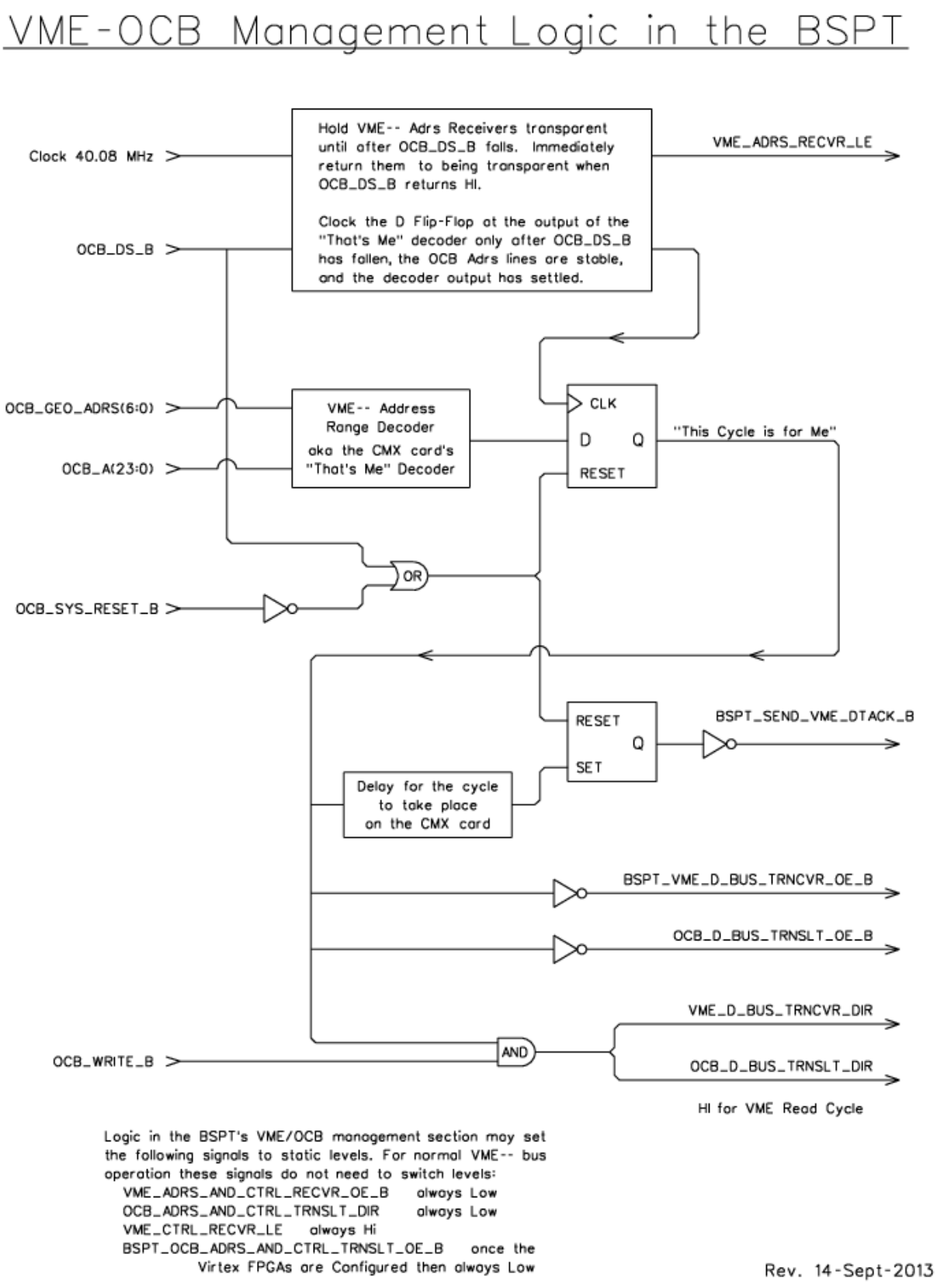


Figure 40: Circuit Diagram for the On-Card Bus Mangement Logic in the BSPT

A current snapshot of the circuit diagrams is included above while the source material is in

- 08_on_card_bus_and_vme_interface.pdf
- 20_vme_ocb_management.pdf
- 25_bspt_management_of_vme_ocb.pdf

found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot of the detailed description is included below while the source material is in cmx_ab_on_card_bus_design.txt found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
                  CMX  OCB  On-Card-Bus
                -------------------------

                                      Original Rev. 31-Oct-2012
                                       Current Rev. 30-Apr-2014


This file describes the CMX circuit board's  On-Card-Bus  and
its connection to the VME-- backplane bus.  The CMX card is a
slave only, A24D16 only device on the VME-- bus.  In this
document I will refer to the L1Calo VME-- bus just as "VME".


The OCB connects to 5 objects on the CMX card:
----------------------------------------------

 - It connects to the VME backplane receiver and driver chips

 - to the VME/OCB Bus Management function in the Board Support FPGA

 - to registers and/or memory in the Board Support FPGA

 - to registers and/or memory in the Base Function FPGA

 - to registers and/or memory in the Topological Processor FPGA


Circuit Diagrams:
-----------------

Please refer to the following circuit diagrams which illustrate
the OCB bus and its connection to the VME backplane bus:

  08_on_card_bus_and_vme_interface.pdf
  20_vme_ocb_management.pdf
  25_bspt_management_of_vme_ocb.pdf

An overall drawing of the Hardwired Oversight Logic, including
its oversight of the OCB/VME,  is shown in the following:

  24_hardwired_oversight_logic.pdf
```

Signals in the On-Card-Bus:

- OCB_D15:OCB_D00 16 Data Bus lines, bi-directional, 2.5V

- OCB_A23:OCB_A01 23 Address lines, always driven from the VME end, 2.5V

- OCB_DS_B Data_Strobe_B, always driven by VME end, 2.5V

- OCB_WRITE_B Write_B data bus Direction, always driven by the VME end, 2.5V

- OCB_SYS_RESET_B System_Reset_B, always driven by the VME end, 2.5V

- OCB_GEO_ADRS_6:OCB_GEO_ADRS_0 Geographic Address lines, always driven by the VME end, 2.5V, 0,4,5,6 come from the backplane, 1,2,3 come from jumpers on the CMX

- Note that only the VME/OCB management function in the BSPT_FPGA controls the DTACK_B signal to the VME backplane bus.

FPGA Connections to the On-Card-Bus:

- All FPGA connections to the On-Card-Bus are via 2.5 Volt I/O Banks on the BSPT, BF, and TP FPGAs.

- The BSPT, BF, and TP all connect to the On-Card_Bus so that their internal registers and/or memory structures will be "visible" on the VME backplane.

- Logically the BSPT makes a second separate connection to the On-Card_Bus to provide certain bus management functions. Inside the BSPT FPGA there are two separate sections related to the OCB: a section for normal VME register and/or memory access and a section for the VME/OCB bus management.

Bus Management:

The OCB is managed by a small set of logic in the Board Support FPGA. This OCB management consists of the following:

- The BSPT_FPGA recognizes when a VME cycle has been started for which this CMX card is the addressed target. The BSPT_FPGA knows its VME address range based on the Geographic Address of the crate and of the slot that this CMX card finds itself in.

A fixed delay after the start of a VME cycle targeting this CMX card the BSPT will assert the DTACK_B signal to the VME bus. The BSPT will then manage the "tear down" of this VME cycle, i.e. when the master releases the DS_B signal the BSPT bus management function will release this card's DTACK_B signal.

- The BSPT_FPGA manages both the Direction of and the Output Enable of the level translators and the data bus transceivers that connect the OCB Data Bus to the VME backplane.

  During a VME Read cycle that addresses this CMX card the data bus translators and transceivers drive data to the VME bus with their outputs enabled

  During a VME Write cycle that addresses this CMX card the data bus transceivers and translators drive data to the OCB with their outputs enabled

  When no cycle is taking place or when there is a cycle taking place that does not address this CMX card the data bus transceivers and translators are in the direction to send data to the OCB with their outputs disabled. Note that in this condition the keepers on the 2.5V to 3.3V translators will maintain valid CMOS logic levels both on the OCB data lines and on the transceiver pins.

- The VME Address lines are received from the backplane bus by 74LVC16373A chips. These parts include both a receiver and a transparent latch. If desired, the OCB management function in the BSPT_FPGA can use the Latch Enable signal to these chips to hold stable the state of the OCB Address lines during cycles on the VME bus.

- The CMX card includes Hardwired Oversight Logic to prevent a CMX card, under fault conditions, from hanging the the VME backplane bus and thus blocking VME communications with any card in that L1Calo crate.

  Specifically this Hardwired Oversight Logic verifies:
  - that the BSPT FPGA is configured,
  - that all CMX card power supplies are running,
  - and that the BSPT FPGA has asserted an OK signal

  before this hardwired logic will allow:
  - the CMX card's DTACK_B signal to be asserted onto the crate backplane or
  - the Data Bus Transceivers to drive data onto the crate backplane.

- NOTES:

  The BSPT_FPGA must be configured and running for any VME communications to take place with the CMX card.

The BSPT has two separate functions wrt the OCB:

It manages the VME/OCB as described above

It is a device on the OCB, i.e. it may have an address range on the OCB and thus have registers or memory that is visible from the backplane VME.

Because the DTACK_B signal is centrally managed, the OCB appears as a synchronous bus to all the registers and/or memories in the 3 FPGA devices that are connected to it. Reading from or writing to these registers and/or memories must take place within a fixed length of time.

Physical Layout of the OCB Traces on the CMX Card:

- If the OCB signals were all layout out on one layer in their natural order they would appear as vertical traces running down on the East side of the BSPT, BF, and TP FPGAs. In their natural order, on one layer, the signals going from West to East are:

  GA1:GA3, D00:D15, A23:A17, DS_B, Write_B, Reset_B, GA0, GA4:GA6, A16:A01

OCB to Backplane VME Connection Details:

- The OCB connects to the VME backplane bus via level translator chips followed by bus transceiver or receiver chips.

- The 2.5V logic level of the OCB is converted to the 3.3V level required by the bus transceiver and receivers using 74AVCAH164245 level translators. This is the same level translators that is used on other parts of the CMX card.

- The bus data transceiver chip is a 74LVT16245B. The bus receiver chips are 74LVC16373As.

- The DTACK_B line is driven by two sections of a 74LVC38A open drain chip.

Details of the Anticipated OCB/VME Management Firmware:

- As on the CMM card, the registers and memories on the CMX are expected to access and provide read cycle data or absorb write cycle data within a fixed amount of time after the VME Master asserts DS_B.

I.E. the asynchronous nature of a real VME Bus is dispensed with on the OCB.

- The VME/OCB management provided by the BSPT will "sync up" the OCB to its 40.08 MHz clock. In this way the registers and memories in the 3 FPGAs that are connected to the OCB do not have to individually worry about OCB cycles at random phases in their clock.

- The OCB cycle starts when the BSPT OCB management firmware detects and confirms that the DS_B signal has gone to its low asserted state and sees that the address lines OCB_A(23:1) indicate an address within the range of this CMX card.

- The VME/OCB management provided by the BSPT detects whether or not a given VME cycle is targeting its CMX card. It generates an internal "this_cycle_is_for_me" signal that is used to enable various control functions.

  The inputs to the decoder that generates the "this_cycle_is_for_me" signal include the 23 OCB Address lines and the 7 Geographic Address lines. 4 of the Geo Adrs signals come from the backplane and the other 3 are set by jumpers on the CMX card.

  The output of the decoder logic that generates the "this_cycle_is_for_me" signal should passed through a D flip-flop that is clocked only after the OCB Address lines are stable and the decoder has had time to settle. The intent of this precaution is to eliminate the chance that natural skew in the decoder or in its inputs will falsely trigger a CMX card into responding to a cycle that does not target it.

  The internal "this_cycle_is_for_me" signal must be terminated as soon as OCB_DS_B returns HI or anytime that the OCB_SYS_RESET_B signal is asserted.

- The internal "this_cycle_is_for_me" signal is used to control the the Enabling of the VME/OCB Data Bus transceiver and level translator. Note that the enable signal from the BSPT to the Data Bus transceivers is protected by Hardwired Oversight Logic.

  CMX has the normal standard requirement of holding valid CMOS signal levels on its OCB Data Bus between VME cycles that target it. This is taken care of by the level "keepers" that are built into the 74AVCAH164245 level translator chips. This simplifies the logic that controls the Direction and Enable signals to these translators.

- The internal "this_cycle_is_for_me" signal along with the OCB_WRITE_B signal are used to control the the Direction of the VME/OCB Data Bus transceiver and level translator.

- The internal "this_cycle_is_for_me" signal along with the OCB_DS_B signal are used to control the DTACK_B signal that is generated by the CMX card.

  CMX asserts DTACK_B a fixed number of 40.08 MHz clock cycles after the bus management logic has detected (and confirmed) the falling edge of OCB_DS_B for a VME cycle that is targeting this card.

  CMX releases DTACK_B as soon as OCB_DS_B returns HI or anytime that the OCB_SYS_RESET_B signal is asserted.

  Note that the CMX card includes Hardwired Oversight Logic to control when it is allowed to assert its DTACK_B signal.

- The VME Reset_B signal, when asserted, should immediately stop all VME/OCB bus activity on a CMX card. When Reset_B is asserted it must clear the internal "this_cycle_is_for_me" signal (thus getting the CMX card off of the VME Data Bus and it must stop asserting DTACK_B if it is doing so.

- Note that the CMX card includes Hardwired Oversight Logic to prevent it from "hanging" the VME backplane bus in a L1Calo crate in the event that there is a failure in an on-board power supply or in the event that the BSPT FPGA looses its configuration (or has not yet been configured).

  This Hardwired Oversight Logic prevents a CMX card from asserting its DTACK_B signal and from sending data onto the VME Bus until: all power supplies on the CMX card are running normally, the BSPT Configuration Done signal is asserted, the BSPT has asserted its "Running OK" signal and jumper JMP59 has been installed on the card.

  This Hardwired Oversight Logic is shown in circuit diagram 24_hardwired_oversight_logic.pdf In the lower left-hand corner you can see the protection on the CMX DTACK_B signal. Near the bottom of the right-hand column you can see the protection on enabling the VME Data Bus Drivers.

- The receivers on the CMX card for the VME Address, DS_B, Write_B, and Reset_B signals are 74LVC16373 chips with transparent latches. When the "Latch Enable" signal to these chips is HI then their outputs will follow their inputs. When LE is LOW then their outputs "hold".

  Note that there are separate Latch Enable signals to the sections of the 74LVC16373 chips that carry the VME Address lines and to the section that carries the VME Control signals, e.g. DS_B, Write_B, and Reset_B. You can see the separate VME_ADRS_RECVR_LE and VME_CTRL_RECVR_LE signals in circuit diagram 20_vme_ocb_management.pdf

Clearly the 74LVC16373 receivers for these VME Control signals must always be transparent. The BSPT generates the Latch Enable signals to all sections of the 74LVC16373 receivers but except for some kind of special testing it is assumed that the Latch Enable to the section of 74LVC16373 receivers for the VME Control signals will just be tied HI in the BSPT (HI --> transparent).

List of Control Signals from the Bus Management Function in the BSPT FPGA to the Transceivers, Receivers, Drivers, and Translators that Connect the OCB to the VME Bus:

All signals that are described in the following table are fully defined in the following net list files:

bspt_fpga_all_other_nets_n2p.txt
vme_bus_interface_chips_n2p.txt
hardwired_oversight_logic_n2p.txt

In the following table the signals are listed in the same order as they appear in circuit diagram 20_vme_ocb_management.pdf

- BSPT_RUNNING_OK_B

  This signal allows the BSPT to tell the Hardwired Oversight Logic that, from its point of view, everything is OK. This is a Low Active signal. BSPT should confirm that the Virtex FPGA(s) are Configured before setting this signal Low.

- BSPT_SEND_VME_DTACK_B

  Controls sending the VME DTACK_B signal from the CMX card. This control signal passes through Hardwired Oversight Logic on its way to the DTACK_B VME driver chip. This signal should be taken LOW to request that the CMX card assert its DTACK_B VME signal.

- VME_D_BUS_TRNCVR_DIR

  Controls the Direction of the VME Data Bus Transceiver U352. This control signal runs directly to the U352 VME Transceiver. Once the CMX is ready for VME access then this signal should be taken LOW for VME Writes and must go HI for VME Reads. This signal MUST always be in the same state as the OCB_D_BUS_TRNSLT_DIR signal.

- BSPT_VME_D_BUS_TRNCVR_OE_B

  Controls the Output_Enable_B of the VME Data Bus Transceiver U352. This is a control signal that passes through Hardwired Oversight Logic on its way to the U352 VME Data Bus Transceiver. Once the CMX is ready for VME access then this signal should be taken LOW when this card is the target of a VME Read or Write cycle.

- OCB_D_BUS_TRNSLT_DIR

  Controls the Direction of the OCB Data Bus Translator U355. This is a control signal that runs directly to the U355 OCB Data Bus Translator. Once the CMX is ready for VME access then this signal should be taken LOW for VME Writes and must go HI for VME Reads. This signal MUST always be in the same state as the VME_D_BUS_TRNCVR_DIR signal.

- OCB_D_BUS_TRNSLT_OE_B

  Controls the Output_Enable_B of the OCB Data Bus Translator U355. This is a control signal that runs directly to the U355 OCB Data Bus Translator. Once the CMX is ready for VME access then this signal should be taken LOW when this card is the target of a VME Read or Write cycle.

- VME_ADRS_RECVR_LE

  Controls the LE signal to the U354 VME Receiver and to the half of the U353 VME Receiver that is used for "Address type" information. This is a control signal that runs directly to U354 and to the Address section of the U353 Receiver. Once the CMX is ready for VME access then between VME cycles this LE signal should remain HI to keep these receivers transparent. During a VME cycle this LE signal may go LOW so that these VME Receivers will "Hold" their address information during the cycle.

- VME_ADRS_AND_CTRL_RECVR_OE_B

  Controls the OE_B signal to all sections of both the U353 and U354 Receivers for the VME Address and Control type signals. This is a control signal that runs directly to the U353 and U354 chips. Once the CMX is ready for VME access then this signal should be taken LOW and stay continuously LOW to enable the output of these VME Receiver chips.

- OCB_ADRS_AND_CTRL_TRNSLT_DIR

  Controls the DIR signal to all sections of both the U356 and the U357 Translators for the OCB Address and Control type signals. This is a control that runs directly to the U356 and U357 chips. Once the CMX is ready for VME access then this signal should be taken LOW and stay continuously LOW to select the B input to A output direction for these translator chips.

- BSPT_OCB_ADRS_AND_CTRL_TRNSLT_OE_B

  Controls the OE_B signal to all sections of both the U356 and the U357 Translators for the OCB Address and Control type signals. This is a control signal that passes through Hardwired Oversight Logic before it goes to U356 and U357. Once the CMX is ready for VME access then this signal should be taken LOW and stay continuously LOW to enable these translator chip outputs.

- VME_CTRL_RECVR_LE

  Controls the LE signal to the half of the U353 VME Receiver that handles "Control type" information. This is a control signal that runs directly to this one section of the U353 VME Receiver. Once the CMX is ready for VME access then this LE signal must continuously be held HI to keep this VME Receiver's latch transparent.

Special note about the VME_ADRS_RECVR_LE, VME_CTRL_RECVR_LE and VME_ADRS_AND_CTRL_RECVR_OE_B control signals:

Because I made a mistake in the orientation of the VME Receiver chips U353 and U354 during layout the control signals listed in the heading of this section are not wired to the correct pins on these chips. This mistake has the following implications:

- The VME_ADRS_RECVR_LE control signal from the BSPT is actually tied to the OE_B pins on U354 and to the OE_B pin on the address half of U353.

  The VME_CTRL_RECVR_LE control signal from the BSPT is actually tied to the OE_B pin on the control half of U353.

  The VME_ADRS_AND_CTRL_RECVR_OE_B control signal from the BSPT is actually tied to all of the LE pins on U353 and U354.

- One can not use the VME_ADRS_RECVR_LE signal to freeze the 24 lines of the OCB Address Bus during a VME cycle. If one wants to design the VME firmware for the CMX card so that the OCB Address Bus is frozen during a VME cycle this can still be done at the I/O Blocks that receive these lines on the FPGAs. Freezing the address bus is only necessary if one wants to pipe-line the VME cycles.

- These 3 control signals are generated in the VME Management section of the BSPT firmware. In this BSPT firmware one must set these 3 control signals as follows:

VME_ADRS_RECVR_LE	permanently set LOW
VME_CTRL_RECVR_LE	permanently set LOW
VME_ADRS_AND_CTRL_RECVR_OE_B	permanently set HI

Appendix J: JTAG Chains and FPGA Configuration

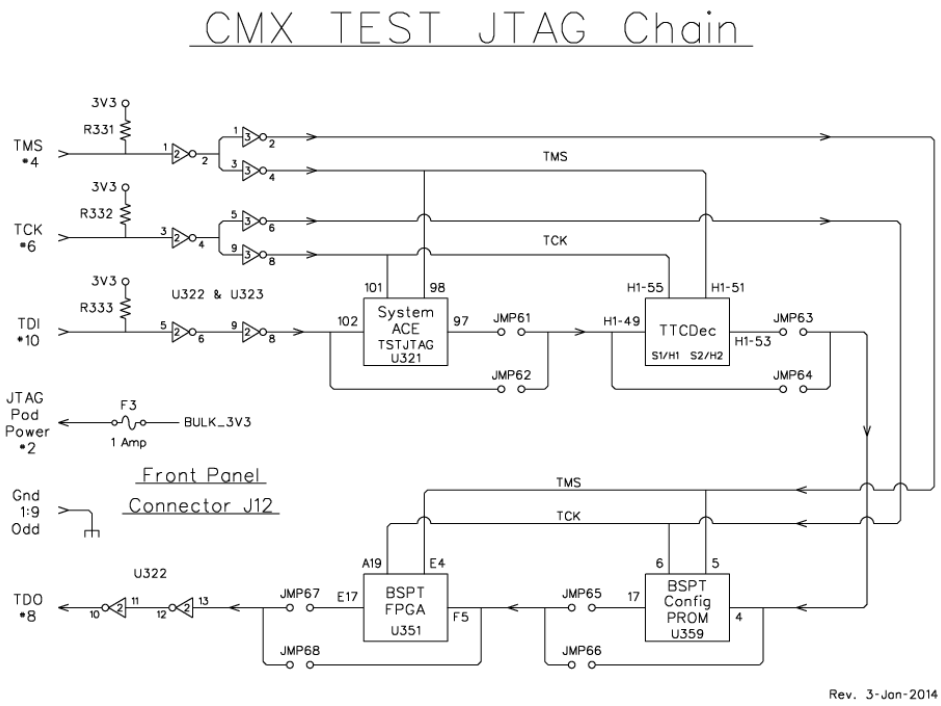


Figure 41: Circuit Diagram for Test JTAG Chain

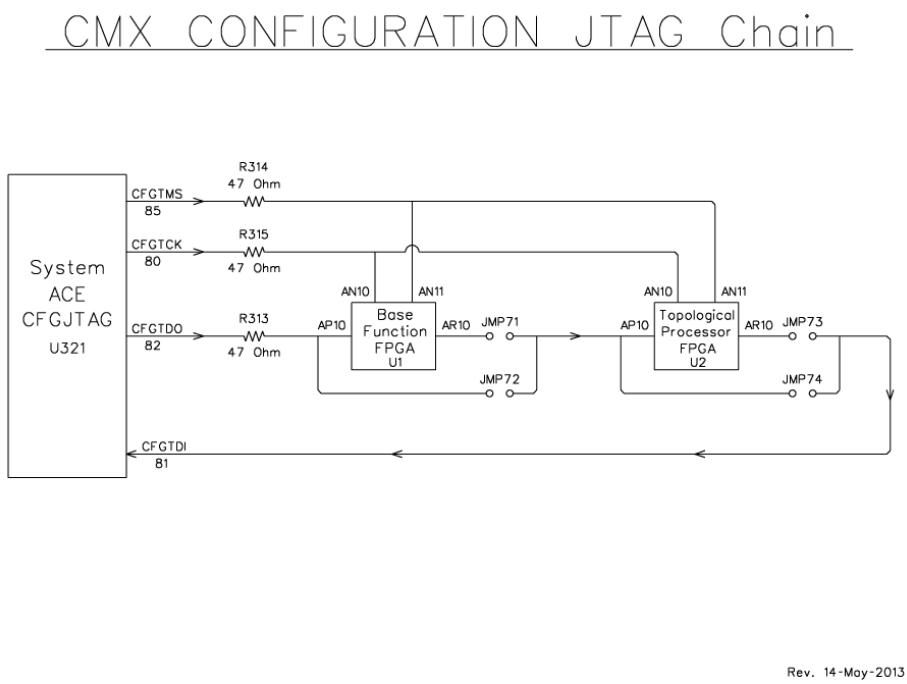


Figure 42: Circuit Diagram for the Virtex-6 FPGAs configuration JTAG Chain

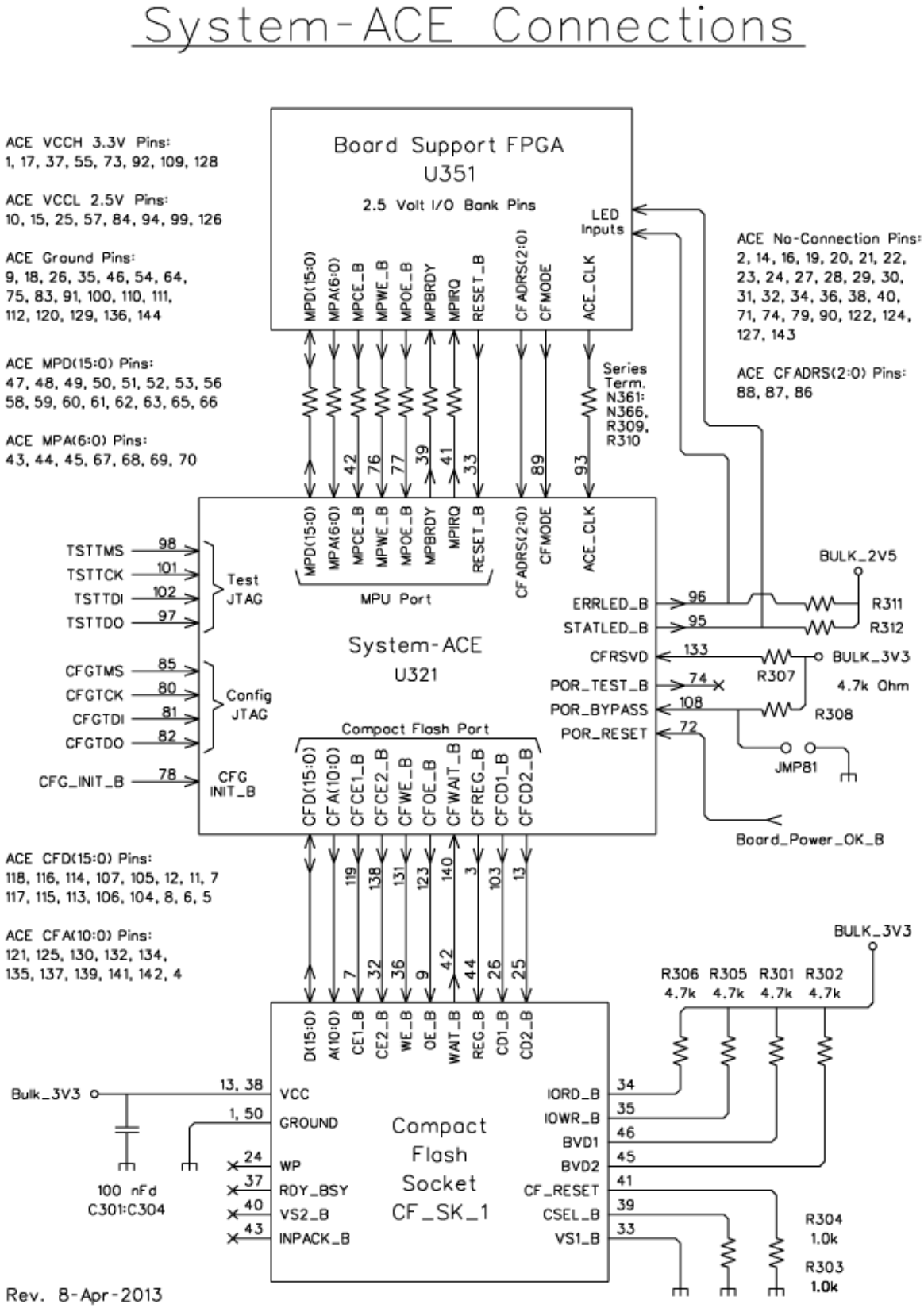


Figure 43: Circuit Diagram for System ACE

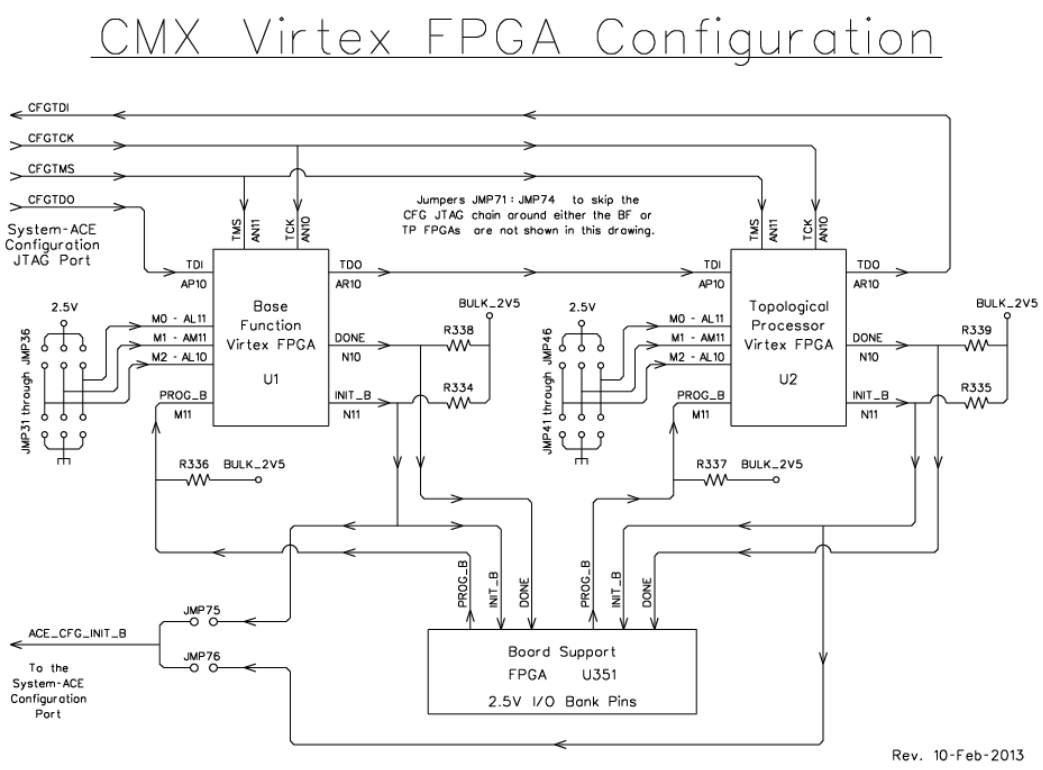


Figure 44: Circuit Diagram for Virtex-6 Configuration

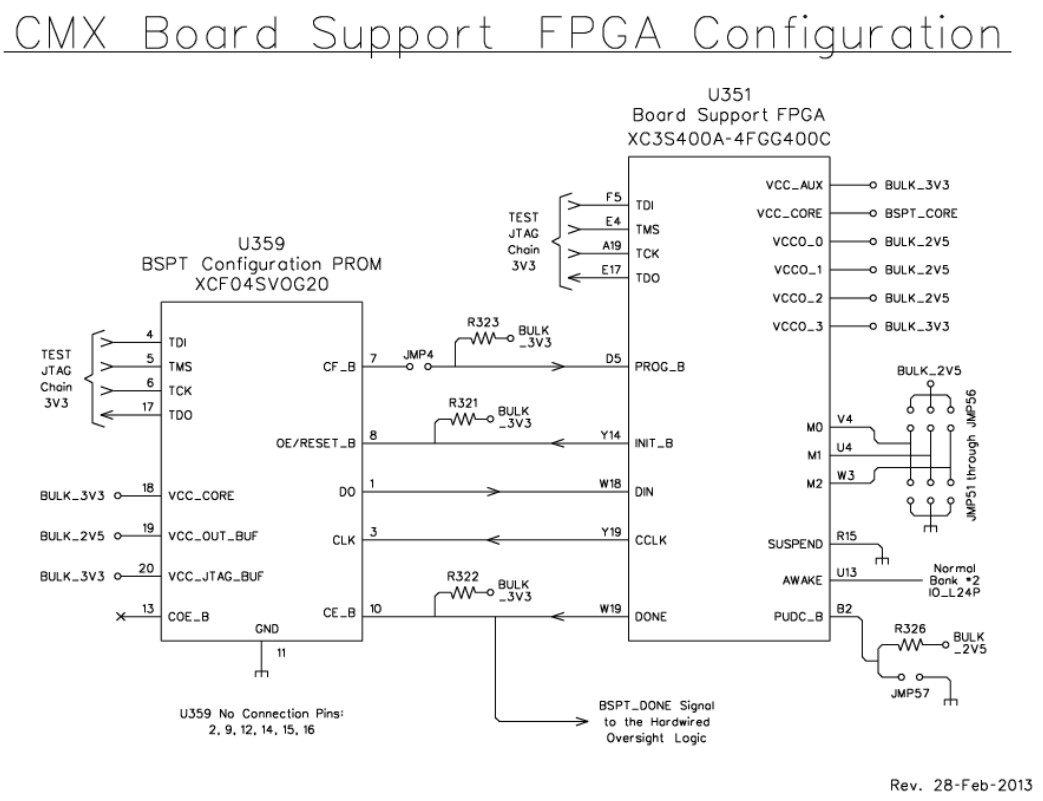


Figure 45: Circuit Diagram for Board Support FPGA Configuration

A current snapshot of the circuit diagrams is included above while the source material is in

- 01_jtag_chain_test.pdf
- 02_jtag_chain_configuration.pdf
- 15_system_ace.pdf
- 17_virtex_fpga_configuration.pdf
- 19_bspt_fpga_configuration.pdf

found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot of the detailed description is included below while the source material is in cmx_ab_jtag_and_config.txt found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
                CMX  JTAG and FPGA Configuration
               ---------------------------------


                                          Current Rev. 25-Apr-2014


This file describes the two JTAG chains on the CMX card and
the configuration of the FPGAs on the CMX card.


JTAG Chains:
------------

The arrangement of the two JTAG chains on the CMX card is
driven by the requirement of using a Xilinx System-ACE chip.
Using System-ACE terminology, the CMX card has a "Test" JTAG
chain and a "Configuration" JTAG chain.


Test JTAG Chain:
----------------

  The "Test" JTAG chain can be accessed from the front panel
  J12 connector.  The following circuit diagram shows the
  layout of the Test JTAG chain:

     01_jtag_chain_test.pdf


  The Test JTAG chain uses 3.3V JTAG signals.  The data path
  in this chain is:  J12 input, the System-ACE TSTJTAG port,
  the TTCDec mezzanine, the Configuration PROM for the BSPT
  FPGA, the BSPT FPGA itself, and finally back to J12 for
  JTAG data output.  There are jumpers in this chain to skip
  around any of these devices.  The jumpers are normally set
  to skip around the TTCDec mezzanine card.
```

At the front panel J12 connector, resistors R331, R332, and R333 provide 4.7k Ohm pull-up on the TMS, TCK, and TDI JTAG signals. Right next to the J12 connector all 4 Test JTAG signals are buffered by U322 and U323 which are 74LVC04A inverters. These inverters buffer the CMX Test JTAG components from signal quality and logic level problems at the J12 connector. The U322 and U323 buffers provide separate TMS and TCK runs to the: System-ACE and TTCDec and to the BSPT Config PROM and BSPT FPGA.

The Test JTAG pins on the CMX J12 connection are:

All odd pins, 1 through 9, are Ground

pin #2 Fused BULK_3V3 reference to the JTAG pod

pin #4 TMS with a 4.7k Ohm pull-up on the CMX

pin #6 TCK with a 4.7k Ohm pull-up on the CMX

pin #8 TDO Test Data from CMX to the JTAG Pod

pin #10 TDI with a 4.7k Ohm pull-up on the CMX This is JTAG data from the Pod to the CMX.

Note that these pin numbers match with the pins that are used for the same signals on the Xilinx model HW-USB-II-G USB JTAG Pod.

The Xilinx JTAG Pod signals: pin #12 --, pin #13 PGND, and pin #14 HALT are not used by the CMX card.

The adaptor cable that is used to connect the Xilinx HW-USB-II-G USB JTAG Pod to the CMX front panel J12 connector connects only pins 1 through 10 between these two devices. The details of this adaptor cable from the JTAG Pod to the CMX J12 connector are show in the drawing:

34_front_panel_j12_connector_and_cables.pdf

Note that the upper 6 pins on the CMX J12 connector (pins 11 through 16) are used for other, non-JTAG, functions on the CMX circuit board.

Configuration JTAG Chain:

The "Configuration" JTAG chain includes only the "CFGJTAG" port on the System-ACE and the JTAG ports on the two Virtex FPGAs on the CMX card. The data on the Configuration JTAG chain flows from the System-ACE, through the Base Function FPGA U1, then through the Topological Processor FPGA U2,

and finally back to the System-ACE. Jumpers are provided to skip this JTAG chain around either U1 or U2. Most CMX cards will not have the Topological FPGA U2 installed and thus will need to use these skip jumpers to bypass U2.

The Configuration JTAG chain uses 2.5V logic levels. 47 Ohm resistors R313, R314, and R315 are located near the System-ACE and provide back termination on the Configuration JTAG TMS, TCK, and TDO signals.

The System-ACE allows the Configuration JTAG chain to be used either for external access to the BF and/or TP FPGAs from the front panel Test JTAG chain or to configure these FPGAs from data stored in the Compact Flash module that is attached to the System-ACE.

The CMX card's Configuration JTAG chain is shown in the drawing:

02_jtag_chain_configuration.pdf

FPGA Configuration:

The CMX card handles the configuration of the Spartan 3A Board Support FPGA in a separate different way from how it handles the configuration of the two Virtex FPGAs, i.e. the Base Function and Topological Processor FPGAs.

- BSPT FPGA Configuration:

The intent is that the BSPT FPGA will be quickly and automatically configured and ready for use whenever the power is turned ON to the CMX. The intent is that the BSPT FPGA on the CMX card will be used in a way that is similar to the use of the CoolRunner CPLDs on the CMM card, i.e. their logic is always available. The configuration of the BSPT FPGA is shown in the drawing:

19_bspt_fpga_configuration.pdf

The BSPT FPGA is automatically configured from a Xilinx XCF04S "Platform Flash" PROM whenever the power is turned ON to the CMX card. Configuration of the BSPT begins once the following 3 power supplies to the BSPT FPGA have stabilized above the required threshold values: VccINT, VccAUX, and VccO_2. Note that these 3 BSPT FPGA supplies come from the CMX BULK_2V5 and BULK_3V3 rails. By design the BULK_2V5 rail will reach its default output value before the BULK_3V3 rail has finished ramping up.

The Master Serial mode configuration of the BSPT FPGA then takes about one second. Once the BSPT is configured then VME-- access to the registers in the BSPT is available.

Before the BSPT is configured there is Hardwired Oversight Logic on the CMX to prevent it from hanging the VME-- bus and thus interfering with VME-- communication to other cards in the crate.

Both the BSPT FPGA itself and the XCF04S "Platform Flash" Configuration PROM appear as devices on the Test JTAG chain. Thus from the front panel new firmware can be loaded into the XCF04S Configuration PROM without removing the CMX card from the crate.

During BSPT FPGA development the Jumper J4 may be installed which will allow a JTAG command to the XCF04S "Platform Flash" Configuration PROM to cause the BSPT FPGA to start a new configuration cycle. That is with J4 installed you do not need to power cycle the CMX card to load new firmware into the BSPT FPGA.

The intent is that the BSPT firmware will be stable and not need to evolve in the same way that the Base Function or Topological Processor firmware may need to develop over time. The BSPT firmware should have the same place in the operation of the CMX card as the firmware for the CoolRunner CPLDs does in the operation of the CMM card.

- Base Function and Topological Processor FPGA Configuration:

The two Virtex FPGAs on the CMX card are configured via their JTAG connection to the CFGJTAG port of the System-ACE chip. Our intent in the CMX design is to implement the standard setup for the configuration of these Virtex FPGAs as is used for FPGA configuration on earlier L1Calo cards. The configuration of the Virtex FPGAs on the CMX card is shown in the following drawings:

15_system_ace.pdf
17_virtex_fpga_configuration.pdf

The System-ACE is controlled via its MPU port. All signals in the System-ACE's MPU port are routed to pins in a 2.5V I/O bank of the BSPT FPGA. Logic and VME-- visible registers in the BSPT allow control of the System-ACE from the VME-- bus. The 20 MHz clock to the System-ACE comes from the BSPT FPGA so that MPU port operations can be synchronized in the required way. The BSPT FPGA also controls the signals to the System-ACE CFGMODE and CFGADRS(2:0) pins.

The BSPT FPGA also has access to 3 pins on each of the Virtex FPGAs that control the configuration of these parts, i.e. their PROG_B, INIT_B, and DONE pins. By monitoring these Virtex FPGA pins the BSPT can monitor the progress of configuring these parts. The 3 "M" pins to each Virtex FPGAs are controlled

by jumpers on the CMX card. These jumpers will normally be set for M2, M1, M0 = 101 to specify that JTAG configuration will be used.

The INIT_B pins on the two Virtex FPGAs are routed to the System-ACE CFGINIT_B pin via Jumper JMP75 and JMP76. This signal prevents the System-ACE from starting the configuration process before the Virtex parts are ready to absorb it. Jumpers JMP75 and JMP76 on the CMX card control which of the Virtex INIT_B pins is connected to the System-ACE.

The two LED pins on the System-ACE (ERRLED_B and STATLED_B) are also routed to the BSPT. From there this information can be read in a VME-- visible register and/or can be used to control front panel LEDs if that is desired.

The POR_RESET pin on the System-ACE is released once the CMX card's BOARD_POWER_OK_B signal goes low which indicates that all DC supplies on the CMX are stable. The state of the System-ACE's POR_BYPASS pin is controlled by jumper JMP81.

Appendix K: CAN Bus

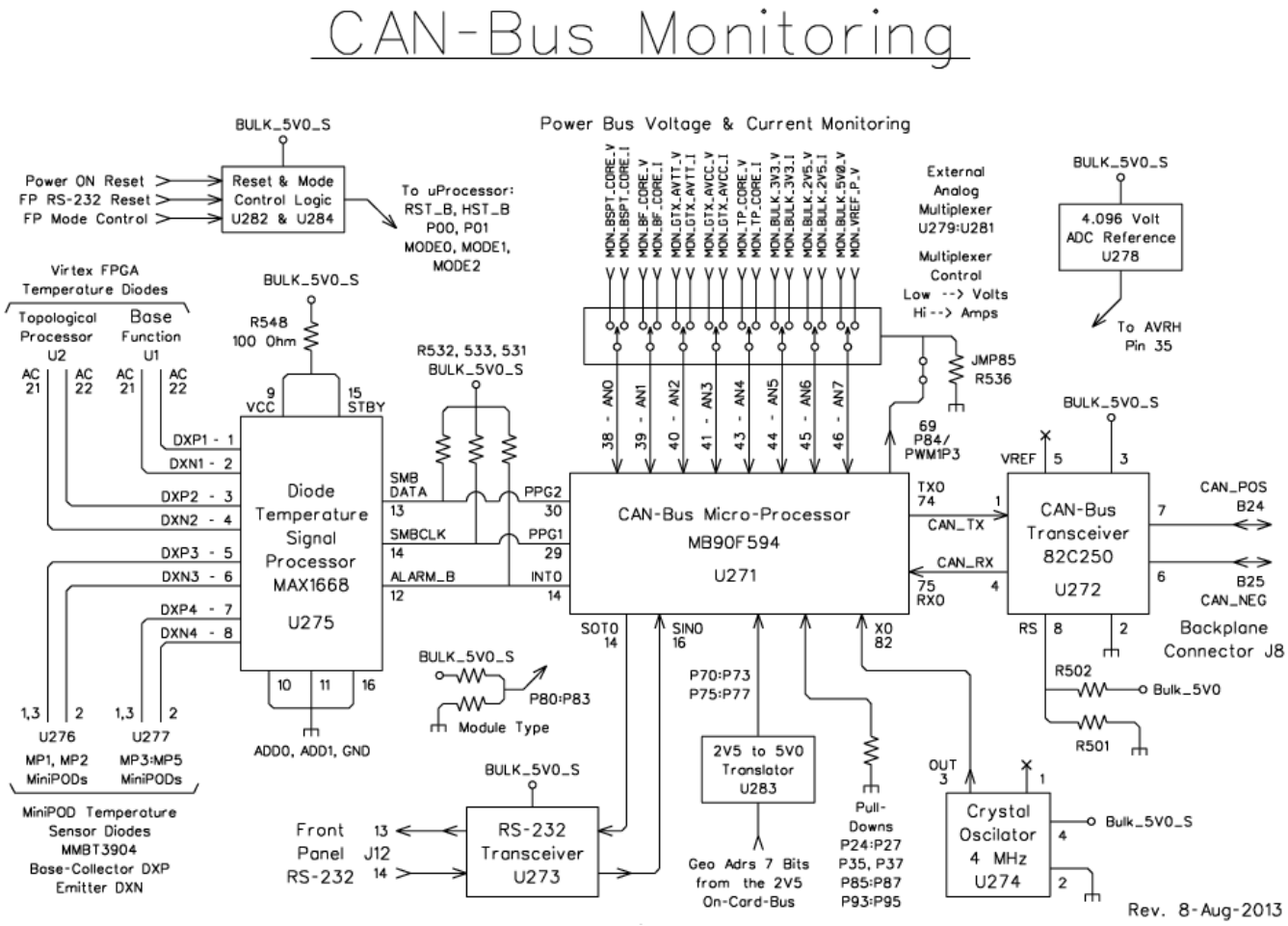


Figure 46: Overall Diagram for CAN Bus monitoring

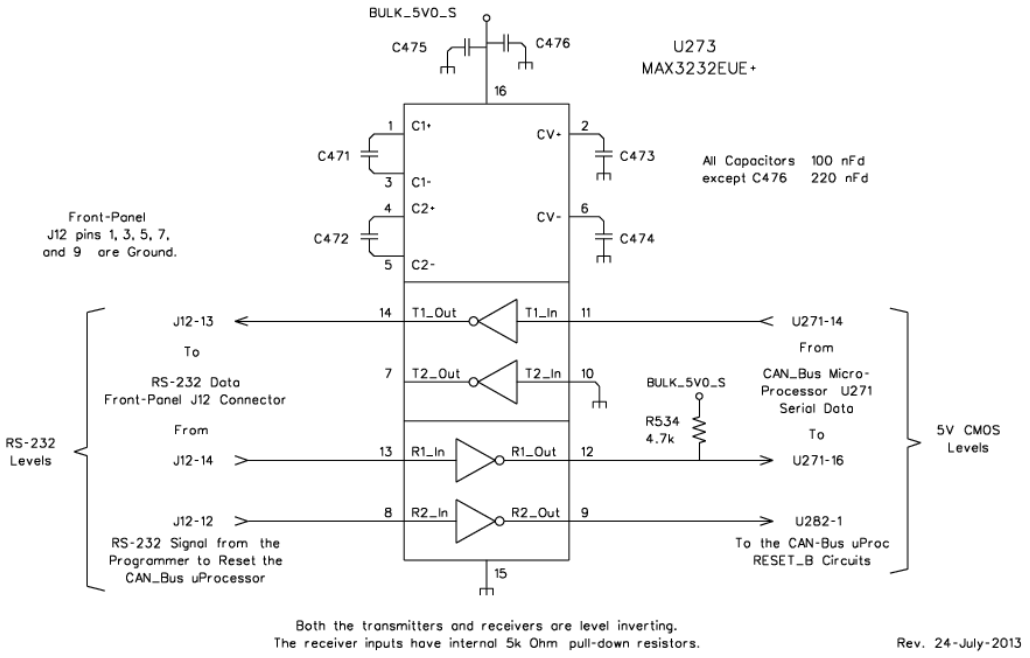


Figure 47: Circuit Diagram for RS-232 Interface to CAN Bus uProcessor

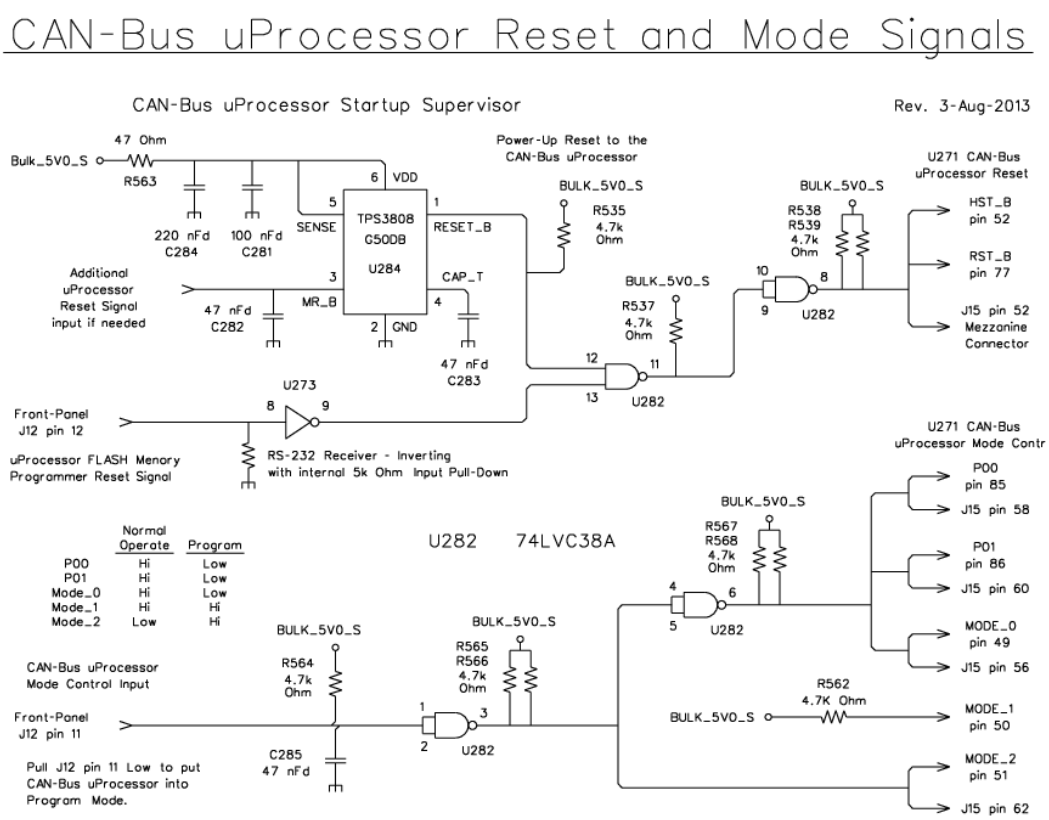


Figure 48: Circuit Diagram for CAN Bus uProcessor Reset and Mode Signals

A current snapshot of the circuit diagrams is included above while the source material is in

- 16_can_bus_monitoring.pdf
- 31_rs_232_to_can_bus_controller.pdf
- 33_can_uprocessor_reset_and_mode_ctrl.pdf

found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot of the detailed description is included below while the source material is in cmx_ab_can_bus_monitoring.txt found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
                  CMX  CAN-Bus Monitoring
                ---------------------------


                                          Original Rev.  12-Feb-2013
                                           Current Rev.  24-Apr-2014


This file describes the CAN-Bus Monitoring system on the CMX
circuit board.

An overall view of the CMX CAN-Bus Monitoring system is shown
in the following drawing in the circuit diagrams section of
the MSU CMX web site:

   16_can_bus_monitoring.pdf


The RS-232 connection to the CAN-Bus Microprocessor, the
Reset and Mode signals to this Microprocessor, and the
Analog Multiplexer inputs to its ADC are all shown in detail
in the following drawings:

   31_rs_232_to_can_bus_controller.pdf
   33_can_uprocessor_reset_and_mode_ctrl.pdf
   35_voltage_and_current_monitor_analog.pdf


The CMX CAN-Bus Monitoring system provides measurements of
9 voltages, 7 currents, and 4 temperatures on the CMX card.
Details about the items that are available for monitoring
via this CAN-Bus system are given later in this file.
```

The following components are used to implement the CAN-Bus Monitoring system on the CMX circuit board:

Fujitsu	MB90F594	CAN-Bus Microprocessor "A" version
NXP	82C250	CAN-Bus Interface
Maxim	MAX1668	Diode Temperature Sensor Processor
Fairchild	MMBT3904	Diode Temperature Sensors
Maxim	MAX3232	RS-232 Interface
NXP	74HC4053	Analog Multiplexer "External"
TI	TPS3808	Power Supply Supervisor uProc Reset
TI B-B	REF3140	4.096V Reference for uProc ADC
TI	TXB0108	Level Translator 5V Geo Adrs for uProc
NXP	74LVC38A	Logic for Mode signal to uProc
4 MHz Crystal Oscillator for the Microprocessor		

The Fujitsu MB90F594 CAN-Bus Microprocessor is a 5 Volt part. The other circuits that work with this microprocessor must also use 5 Volt logic signals. The 5 Volt power supply for this section of the CMX card is provided through a 3 Amp SMD mount fuse. This 5 Volt power is distributed on a separate fill under this section of the CMX circuit board.

The MB90F594 CAN-Bus Microprocessor is provided with a 4 MHz clock from a separate 5 Volt crystal oscillator.

The general design of the Fujitsu MB90F594 CAN-Bus Microprocessor section of the CMX circuit board is based only on studying the following: CMM schematics, CAM CAN schematics, PPM CAN Mezzanine schematics, MB90F594 data sheet and users guide. I found no overall reference document about hardware design requirements for the L1Calo CAN-Bus Monitoring.

Isolation form other Sections of the CMX Card:

The CAN-Bus Monitoring system on the CMX card is separate from other sections of the CMX card. There is no coupling between the FPGAs on the CMX and its CAN-Bus Monitoring System. There are no VME visible registers to allow "spying" on the CAN-Bus monitoring data or to provide control (e.g. interrupts) of the CAN-Bus Microprocessor. The intent is that failure of FPGAs to configure or "hangs" in the logic in other parts of the CMX card will not prevent the CAN-Bus Monitoring system from working.

The CAN-Bus Microprocessor does receive the full 7 bit Geographic Address of the CMX card that it is on. The Geographic Address is received from U283 which is a 2.5V to 5V level translator.

RS-232 Connection to the CAN-Bus Microprocessor:

The CMX card provides a front panel RS-232 connection to the CAN-Bus Microprocessor via its J12 connector which is located near the bottom of the front panel. The J12 connector also provides other functions to the CMX card so its pin out is not standard RS-232. A drawing showing the details of the J12 connector and the required cable for RS-232 connection to the CAN-Bus Microprocessor is shown in the following:

34_front_panel_j12_connector_and_cables.pdf

The direction of the RS-232 signals, their J12 connector pins, and their CAN-Bus Microprocessor pins that handle these signals is shown in the following table:

RS-232 Data Direction	J12 Pin Number	Microprocessor Pin	Signal
Arrives to CMX	14	16	P36/SIN0
Sent from CMX	13	14	P34/SOT0

Mode Control of the CAN-Bus Microprocessor:

The Fujitsu MB90F594 CAN-Bus Microprocessor has separate "Modes" that provide either normal operation or allow programming of its internal Flash Memory. It is convenient if the Mode of this microprocessor can be controlled from the front panel. In that way the CMX card does not need to be removed from a slot in a full crate just to program its CAN-Bus Microprocessor's Flash Memory.

On the CMX card control of its CAN-Bus Microprocessor's Mode is provided by a pin in the J12 connector near the bottom of the front panel. This pin is a 5 Volt logic level input to the CMX card. It is normally pulled HI by a pull-up resistor to +5V on the CMX card. This provides for normal operation of the CAN-Bus Microprocessor. The front panel J12 Mode pin needs to be grounded to put the CAN-Bus Microprocessor into the mode that allows programming its Flash Memory.

The following 2 tables show the signal levels for both normal operation and Flash Memory Programming of the CAN-Bus Microprocessor:

Front Panel J12 Pin Number 11	Can-Bus uProcessor Mode
Open --> Hi by Internal Pull-Up	Normal Operation
Tied Low	Program Flash Mem

Microprocessor Pin	Signal	Mode: Normal Operate	Mode: Program Flash Mem
85	P00/IN0	HI	Low
86	P01/IN1	HI	Low
49	MD0	HI	Low
50	MD1	HI	Hi
51	MD2	Low	Hi

The details of the CAN-Bus Microprocessor Mode control are show in the Front Panel J12 and the Reset/Mode Signal drawings that were mentioned above.

Reset of the CAN-Bus Microprocessor:

There are 2 conditions on the CMX card that will cause a Reset of the CAN-Bus Microprocessor:

- Failure of the +5V power to the CAN-Bus Monitoring section of the CMX card
- A front panel signal received on connector J12 pin 12

During normal cold power up of the CMX card the Reset signal to the CAN-Bus Microprocessor is released about 1 second after the +5V power supply has reached a normal operating level. This function is provided by a TI TPS3808 power supply supervisor circuit.

The Fujitsu MB90F594 CAN-Bus Microprocessor also needs to be Reset during the sequence of operations that loads new information into its Flash Memory. This Reset signal comes from the Microprocessor Flash Memory Programmer as an RS-232 level signal. This Reset signal is received on the front panel J12 (along with the other RS-232 signals from the programmer) converted to 5V logic level and ORed with the power up Reset signal. The details of this are show in the Front Panel J12 and the Reset/Mode Signal drawings that were mentioned above.

Independent of its source, front panel or power up, the active Low Reset signal that is send to the CAN-Bus Microprocessor is delivered to its: pin number 52 HST_B and to its pin number 77 RST_B.

Static Inputs to the CAN-Bus Microprocessor:

There are a number of static logic level inputs to the CAN-Bus Microprocessor. Some of these are used to pass Card ID type information to the microprocessor. In addition, all pins of the microprocessor need to be at valid 5V logic levels (note that some pins on the Fujitsu MB90F594 appear to have special voltage level requirements. Some unused pins are (must be) defaulted to a valid logic level by programming them to be an Output from the microprocessor. Other used or unused pins are tied to valid logic level signals with pull-up or pull-down resistors.

The following table shows the the microprocessor pins/signal that are used to receive static ID type information form the CMX card:

Microprocessor Pin	Signal	Input Signal
54	P70/PWM1P0	Geo_Adrs_0
55	P71/PWM1M0	Geo_Adrs_1
56	P72/PWM2P0	Geo_Adrs_2
57	P73/PWM2M0	Geo_Adrs_3
60	P75/PWM1M1	Geo_Adrs_4
61	P76/PWM2P1	Geo_Adrs_5
62	P77/PWM2M1	Geo_Adrs_6
64	P80/PWM1P2	Module Type Bit Low
65	P81/PWM1M2	Module Type Bit Low
66	P82/PWM2P2	Module Type Bit Hi
67	P83/PWM2M2	Module Type Bit Low

The following table shows the the microprocessor pins/signal that are tied to static levels via jumper resistors because that's how they were handled on other L1Calo cards:

Microprocessor Pin	Signal	Input Signal
5	P24/INT4	jumper R561 tie Low
6	P25/INT5	jumper R560 tie Low
7	P26/INT6	jumper R559 tie Low
8	P27/INT7	jumper R558 tie Low
15	P35/SCK0	jumper R557 tie Low
17	P37/SIN1	jumper R556 tie Low
59	P74/PWM1P1	jumper R542 tie Hi
70	P85/PWM1M3	jumper R550 tie Low

71	P86/PWM2P3	jumper R551 tie Low
72	P87/PWM2M3	jumper R552 tie Low
78	P93/INT1	jumper R553 tie Low
79	P94/INT2	jumper R554 tie Low
80	P95/INT3	jumper R555 tie Low

Temperature Measurement:

The temperatures at 4 locations on the CMX can be monitored via the CAN-Bus system. These 4 locations are: Base Function FPGA silicon temperature, Topological Processor FPGA silicon temperature, air flow temperature above the 2 Transmitting MiniPODs MP1 and MP2, and the air flow temperature above the 3 Receiving MiniPODs MP3, MP4, MP5.

These temperatures are measured by the forward voltage drop across a diode junctions. The required temperature measuring diodes are built into the Virtex FPGAs. The base-emitter drop in MMBT3904 transistors is used to measure the temperature above the MiniPOD devices. A Maxim MAX1668 Diode Temperature Sensor Processor is used to convert these diode forward voltage drops into a temperature measurements.

The following table shows which MAX1668 channel is used to measure the temperature at a given location.

MAX1668 Channel	Location of the Temperature Sensor
DX1	BF Virtex FPGA Silicon Temperature
DX2	TP Virtex FPGA Silicon Temperature
DX3	MMBT3904 at the "hot end" of MiniPODs MP1, MP2
DX4	MMBT3904 at the "hot end" of MiniPODs MP3:MP5

The MAX1668 Diode Temperature Sensor Processor communicates with the CAN-Bus Microprocessor via a 2-wire serial bus. In this setup: pin number 30 P52/PPG2 provides the Data connection to the CAN-Bus Microprocessor and pin number 29 P51/PPG1 provides the Clock connection. An Alarm signal from the MAX1668 is routed to pin number 14 p92/INT0 on the CAN-Bus Microprocessor.

Voltage and Current Measurement:

A total of 16 analog signals need to be measured by the ADC in the CAN-Bus Microprocessor. Multiplexing these 16 analog signals into the one ADC is accomplished in 2 stages:

- An "External" 8 wide 2 to 1 analog multiplexer is used to select which 8 of the 16 available signals will be sent to the CAN-Bus Microprocessor at a given point in time. This function uses 74HC4053 analog mux chips.

- An 8 to 1 multiplexer inside the CAN-Bus uProc selects which one of its 8 analog inputs will be selected and sent to its ADC for digitization.

When the control signal to the External Analog Multiplexer is Low then the following signals are sent to the CAN-Bus Microprocessor analog inputs:

CAN-Bus Micro-Processor Analog Input	Analog Quantity Measured when External Multiplexer Control Signal is Low
AN0	BSPT_CORE Voltage
AN1	BF_CORE Voltage
AN2	GTX_AVTT Voltage
AN3	GTX_AVCC Voltage
AN4	TP_CORE Voltage
AN5	BULK_3V3 Voltage
AN6	BULK_2V5 Voltage
AN7	BULK_5V0 Voltage

When the control signal to the External Analog Multiplexer is HI then the following signals are sent to the CAN-Bus Microprocessor analog inputs:

CAN-Bus Micro-Processor Analog Input	Analog Quantity Measured when the External Multiplexer Control Signal is HI
AN0	BSPT_CORE DCDC Converter Input Current
AN1	BF_CORE DCDC Converter Input Current
AN2	GTX_AVTT DCDC Converter Input Current
AN3	GTX_AVCC DCDC Converter Input Current
AN4	TP_CORE DCDC Converter Input Current
AN5	BULK_3V3 DCDC Converter Input Current
AN6	BULK_2V5 DCDC Converter Input Current
AN7	VREF_P Voltage to BF FPGA I/O Banks

Control of the External Analog Multiplexer is provided by signal P84/PWM1P3 on pin number 69 of the CAN-Bus uProc.

Note that jumper JMP85, when removed, forces the control signal to the External Analog Multiplexer Low independent of what pin number 69 on the CAN-Bus uProc says. This forced state enables monitoring of voltages only.

The current measurement at the input to the 7 DC/DC Converter is made by the ADC measuring the voltage at the output of an LT6105 Hi Side Current Monitor. The LT6105 is in turn using the voltage drop across a 5 or 10 mOhm 4 wire resistor at the

input to the DC/DC converter to make its measurement.

Note that these converter input current measurements should be good to 1 or 2 percent. To more accurately estimate the converter output current one could take into consideration the expected efficiency of the converter at the measured load point. The expected efficiency information for the DC/DC converters on the CMX card is available in the data sheets for these converters which are on the CMX web site.

Both the analog Voltage measurement signals and the analog Current measurement signals need to be "scaled" to fit nicely into the dynamic range of the ADC in the CAN-Bus uProc. This is an important issue because this ADC has at best about 8 bits of accuracy. For the Voltage measurement signals it is straight forward to pick a reasonable full scale range.

Optimum scaling is a bigger problem for the Current measurement signals, i.e. do we scale the signals so that we set the full scale of the ADC to be the maximum current that a given DC/DC converter can provide (and thus loose resolution and accuracy at the lower currents where we expect the system to run) or do we set the full scale of the ADC to be just 20 or 30 percent above the expected operating point and loose the ability to measure higher currents ?

The detailed analog circuits for one channel of Voltage and Current monitoring are shown in the following drawing:

35_voltage_and_current_monitor_analog.pdf

CAN-Bus Microprocessor ADC Voltage Reference:

The CMX card uses a separate reference voltage supply for the CAN-Bus Microprocessor ADC reference input. The intent of this is to get most accurate data that we can out of the limited ADC in the CAN-Bus Microprocessor.

This external reference to the CAN-Bus ADC is 4.096 Volts with a tolerance of about +- 0.2%. Scaling of the analog signals to the CAN-Bus ADC and conversion of the numbers from the ADC into engineering units will need to take into consideration the 4.096 Volt reference that it is using.

ADC Readout Scale for Voltage and Current Monitoring:

The "scale" of the CAN-Bus voltage and current monitoring depends on the reference voltage used by the CAN-Bus Microprocessor ADC and it depends on all of the scale

setting resistors that are used in the analog circuits in the CMX monitoring system. The following scale values assume that the scale setting resistors that are described in the CMX Final Assembly document have been installed.

Additionally I will assume that 8 bit values are being used from the CAN-Bus Microprocessor ADC (i.e. the high order 8 bits of the 10 bit value that this ADC can provide). In the MB90F594 data sheet its ADC is called a 10 bit converter with a +- 5 bit conversion error. Thus I will *assume* that people are only using the high order 8 bits of this 10 bit value. Note that not even the high order 8 bits are guaranteed accurate.

Using a 4.096 Volt reference and taking only the high order 8 bits gives a basic scale of 4.096V / 255 = 16.06 mV per LSB in the ADC readout.

Thus the scale of the CAN-Bus Voltage Monitor Readouts is expected to be:

CAN-Bus uProcessor Analog Input	Analog Voltage Measured	mVolts per LSB	Full Scale Volts
AN0	BSPT_CORE Voltage	16.06 mV	4.096 V
AN1	BF_CORE Voltage	16.06	4.096
AN2	GTX_AVTT Voltage	16.06	4.096
AN3	GTX_AVCC Voltage	16.06	4.096
AN4	TP_CORE Voltage	16.06	4.096
AN5	BULK_3V3 Voltage	16.06	4.096
AN6	BULK_2V5 Voltage	16.06	4.096
AN7	BULK_5V0 Voltage	21.80	5.559

Notes: Voltage Monitor signals are digitized by the CAN-Bus uProcessor ADC when the control signal to the External ADC Multiplexer is set Low.

Recall that the AN7, the BULK_5V0 voltage monitor input has an attenuator consisting of a 1.00k Ohm series resistor R1915 and a 2.80k Ohm resistor to ground in parallel with C1885. 2.80k / (1.00k + 2.80k) = 0.7368 For details see the Final Assembly document.

The scale of the CAN-Bus Current Monitor Readout is expected to be:

CAN-Bus uProcessor Analog Input	Analog Quantity Measured	mAmps per LSB	Full Scale
AN0	BSPT_CORE Current	40.16 mA	3.75 Amps
AN1	BF_CORE Current	80.31	7.50
AN2	GTX_AVTT Current	40.16	3.75
AN3	GTX_AVCC Current	40.16	3.75
AN4	TP_CORE Current	80.31	7.50
AN5	BULK_3V3 Current	80.31	7.50

AN6	BULK_2V5 Current	80.31	7.50
AN7	VREF_P Voltage	16.06 mV	4.096 Volts

Notes: Current Monitor signals are digitized by the CAN-Bus uProcessor ADC when the control signal to the External ADC Multiplexer is set Hi.

The Full Scale CAN-Bus Current Monitor readout is set by the 1.5 Volt maximum swing of the LT6105 high side current monitor circuit - not by the 4.096 Volt maximum input to the CAN-Bus uProcessor ADC.

Recall that with the External ADC Multiplexer control line set Hi to read Currents that the AN7 analog input is still used for Voltage Monitoring, i.e. to read the VRef-P voltage.

CAN-Bus Microprocessor Software:

For full operation the CAN-Bus Microprocessor on the CMX card will need somewhat different software than what is in use on the CMM cards. The required difference include (but I expect are not limited to):

1. CMM uses 3 channels of its MAX1668 and has 2 LM35 temp sensors running to ADC inputs.

   CMX used all 4 channels of its MAX1668 and has no other temperature sensors.

2. CMM has 3 duplicate inputs to its ADC multiplexer.

   CMX is using all 8 inputs to its ADC multiplexer.

3. CMX needs a control signal for its External Analog Multiplexer. Allowing time for this External Analog Multiplexer to settle before making ADC conversions on the signals from it will have to be built into the Can-Bus Microprocessor code.

4. CMX needs to be able to send the ADC data from 16 different quantities out from the CAN-Bus Microprocessor and into the overall monitoring system. CMM had only 8 of these quantities.

5. The code for CMX may need more or different unused I/O pins on the CAN-Bus Microprocessor programmed to be outputs so that the unused / unconnected pins have valid CMOS signal levels on them.

At this time I have no understanding of how this new software is going to be written.

Appendix L: CMX Jumpers

A current snapshot is included below while future updates to this description will be in cmx_ab_board_jumpers.txt located in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
                CMX Board Jumpers
              ----------========--

                                          Original Rev.   5-Nov-2012
                                           Current Rev.  23-Apr-2014


This file describes all of the jumpers that are on the CMX
circuit board.  These 114 jumpers are used to setup and control
various functions of the CMX card.



JMP1, JMP2, JMP3   Geographic Address Jumpers

  Geographic Address lines 0, 4, 5, 6  come from the backplane.
  Geographic Address lines 1, 2, 3  come from jumpers 1, 2, 3.

  When one of these 3 jumpers is installed the corresponding
  Geographic Address line is pulled LOW.  E.G. if JMP2 is
  installed then Geographic_Address_2  is pulled LOW.

  notes:

  For the CMM slots, the value of GeoAddr 0 identifies the
  left-side slot number 3 with GA0 = 0  from the right-slide
  slot number 20 with GA0 = 1.

  GA4, GA5, GA6 identify the crate in the overall L1Calo system.

  Prototype build default:
    Set GA1, GA2, GA3  Low
    --> Install jumpers JMP1, JMP2, JMP3.

  Production build default:
    TBD
```

JMP4 Board Support FPGA Configuration PROM CF_B signal to PROG_B

Installing JMP4 allows the JTAG connection to the Configuration PROM for the Board Support FPGA to initiate the configuration of this FPGA. When installed, JMP4 connects the PROM's CF_B signal to the BSPT FPGA's PROG_B pin.

Prototype build default:
PROM cannot initiate configuration
--> JMP4 NOT installed

Production build default:
TBD

JMP5, JMP6, JMP7 Backplane LVDS Receiver Failsafe

When installed the corresponding set of backplane LVDS receivers are in normal "Type 1" mode, i.e. symmetric voltage thresholds. When removed the corresponding set of LVDS receivers are in "Type 2" Failsafe mode with offset voltage thresholds. Normally we expect that all 3 of these jumpers will be installed. JMP5 controls the Upper Backplane Cable receivers. JMP6 the Middle and JMP7 the Lower cable receivers.

Prototype build default:
Symmetric voltage threshold
--> JMP5, JMP6, JMP7 Installed

Production build default:
TBD

R181, R182, R183 Backplane LVDS Transceiver Master_Enable

These 3 "jumpers" are really 100 Ohm resistors. When they are installed they pull the Master Enable pin on the associated LVDS transceivers voltage HI there by enabling normal operation of these DS91M040 LVDS transceivers. We expect that normally all 3 of these "jumpers" will be installed. R181 controls the Upper Backplane Cable transceivers. R182 the Middle and R183 the Lower cable transceivers.

Prototype build default:
LVDS Transceivers enabled
--> R181, R182, R183 Installed

Production build default:
TBD

JMP8 and JMP9 Front Panel CTP LVDS Receiver Failsafe

When installed the corresponding set of Front Panel CTP LVDS receivers are in normal "Type 1" mode, i.e. symmetric voltage thresholds. When removed the corresponding set of LVDS receivers are in "Type 2" Failsafe mode with offset voltage thresholds. Normally we expect that both of these jumpers will be installed. JMP8 controls the receivers for the Upper CTP connector J10. JMP9 controls the receivers for the Lower CTP connector J11.

Prototype build default:
Symmetric voltage threshold
--> JMP8 and JMP9 Installed

Production build default:
TBD

R184 and R185 Front Panel CTP LVDS Transceiver Master_Enable

These 2 "jumpers" are really 100 Ohm resistors. When they are installed they pull the Master Enable pin on the associated set of LVDS transceivers voltage HI there by enabling normal operation of these DS91M040 LVDS transceivers. We expect that normally both of these "jumpers" will be installed. R184 controls the LVDS Transceivers for the Upper CTP connector J11. R185 controls the LVDS Transceivers for the Lower CTP connector J11.

Prototype build default:
LVDS Transceivers enabled
--> R184 and R185 Installed

Production build default:
TBD

JMP10 through JMP27   TTCDec Chip_ID and Master_Mode Bits

These 18 jumpers are used to set 9 of the TTCDec CHIP_ID and MASTER_MODE bits when the TTCDec is Reset. Where installed, these "jumpers" are actually 4.7k Ohm 0603 resistors.   They are setup as follows:

Jumper to		
Pull Low	Pull High	
JMP10	JMP11	---> CHIP_ID(0)
JMP12	JMP13	---> CHIP_ID(1)
JMP14	JMP15	---> CHIP_ID(2)
JMP16	JMP17	---> CHIP_ID(3)

```
      JMP18   JMP19   --->  CHIP_ID(4)
      JMP20   JMP21   --->  CHIP_ID(5)
      JMP22   JMP23   --->  CHIP_ID(13)
      JMP24   JMP25   --->  MASTER_MODE(0)  aka  CHIP_ID(14)
      JMP26   JMP27   --->  MASTER_MODE(1)  aka  CHIP_ID(15)
```

The remaining 7 bits of the CHIP_ID i.e. 12:6 are controlled by the 7 Geographic Address lines.

Prototype build default:
- Set all of these TTCDec Chip ID signals LOW.
- --> Jumpers 10, 12, 14, 16, 18, 20, 22, 24, 26 Installed
- --> Jumpers 11, 13, 15, 17, 19, 21, 23, 25, 27 NOT installed

Production build default:
- TBD

R254, R255, R256 TTCDec CMX Clock Select

Resistors R254 and R256 select whether the CLK_40_DES_1 or the CLK_40_DEC_1_PLL signal from TTCDec is used as the reference for the 40.08 MHz DeSkew-1 clock and thus also for the 320.64 MHz clock on the CMX card.

- Install R254 to select TCC_CLK_40_DES_1_PLL
- Install R256 to select TCC_CLK_40_DES_1

Note that resistor R255 is always installed to provide the CLK_40_DEC_2_PLL signal from TTCDec as the reference for the 40.08 MHz DeSkew-2 clock on the CMX card.

These Jumper-Resistors also acts as a series back terminators on the traces that take the TTCDec output to the CMX Clock Generator. When installed, these "jumpers" are actually 47 Ohm 0603 resistors.

Prototype build default:
- We will use the TTCDec signal CLK_40_DEC_1_PLL as the reference for the DeSkew-1 clocks on the CMX card.
- --> R254 Installed
- --> R256 NOT Installed

Production build default:
- TBD

JMP28 TTCDec Buffer Direction Control

Jumper 28 sets the Direction of the Translator/Buffer chips U151:U154 (only 1/2 of U154) for the TTCDec Output Bus. The TTCDec output signals are converted to 2.5V and driven onto the TCCDec Output Bus to go to the Board Support FPGA and optionally to the Base Function and Topological Processor FPGA. The required Direction

```
  is "B"-->"A"  so Direction control signal must be LOW.
  JMP28 is normally always installed,  i.e. pull DIR Low.

  Prototype build default:
    Direction TTCdec -> BSPT
    --> JMP28    Installed

  Production build default:
    TBD


JMP31 through JMP36    Base Function FPGA M2,M1,M0

  These 6 jumpers control the M2, M1, and M0 Configuration
  signals to the Base Function Virtex FPGA.  Normally the
  Base Function FPGA is Configured via JTAG which requires
  the M2, M1, M0 signals to be set to "101".   Never
  install both the HI and LOW jumpers for a given signal.

    Install JMP31 to pull M2 LOW   JMP32 to pull M2 HI
    Install JMP33 to pull M1 LOW   JMP34 to pull M1 HI
    Install JMP35 to pull M0 LOW   JMP36 to pull M0 HI

  Prototype build default:
    Select JTAG programming (101)
    --> JMP32, JMP33, JMP36   Installed
    --> JMP31, JMP34, JMP35   NOT installed

  Production build default:
    TBD


JMP37 and JMP38    Base Function FPGA  HSWAPEN Pin

  These 2 jumpers control the state of the HSWAPEN pin on
  the Base Function FPGA.  Install only one of these
  jumpers - installing both will short the Bulk_2V5 bus.

    Install JMP37 to pull HSWAPEN Low
    Install JMP38 to pull HSWAPEN Hi

  Prototype build default:
    Enable the BF FPGA's weak pull-ups during configuration.
    --> JMP37   Installed
    --> JMP38   NOT installed

  Production build default:
    TBD
```

JMP41 through JMP46 Topological FPGA M2,M1,M0

These 6 jumpers control the M2, M1, and M0 Configuration signals to the Topological Processor Virtex FPGA. Normally the Topological Processor FPGA is Configured via JTAG which requires the M2, M1, M0 signals to be set to "101". Never install both the HI and LOW jumpers for a given signal.

Install JMP41 to pull M2 LOW JMP42 to pull M2 HI
Install JMP43 to pull M1 LOW JMP44 to pull M1 HI
Install JMP45 to pull M0 LOW JMP46 to pull M0 HI

Prototype build default:
Select JTAG programming (101)
--> JMP42, JMP43, JMP46 Installed
--> JMP41, JMP44, JMP45 NOT installed

Production build default:
TBD

JMP47 and JMP48 Topological Processor FPGA HSWAPEN Pin

These 2 jumpers control the state of the HSWAPEN pin on the Topological Processor FPGA. Install only one of these jumpers - installing both will short the Bulk_2V5 bus.

Install JMP47 to pull HSWAPEN Low
Install JMP48 to pull HSWAPEN Hi

Prototype build default:
Enable TP FPGA's weak pull-ups during configuration.
--> JMP47 Installed
--> JMP48 NOT installed

Production build default:
TBD

JMP49 Topological Processor FPGA Installed

This jumper unambiguously indicates to the Board Support FPGA whether or not the Topological Processor FPGA is installed on this card. This signal, TP_FPGA_INSTALLED_B, has a pull-up resistor to BULK_2V5 and the jumper JMP49 runs to Ground. Thus the TP_FPGA_INSTALLED_B signal is Low active. Low means that the TP FPGA is installed.

Install JMP49 only on cards that have a Topological Processor FPGA installed on them

```
  Prototype build default:
    3 of 4 prototypes can have it and easier to remove than add
    --> JMP49   Installed

  Production build default:
    TBD



JMP51 through JMP56    Board Support FPGA M2,M1,M0

  These 6 jumpers control the M2, M1, and M0 Configuration
  signals to the Board Support Spartan FPGA.  Normally the
  Board Support FPGA is Configured via Master Serial mode
  from its dedicated Configuration "Platform FLASH" PROM
  which requires the M2, M1, M0 signals to be all set LOW.
  Never install both the HI and LOW jumpers for a given
  signal.

    Install JMP51 to pull M2 LOW   JMP52 to pull M2 HI
    Install JMP53 to pull M1 LOW   JMP54 to pull M1 HI
    Install JMP55 to pull M0 LOW   JMP56 to pull M0 HI

  Prototype build default:
    Select serial EPROM configuration for the BSPT (000).
    --> JMP51, JMP53, JMP55   Installed
    --> JMP52, JMP54, JMP56   NOT installed

  Production build default:
    TBD



JMP57    Board Support FPGA  PUDC_B Pin

  JMP57 controls the state of the PUDC_B pin on the Board
  Support FPGA.  The BSPT PUDC_B pin is like the HSWAPEN
  pin on the Virtex devices.  When PUDC_B is LOW then
  before the initial configuration and during subsequent
  confirguration processes the I/O and Input pins have
  pull-up resistors to define a valid logic level on them
  JMP57 pulls BSPT PUDC_B LOW.  R326 pulls PUDC_B HI.

    Install JMP57 to pull PUDC_B Low
     Remove JMP57 and PUDC_B will go Hi

  Prototype build default:
    Enable BSPT FPGA's weak pull-ups during configuration.
    --> JMP57  Installed

  Production build default:
    TBD
```

JMP59 CMX Card Safe Jumper

JMP59 indicates that it is safe to use buses on this CMX card. JMP59 is used to make the signal JUMPER_CMX_SAFE_B.

This signal has a pull-up resistor to BULK_3V3 and the jumper JMP59 runs to Ground. Thus the JUMPER_CMX_SAFE_B signal is Low active. Low means that it is safe to use the buses on this CMX card. The signal JUMPER_CMX_SAFE_B is used by the Hardwired Oversight Logic.

Install JMP59 only on card where it is safe to enable the VME-OCB drivers and the CTP and Cable Translator outputs.

Prototype build default:
Start in safe mode
--> JMP59 NOT installed

Production build default:
TBD

R257 Geographic Address Buffer Direction Control

Jumper R257 is a 1k Ohm resistor that controls the Direction pin of the section of U154 that sends the Geographic Address lines to some of the TTCDec CHIP ID input pins when the TTCDec is being Reset. The Direction of just this section of U154 is always "A"-->"B" so the Direction control pin must be HI. R257 is normally always installed, i.e. pull DIR HI.

Prototype build default:
Direction GeoAddr -> TTCdec
--> R257 Installed

Production build default:
TBD

JMP61 through JMP68 TEST JTAG Chain Device Skip Jumpers

JMP61 and JMP62 allow the front panel TEST JTAG chain to skip across the System-ACE device. Install either JMP61 or JMP62 - not both. Install JMP61 to include the System-ACE. Install JMP62 to skip the System-ACE.

JMP63 and JMP64 allow the front panel TEST JTAG chain to skip across the TTCDec device. Install either JMP63 or JMP64 - not both. Install JMP63 to include the TTCDec. Install JMP64 to skip the TTCDec.

JMP65 and JMP66 allow the front panel TEST JTAG chain to skip across the Configuration PROM for the BSPT FPGA.

```
  Install either JMP65 or JMP66 - not both.  Install JMP65
  to include the Configuration PROM.  Install JMP66 to
  skip the Configuration PROM for the BSPT FPGA.

  JMP67 and JMP68 allow the front panel TEST JTAG chain
  to skip across the BSPT FPGA.  Install either
  JMP67 or JMP68 - not both.  Install JMP67 to include
  the BSPT FPGA.  Install JMP68 to skip the BSPT FPGA.
  Note that to include the BSPT FPGA and provide back
  termination on the TDO data being sent to the JTAG
  interface pod that a resistor could be used in JMP67.

  Prototype build default:
    Include System-ACE, skip TTCdec, include BSPT EPROM, include BSPT
    --> JMP61, JMP64, JMP65, JMP67  Installed
    --> JMP62, JMP63, JMP66, JMP68  NOT  installed

  Production build default:
    TBD



JMP71 through JMP74   Configuration JTAG Chain Skip Jumpers

  JMP71 and JMP72 allow the System-ACE Configuration JTAG
  chain to skip across the Base Function FPGA U1.  Install
  either JMP71 or JMP72 - not both.  Install JMP71 to
  include the Base Function FPGA in the Configuration JTAG
  chain.  Install JMP72 to skip the Base Function FPGA.

  JMP73 and JMP74 allow the System-ACE Configuration JTAG
  chain to skip across the Topological Processor FPGA U1.
  Install either JMP73 or JMP74 - not both.  Install JMP73
  to include the Topological Processor FPGA in the
  Configuration JTAG chain.  Install JMP74 to skip the
  Topological Processor FPGA.

  Prototype build default:
    Include Base FPGA, skip TP FPGA
    --> JMP71, JMP74  Installed
    --> JMP72, JMP73  NOT  installed

  Production build default:
    TBD



JMP75 and JMP76    BF and TP INIT_B to System-ACE Select

  JMP75 and JMP76 allow selection of which Virtex FPGAs
  have their INIT_B Configuration signals connected to the
  System-ACE  CFGINIT_B  pin.  This controls which subset
  of the two Virtex FPGAs the System-ACE will confirm is
  ready to receive a configuration before starting to
  send the bitstream to it via the Configuration JTAG.

  Installing JMP75 connects the Base Function FPGA's
```

```
  INIT_B signal to the System-ACE's CFGINIT_B pin.
  Installing JMP76 connects the Topological Processor
  FPGA's INIT_B signal to the System-ACE's CFGINIT_B pin.
  Note that the System ACE's CFGINIT_B pin is pulled up
  to 2.5 Volts with a 4.7k Ohm resistor.

  Prototype build default:
    Only listen to Base FPGA
    --> JMP75   Installed
    --> JMP76   NOT  installed

  Production build default:
    TBD



JMP78 and JMP79    TP_CORE DC/DC Converter Disable Jumpers

  Jumpers JMP78 and JMP79 are used to disable the TP_CORE
  DC/DC Converter on CMX cards that do not include a
  Topological Processor FPGA.  JMP78 is associated with
  this converter's Inhibit pin.  JMP79 is associated with
  this converter's Track pin.

  To disable the TP_Core DC/DC Converter install jumper
  JMP78 to pull this converter's Inhibit pin to Ground,
  and remove JMP79 to isolate this converter's Track pin
  from the Track bus that spans the other 6 converters.

  For operation of CMX cards with a Topological Processor
  FPGA remove JMP78 and install JMP79.

  Prototype build default:
    3 of 4 prototypes can enable TP_CORE
    --> JMP78   Installed
    --> JMP79   NOT  installed

  Production build default:
    TBD



JMP81    System-ACE POR_BYPASS Pin

  Jumper JMP81 controls the state of the Xilinx System-ACE
  POR_BYPASS pin.  When JMP81 is installed then the
  POR_BYPASS pin is held LOW and the System-ACE's internal
  power on reset circuits are used.  With JMP81 removed
  the external POR_RESET  signal can be used.  The pull-up
  resistor for JMP81 is R308.

    Install JMP81  ACE uses internal Power On Reset circuit
     Remove JMP81  ACE uses external POR_RESET pin signal

  Prototype build default:
    Use External POR_RESET
    --> JMP81   NOT installed
```

Production build default:
TBD

JMP85 CAN-Bus Monitoring Analog Multiplexer Control

Jumper JMP85 determines whether the CAN-Bus uProcessor controls the External Analog Multiplexer or whether the External Analog Multiplexer is held in the state that sends the Voltage Monitoring signals to the ADCs in the CAN_Bus uProcessor.

Install JMP85 CAN-Bus uProc controls the Analog Mux.
Remove JMP85 Analog Mux sends Voltage Monitoring to ADCs.

Prototype build default:
Analog Mux sends only Voltage monitoring information
--> JMP85 NOT Installed

Production build default:
TBD

R481, R482, R483 PLL Lock-Detect to BSPT FPGA DEBUG Input

These 3 jumpers are used to connect the Lock-Detect output signal from the 3 PLLs to Board Support FPGA DeBug signals input pins. These 3 jumpers are located near the J14 FPGA DeBug Connector. If these BSPT FPGA DeBug signals are needed for some other purpose then these jumpers must be removed. If these BSPT DeBug signals are not needed for some other purpose then they may be used to monitor the Lock Status of the 3 PLL circuits on the CMX card.

When installed, these "jumpers" are actually 1.0k Ohm 0603 resistors.

Installing R481 connects the Lock-Detect signal from the 320.6296 MHz PLL to the BSPT FPGA DEGUG_6 input.

Installing R482 connects the Lock-Detect signal from the DeSkew-1 40.08 MHz PLL to the BSPT FPGA DEGUG_5 input.

Installing R483 connects the Lock-Detect signal from the DeSkew-2 40.08 MHz PLL to the BSPT FPGA DEGUG_7 input.

The default build option is to install these 3 jumpers.

Prototype build default:
Connect the Lock-Detect signals:
--> R481, R482, R483 Installed

Production build default:
TBD

R365 through R370 Select the Two Front Panel Access Signals

The CMX card provides two Front Panel Access Signals. The jumper resistors R365 through R370 are used to select the source of the two FP Access Signals. Either the Base Function FPGA, the Topological Processor FPGA or the Board Support FPGA may be the source of a given FP Access Signal.

When installed, these "jumpers" are actually 47 Ohm 0603 resistors.

Select FP_Access_Signal_1:

Installation of R365 selects BSPT FPGA DEBUG_8 as the source of the FP_Access_Signal_1

Installation of R366 selects Base Function FPGA DEBUG_8 as the source of the FP_Access_Signal_1

Installation of R369 selects Topological FPGA DEBUG_8 as the source of the FP_Access_Signal_1

Select FP_Access_Signal_2:

Installation of R367 selects BSPT FPGA DEBUG_9 as the source of the FP_Access_Signal_2

Installation of R368 selects Base Function FPGA DEBUG_9 as the source of the FP_Access_Signal_2

Installation of R370 selects Topological FPGA DEBUG_9 as the source of the FP_Access_Signal_2

Install only R365, R366, or R369 - only one
Install only R367, R368, or R370 - only one

If the BF or BSPT DeBug signals are used for some other purpose then you may not want to install any of these jumper resistors.

The default build option is to install R365 and R367 i.e. both FP Access Signals will come from the BSPT FPGA.

Prototype build default:
BSPT debug signal 8 and 9 sent to front panel
--> R365, R367 Installed
--> R366, R368, R369, R370 NOT installed

Production build default:
TBD

JMP91A, JMP91B : JMP96A, JMP96B, JMP97, JMP98

Installing any of these 14 jumpers grounds the associated object to the CMX pcb ground planes. These jumpers may be left open, have a Zero Ohm jumper installed, or have any appropriate value resistor installed to optimize the ground loop and ground noise environment of the CMX card and the other cards in the L1Calo Processor Crate.

JMP91A, JMP91B	2 jumpers to ground the SFP1 Cage
JMP92A, JMP92B	2 jumpers to ground the SFP2 Cage
JMP93A, JMP93B	2 jumpers to ground the SFP3 Cage
JMP94A, JMP94B	2 jumpers to ground the SFP4 Cage
JMP95A, JMP95B	2 jumpers to ground the bodies of front panel CTP connectors J10 and J11
JMP96A, JMP96B	2 jumpers to ground the 18 <CG> pins in the backplane connectors: J4, J5, J6
JMP97	jumper to ground pins 34 & 68 in CTP conn J10.
JMP98	jumper to ground pins 34 & 68 in CTP conn J11.

Note that in assembly of the CMX cards that the Front Panel, the SFP Cages, and the bodies of CTP connectors J10 and J11 may all be mechanically and electrically bonded together. The possible electrical connection of all (or just of some) of these objects will effect which of the above jumpers should be installed.

Prototype build default:

Hold the SFP Cages quiet with a semi weak connection to the CMX ground planes. Note that the SFP Cages will most likely make electrical contact with the front-panel.
--> Install 4.7k Ohm 0603 resistors at JMP91A, JMP91B
--> Install 4.7k Ohm 0603 resistors at JMP92A, JMP92B
--> Install 4.7k Ohm 0603 resistors at JMP93A, JMP93B
--> Install 4.7k Ohm 0603 resistors at JMP94A, JMP94B

The Front Panel and Stiffener Bars will be tied to the CMX's ground planes via connection through the all metal CTP connector bodies. We want a strong enough connection to provide ESD protection. We want a weak enough connection to prevent ground loops.
--> Install 4.7k Ohm 0603 resistors at JMP95A, JMP95B

Hold the backplane <CG> pins quiet with a semi stiff connection to the CMX ground planes.
--> Install 100 Ohm 0603 resistors at JMP96A, JMP96B

Hold the CTP connector pins 34 & 68 quiet with a semi stiff connection to the CMX ground planes.
--> Install 100 Ohm 0603 resistors at JMP97 & JMP98

```
  Production build default:
    TBD



R801 through R804

  R801 and R802 control the grounding of the Base Function
  FPGA's Heat-Sink.   R803 and R804 control the grounding
  of the Topological Processor FPGA's Heat-Sink.  One may
  install either low value resistors, e.g. 10 to 100 Ohm,
  or Zero-Ohm jumpers in these locations.  The FPGA's top
  surface heat spreader is at ground potential but it is
  not clear that this surface should be hard connected to
  the pcb's ground planes.  Electro Static Discharge from
  people touching the heat-sink is another consideration
  in the grounding of the Virtex heat-sinks.

    R801 and R802  install jumper or resistor to ground
                   the Base Function FPGA Heat-Sink

    R803 and R804  install jumper or resistor to ground
                   the Topological Processor FPGA Heat-Sink

  Prototype build default:
    Semi stiff ground connection to both Virtex heat-sinks.
    --> Install 100 Ohm 0603 resistors at R801,R802, R803, R804.

  Production build default:
    TBD



JMP101 through JMP105    Set a unique CMX Card Serial Number

  Jumpers JMP101 through JMP105  set a unique 5-bit CMX Card
  Serial Number.   This 5-bit CMX Card Serial Number is used
  by the BSPT to make a unique 8-bit Module Serial Number.

  The 8-bit Module Serial Number  together with the
  4-bit Hardware Revision Number  (which is common to all
  CMX cards and held in BSPT programming)  make up the
  L1Calo 12-bit Module ID.

    Install JMP101:JMP105 - to set CMX Card Serial Num bit (1:5) Low
     Remove JMP101:JMP105 - to set CMX Card Serial Num bit (1:5) Hi

  Prototype build default:
    These jumpers must be set to give each CMX card a unique
    CMX Card Serial Number.  They will be installed at MSU
    as we test each CMX card.
    --> JMP101 : JMP105    NOT Installed by assembly vendor

  Production build default:
    --> JMP101 : JMP105    NOT Installed by assembly vendor
```

Appendix M: CMX Power Supplies and Voltage References

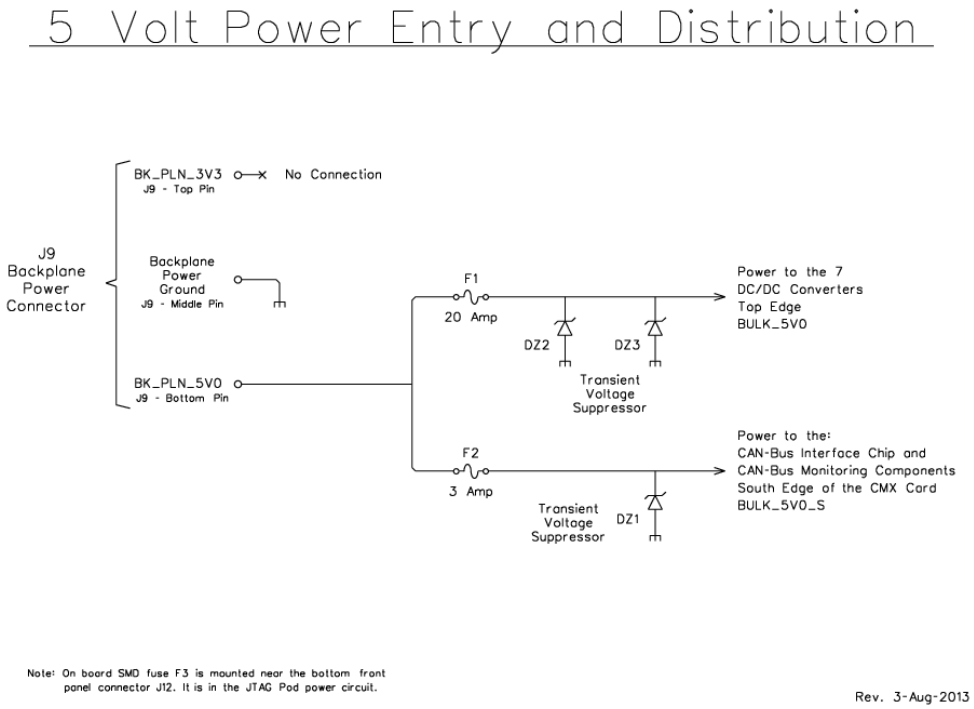


Figure 49: Circuit Diagram for the 5V Power Distribution

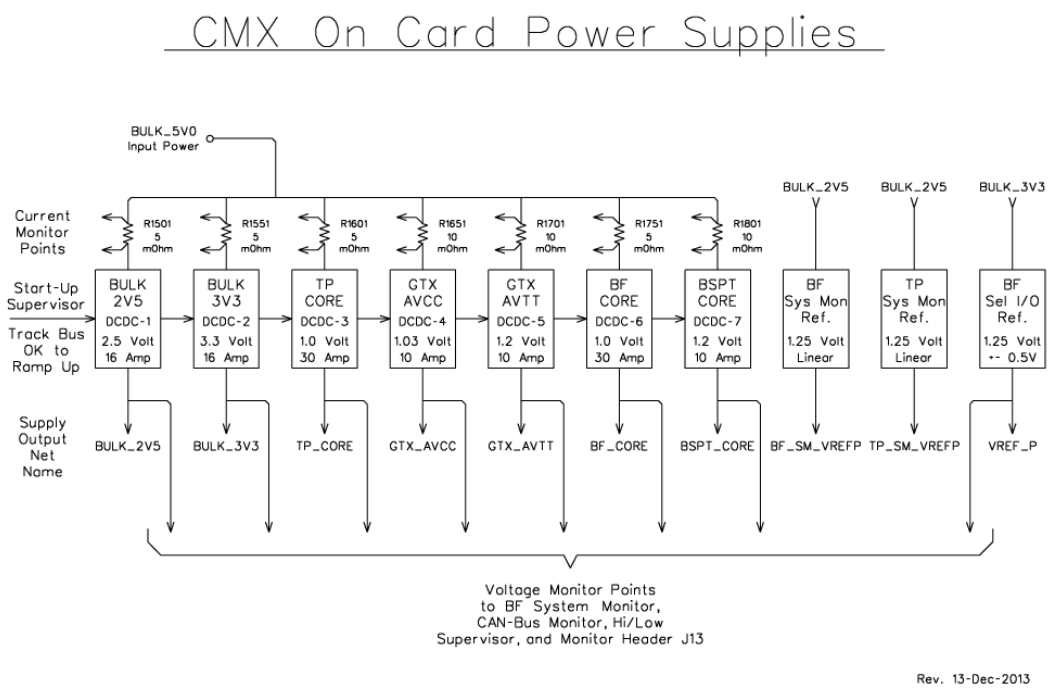


Figure 50: Circuit Diagram of the On-Card Power Supplies

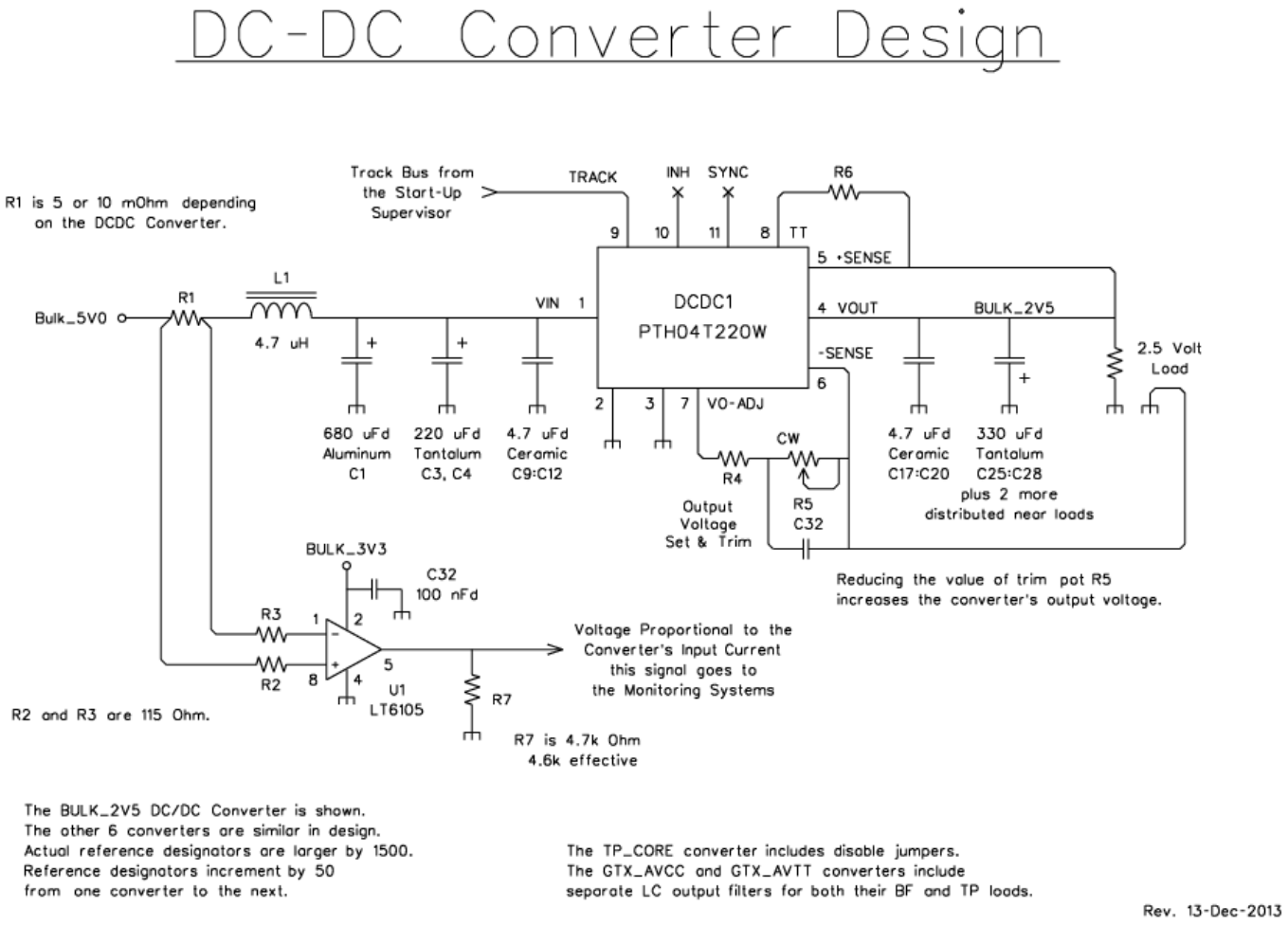


Figure 51: Circuit Diagram for the DC-DC converters

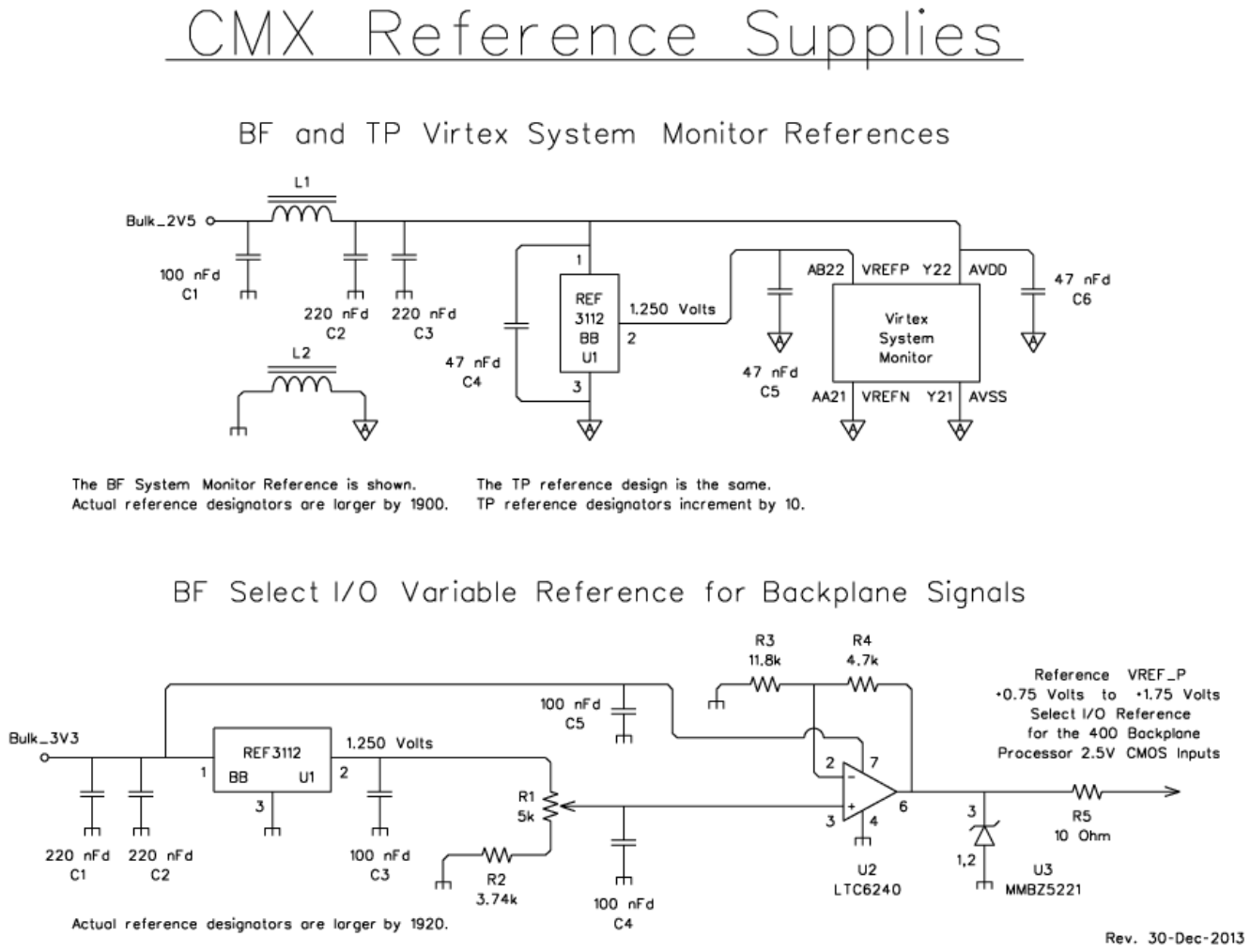


Figure 52: Circuit Diagram for the Reference Supplies

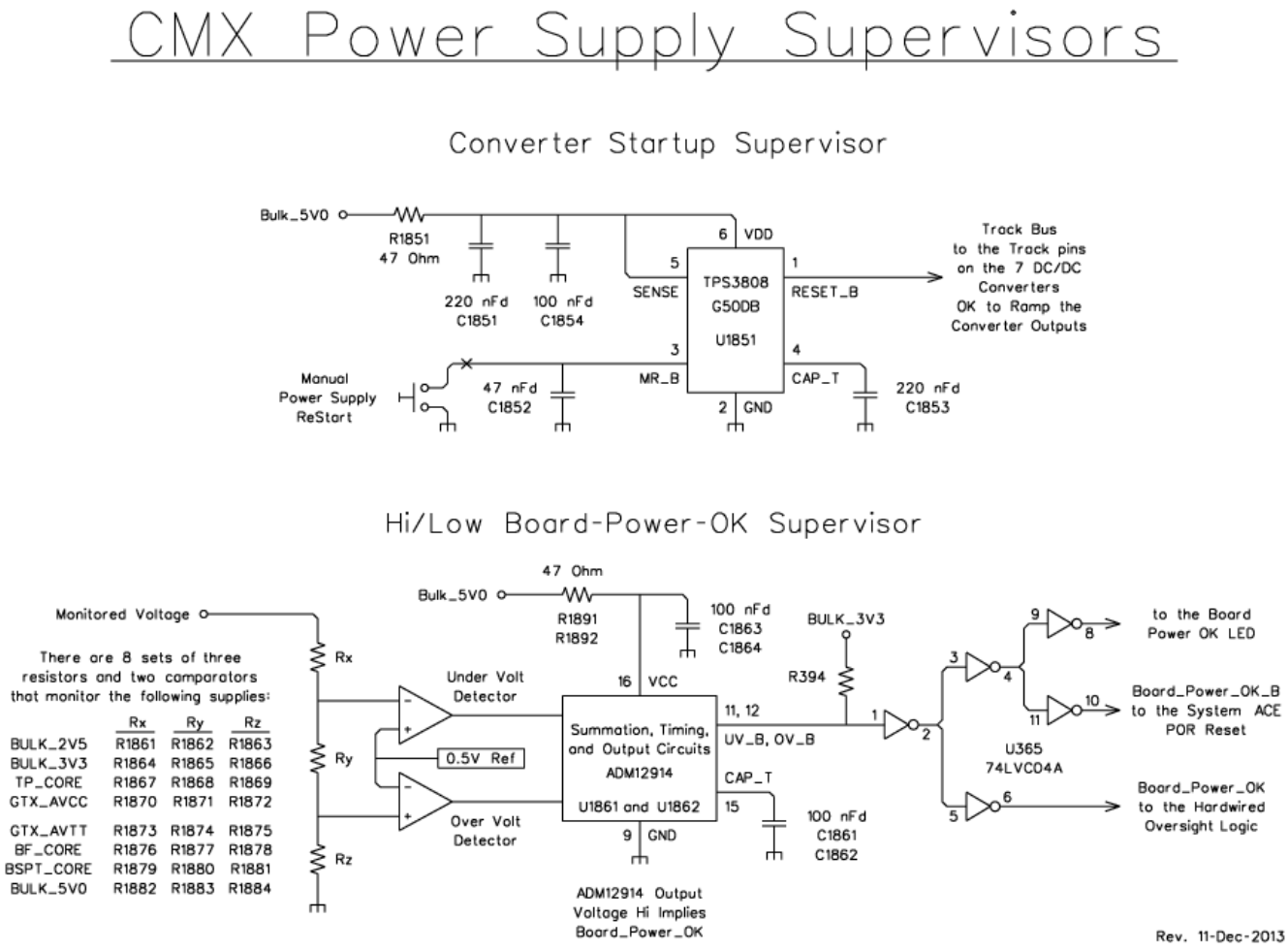


Figure 53: Circuit Diagram for the Power Supply Supervisors

A current snapshot of the circuit diagrams is included above while the source material is in

- 03_5v_power_entry_and_distribution.pdf
- 04_on_card_power_supplies.pdf
- 05_dc_dc_converter_design.pdf
- 06_reference_supplies.pdf
- 07_power_supplies_supervisor.pdf

found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot of the detailed description is included below while the source material is in cmx_ab_power_supply_design.txt found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

CMX On-Card Power Supply Design

Original Rev. 17-Sept-2012
Current Rev. 27-April-2014

The intent of this file is to describe both the functionality and the implementation details of the on board power supplies for the CMX card.

The following is the list of items that must be powered on the CMX card. The official summation of the expected current loads on the various CMX card power supplies is in another document.

Summary of Items on CMX that Must Be Powered:

2x	Virtex-6 FPGAs:	AUX, Core, 2.5V I/O, GTX_AVCC, GTX_AVTT, I/O Reference, System Monitor Reference
1x	Spartan XC3S400A FPGA:	AUX, Core, 2.5V I/O, 3.3V I/O
1x	System-ACE:	2.5V, 3.3V
2x	MiniPOD FO Transmitter:	2.5V, 3.3V
3x	MiniPOD FO Receiver:	2.5V, 3.3V
4x	SFP FO Transceiver:	3.3V
1x	Compact Flash Module:	3.3V
39x	CMOS<->LVDS Transceiver:	3.3V
24x	2.5V<->3.3V Translator:	2.5V, 3.3V
3x	VME Bus Interface:	3.3V
	CAN-Bus Processor and I/F	5.0V
9x	Logic Chips e.g. Oversight	3.3V

List on CMX On-Card Power Supplies Showing their Converter-Name = Power Bus Net-Name, Loads, Voltage, and Current:

Power Bus Converter Net-Name	Loads Supplied by this Converter		Current Capability
Bulk_2V5	all 2.5V logic, Virtex-6 VCCAUX, all Virtex I/O banks, and some Spartan I/O Banks		16 A
Bulk_3V3	all 3.3V logic, some Spartan I/O Banks, and Spartan VCCAUX		16 A
BF_Core	Base Function Virtex-6 Core	1.000 V nom	30 A
TP_Core	TP Virtex-6 Core	1.000 V nom	30 A
GTX_AVCC	GTX Transceiver AVCC	1.030 V nom	10 A

GTX_AVTT	GTX Transceiver AVTT	1.200 V nom	10 A
BSPT_Core	Board Support Spartan Core	1.200 V nom	10 A
BF_IO_REF	Reference for the 400 backplane signals e.g. 0.75 to 1.75V Adjustable i.e. 2.5V divided by 2 +- 0.5V		Analog
BF_SM_REF	Reference for the System Monitor in the Base Func FPGA 1.250 Volt fixed		Analog
TP_SM_REF	Reference for the System Monitor in the TP FPGA 1.250 Volt fixed		Analog
REF_TO_CAN_ADC	Reference for the CANBus uProcessor ADC 4.096 Volt fixed		Analog

Circuit Drawings Showing the CMX Supplies:

03_5v_power_entry_and_distribution.pdf
04_on_card_power_supplies.pdf
05_dc_dc_converter_design.pdf
06_reference_supplies.pdf
07_power_supplies_supervisors.pdf

List of Power Supply Requirements and Permissions:

- All of the supplies should ramp up together to prevent powering of buses through I/O pins.

- The power supplies must meet the ramp time requirements of the Xilinx FPGAs.

- The high speed serial I/O analog supplies for the Virtex parts must meet the Xilinx specified noise requirements and be separate from other loads.

- The FPGA AUX and I/O supplies may be shared with other loads just as long as these power buses meet certain noise requirements.

- Most of the CMX power buses have a +- 5% tolerance requirement except for the GTX_AVCC bus which must be within +- 2.9% of its 1.030V target. Note also that during normal operation the GTX_AVCC bus is within 70 mV of its absolute maximum specification. The 4 reference supplies have tighter accuracy and drift requirements.

- When OFF the 2.5 Volt and 3.3 Volts supplies to the MiniPOD fiber optic components must fall to within 50 mV of ground. If they do not fall to < +50 mV then the module may fail to start up the next time that it is powered up.

Notes on the Selection of these Supplies and Power Buses:

- The GTX_AVCC and GTX_AVTT supplies require converter output filtering (beyond the normal output capacitor bank) to meet the noise requirements for these buses.

- The GTX_AVCC and GTX_AVTT supplies are shared between the Base Function and TP Function FPGAs. Very careful layout is required to meet the GTX noise and voltage tolerance specifications at both loads.

- The GTX_AVCC and GTX_AVTT converters could perhaps have been 6 Amp modules (instead of the selected 10 Amp modules) but they would have been at a 60% limit when running with the TP Function, and these supplies must be very quiet, and it appears that the 10 Amp module design is quieter then the 6 Amp design. Clearly 10 Amps is more than adequate when running only the Base Function.

- The Board Support Core supply clearly could have been a 6 Amp module but using a 10 Amp module saves on the overall part types count for this card.

Functional Description of the
Power Supply System on the CMX Card:
---

1. All power to the CMX card come from the backplane +5 Volt supply that is received on the 3 pin power connector J9. As soon as the backplane +5 Volt power comes onto the CMX card it passes through a 20 Amp main power fuse. The card side of this fuse includes a Transient Voltage Suppressor to help protect circuits on the CMX card from spikes on the +5 Volt supply.

   The principal consumer of the +5 Volt backplane input power is the 7 DC/DC converters that are located along the top edge of the CMX card. The backplane +5 Volt power is used directly by only a few other circuits on the CMX card which include: the CAN-Bus monitoring system and parts of the supervisor circuits for the 7 DC/DC converters. There are separate 3 Amp fuses to help protect the +5 Volt distribution to these circuits.

   The CMX card makes no connection to the backplane +3.3 Volt supply.

2. There is a delay between when the CMX card first senses that it has valid +5V backplane power and when it begins ramping up the output voltage of its 7 DC/DC Converters. The backplane input power monitoring and DC/DC converter ramp up delay is provided by a Texas Instruments TPS-3808 Power Supervisor circuit U1851.

   The TPS-3808 provides a 4.65 Volt under-volt lock out on the operation of the DC/DC converters. The delay from when the backplane input power is > 4.65V until the start of the DC/DC converter output ramp is about 1.2 seconds.

   Although we do not plan to include it in the production build of the CMX cards, pads have been provided on the CMX for a "power re-start switch" to aid in the testing of the card.

   These power up supervisor circuits are shown in circuit drawing: 07_power_supplies_supervisors.pdf

3. Once enabled all DC/DC converter output voltages will ramp up in sync with each other on a volt per volt bases and at controlled ramp rate. The 1.0 Volt converters reach their nominal output in about 8 msec. The 3.3 Volt converter reaches its nominal output in about 40 msec. The Xilinx DC Specifications Manual calls for a Ramp Time between 0.20 and 50.0 msec.

   The DC/DC converters use remote sensing to control their output voltage at the load point. The remote sensing also reduces the problems of regulating the converter's output voltage based on a noisy feedback signal taken immediately adjacent to the converter itself.

   The DC/DC converters include ample bulk ceramic, aluminum and tantalum capacitors on there power input lines. The high input switching currents (at a nominal frequency of 300 kHz) will flow mainly in these capacitors. This switching noise is somewhat isolated from the ground plane by slices in the ground plane that restrict the path of these switching currents. The converter inputs are isolated from the backplane +5 Volt power by high current 4.7 uH chokes. Further but limited isolation of the input switching noise is provided by the 5 or 10 mOhm current measuring resistor in series with each DC/DC converter input and by the main backplane +5V fuse.

   The basic circuit layout of all 7 DC/DC Converters is the same. It is shown in circuit diagram:

   05_dc_dc_converter_design.pdf

The details of the components used with each converter are shown in a table later in this document.

All 7 converters include a 3 turn output voltage trim pot with an adjustment range of about +/- 5%. Without such a trim the initial +/- 3% calibration of the supplies is only marginally good enough. The expect drift over temperature and time is at the 1% level.

The Topological Core supply converter includes two jumpers to disable this supply on boards that do not include the TP FPGA.

The GTX_AVCC and GTX_AVTT supplies include a separate stage of output LC filtering in order to meet the strict low noise requirements on these power buses. The BF FPGA and TP FPGA share common DC/DC converters for these supplies but each FPGA has its own LC filter on them. Remote sense voltage feedback for the GTX_AVCC and GTX_AVTT supplies is taken before these LC filters so that their pole does note appear in the servo loop of these supplies. A low resistance (6.4 mOhm) inductor is used in these LC filters to reduce the problem of voltage drop across these filters.

4. The CMX card includes under-Volt / over-Volt monitors on 8 of its basic power supply voltages. This monitoring is done with Analog Devices ADM12914-2 supervisor chips U1861 and U1862. These 6 of the DC/DC Converter outputs are tested at the +- 5% tolerance level. The GTX_AVCC converter is tested at the +- 2.9% level and the main +5V input power is tested at the +- 9.5% level. The details of the installed resistors that set the under/over monitor thresholds are given in the CMX Final Assembly document.

   When all 8 voltages are within their target values, and have remained within tolerance for about 1 second, then the "Board_Power_Good" signal is asserted. Assertion of the Board_Power_Good signal causes a front panel LED to illuminate and causes the configuration of the Board Support Spartan 3A FPGA.

   The under-Volt / over-Volt monitors are shown in circuit diagram: 07_power_supplies_supervisors.pdf

5. The CMX card's power system provides monitoring of the input current to each DC/DC Converter. This allows us to monitor the CMX card's power consumption at the 5% accuracy level. Monitoring the DC/DC converter output current is more difficult as it would require compensating the converter's servo loop for the additional pole caused by the added RC circuit within its feedback loop.

DC/DC converter input current monitoring is accomplished with input series resistors R1501, R1551, ... which are either 5 mOhm or 10 mOhm depending on the DC/DC converter. These are 4 terminal Kelvin resistors. Linear Technology LT6105 high-side sense amplifiers U1501, U1551, ... are used to measure the voltage drop across these resistors.

The detailed component values that are used in each of the 7 current monitors and their scaling factors are shown in a table later in this document.

The input current monitors are shown in circuit diagram:

04_on_card_power_supplies.pdf
05_dc_dc_converter_design.pdf

6. The CMX card's power system includes connector J13 that allows one to check all of the voltages and currents on the CMX card using a DVM without needing to probe various hard to locate test points on the card. This is a convenient way to both check that the power system on the card is operating correctly and to confirm that the CAN-Bus based and the Virtex System Monitor based readouts are reporting accurate data.

   A table later in this document shows the pinout of the J13 power system test connector. For initial power up tests we have made a rotor switch box so that we can easily connected the DVM to any one of the 20 monitor points that are available on connector J13.

Part Types Used in the CMX On-Card Power Supplies:

To help eliminate assembly errors there is a strong desire to control the number of types of components that are used on the CMX card. This design technique is followed in the power supply section of the CMX card. The main components that are used in the power supply section of the CMX are the following:

Power Trends Part Number	V In	V Out	I Out	Foot Print
PTH04T240W	2.2-5.5V	0.69-3.6 V	10 Amp Max	EAY R-PDSS-T11
PTH04T220W	2.2-5.5V	0.69-3.6 V	16 Amp Max	EBP R-PDSS-T11
PTH05T210W	4.5-5.5V	0.70-3.6 V	30 Amp Max	ECP R-PDSS-T14

CMX uses the through hole version of these supplies so that we have the possibility to replace them in house if necessary.

Filter Inductor: 4.7 uH 15.5 Amp 6.4 mOhm Wurth 7443320470

Current Measurement Resistor 4 Wire:

```
   5 mill-Ohm  4 terminal resistor   Ohmite Part No. FC4L110R005FER
  10 mill-Ohm  4 terminal resistor   Ohmite Part No. FC4L110R010FER
```

Overall Start-Up Supervisor: TI TPS 3808 TPS3808G50DBVR SOT-23-6

Quad Hi/Low Voltage Monitors: AD ADM12914-2ARQZ QSOP-16

Hi-Side Sense Amps: LT LT6105   LT6105HMS8#PBF TSSOP-8

Reference: 1.250 Volt Fixed: TI-Brown REF3112AIDBZT   SOT-23-3
Reference: 4.096 Volt Fixed: TI-Brown REF3140AIDBZT   SOT-23-3

Op-Amp: Linear Technology LTC6240 LTC6240HVIS8#PBF   SOIC-8

Trim Pots: Copal SM-43 Top Adjust 5 Turn 500 5k 20k Ohm

Tantalum Capacitors:

```
  220 uFd  10 Volt  25 mOhm ESR  D Case  Kemet T520D227M010ATE025
  330 uFd  6.3 Volt 15 mOhm ESR  D Case  Kemet T520D337M006ATE015
```

Aluminum Electrolytic:

```
  680 uFd  16 Volt  80 mOhm ESR  G Case  Panisonic EEE-FK1C681GP
```

Ceramic Capacitors: 4.7 uFd 16 Volt X7R 0805 Kemet C0805C475K4RACTU

FPGA Power Requirements Summary:

For the Virtex 6 parts (2 of them) all 2.5V I/O:

```
   VCCINT    1.000 V nominal    0.950 V min   1.050 V max
             about 4.5 A Quiescent

   VCCAUX    2.500 V nominal    2.375 V min   2.625 V max
             about 0.3 A Quiescent   use Bulk_2V5

   VCCO      2.500 V nominal    2.375 V min   2.625 V max
             about  3 mA Quiescent per bank   use Bulk_2V5

   Reference supply for receiving the 400 backplane lines.
   The DC Specifications Manual says that there is only a
   10 uAmp per pin load on this supply.

   Reference supply for the Virtex 6 System Monitor.  This is
   a 1.250 Volt reference at 50 uAmp.  The AVdd supply requires
   about 12 mAmp.  See the System Monitor book pages 12 and 46.

   GTX  MGTAVCC   1.030 V nominal    1.000 V min   1.060 V max
                  about 56 mA per transceiver
                  about 1.6 Amps for 24 + 2  Base Function
                  about 3.6 Amps for 24+36+4 Base and TP Function
```

```
                    +/- 2.9% set point

     GTX  MGTAVTT   1.200 V nominal    1.140 V min   1.260 V max
                    about 56 mA per transceiver
                    about 1.6 Amps for 24 + 2  Base Function
                    about 3.6 Amps for 24+36+4 Base and TP Function

  For the Spartan 3a Board Support FPGA  XC3S400A in the
  FG400/FGG400 package  CMX uses mixed 2.5V and 3.3V I/O:

     VCCINT    1.200 V nominal    1.140 V min   1.260 V max

     VCCAUX    2.500 V or 3.300 V nominal    2.250 V min   2.750 V max
                                          or  3.000 V min   3.600 V max
               This part can use either 2.5V or 3.3V VCCAUX.
               We are using 3.3V VCCAUX so that BSPT JTAG is 3.3V
               Spartan 3A BSPT VCCAUX power comes from BULK_3V3.

     VCCO      2.500 V and 3.300 V nominal   1.100 V min   3.600 V max
               use Bulk_2V5 and Bulk_3V3


Components Requiring +5V Power:
-------------------------------

There are a few components on the CMX card that require
normal old +5 Volt power.  These components include:

  CAN-Bus Interface chip                   PCA82C250
  CAN-Bus Microprocessor                   MB90F594
  4 MHz Xtal Osc for CAN Microprocessor
  Temperature Sensors                      LM35
  Diode IC Temp Sensor chip                MAX1668
  RS-232 Transceiver  MAC3232              MAX3232EUE+
  7 Geo Adrs for 2.5V to 5V                TXB0108PWR
  Power Supply Startup Supervisor          TPS3808G50DBVR



Power Entry and +5V Power Net Names and Components:
---------------------------------------------------

The CMX receives +5V DC power on the bottom pin of the J9
backplane connector.  The middle pin of J9 is ground.  The
top pin of J9 is not used but is loaded into the J9 connector
housing.

From the bottom pin of the J9 connector the +5V is brought
into the card via a small power fill that occupies just the
South East corner of the CMX card.  This power fill is on 6
of the pcb signal layers.

This small power entry power fill delivers the backplane
+5V to 2 components:

  - A 20 Amp fuse  F1  that is mounted on the lower end of
    the vertical stiffener bar.  F1 is connected to the
```

power entry power fill via 4 AWG #22 wires.

- A 3 Amp SMD Fuse F2 that feeds +5V to the CAN-Bus transceivers in the SE corner of CMX and to the CAN-Bus microprocessor and its associated components in the middle of the South edge of the CMX card.

At the output of both the the 20 Amp fuse F1 and at the output of the 3 Amp SMD fuse F2 there are Transit Voltage Suppressor to Ground.

The output of the 20 Amp fuse F1 runs on 4 AWG #22 wires to the top edge of the CMX card. These 4 wires are held to the top surface of the CMX card with super glue. At the top of the CMX card these 4 wires distribute the backplane +5V power to the DC/DC converters. This power is distributed via a power fill along the top edge of the CMX. This power fill uses 5 of the signal layers to achieve a low voltage drop to the input of all of the DC/DC converters.

This top edge +5V power fill also feeds +5V to the few components in the Power Supply Supervision circuits and the Voltage Monitor circuits that need it.

+5V Power Net Names

Net Name	Function
BK_PLN_5V0	+5V Power Entry from the J9 Power Connector
BULK_5V0	20 Amp Fused Bulk +5V Power for the DC/DC Converters. This is fuse F1.
BULK_5V0_S	3 Amp Fused power for the Lower edge of the card for the CAN-Bus transceiver and the CAN-Bus microprocessor and associated components. This is fuse F2.

The following components are used in the +5V power entry section of the CMX design:

Fuse Blocks with Fuse: 3 Amp SMD Littelfuse R154003T

Transient Voltage Suppressor: 5.0 Volt OnSemi 1SMA5.0AT3

Fuse Block: Littelfuse 03540001ZXGY

Fuse: 20 Amp Slow Blow 3AB/3AG Littelfuse 0326020.HXP

Design of the Power Trends DC/DC Converters:

There are 7 Power Trends DC/DC converters on the CMX card:

Supplies Power Bus	Output Voltage	Current Capacity	Power Trends Model Number
Bulk_2V5	2.500 V	16 A	PTH04T220WAD
Bulk_3V3	3.300 V	16 A	PTH04T220WAD
BF_Core	1.000 V	30 A	PTH05T210WAD
TP_Core	1.000 V	30 A	PTH05T210WAD
GTX_AVCC	1.030 V	10 A	PTH04T240WAD
GTX_AVTT	1.200 V	10 A	PTH04T240WAD
BSPT_Core	1.200 V	10 A	PTH04T240WAD

We want to provide about a +-5% adjustment range on all 7 of these supplies to take care of their initial calibration error (about +- 2%) and the 0.1% tolerance resistors in their feedback networks.

The following table list the components in each type of supply:

Component	16 Amp PTH04T220WAD 2.50V & 3.30V	30 Amp PTH05T210WAD 1.000V	10 Amp PTH04T240WAD 1.03V and 1.20V
Cin Total Min	330 uFd Min. 680 uFd Recom	1000 uFd Min. 2000 uFd Recom	220 uFd Min. 680 uFd Recom
Cin Al	1x 680 uF 16V F	2x 680 uF 16V F	1x 680 uF 16V F
Cin Tant	2x 220 uF 10V D	6x 220 uF 10V D	2x 220 uF 10V D
Cin Cerm	4x 4.7uF 16V 85	8x 4.7uF 16V 85	4x 4.7uF 16v 85
Cin Installed	1120 uFd	2680 uFd	1120 uFd
Cout Total Min	220 uFd Min.	470 uFd Min.	220 uFd Min.
Cout Total Max	-	12000 uFd Max.	10000 uFd Max.
Cout Tant	4x 330 uF 6V3 D or 6x 220 uF 10V D	6x 330 uF 6V3 D	6x 330 uF 6V3 D 6x 330 uF 6V3 D
Cout Cerm	4x 4.7uF 16v 85	8x 4.7uF 16v 85	4x 4.7uF 16v 85
Cout @ Load	2x 330 uF 6V3 D or 3x 220 uF 10V D	4x 330 uF 6V3 D	Output Filter Output Filter
Cout Installed	1980 uFd	3300 uFd	1980 uFd
Min Cout for Rtt=0	1100 uFd	2350 uFd	1100 uFd

Resistor Rtt	0 Ohm	0 Ohm	0 Ohm
Vout Rset	1.21k Ohm @3V3 2.37k Ohm @2V5	63.4k Ohm @1V0	18.86k Ohm @1V03 12.1k Ohm @1V20
Rset Slope	1.15kOhm/V @3V3 2.30kOhm/V @2V5	215kOhm/V @1V0	54kOhm/V @1V03 30kOhm/V @1V20
10% of Vout is	0.33 Volt @3V3 0.25 Volt @2V5	0.10 Volt @1V0	0.103 Volt @1V03 0.120 Volt @1V20
--> Rset Var	380 Ohm @3V3 575 Ohm @2V5	21.5k Ohm @1V0	5.56k Ohm @1V03 3.6k Ohm @1V20
Vout Rset Var	500 Ohm @3V3 500 Ohm @2V5	20.0k Ohm @1V0	5.0k Ohm @1V03 5.0k Ohm @1V20
Vout Rset Fix	953 Ohm @3V3 2.10k Ohm @2V5	53.6k Ohm @1V0	16.5k Ohm @1V03 9.76k Ohm @1V20
Design Notes:	-	Rset to Gnd	Output Filters

See the Final Assembly document for details about the Vout Rset resistors and the expected Vout adjustment range for each of the 7 DC/DC Converters..

The 10 Amp 4T240 and the 16 Amp 4T220 have the same relationship between the value of the Vo Rset resistor value and the output voltage. The 30 Amp 5T210 has a different relationship between Rset and the output voltage and it requires significant higher value resistors for a 1 Volt output than the lower current models.

On the DC/DC converters, the Inhibit/Under_Volt_Lockout pins should be floated, the Synchronization pins are also floated on all 7 converters.

It is only the Track pin that is used to manage these supplies. On the CMX one can isolate the Track pin on the TP_CORE supply.

Include an rc0603 in the layout for the connection to the "Turbo-Trans" pins on all converters just in case we need something other than zero Ohms Rtt.

We need to be able to disable the TP_CORE converter on CMX cards that do not include the Topological FPGA. The TP_CORE converter is disabled by installing jumper JMP78 that ties this converter's Inhibit/Under_Volt_Lockout pin to ground and by removing jumper JMP79 which disconnects this converter's Track pin from the Track bus that connects the other 6 DC/DC converters.

The ground plane under each DC/DC converter and its input and output capacitor banks are slit to control and isolate the ground noise from the large circulating currents generated by these buck converters.

LC Input Filter Design:

At what frequency do the LC power input filters become series resonant and thus loose effectiveness ? The inductor is about 5 uH. The capacitor is about 1000 uFd. This gives a series resonant at about 2252 Hz. This is more than 2 orders of magnitude below the 300 kHz switching frequency of the DC/DC converters.

The inductor in these filters is a Wurth 7443320470 4.7uH that can handle a current of 15.5 Amps without saturating and has a DC resistance of 6.35 mOhm. The estimated AC reactance at 2 kHz is about 60 mOhm.

Input Current Monitor Circuits:

Each of the 7 DC/DC converters has a Kelvin current sense resistor and a "high-side" current measuring circuit at its input. The following table looks at how these current monitoring circuits are setup for full scale operation:

	Converter			Input Current	At Full Load	
Converter	Output Voltage	Max. Output Currnt	Max. Output Power	Sense Resistor mOhm	+5 Volt Input Current	Sense Resist V Drop
Bulk_2V5	2.500 V	16 A	40.0 W	5 mOhm	8.0 A	40 mV
Bulk_3V3	3.300 V	16 A	52.8 W	5 mOhm	10.6 A	53 mV
TP_Core	1.000 V	30 A	30.0 W	5 mOhm	6.0 A	30 mV
GTX_AVCC	1.030 V	10 A	10.3 W	10 mOhm	2.1 A	21 mV
GTX_AVTT	1.200 V	10 A	12.0 W	10 mOhm	2.4 A	24 mV
BF_Core	1.000 V	30 A	30.0 W	5 mOhm	6.0 A	30 mV
BSPT_Core	1.200 V	10 A	12.0 W	10 mOhm	2.4 A	24 mV
			+		+	
Totals:			187 Watts		37.5 Amps	

The gain of the Hi-Side LT6105 Sense Amplifiers can be set to emphasize the measurement of either the expected current draw of a given converter or else its full load current draw. The following table shows how the Current Monitor Amplifiers are actually setup as described in the CMX Final Assembly document. Note that the actual load to ground on the LT6105 high side current sense amplifiers is 4.60k Ohm.

Converter		Installed Rin Resistors: Reference Designators	Value Ohms	Sense Resistor mOhms	LT6105 Volts Out per Amp In	Vout =1.5V --> F.S. Amps
DCDC1	BULK_2V5	R1502 R1503	115	5	0.200V	7.5 A
DCDC2	BULK_3V3	R1552 R1553	115	5	0.200	7.5
DCDC3	TP_Core	R1602 R1603	115	5	0.200	7.5
DCDC4	GTX_AVCC	R1652 R1653	115	10	0.400	3.75
DCDC5	GTX_AVTT	R1702 R1703	115	10	0.400	3.75
DCDC6	BF_Core	R1752 R1753	115	5	0.200	7.5
DCDC7	BSPT_Core	R1802 R1803	115	10	0.400	3.75

- The value of the Rout load to ground on each of the LT6105 high side current sense amps is about 4.60k Ohm. This is a 4.70k Ohm 1% resistor in parallel with two series 100k Ohm resistors that make the voltage divider for the input to the Virtex System Monitor. The actual value is 4.592k Ohm, i.e. 0.2% under 4.6k Ohm.

- 4.60k Ohm divided by 115 Ohm gives a gain of 40 to all 7 of the LT6105 high side current sense amplifiers.

- Both the CAN-Bus uProcessor ADC and the Virtex-6 System Monitor ADC are used to readout these DC/DC Converter Input Currents. Note that these two readout have different scales per LSB and different full scales.

- The LT6105 high-side current sense amplifiers are powered from BULK_3V3 bus and all use 4.60k Ohm effective output resistors. Because the output of these high-side amps could swing higher than +2.5V a series resistor is used before the analog multiplexer input to these ADCs. These series resistors are also part of RC filters in front of each analog multiplexer input channel.

Reference Supplies and Their Design:

- The Reference Inputs to the Virtex-6 System Monitor are high impedance. These are pins Vrefp and Vrefn. The voltage between these pins is to be 1.250 Volts. The Reference supply current draw is 100 uAmp maximum. Pin Vrefn must be in the range of -50 mV to +100 mV of ground.

- In the System Monitor circuit there is an inductor to isolate the CMX GROUND plane from the System Monitor AVSS "analog ground". There is also an inductor to isolate the BULK_2V5 supply from the System Monitor AVDD pin. Page 46 of the System Monitor reference book indicate the requirements for these inductors. They have a reactance of about 500 Ohms at 100 MHz. This works out to about 1 uH.

- The Select I/O Reference Supply needs to be able to provide 10 uAmp of current per pin. There are 24 reference pins that must be supplied on the Base Function FPGA for the I/O Banks that handle the 400 Processor inputs. This means that the 0.75 to 1.75 Volt Reference Supply needs to provide 240 uAmp of current.

- Xilinx wants a 22 nFd to 470 nFd capacitor on each of the Select I/O Reference pins. With 24 reference pins on the Base Function FPGA this implies that the 0.75 to 1.75 Volt Select I/O Reference Supply needs to work into a 0.528 uFd to 11.28 uFd capacitive load.

- The output of the Select I/O Reference supply is isolated with a 10 Ohm resistor and includes a zener clamp. The maximum voltage drop across this 10 Ohm resistor should be 240 uAmp max x 10 Ohms = 2.4 mV max.

Physical Layout Location of the DC/DC Converters:

- The DC/DC Converters are located along the top edge of the CMX circuit board.

- Working from West to East the converters are:

Bulk_2V5,	Bulk_3V3,	TP_Core,	GTX_AVCC,
16 Amp	16 Amp	30 Amp	10 Amp

followed by

GTX_AVTT,	BF_Core,	BSPT_Core
10 Amp	30 Amp	10 Amp

Design of the Voltage Monitor Circuits:

The CMX card includes Under-Volt / Over-Volt monitors on 8 of its power supplies. When all 8 of these supplies are operating within their required range then the BOARD_POWER_OK signal is asserted high. There is a delay of about 1 second between all 8 monitored supplies becoming stable within their required operating range and the assertion of the BOARD_POWER_OK signal.

Two Analog Devices type AD12914-2 quad voltage monitors are used to generate the BOARD_POWER_GOOD signal. All signals sent to these voltage monitors are compared to an internal 500 mV reference.

A separate resistor divider on each monitored supply provides the comparator input signals to the voltage monitor. The standing current in these resistor dividers must be significantly greater than the 10 nA input current to the comparators. The CMX card uses a standing current of about 1 mA in its resistor dividers, i.e. swamp the input current but still avoid any heating of these resistors.

The resistor values selected for these dividers sets the "OK" operating range for each supply. The resistor values currently installed in each of these 8 voltage dividers and the resulting Voltage OK Ranges are given in the CMX Final Assembly document. The circuit diagram of the Under-Volt Over-Volt monitor is given in:

07_power_supplies_supervisors.pdf

Voltage and Current Monitoring Points:

The following 3 tables list the various Voltage and Current Monitoring Points that are on the CMX card.

The calibration, e.g. mV per LSB readout by one of the ADCs or monitor signal Volts per Amp of DC/DC Converter Input Current are controlled by a number of scale setting resistors that are installed during Final Assembly of the CMX cards.

The calibration constants can be found in the CMX Final Assembly document or in the CAN-Bus Monitoring or Virtex System Monitor documents.

CAN-Bus Micro-Processor Analog Input
Voltage and Current Monitoring

CAN-Bus Micro-Processor Analog Input	External Multiplexer Control Signal = Low --> Power Bus Voltage Monitored	External Multiplexer Control Signal = Hi --> Power Bus Current Monitored
AN0	BSPT_CORE Volts	BSPT_CORE Current
AN1	BF_CORE Volts	BF_CORE Current
AN2	GTX_AVTT Volts	GTX_AVTT Current
AN3	GTX_AVCC Volts	GTX_AVCC Current
AN4	TP_CORE Volts	TP_CORE Current
AN5	BULK_3V3 Volts	BULK_3V3 Current
AN6	BULK_2V5 Volts	BULK_2V5 Current
AN7	BULK_5V0 Volts	VRef_P Volts

Base Function Virtex System Monitor
Auxiliary Analog Input
Power Bus Voltage and Current Monitoring

BF FPGA System Monitor Input	Power Bus Voltage or Current Monitored by this Input
SYSMON_00	input not used for monitoring
SYSMON_01	GTX_AVTT Voltage
SYSMON_02	input not used for monitoring
SYSMON_03	BF_CORE Current
SYSMON_04	BF_CORE Voltage
SYSMON_05	input not used for monitoring
SYSMON_06	input not used for monitoring
SYSMON_07	GTX_AVTT Current
SYSMON_08	GTX_AVCC Current
SYSMON_09	BULK_2V5 Voltage
SYSMON_10	BULK_3V3 Current
SYSMON_11	GTX_AVCC Voltage
SYSMON_12	BULK_3V3 Voltage
SYSMON_13	BULK_2V5 Current
SYSMON_14	TP_CORE Current
SYSMON_15	VREF_P Voltage Select I/O Ref

This strange mapping of monitored quantity to BF FPGA Virtex System Monitor Input is forced by routing constraints.

Power Bus Voltage and Current Monitoring Via the J13 Header Connector

J13 Pin	Monitor Connection
1	BSPT_CORE Voltage
3	BSPT_CORE Current
5	BF_CORE Voltage
7	BF_CORE Current
9	GTX_AVTT Voltage
11	GTX_AVTT Current
13	GTX_AVCC Voltage
15	GTX_AVCC Current
17	TP_CORE Voltage
19	TP_CORE Current
21	BULK_3V3 Voltage
23	BULK_3V3 Current
25	BULK_2V5 Voltage
27	BULK_2V5 Current
29	BULK_5V0 Voltage
31	V_REFP Voltage Select I/O Ref
33	not assigned, access via SR71
35	not assigned, access via SR72
37	not assigned, access via SR73
39	not assigned, access via SR74

All even pin numbers on J13 are Ground.

Appendix N: Virtex-6 Bypass Capacitors

A current snapshot of the detailed description is included below while the source material is in cmx_ab_fpga_bypass_caps.txt found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
      CMX  Virtex-6 FPGA  Bypass Capacitor  Design Layout
     ------------------------------------------------------


                                        Original Rev.   22-June-2012
                                         Current Rev.  24-April-2014


This file gives both the background and then the full details
of the bypass capacitor design layout that is used on the CMX
card's Virtex-6 FPGAs.


Virtex-6 Bypass Capacitor Rules from Xilinx:
-------------------------------------------

Most of this information is from Chapter 2 of the, "Virtex-6
PCB Design Guide".   Stired into this will be the capacitor
requirements on the output of the DC/DC power converters that
will be used on the CMX card.

Their table 2.1 in Chapter 2 does not show the need for any
bulk or high frequency VCCAUX or VCCO bypass capacitors.
They do have VCCAUX and VCCO bypass capacitors on their
demo boards as noted below.

Chapter 2 says that as long as the plane noise is under 5%
(250 mVpp on a 2.5 Volt supply)  then the same power plane
may be used for VCCAUX and VCCO  with the Virtex-6 device.

Information about the required bypass capacitors on the
analog supplies for the GTX high speed serial transceivers
comes from Chapter 5 of the GTX Transceiver User's Guide.
```

VCCINT from the CMX Base_Core and TP_Core Supplies:

- Xilinx says that for the XC6VLX550T FPGA in the FF1759 package they want 9x 330 uFd caps on the VCCINT core supply pins

  By 330 uFd Xilinx means, 330 uFd Tantalum V-Case 15 mill-Ohm < ESR < 40 mill-Ohm 2.5 Volt for VCCINT T520V337M2R5ATE025

- The Xilinx ml623 demo board explicitly uses the following on its VCCINT Core supply:

  2x 330 uFd 2.5V Tant Kemet T520V337M2R5ATE025
  4x 2.2 uFd 10V X7R Kemet C0805C225K8RACTU
  8x 220 nFd 10V X7R Panisonic ECJ-0EF1A224Z

  The Xilinx ml623 demo board has a XC6LVX240T FPGA in a FFG1156 package.

- We are using a 30 Amp Power Trends PTH05T210WAD DC/DC converter to supply the VCCINT Core power. This supply has a complicated set of output capacitor requirements that depend on how good of a transient responce you want and on how much of its "Turbo-Trans" function you are using. A quality setup of this converter requires:

  Capacitors with a capacitance uFd times ESR mOhm of less than 10,000 uFd_mOhm are reqiored

  The absolute minimum capacitance is 470 uFd and the maximum capacitance is 12,000 uFd.

  The bulk of the output capacitance on the CMX will be tantalum T520 with a uFd_mOhm in the range 5,000 to 10,000 i.e. type "C" in Power Trends speak.

  Power Trends is happy with Kemet T520 series capacitors. Specifically the T520D337M006ATE015 looks good, i.e. it is 6.3V so it can also be used on the 3.3V bus and it is the standard "D" case instead of the special and expensive "V" case.

  For Cout > 2350 uFd the converter's Rtt feedback resistor can be a short.

- Remote sensing feedback from immediately under the FPGA will be needed for both the Base_Core and TP_Core supplies.

- Final Definitive CMX VCCINT Core Bypass Capacitor Design per Virtex FPGA:

  10x 330 uFd 6.3V D Case T520 Tantalum 3300 uFd total location split between FPGA and converter output.

  6x 33 uFd 10V Tant B Kemet T520B336M010ATE025

```
       6x  4.7 uFd   16V  X7R  0805  Kemet  C0805C475K4RACTU

      10x  220 nFd   10V  X7R  0603  Kemet  C0603C224K8RACTU
```

VCCAUX from the CMX BULK_2V5 Supply:

- Xilinx table 2.1 says that the XC6VLX550T FPGA in the FF1759 package needs Zero bypass capacitors on its VCCAUX supply pins.

- But the Xilinx ml623 demo board explicitly uses the following on its VCCAUX supply:

```
      1x   33 uFd 6.3V Tant   Kemet  T520B336M006ATE040
      1x  2.2 uFd 10V X7R     Kemet  C0805C225K8RACTU
      1x  220 nFd 10V X7R     Panisonic  ECJ-0EF1A224Z
```

- The output capacitors on the DC/DC converter for the BULK_2V5 supply are not included in this Virtex-6 VCCAUX bypass calculation.

- Final Definitive CMX VCCAUX Bypass Capacitor Design per Virtex FPGA:

```
      1x   33 uFd   10V  Tant   B   Kemet  T520B336M010ATE025

      1x  4.7 uFd   16V  X7R  0805  Kemet  C0805C475K4RACTU

      1x  220 nFd   10V  X7R  0603  Kemet  C0603C224K8RACTU
```

VCCO from the CMX BULK_2V5 Supply:

- Xilinx table 2.1 says that the XC6VLX550T FPGA in the FF1759 package needs Zero bypass capacitors on its VCCO supply pins.

- But the Xilinx ml623 demo board explicitly uses the following on its VCCO supply pins:

```
      1x   47 uFd 6.3V Tant   Kemet  T520B476M006ATE070
      1x  2.2 uFd 10V X7R     Kemet  C0805C225K8RACTU
      1x  220 nFd 10V X7R     Panisonic  ECJ-0EF1A224Z
```

  The VCCO caps are per I/O Bank: there are 16 sets of these 3 capacitors on the Xilinx ml623 Demo Card. 3 capacitors per I/O bank all powered from a common VCCO power supply module.

- The CMX XC6VLX550T FPGA in the FF1759 package has 21 I/O Banks. The bulk of the Select I/O pins on the CMX Virtex-6 FPGAs will be inputs. Simultaniously switched outputs on the Base Function FPGA will include:

  66 lines to the CTP outputs from I/O Banks ?
  16 data lines to the On-Card-Bus from I/O Bank ?
  81 lines to the Backplane LVDS cables from I/O Banks ?

- The output capacitors on the DC/DC converter for the BULK_2V5 supply are not included in this Virtex-6 VCCO bypass calculation.

- Final Definitive CMX VCCO Bypass Capacitor Design per Bank:

1x	33 uFd	10V	Tant	B	Kemet	T520B336M010ATE025
1x	4.7 uFd	16V	X7R	0805	Kemet	C0805C475K4RACTU
1x	220 nFd	10V	X7R	0603	Kemet	C0603C224K8RACTU

Select I/O Bank Reference Pin Bypass Capacitors:

- For VREF_P supplies Xilinx wants one capacitor per pin placed as close to the pin as possible. The capacitor should be in the 22 nFd to 470 nFd range. Its purpose is to reduce the VREF node impedance. No low frequency energy is needed on VREF so no bulk capacitors are needed.

- Final Definitive CMX Design of the VREF_P Bypass Capacitors:

4x	4.7 uFd	16V	X7R	0805	Kemet	C0805C475K4RACTU
10x	220 nFd	10V	X7R	0603	Kemet	C0603C224K8RACTU
10x	100 nFd	25V	X7R	0603	Kemet	C0603C104K3RACTU

MGTAVCC from the CMX GTX_AVTT Supply:
MGTAVTT from the CMX GTX_AVTT Supply:

- These are the analog supplies for the high speed serial GTX transceivers in the Virtex-6 FPGAs.

- Although both VCCINT and AVCC are both nominally 1.0 Volt separate supplies should be used for these 2 loads. (and separate planes - duh)

- The noise on the AVCC and AVTT planes must be under 10 mVpp in the 10 kHz to 80 MHz range.

- Switching regulators generally require additional filtering before their power is delivered to the GTX Transceivers.

- The AVCC and AVTT supplies need their own private plane islands which must not run under the Select I/O section of the FPGA's footprint.

- We will always be using a large enough fraction of the GTX Transceivers that it makes sense to always power both the North and South Quads.

- The minimum bypassing of the AVCC and AVTT supplies that is specified in Chapter 5 is the following:

  1x 220 nFd 0402 ceramic per power supply pin
  1x 4.7 uFd 0402 ceramic per two quads
  1x 330 uFd bulk capacitor per supply

- The XC6LVX550T-2FFG1759C has 9 quads. It has:

  9 pins for AVCC_N 9 pins for AVCC_S
  13 pins for AVTT_N 14 pins for AVTT_S

- So the minimum suggested AVCC and AVTT bypassing for the GTX supplies is:

  On AVCC: 18x 220 nFd
  5x 4.7 uFd
  1x 330 uFd bulk

  On AVTT: 27x 220 nFd
  5x 4.7 uFd
  1x 330 uFd bulk

- The ml623 with its 5 Quads used 16 bypass capacitors of 220 nFd on its AVCC island and 16x 220 nFd capacitors on its AVTT island. Scale this up to the CMX's 9 Quads --> 29 capacitors on each power island.

- The ml623 also used the following on both its AVCC and AVTT:

  1x 47 uFd 6.3V Tant-B "DNP" and
  3x 1 uFd 16V X5R ceramics and
  1x 33 uFd 16V Tant-C "DNP" and
  1x 330 uFd 10V Tant-D "DUP"

- The intent on the CMX is to use a common GTX_AVcc supply and a common GTX_AVtt supply for the GTX Transceivers in both the Base Function and Topological Processor FPGAs.

- To reduce the noise on the GTX_AVcc and GTX_AVtt supplies the CMX uses LC filters between the DC/DC Converters for these supplies and the loads in the BF and TP FPGAs. Separate filters are used for each supply and for each FPGA. The L in these filters are Wurth Part No. 7443320470 4.7 uH 15.5 Amp 6.4 mOhm inductors. There us no chance of saturating these inductors during normal operation.

Low DC resistance inductors are used to minimize the IR drop of the filter. The IR drop is about 15 mV to the Base Function FPGA. Note that the remote sense for the GTX_AVcc and GTX_AVtt DC/DC converters is taken before these LC filters. Sensing before the filter removes the need to compensate for the extra pole that the filter adds to the DC/DC converter's servo loop. The series resonance of these LC filters is at about 4 kHz but should not have a significant noise peak because of the low Q of the filter.

- Final Definitive Design of the GTX_AVCC and GTX_AVTT Bypass Capacitors, per Virtex FPGA, located at the GTX side of each FPGA:

  On GTX_AVCC:

18x	220 nFd	10V	X7R	0603	Kemet	C0603C224K8RACTU
5x	4.7 uFd	16V	X7R	0805	Kemet	C0805C475K4RACTU
2x	33 uFd	10V	Tant	B	Kemet	T520B336M010ATE025
1x	330 uFd	6.3V	Tant	D	Kemet	T520D337M006ATE015

  On GTX_AVTT:

27x	220 nFd	10V	X7R	0603	Kemet	C0603C224K8RACTU
5x	4.7 uFd	16V	X7R	0805	Kemet	C0805C475K4RACTU
2x	33 uFd	10V	Tant	B	Kemet	T520B336M010ATE025
1x	330 uFd	6.3V	Tant	D	Kemet	T520D337M006ATE015

- In addition to the GTX_AVCC and GTX_AVTT Bypass Capacitors located at the GTX side of each Virtex FPGA, there are 6 of the 330 uFd Tantalum capacitors for bulk filtering located right at the output of both the GTX_AVCC and the GTX_AVTT DC/DC converters.

List of Capacitors actually use on CMX_0:

Cap_10_nFd_0402	Ceramic Capacitor 10 nFd 25 Volt X7R Ceramic 0402 Size SMD Kemet Part No. C0402C103K3RACTU	32
Cap_47_nFd_0603	Ceramic Capacitor 47 nFd 25 Volt X7R Ceramic 0603 Size SMD Kemet Part No. C0603C473K3RACTU	168
Cap_100_nFd_0201	Ceramic Capacitor 100 nFd 6.3 Volt X5R Ceramic 0201 Size SMD Kemet Part No. C0201C104K9PACTU	72
Cap_100_nFd_0603	Ceramic Capacitor 100 nFd 25 Volt X7R Ceramic 0603 Size SMD Kemet Part No. C0603C104K3RACTU	231

Cap_220_nFd_0603	Ceramic Capacitor 220 nFd 10 Volt X7R Ceramic 0603 Size SMD Kemet Part No. C0603C224K8RACTU	189
Cap_4.7_uFd_0805	Ceramic Capacitor 4.7 uFd 16 Volt X7R Ceramic 0805 Size SMD Kemet Part No. C0805C475K4RACTU	168
Cap_33_uFd_Tant_B	Tantalum Capacitor 33 uFd 10 Volt 25 mOhm ESR "B" Case SMD Kemet Part No. T520B336M010ATE025	111
Cap_220_uFd_Tant_D	Tantalum Capacitor 220 uFd 10 Volt 25 mOhm ESR "D" Case SMD Kemet Part No. T520D227M010ATE025	28
Cap_330_uFd_Tant_D	Tantalum Capacitor 330 uFd 6.3 Volt 15 mOhm ESR "D" Case SMD Kemet Part No. T520D337M006ATE015	46
Cap_680_uFd_16V	Aluminum Electrolytic Capacitor 680 uFd 16 Volt 80 mOhm ESR "G" Case SMD Panisonic Part No. EEE-FK1C681GP	9

Appendix O: Geographical View of Power Usage

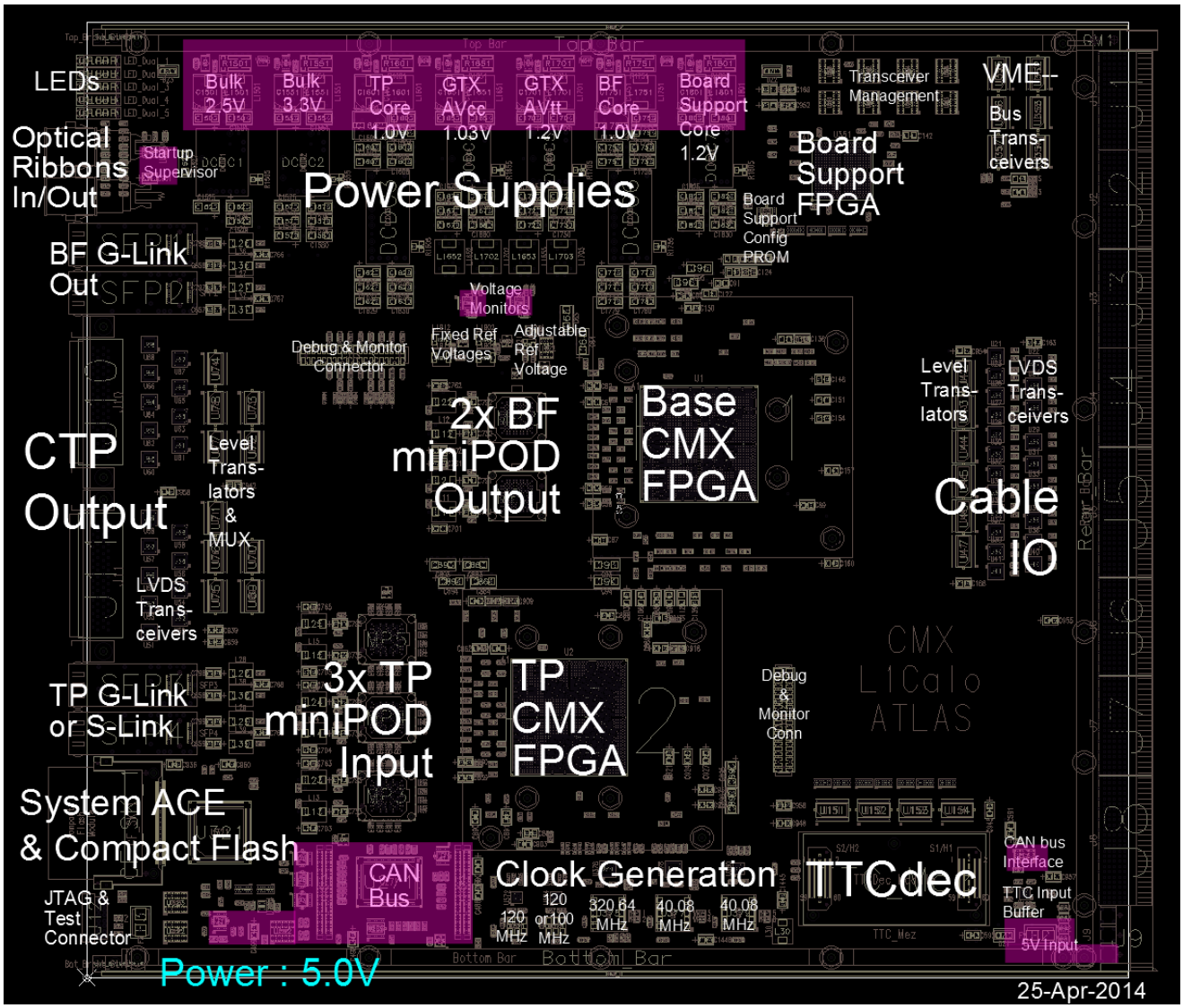


Figure 54: Power: 5.0V Input power

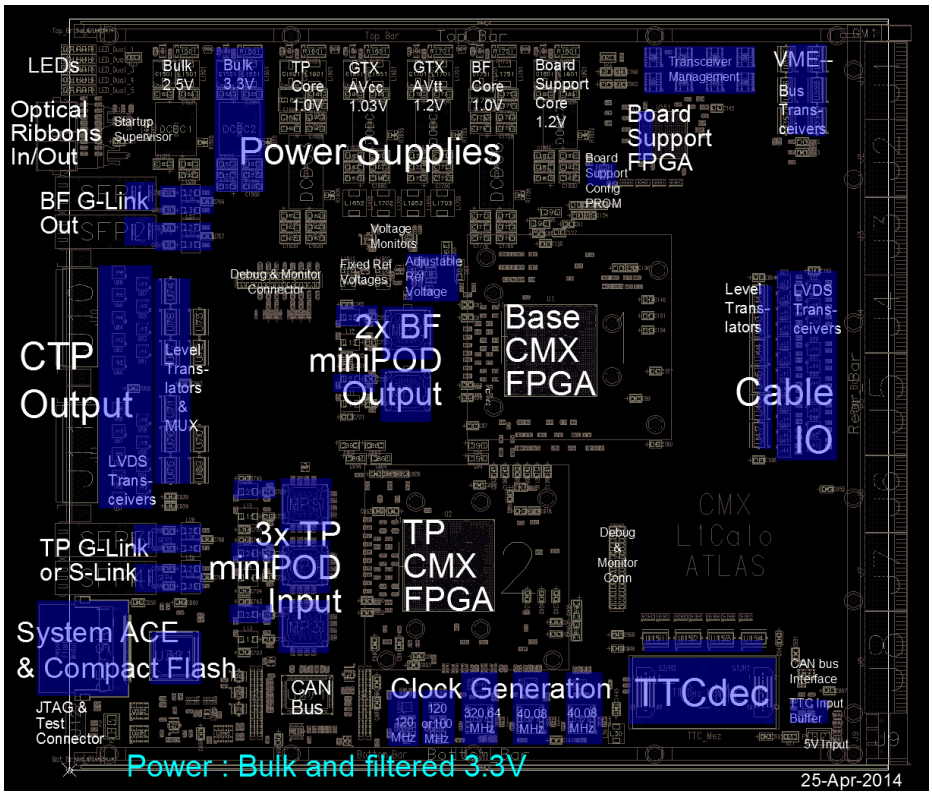


Figure 55: Power: Bulk and Filtered 3.3V

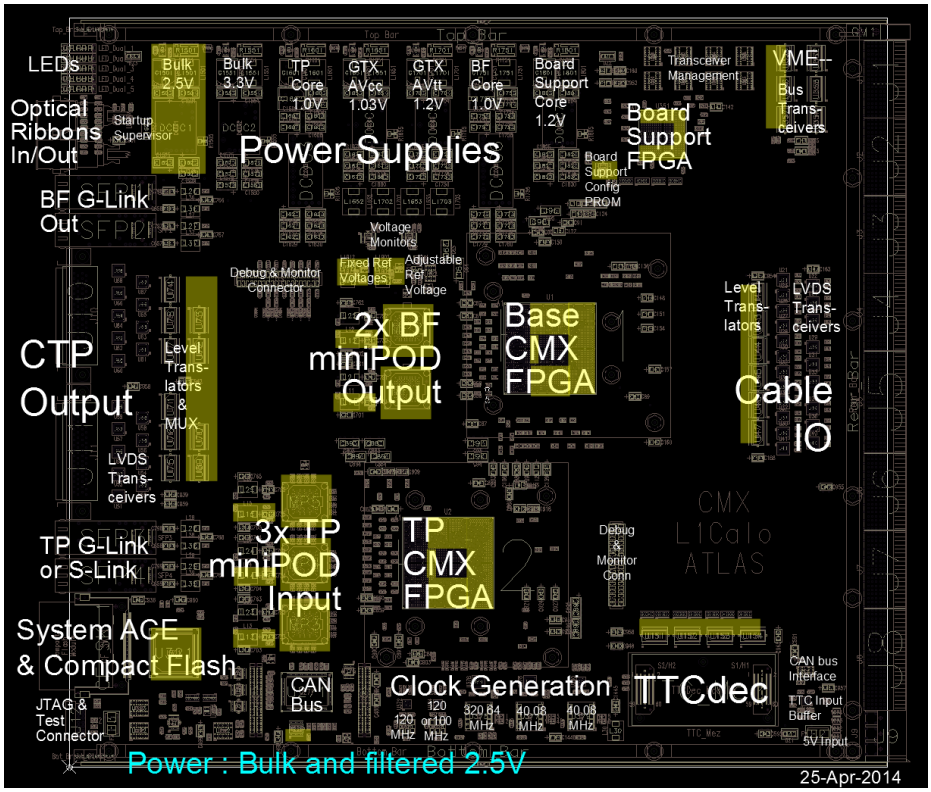


Figure 56: Power: Bulk and Filtered 2.5V

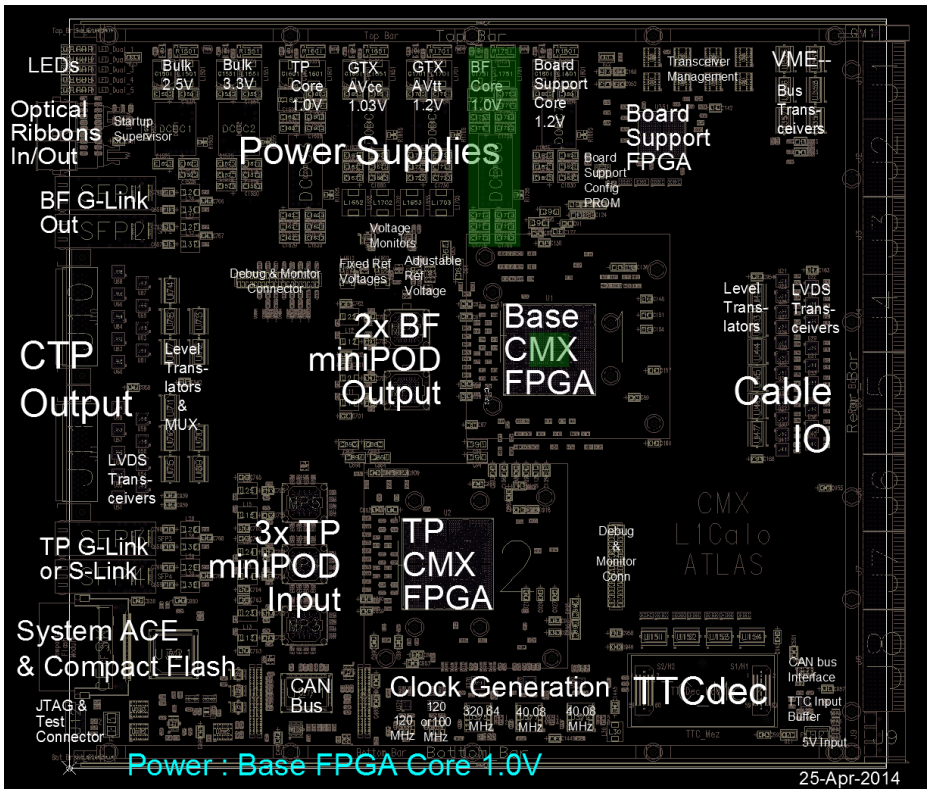


Figure 57: Power: Base FPGA Core 1.0V

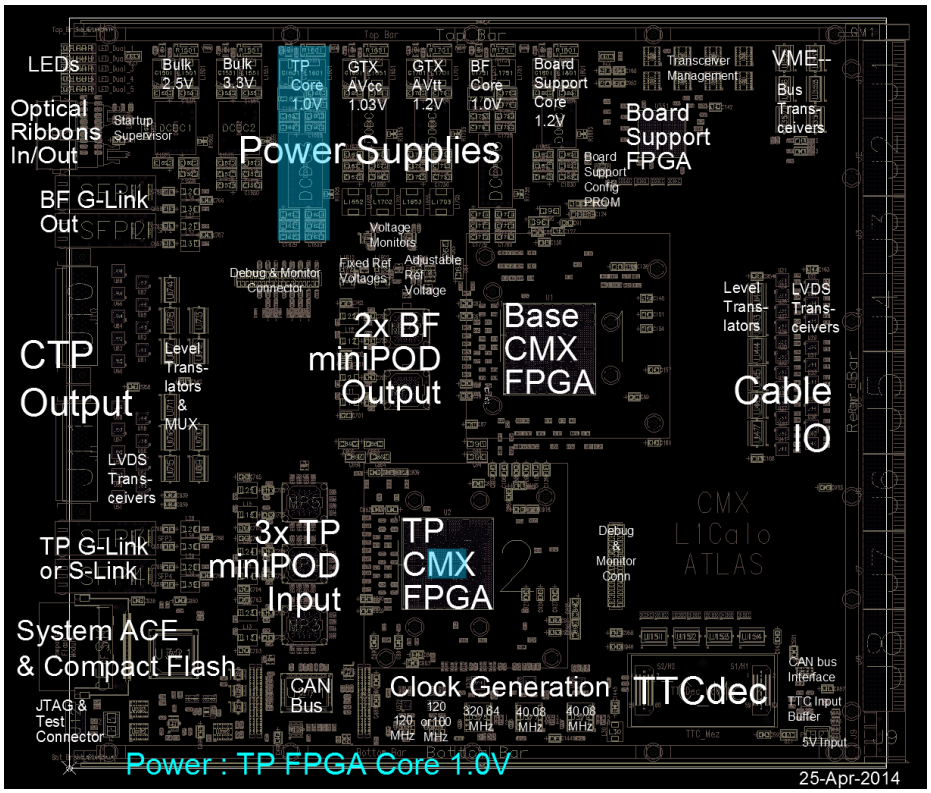


Figure 58: Power: TP FPGA Core 1.0V

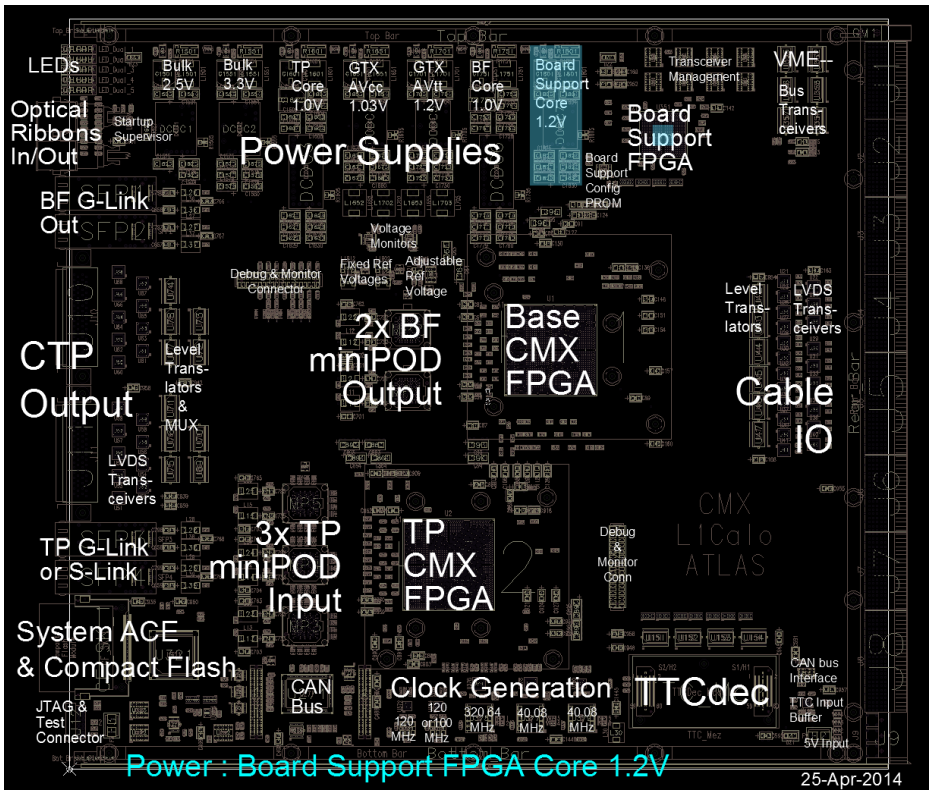


Figure 59: Power: Board Support FPGA Core 1.2V

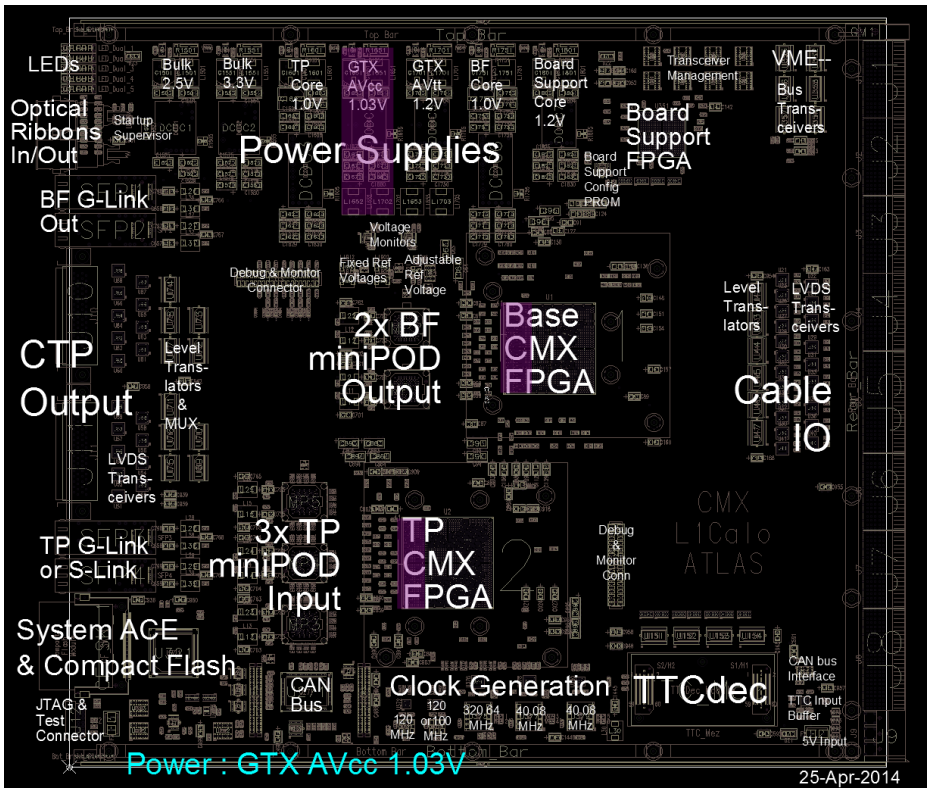


Figure 60: Power: GTX AVcc 1.03V

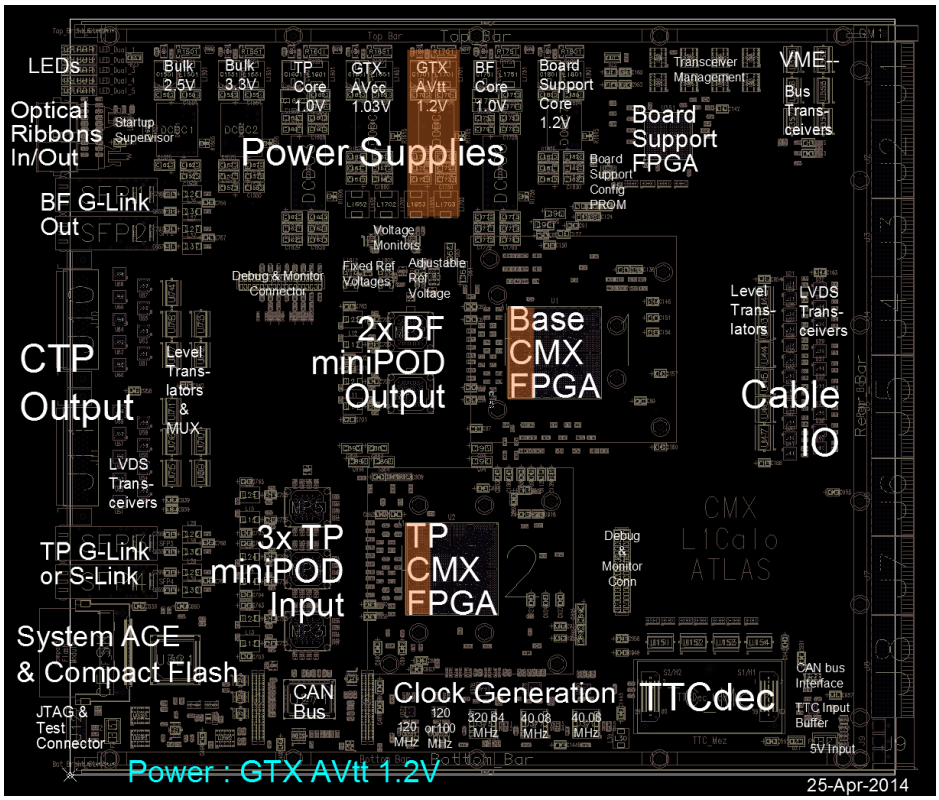


Figure 61: Power: GTX AVtt 1.2V

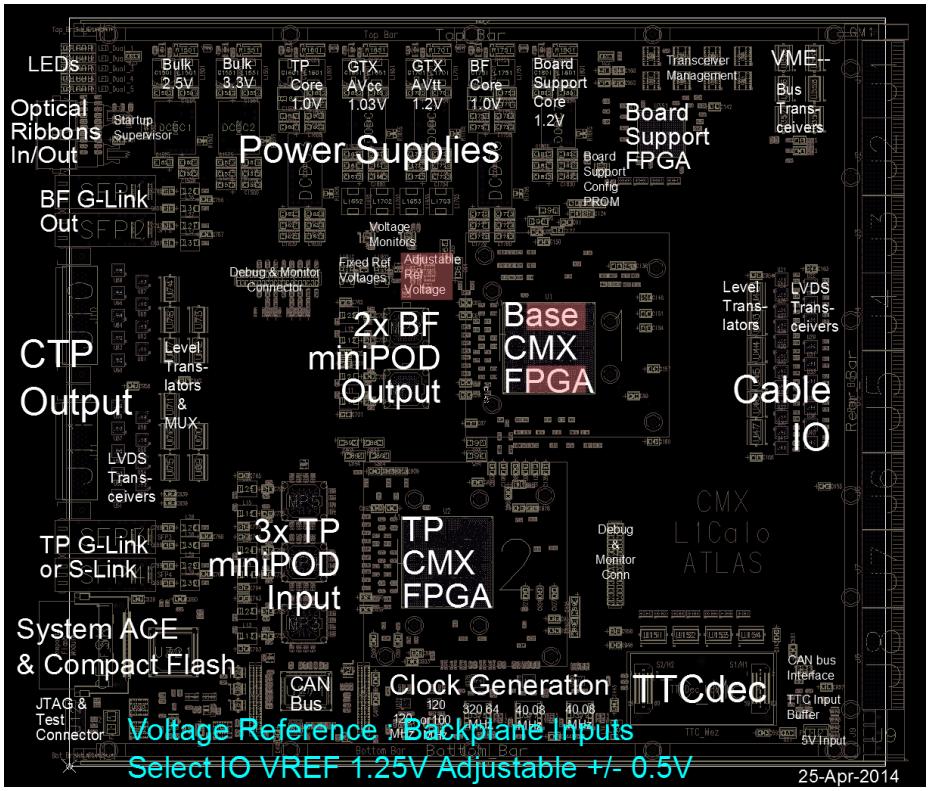


Figure 62: Select IO VREF 1.25V Adjustable Reference Voltage

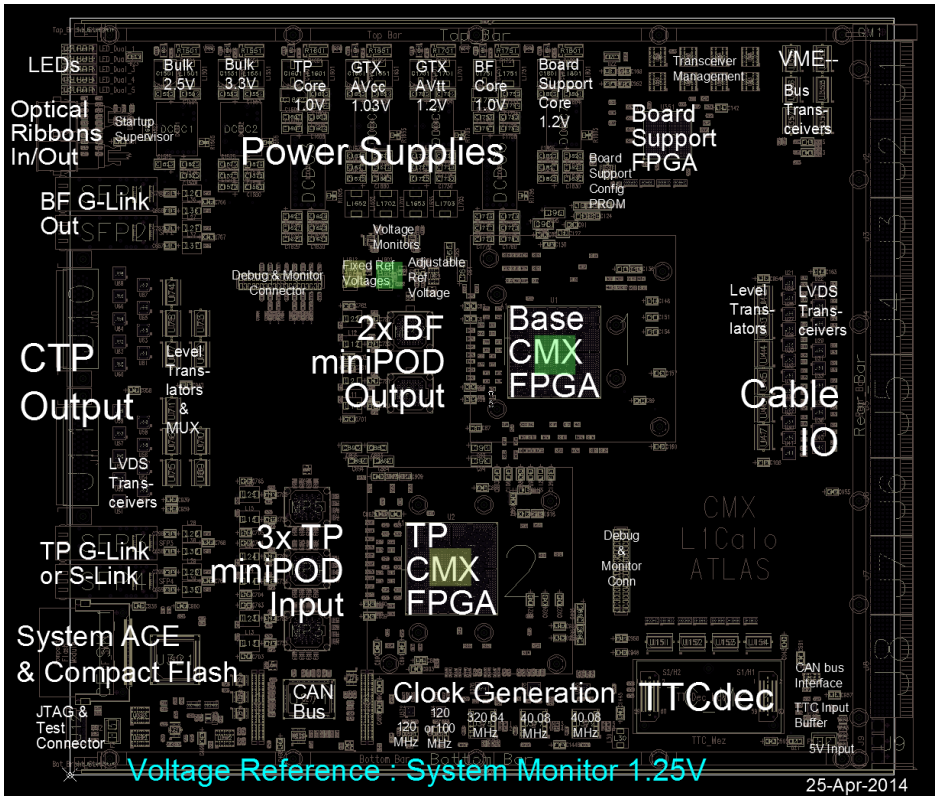


Figure 63: System Monitor 1.25V Reference Voltage

A current snapshot of all the power usage diagrams is included above while the source material for these diagrams is in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/block_diagrams/

Appendix P: CMX card layers

A current snapshot of the detailed description is included below while the source material is in cmx_ab_routing_layer_strategy.txt found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
                  CMX  Routing Layer Strategy
                 ------------------------------


                                        Current Rev.  25-April-2014


This file describes the pcb layer strategy that is used on
the circuit board for the CMX.

-------------------------------------------------------------


Notes added on 10-Jan-2014

Some details of this file have not been kept up to date and
this whole topic has grown rather complicated.

 - I'm not going to touch anything in this file below this
   entry.  Warning some stuff below here may have changed.

 - Recall different people mean different things by "layer"
   e.g.  Mentor Logical Layer,  PCB Physical Stackup Layer,
   Artwork File Number,  Signal Routing Layers Only Numbering,

 - Recall that there were  three  major "layer" changes near
   the end of the design work on CMX:

   1. We moved Mentor Signal Layer 8   which is all Area Fills
      to be Physically in the Stackup just under the Ground
      Plane that is immediately under the other Area Fill
      layers for power distribution.  This was about 23-Aug-2013.

   2. The pcb house changed their mind and wanted the blind
      vias to go 1-6 instead of the originally planned 1-5.
      This required pads for these vias on stackup layer 6
      which is a ground plane.  This required a special 4th
      type of ground plane.  Adding this 4th new special
      ground plane was done at the end of the Default Artwork
      Order "geometry".   To keep a rational order/numbering
      of the ArtWork files, they were renumbered,  after they
      were generated.  Specifically:
        The new 4th Ground Plane was re-numbered ArtWork_14
        The existing ArtWork files 14:22 had their numbers
          incremented to become 15:23.
      The ArtWork files were only renumbers in the
      /Release_4_Final/  directory and in  /for_production/
```

on the web. The ArtWork files were not renumbered
in the /pcb/mfg/ directory where they were generated.
This work was done about 25-Oct-2013 to 4-Nov-2013.

3. The pcb house had trouble balancing the 1-6 sub-stack
with the rest of the card when trying to make controlled
impedance traces on stackup layer 7. Instead we will
have these controlled impedance traces on stackup
layer 18. This involves just:
Use the file cmx_artwork_4 for stackup Layer 18
Use the file cmx_artwork_10 for stackup Layer 7
This was done about 26-Nov-2013

- The description of the CMX stackup and the ArtWork files
shown for the various Physical Stackup Layers in the
cmx_pcb_description.txt file in /for_manufacturing/
on the web and in /Release_4_final/ on moto are correct.

- The actual PCB stackup that is used to manufacture the
bare CMX PCBs is given in:

http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/manufacturing/

for_production/cmx_stackup_fr4_14jan2014.pdf

Modification on 23-Aug-2013

- In the actual pcb stackup, the Mentor design layer Signal_8
i.e. an all Area Fill layer, has been moved so that it is
just below the center power distribution layers for
Bulk_2v5 and Bulk_3V3.

Below Signal_8, Signals 6, 7, 9, and 10 will follow in order.

New PCB Stackup

PCB Stackup Layer	Mentor Logical Design Layer
1	Signal_1
2	Ground Plane - Upper Type
3	Signal_2
4	Ground Plane - Upper Type
5	Signal_3
6	Ground Plane - Specific L6 Type

```
       7        Signal_4

       8        Ground Plane - Upper Type

       9        Signal_5

      10        Ground Plane - Middle Type

      11        Signal_11: Bulk_2V5, GTX_AVTT, and other Fills

      12        Signal_12: Bulk_3V3, GTX_AVCC, BF_Core, and other Fills

      13        Ground Plane - Middle Type

      14        Signal_8: BF VREF_P, TP_CORE, and other Fills

      15        Ground Plane - Middle Type

      16        Signal_6

      17        Ground Plane - Middle Type

      18        Signal_7

      19        Ground Plane - Middle Type

      20        Signal_9

      21        Ground Plane - Lowest Type

      22        Signal_10
```

- In all Area Fills there is relief around all GTX type blind vias and component pins.

- In all Area Fills these is no relief for any non-GTX type blind vias or pins.

- Upper and L6 type ground planes provide relief around all types of blind vias and component pins.

- Middle type ground planes provide relief around only GTX type blind vias and pins. There is no relief around non-GTX type blind vias and pins.

- Lowest type ground planes do not provide relief around any type of blind vias or pins.

CMX Layer Strategy:

The word Layer means various things:

- Physical layers in the actual pcb
- Mentor design Logical layers
- Thinking about just the Signal Trace layers
- Recall that a Physical Layer may be used for example as a signal trace layer in one part of the CMX card and as a power plane in another area of the card.

The design of the 400 backplane inputs and the backplane LVDS signals thinks in terms of "Signal Layers" (not in terms of Physical layers.

- There are 10 signal layers used in the CMX design.
- Signal layer number 1 is the top surface of the card. Signal layer number 10 is the bottom surface of the card.
- Some of the 10 signal layers can have 65 Ohm traces and some can not reach above 50 Ohm Zo.
- In our technical slang the 65 Ohm layers are called the "privileged layers".

Use of the 10 Signal Layers in the 400 Backplane Processor Input to Base Function FPGA connections.

Full Run --> Continuous traces on this layer the whole way from the backplane connector to the BF FPGA pin.

Main Run --> Continuous traces on this layer from the backplane connector to the via array near the BF FPGA.

Last Inch --> Continuous traces on this layer from the via array near the BF FPGA to a BF FPGA pin.

Signal Layer	Use in the 400 Backplane Inputs Connecting to BF-FPGA	Trace Zo
1	Last Inch only CMX Top Physical Layer	
2	Full Run, Main Run or Last Inch	65
3	Full Run, Main Run or Last Inch	65
4	Full Run, Main Run or Last Inch	65

5	Full Run, Main Run or Last Inch	65
6	Last Inch only	50
7	Last Inch only	50
8	24 V_Ref, 8 DCI, 0-2 Last Inch	50
9	Full Run for 14 of the 16 Clks & Full Run or Last Inch for some normal signals	65
10	none CMX Bottom Physical Layer	

Use of the 10 Signal Layers in the Backplane LVDS Cable IO connections to the Base Function.

Conn-TX --> Traces on this layer from the backplane connector to the LVDS<-->3V3CMOS transceiver

Transl-FPGA --> Traces on this layer from the 3V3CMOS<--<2V5CMOS translator to the BF FPGA.

Signal Layer	Use in the Backplane LVDS Cable IO Connection to the BF-FPGA	Trace Zo
1	i.e. CMX Top Physical Layer Transceiver <--> Translator and the last ~2mm to pads for these parts and the ~1/2mm to pads under the BF FPGA	
2	Conn-TX and Transl-FPGA	50
3	Conn-TX and Transl-FPGA	50
4	Conn-TX and Transl-FPGA	50
5	Conn-TX and Transl-FPGA	50
6	Conn-TX for the 3 "extra pairs"	50
7	- none -	
8	- none -	
9	Conn-TX and Transl-FPGA	50
10	i.e. CMX Bottom Physical Layer - none -	

Use of Signal Layers #6, #7, #8 in the area between the Base Function FPGA and the Backplane Connectors:

- Signal Layers #6, #7 will carry the vertical mat of traces that involve many non principal signal flow

signals (OCB, TTCdec, debug connector signals,
BF to TP S-link back channel, one fabric clock)
and the horizontal mat of traces in the nearby region
south of the BF FPGA that involve the signals
to the front panel LVDS CTP connectors.

- Signal Layers #8 is so far still unallocated except near the BF FPGA for a VREF plane area fill and for the DCI control resistors to the IO banks used with the 400 backplane inputs.

Physical Layer Rules:

- Follow exactly the GTX layer rules.

- All power planes must have an immediately adjacent ground plane on at least one side.

Common Sense:

- Ground planes should be contiguous Physical Layers.

Physical Layer Design:

There are 22 Physical Layers in the CMX circuit board.

Stackup Layer	High Speed Ser IO FPGA and Optic TX	Rest of BF FPGA	PB 400 & LVDS & TX and Translate
1	50 Ohm Microstrip	Signal Layer #1	Signal Layer #1
2	Ground Plane	Ground Plane	Ground Plane
3	50 Ohm Stripline	Signal Layer #2	Signal Layer #2
4	Ground Plane	Ground Plane	Ground Plane
5	50 Ohm Stripline	Signal Layer #3	Signal Layer #3
6	Ground Plane	Ground Plane	Ground Plane
7	Diff FPGA Clocks	Signal Layer #4	Signal Layer #4
8	Ground Plane	Ground Plane	Ground Plane
9	Diff FPGA Clocks	Signal Layer #5	Signal Layer #5
10	Ground Plane	Ground Plane	Ground Plane
11	AVTT Fill	Bulk_2V5 Fill	Bulk_2V5 Fill
12	AVCC Fill	BF_Core Fill	Bulk_3V3 Fill
13	Ground Plane	Ground Plane	Ground Plane
14		Signal Layer #6	Signal Layer #6
15	Ground Plane	Ground Plane	Ground Plane
16		Signal Layer #7	Signal Layer #7
17	Ground Plane	Ground Plane	Ground Plane
18		Fill Sig Layer #8	Signal Layer #8
19	Ground Plane	Ground Plane	Ground Plane
20		Signal Layer #9	Signal Layer #9
21	Ground Plane	Ground Plane	Ground Plane
22		Signal Layer #10	Signal Layer #10

- The non high speed serial IO area under the TP FPGA is like the non high speed serial IO area under the BF FPGA except that it uses Physical Layer 12 for the TP_Core fill.

- The area under the Board Support FPGA needs: Bulk_3V3, Bulk_2V5, and BSPT_Core 1.2V power.

- The area under the 12 channel high speed optical parts needs Filtered 2.5V and 3.3V power. Each supply is filtered by a capacitor to Gnd, a series inductor, and a final capacitor to Gnd at the component power pin.

- The area under the low speed SFP optical parts needs to have filtered 3.3V supplies, a separate filtered 3.3V supply for that SFP packages transmitter and for its receiver. Each supply is filtered by a capacitor to Gnd, a series inductor, and a final capacitor to Gnd at the component power pin.

- These are all 1/2 oz copper layers except for the main power planes on layers 11 and 12 which are 1 oz. 1/2 oz copper is about 1 mOhm per square. The tolerance on the Virtex Core supply is 50 mV. The tolerance on the 12 channel optical part is 30 mV. The final design may require power fills on multiple layers.

From the Mentor System:

Setup on 12-Apr-2013

Mentor Physical & Signal			Philippe's CMX Signal	CMX PCB Physical Stack Up
PHYSICAL_1	SIGNAL_1	PAD_1	<-- CMX Signal 1	- Physical 1
PHYSICAL_2	SIGNAL_2		<-- CMX Signal 2	- Physical 3
PHYSICAL_3	SIGNAL_3		<-- CMX Signal 3	- Physical 5
PHYSICAL_4	SIGNAL_4		<-- CMX Signal 4	- Physical 7
PHYSICAL_5	SIGNAL_5		<-- CMX Signal 5	- Physical 9
PHYSICAL_6	SIGNAL_6		<-- CMX Signal 6	- Physical 14
PHYSICAL_7	SIGNAL_7		<-- CMX Signal 7	- Physical 16
PHYSICAL_8	SIGNAL_8		<-- CMX Signal 8	- Physical 18
PHYSICAL_9	SIGNAL_9		<-- CMX Signal 9	- Physical 20
PHYSICAL_10	POWER_1		<-- Ground on PCB Physical: 2, 4, 6, 8, 10 13, 15, 17, 19, 21	
PHYSICAL_11	SIGNAL_11		<-- Area Fill on PCB Physical: 11	
PHYSICAL_12	SIGNAL_12		<-- Area Fill on PCB Physical: 12	
PHYSICAL_13	SIGNAL_10	PAD_2	<-- Phlp Signal 10 - PCB Physical 22	

Notes During Routing About What Is On Which Layer:

- In the Backplane Cable LVDS section we need two layers for some general signal traces a North-South layer and a East-West layer. For now I will use:
  signal layer 6 for North-South
  signal layer 7 for East-West

- Under the Base Function FPGA there are a couple of choices about how to best use the 3 layers that are assigned for Area Fills. Under the Base Function FPGA these 3 layers must contain the area fills for the following supplies:

  BULK_2V5, BF_CORE, BF_GTX_AVCC, BF_GTX_AVTT, and VREF_P

  Recall that over most of the CMX pcb that BULK_2V5 is on layer 11 and that BULK_3v3 is on Layer 12.

  We do not need BULK_3V3 under the Base Function FPGA. We plan it use its layer 12 for the BF_CORE supply.

  11 West of 219mm must be AVTT - East of 223mm must be Bulk_2V5

  12 West of 221mm must be AVCC - East of 225mm must be BF_CORE

  8 signal routing traces - East of 226mm must be VREF_P

  BF_CORE must go on the pcb physical layer that is normally used for BULK_3V3 in most places on the card.

  If 3 pcb physical layers are going to be used then a rational setup is:

  11 - - - - - - - - - - - - Bulk_2V5 - - - - - - - - - - - - -

  12 West of 219mm must be AVTT - East of 225mm must be BF_CORE

  8 West of 221mm must be AVCC - East of 226mm must be VREF_P

Appendix Q: Virtex System Monitor

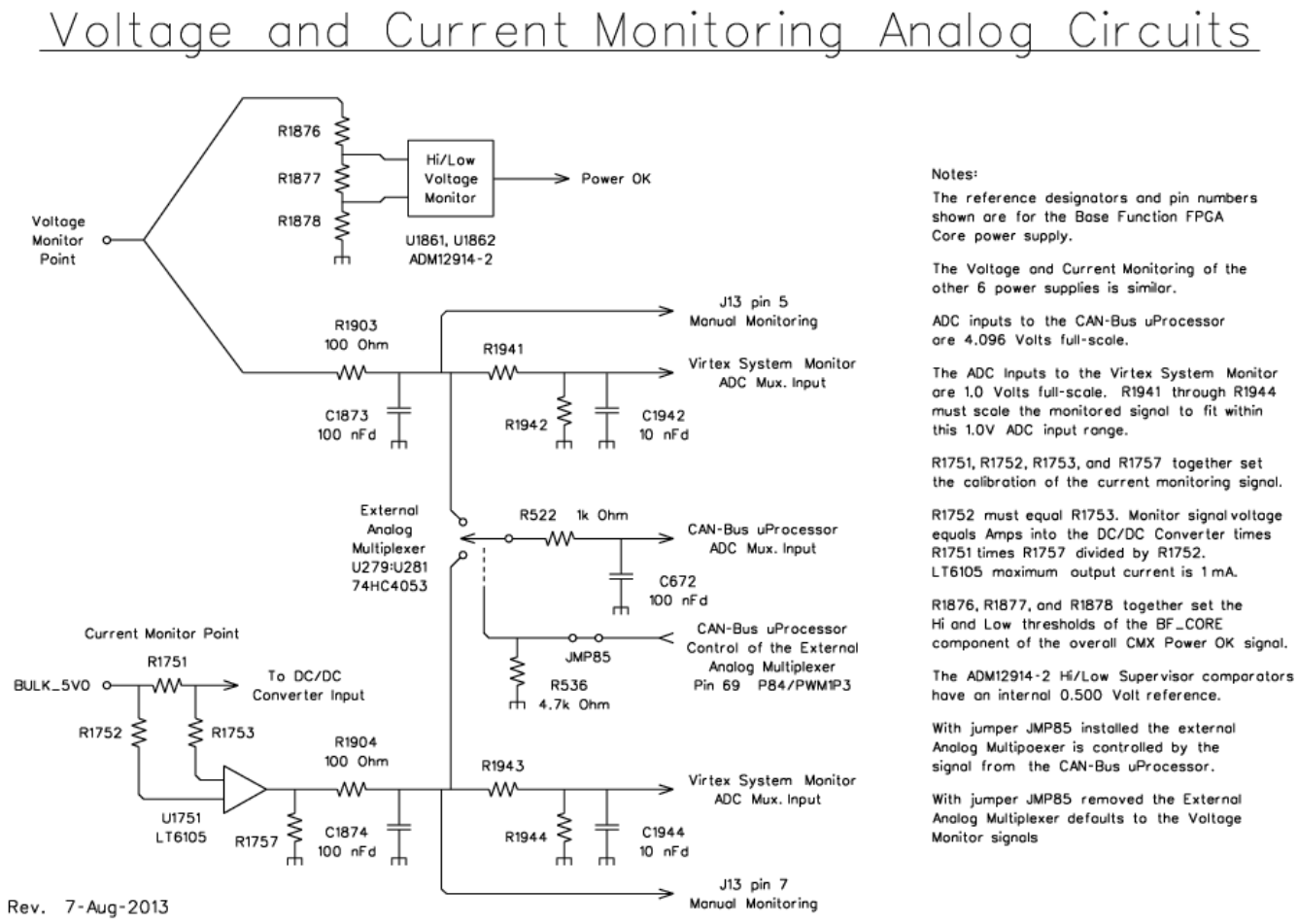


Figure 64: Circuit Diagram for Voltage and Current Monitoring

A current snapshot of the circuit diagrams is included above while the source material is in 35_voltage_and_current_monitor_analog.pdf found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot of the detailed description is included below while the source material is in cmx_ab_virtex_system_monitor.txt found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

CMX BF FPGA Virtex System Monitor

Original Rev. 30-Dec-2013
Current Rev. 27-Apr-2014

This file describes the use of the Virtex System Monitor function in the Base Function and TP FPGAs on the CMX circuit board.

A drawing of the reference supplies for the Virtex System Monitors and a general view of the inputs to the Base Function Virtex System Monitor are shown in the circuit diagrams:

06_reference_supplies.pdf
35_voltage_and_current_monitor_analog.pdf

The Xilinx documentation about the Virtex-6 System Monitor is available on the MSU CMX web site in the file:

virtex_6_system_monitor_ug370_v1_1.pdf

As shown in figure 24 on page 46 of the Xilinx document listed above, the +2.5V AVDD power and the AVSS ground connection to the System Monitors on the CMX card are made through LC filter components as shown in the circuit diagram:

06_reference_supplies.pdf.

Components: L1901, L1902, C1902, C1903, and C1906 together provide the LC filtering on the power and ground connections to the Base Function FPGA Virtex System Monitor. The traces for the FPGA AVDD and AVSS pins run from this LC filter and then under the FPGA on design layer Signal_7. Similar LC components provide the AVDD power and AVSS ground connections to the System Monitor in the Topological FPGA.

The 1.250 Volt reference supply for the Base Function System Monitor is generated by IC U1901 starting from filtered power that is provided by the LC components listed above. IC U1901 is a TI Burr-Brown Part No. REF3140AIDBZT which has an initial accuracy of +- 0.2%, a temperature coefficient of 20 ppm/deg C, and a long term drift of 70 ppm. The 1.250 Volt reference is bypassed by C1905 and then VREFP and VREFN traces are run under the BF FPGA on design layer Signal_7.

The direct inputs to the Base Function System Monitor VP and VN pins are not used on the CMX card - rather 12 of the 16 available auxiliary System Monitor input pin pairs are used on the BF FPGA. Neither the direct or auxiliary System Monitor inputs are used on the Topological Processor FPGA.

In all uses on the CMX card the external inputs to the System

Monitor are setup for unipolar ADC operation, that is the VAUXN(x) analog input pin is tied to ground via a differentially routed trace pair. The quantity to be measured is always positive wrt ground and is tied to the VAUXP(x) analog input pin through a voltage divider and/or an isolation current limiting resistor. All circuits include a 10 nFd anti-alias filter capacitor across the VAUXP(x) VAUXN(x) pin pair.

In its basic form the ADC in the Virtex-6 System Monitor is a 10 bit device with a 1.000 Volt full scale input. Thus the basic calibration of this ADC is 0.9775 mV per LSB.

The following connections have been made to the Auxiliary analog inputs to the Base Function FPGA System Monitor on the CMX circuit board:

Base Func FPGA System Monitor Auxiliary Input	Power Bus Voltage or Current Monitored by this Input
SYSMON_00	input not used for monitoring
SYSMON_01	GTX_AVTT Voltage
SYSMON_02	input not used for monitoring
SYSMON_03	BF_CORE Current
SYSMON_04	BF_CORE Voltage
SYSMON_05	input not used for monitoring
SYSMON_06	input not used for monitoring
SYSMON_07	GTX_AVTT Current
SYSMON_08	GTX_AVCC Current
SYSMON_09	BULK_2V5 Voltage
SYSMON_10	BULK_3V3 Current
SYSMON_11	GTX_AVCC Voltage
SYSMON_12	BULK_3V3 Voltage
SYSMON_13	BULK_2V5 Current
SYSMON_14	TP_CORE Current
SYSMON_15	VREF_P Voltage Select I/O Ref

This mapping of System Monitor inputs to the quantities to be measured is forced by routing constraints.

The calibration of these various external inputs to the BF System Monitor, based on the resistor values specified in CMX Final Assembly document. As of December 2013 the following scale factors are in use:

Refer Desig	Value	Monitored Quantity	Gain	SysMon Input	LSB Scale
R1941	100k Ohm	BF_Core V	0.50	4	1.955 mV
R1942	100k Ohm				
R1943	100k Ohm	BF_Core I	0.50	3	9.775 mA
R1944	100k Ohm				
R1945	100k Ohm	GTX_AVTT V	0.50	1	1.955 mV
R1946	100k Ohm				

R1947	100k Ohm	GTX_AVTT I	0.50	7	4.888 mA
R1948	100k Ohm				
R1949	100k Ohm	GTX_AVCC V	0.50	11	1.955 mV
R1950	100k Ohm				
R1951	100k Ohm	GTX_AVCC I	0.50	8	4.888 mA
R1952	100k Ohm				
R1953	100k Ohm	TP_Core I	0.50	14	9.775 mA
R1954	100k Ohm				
R1955	300k Ohm	BULK_3V3 V	0.25	12	3.910 mV
R1956	100k Ohm				
R1957	100k Ohm	BULK_3V3 I	0.50	10	9.775 mA
R1958	100k Ohm				
R1959	300k Ohm	BULK_2V5 V	0.25	9	3.910 mV
R1960	100k Ohm				
R1961	100k Ohm	BULK_2V5 I	0.50	13	9.775 mA
R1962	100k Ohm				
R1963	100k Ohm	Select I/O	0.50	15	1.955 mV
R1964	100k Ohm	VRef_P V			

This LSB Scale is based on assuming that the System Monitor ADC has a 1 Volt Full Scale Input and will be used to produce 10 bit outputs, i.e. the LBS of the raw converter is about 1 Volt / 1023 = 0.9775 mV per LSB.

The one, currently unused, dedicated VP VN analog input pin pair to the Virtex System Monitor has an input current specification of 1 uAmp.

The auxiliary analog inputs to the Virtex System Monitor, i.e. the VAUXP(x) VAUXN(x) pin pairs, have a maximum input current specification of 10 uAmps. This could be a problem working with the 50k Ohm source impedance of the voltage dividers as currently defined in the Final Assembly document. This source impedance can be lowered by a factor of 10 if this proves to be a problem.

Appendix R: Hardware Oversight Logic

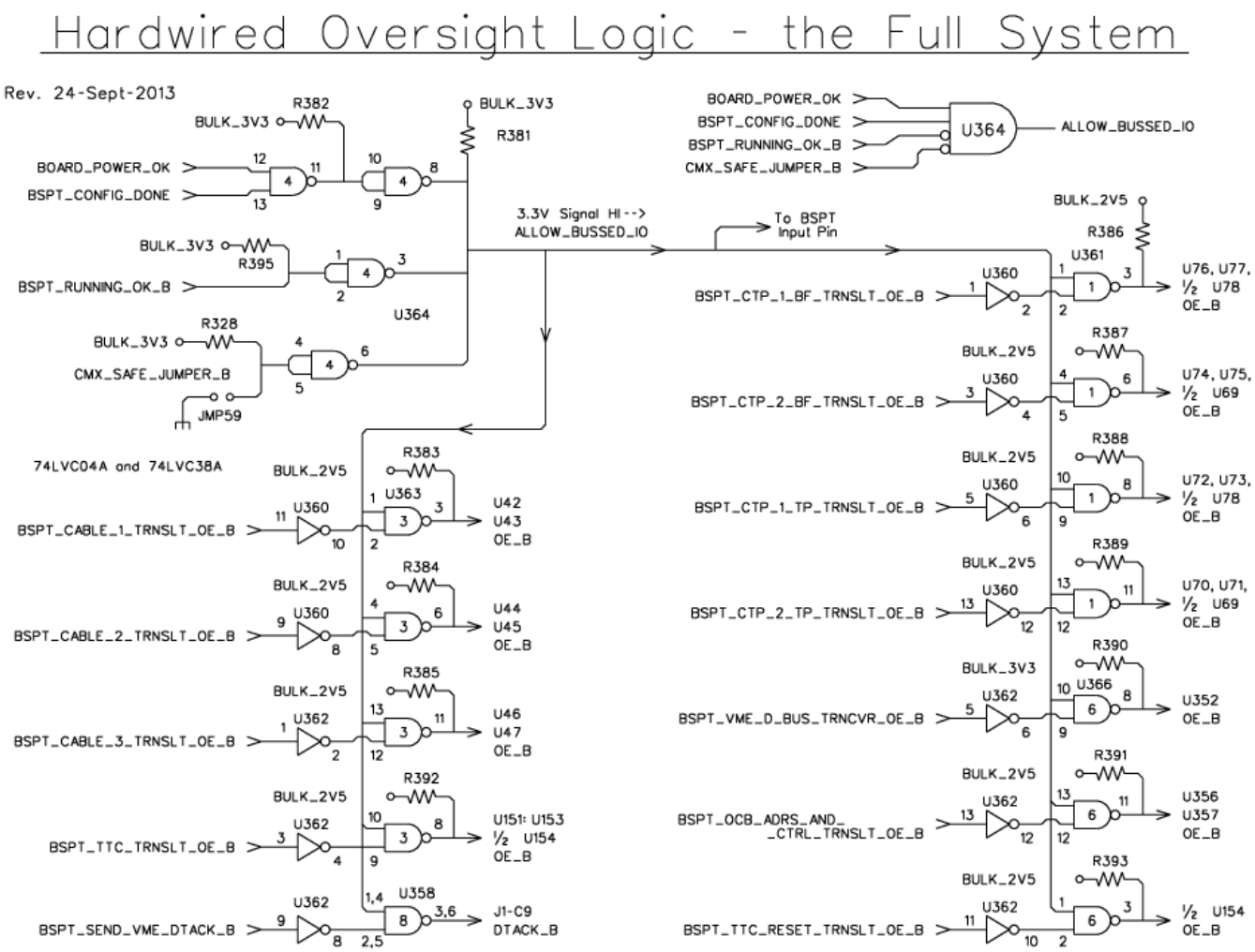


Figure 65: Overall Diagram for Hardware Oversight Logic

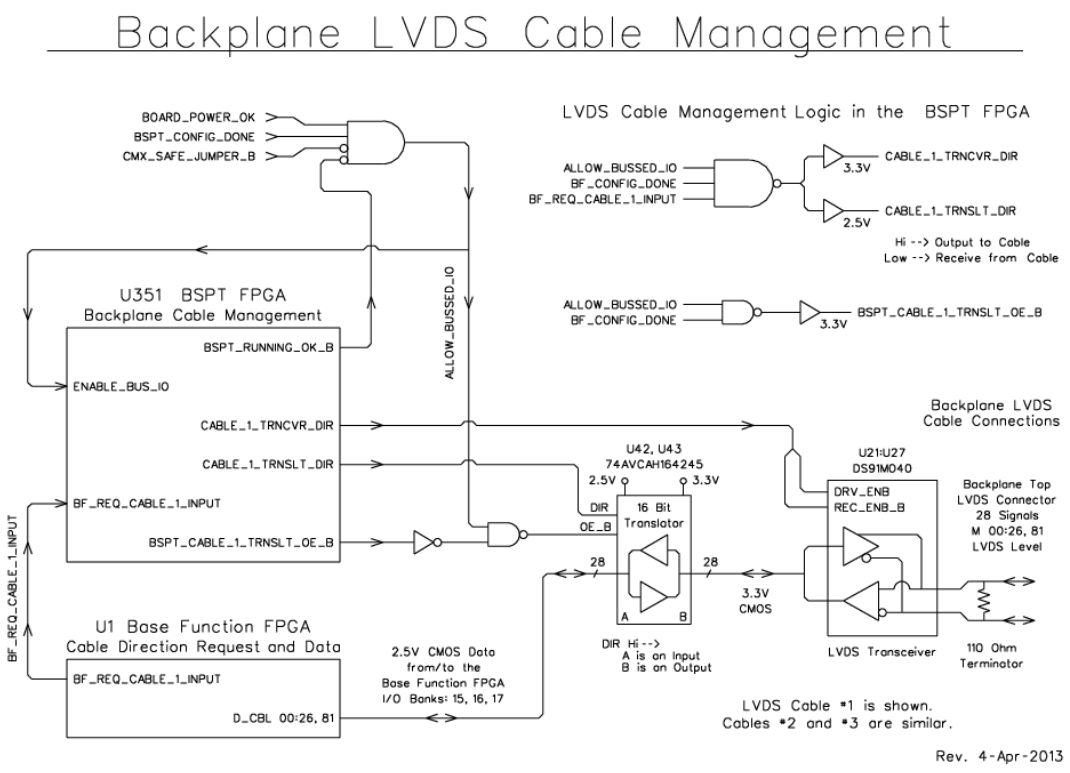


Figure 66: Circuit Diagram for Backplane LVDS Merger Cable Management

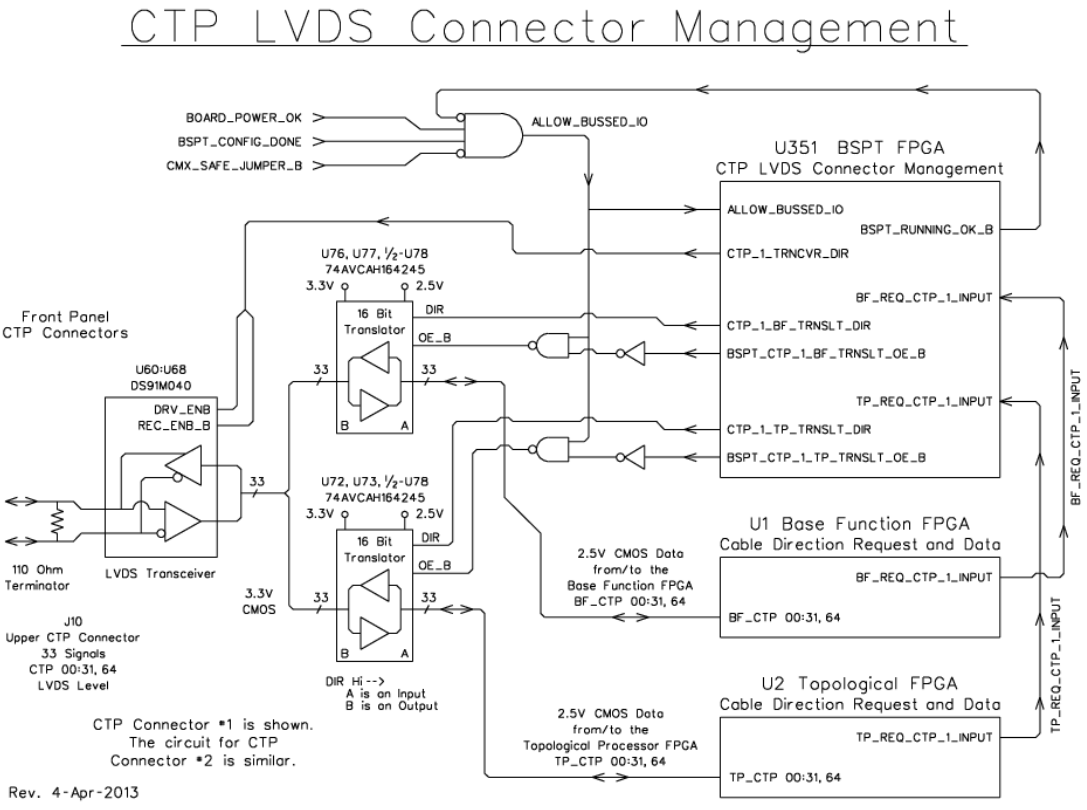


Figure 67: Circuit Diagram for CTP LVDS Connector Management

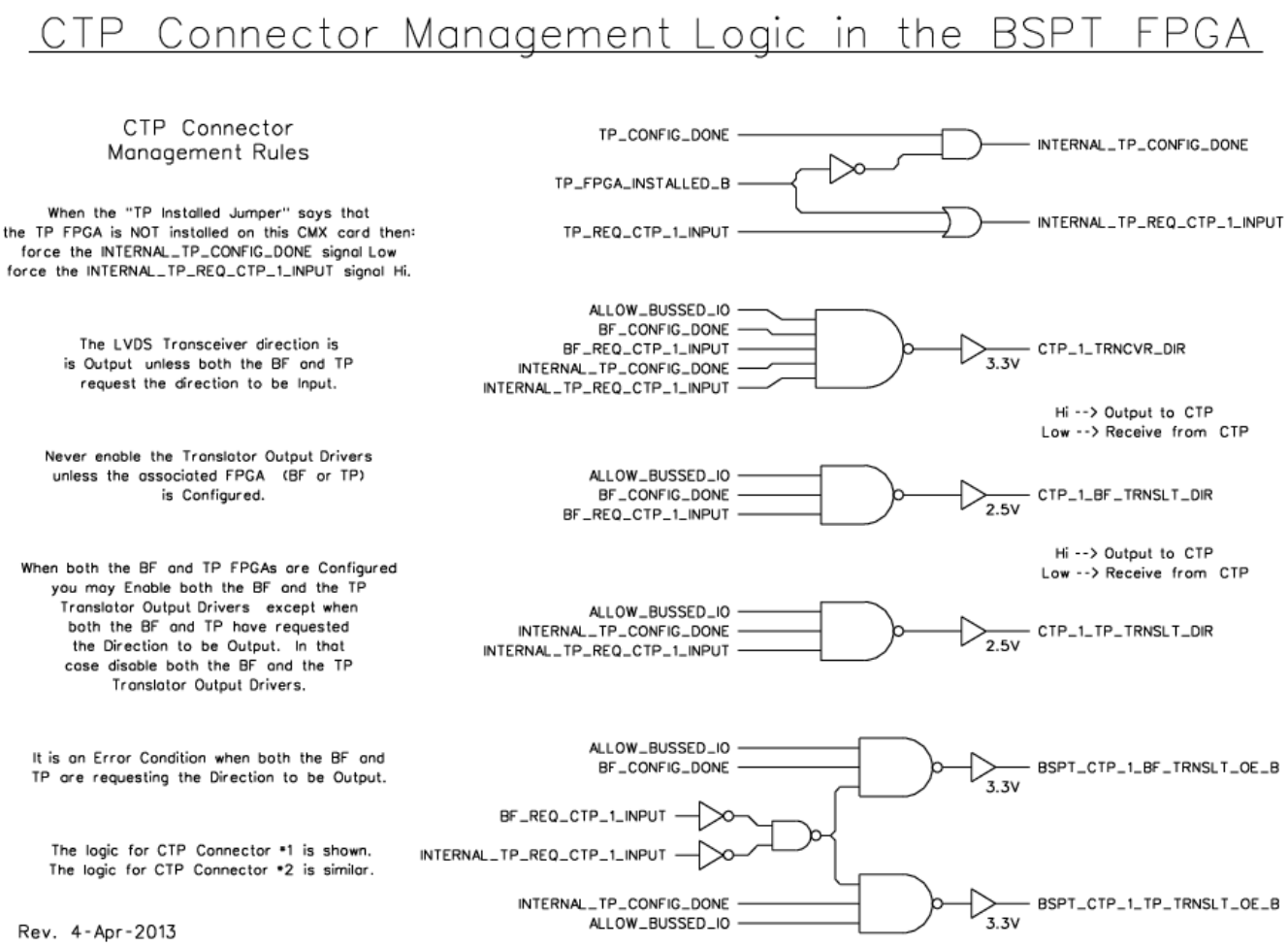


Figure 68: Circuit Diagram for CTP Management Logic in the BSPT FPGA

A current snapshot of the circuit diagrams is included above while the source material is in

- 24_hardwired_oversight_logic.pdf
- 21_backplane_cable_management.pdf
- 22_ctp_connector_management.pdf
- 23_ctp_connector_bstp_logic.pdf

found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

The details of the Hardware Oversight Logic are described in:

- Appendix D: LVDS Connections
- Appendix I: VME-- and On-Card Bus

Appendix S: Front Panel LEDs

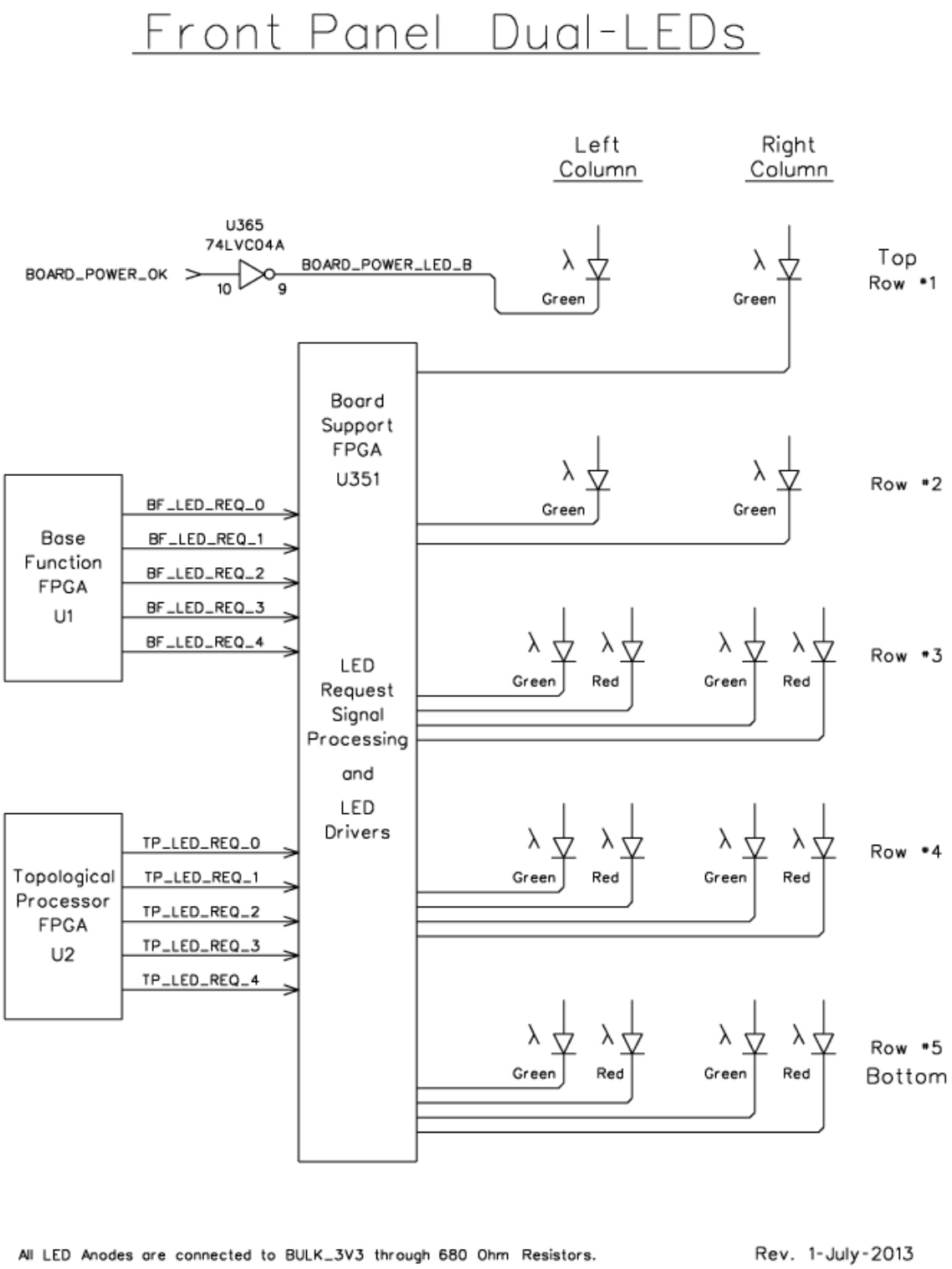


Figure 69: Circuit Diagram for Front-Panel LEDs

A current snapshot of the circuit diagrams is included above while the source material is in 30_front_panel_leds.pdf found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot of the detailed description is included below while the source material is in cmx_ab_leds_on_front_panel.txt found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
              CMX  LEDs  on the Front Panel
            ---------------------------------

                                  Original Rev. 18-Feb-2013
                                   Current Rev. 27-Apr-2014


The large number of front panel connectors on the CMX card
leaves space for only 5 Dual LED components.  This is less
than the 24 LEDs on the CMM card.  A circuit diagram showing
the CMX card's front panel LEDs is available:

  30_front_panel_leds.pdf


The 5 Dual LED components used on the CMX card are bi-color
Red/Green LEDs, Dialight Part No 592-3030-313F.  These LED
components are referred to in the CMX documentation as number
1 through 5  (top to bottom)  and  Left/Right as viewed from
the Front Panel.

One of these 10 bi-color LEDs,  Number 1 Left,  is hardwired
to illuminate Green when the CMX BOARD_POWER_OK signal is
asserted.

The other 9 bi-color LEDs are all controlled by Select I/O
pins on the BSPT FPGA.

   3 of these bi-color LEDs,  Number 1 Right, and Number 2
   Left and Right can only have their Green LED illuminated
   under control of the BSPT FPGA.

   6 of these bi-color LEDs,  Numbers 3, 4, 5  Left and
   Right can have either their Red or Green LED illuminated
   under control of the BSPT FPGA.


The Cathodes of the LEDs that are controlled by the BSPT FPGA
are tied to Select I/O pins in the 3.3 Volt I/O Bank #3 of
the BSPT FPGA.  Thus the FPGA I/O pin must be set Low to cause
the associated LED to illuminate.  Using a Low FPGA output to
cause the LED to illuminate is done  (vs FPGA Hi output to
cause LED to illuminate)  because of the lower resulting
voltage drop in the FPGAs I/O block when its pulling current
to ground.
```

The value of the LED anode resistors installed on the CMX card results in a LED current of about 2 mA which is plenty for this front panel application. In the BSPT FPGA firmware the Drive Level on these LED drive pins should be set high enough so that their output pull down transistors will saturate. These FPGA outputs should be setup as Open-Drain to eliminate potential noise generation from a fast turn OFF transition. To minimize noise, the FPGA I/O Blocks driving the front panel LEDs should have a slow output signal speed.

Both the Red and the Green LED in each of these 10 bi-color LEDs has its Anode pulled up to the BULK_3V3 rail by a 680 Ohm resistor. These resistors are reference designators R271 through R290. They are located near the front panel just under the LEDs on the top side of the circuit board. The high speed MTP fiber optic cables will run over these resistors.

Although all 9 of the FPGA controlled LEDs are driven by the BSPT FPGA, traces have been provided on the CMX card to carry LED Control Signals from the Base Function FPGA and from the Topological FPGA to the BSPT FPGA. These are 2.5V signals which are defined to be Hi when the BF or TP "Requests" that the associated LED be illuminated. The net names of these LED Control signals are: BF_LED_REQ_0 ,..., BF_LED_REQ_4 and TP_LED_REQ_0 ,..., TP_LED_REQ_4. The mapping of which Front Panel LED is illuminated in response to one of these LED control signals is contained in the BSPT firmware.

The CMM card used 74123 one-shots to "stretch" LED drive signals that otherwise might persist for such a short period of time that one would not see the LED illuminate. This same function, i.e. stretching the LED drive signal so that whenever it goes ON, it will remain ON long enough to be visible to the eye, will be performed on the CMX card with simple logic in the BSPT FPGA. A counter can stretch the LED drive signal to a minimum of 100 msec (or more) to help guarantee that the eye can see it flash ON.

There is not enough space on the CMX Front Panel to provide descriptive labels for each of the 10 LEDs. In any case the meaning of 9 of them is under control of the FPGA firmware. The Board Power OK LED will be labeled. The other 9 LEDs will have labels of the form: 2L ,..., 5L and 1R ,..., 5R.

Some of the potential uses for the Front Panel LEDs on the CMX card (many copied from the CMM card) may include:

- There are 6 LEDs that do not require a control signal from either the BF or TP FPGAs:

  Board_Power_OK
  VME_Access
  All_FPGAs_Are_Configured
  TTCDec_Ready
  CAN-Bus_Active
  L1_Accept
  Status of the Xilinx System-ACE

- There are 5 LED that do require a control signal from either the BF or TP FPGAs:

  FIFO_Full
  FIFO_Empty
  Trigger_Hit
  Parity_Error
  G-Link_Active

Appendix T: Front Panel Access Signals

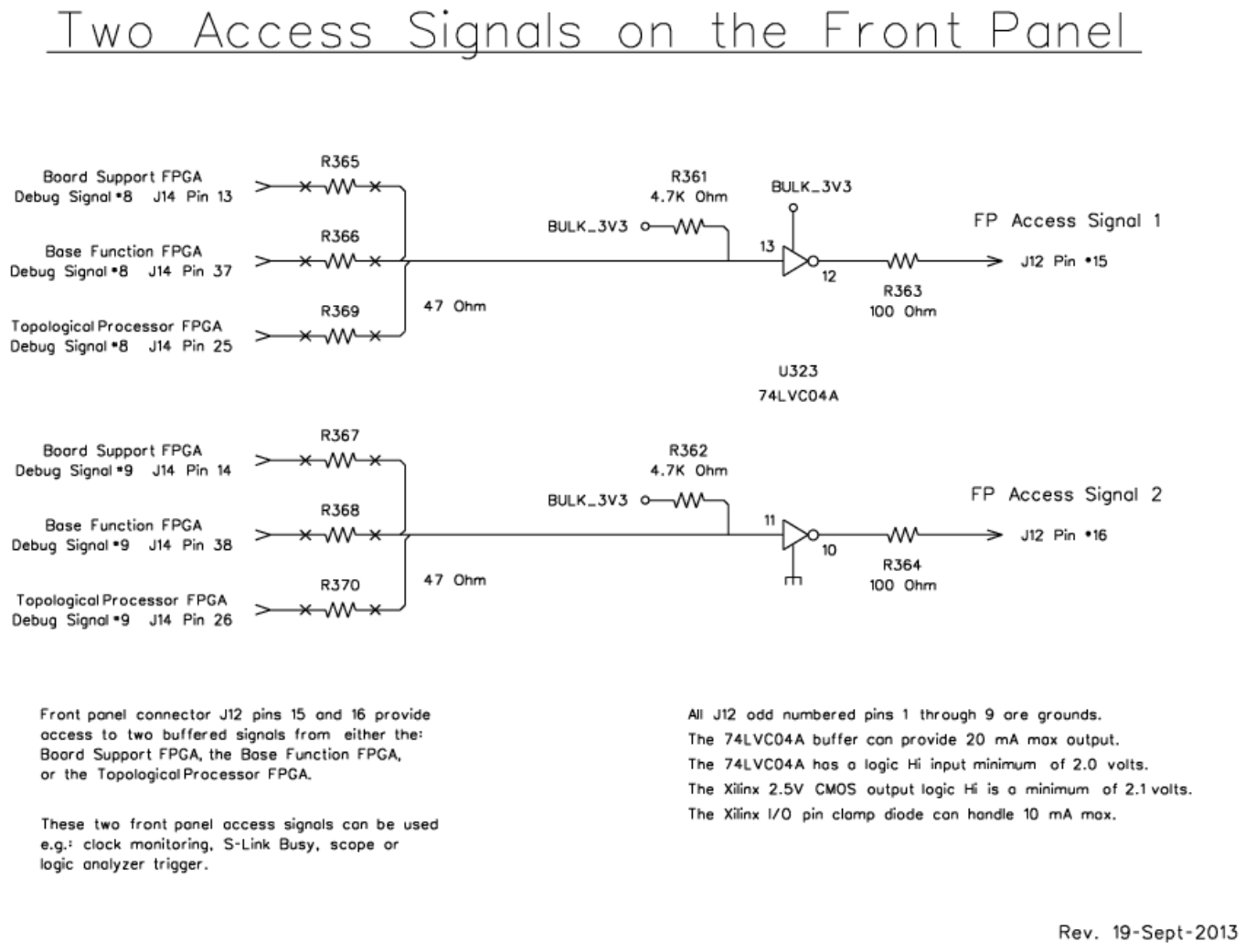


Figure 70: Circuit Diagram for the 2 Access Signals on the Front-Panel

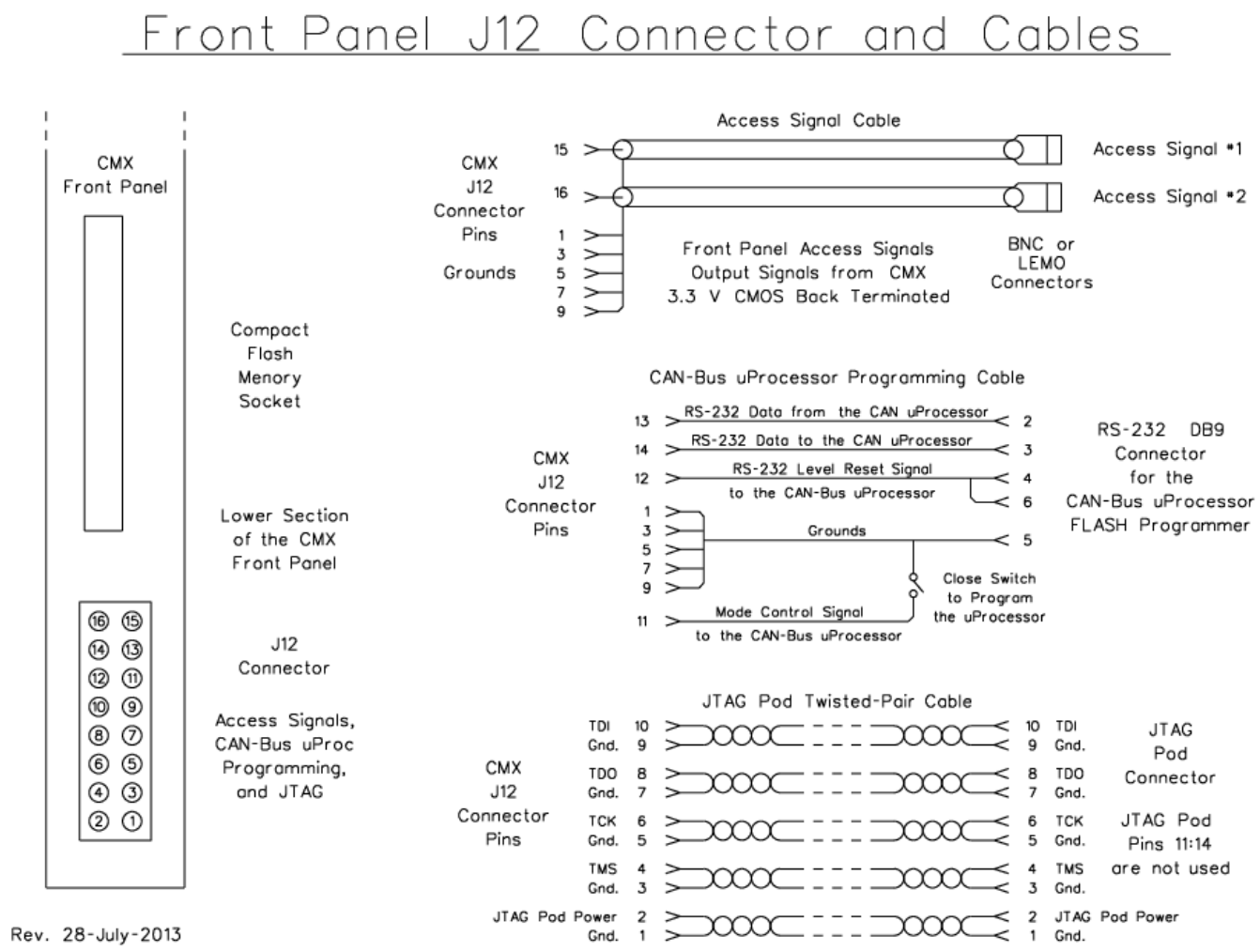


Figure 71: Front-Panel Test Connector Pinout and Cables

A current snapshot of the circuit diagrams is included above while the source material is in

- 29_front_panel_access_signals.pdf
- 34_front_panel_j12_connector_and_cables.pdf

found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

Appendix U: Ground Connections

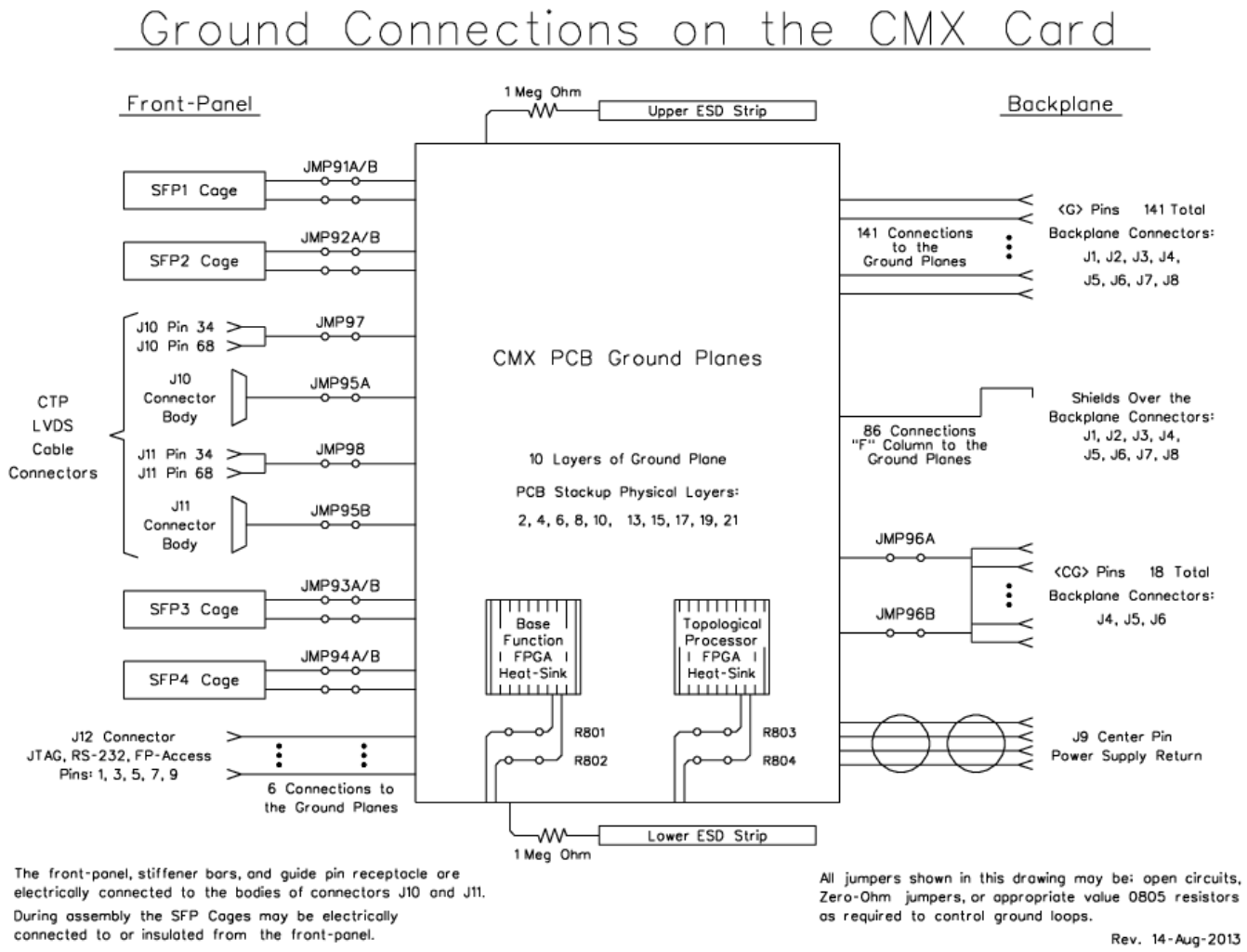


Figure 72: Circuit Diagram for the Ground Connections on the CMX Card

A current snapshot of the circuit diagrams is included above while the source material is in 32_cmx_ground_connections.pdf found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/circuit_diagrams/

A current snapshot of the detailed description is included below while the source material is in cmx_ab_ground_connections.txt found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

CMX Ground Connections

Original Rev. 15-July-2013
Current Rev. 25-April-2013

This file describes the ground connections on the CMX card.

The various ground connections on the CMX circuit board are illustrated in the following circuit diagram drawing on the MSU CMX web site:

32_cmx_ground_connections.pdf

Direct Ground Connections:

The CMX card's Ground net (called GROUND net in the Mentor design) directly connects to:

- All 10 of the ground planes in the CMX pcb itself.
- The 141 Backplane connector <G> Grounds pins, e.g.
  connector J1 pins B1, B3, B5, ... through
  connector J8 pins ..., D24, B25, D25
- The metal shields over the top of the backplane connectors J1 through J8. There are 86 of these shield "F" column pins directly connecting to the CMX ground planes.
- The backplane J9 power connector middle ground pin, i.e. the power supply return pin.
- The front panel connector J12 pins 1,3,5,7, and 9. This front panel connector is for: JTAG, CAN-Bus RS232, and it provides two front panel Access Signals.

Objects Connected to the CMX Card's Ground Planes Via Jumpers or Isolation Resistors:

- The CMX card's front panel is electrically directly connected to the all metal body of the front panel CTP connectors J10 and J11. The metal body of connectors J10 and J11 are connected to the CMX ground planes via jumpers JMP95A and JMP95B. 4.7k Ohm resistors will be installed in these jumper locations.

  The intent is to provide a strong enough ground connection to provide some ESD protection when the card is handled by its front panel and a weak enough ground connection to

prevent ground loops via the front panel's uncertain connection to the crate mechanics.

The stiffener bars and the backplane Guide Pin Receptacle on the CMX card are directly electrically connected to its front panel.

- The ESD Ground Strip at the top and at the bottom of the CMX card is tied to its ground planes via 1 Meg Ohm resistors R631 and R632.

- Each of the 4 SFP Optical Module Cages on the CMX card is tied to the CMX ground plane via 2 parallel jumpers. These jumpers are JMP91A/B (for SFP1) through JMP94A/B (for SFP4). 4.7k Ohm resistors will be installed in all 8 of these jumper locations.

  The spring fingers at the front of the SFP Cages will most likely make an uncertain electrical connection to the CMX card's aluminum front panel.

- Pins 34 and 68 in each of the front panel CTP connectors (J10 and J11) are not used for carrying LVDS signals. These pins and the wires in the CTP cables that are plugged to them may be grounded via jumpers J97 and J98.
  J97 grounds pins 34 and 68 in CTP connector J10.
  J98 grounds pins 34 and 68 in CTP connector J11.
  100 Ohm resistors will be installed in these two jumper locations.

- There are 18 Backplane connector <CG> Grounds pins that may be connected to the CMX ground planes through parallel jumpers JMP96A and JMP96B. These 18 backplane connector <CG> ground pins are:

  J4-D10, J4-D11, J4-B14, J4-B15, J4-D18, J4-D19,
  J5-B3, J5-B4, J5-D7, J5-D8, J5-C11, J5-C12,
  J5-C15, J5-C16, J5-D19, J6-E2, J6-E3, J6-E8.

  100 Ohm resistors will be installed in jumpers JMP96A and JMP96B to hold these 18 backplane <CG> pins at ground potential. As I understand it, no connection is made to these backplane <CG> ground pins by the Cable Transition board that is plugged into the back side of the backplane.

- The heat-sinks on the two Virtex FPGAs will most likely make a direct electrical connection to the heat-spreader on the top of the Virtex FPGA packages. The FPGA heat-spreader makes a connection to the back side of the FPGA silicon die which is at ground potential. Thus these heat-sinks should not be forced far from ground potential.

Each of these Virtex heat-sinks is tied to the CMX ground planes via two parallel resistors. The Base Function FPGA heat-sink is tied to ground via R801 and R802. The Topological Processor FPGA heat-sink is tied to ground via R803 and R804. A 100 Ohm resistor is installed in each of these locations.

Appendix V: Layout Details

A current snapshot of the detailed description is included below while the source material is in cmx_ab_layout_details.txt found in http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
              CMX_0  Mentor Layout Details
             ------------------------------

                                        Original Rev.  25-Aug-2011
                                         Current Rev.  29-Apr-2014


This file collects the details of the Mentor layout of the
CMX version 0 card.

In the Mentor system we will always display the CMX-0 card in
our "standard format",  i.e. you are looking at the component
side of the card, its front panel is to the left and its back
plane connectors are to the right.

CMX-0 is a "9U by 400mm" card,  i.e.  366.70 mm +0 -0.3 tall
by 400mm +0 -0.3  wide.

The CMX-0 uses the fancy IEEE 1101.11  (or whatever it is)
front panel hardware.


=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=


Layer Strategy and Usage in the CMX Card:
-----------------------------------------


  Be carefull - does "layer" mean:  1:10 Signal Layers      or
                                    Mentor Logical Layers   or
                                    Physical Stack Up Layers ?

  All information about layers in the
  CMX project is in the file:

       cmx_ab_routing_layer_strategy.txt


=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=
```

```
Routing Vias used on the CMX Card:
----------------------------------

  The following vias are used to  route  the CMX card.
  The numeric field in the  via name  should indicate
  the via's pad diameter  aka land diameter.


    via_0mm60:
                finished hole diameter         0.30  mm
                land pad                       0.60  mm
                plane relief                   0.87  mm
                --> ring width                 0.150 mm
                --> plane isolation Air Gap    0.135 mm
                    from the pad
                Tented


    via_0mm65:
                finished hole diameter         0.30  mm
                land pad                       0.65  mm
                plane relief                   1.00  mm
                --> ring width                 0.175 mm
                --> plane isolation Air Gap    0.175 mm
                    from the pad
                Tented


    via_1mm1:
                finished hole diameter         0.60  mm
                land pad                       1.10  mm
                plane relief                   1.60  mm
                --> ring width                 0.25  mm
                --> plane isolation Air Gap    0.25  mm
                    from the pad
                Tented


    via_gtx_blind:
                finished hole diameter         0.25  mm
                land pad                       0.56  mm
                plane relief                   1.00  mm
                --> ring width                 0.155 mm
                --> plane isolation Air Gap    0.220 mm
                    from the pad
                This via connects only layers:
                    Signal_1 - Signal_2 - Signal_3
                Tented


    via_proc_in_blind  and  via_std_blind

                Currently these 2 types of blind vias have
                exactly the same dimensions as the via_gtx_blind.
                A difference is that in the current "Tech" files
                that via_gtx_blind has ground plane relief in the
                middle type of ground plane where as
```

```
            via_proc_in_blind  and  via_std_blind  have the
            ground plane fill in in the middle type of
            ground plane.


    cf. section below for note about special versions of blind vias
    to generate the needed "donuts" for the L6 ground plane a the bottom
    of the blind via and pad stacks.


=========================================================================


Blind Pin Padstacks:
--------------------

Both the Virtex BGA and the MiniPOD Transmitter geometries
will need  Blind Pin Padstacks  for their pins that carry
the high-speed differential signals.   These Blind Pin Padstack
will connect only Signal Layers 1, 2, and 3.   The dimensions
of these Blind Pin Padstack are setup the similar to those of
the  via_gtx_blind  via.    That is:

    MiniPOD Transmitter Blind Pin Padstack:
            finished hole diameter         0.25  mm
            land pad                       0.56  mm
            plane relief                   1.00  mm
            --> ring width                 0.155 mm
            --> plane isolation Air Gap    0.220 mm
                from the pad
            This via connects only layers:
                Signal_1 - Signal_2 - Signal_3
            Tented

        Note that the MiniPOD Transmitter Blink Pin Padstack
        may use the "large"  1.00mm  plane relief because the
        pins in the MAG-Array connector are spaced  1.27mm
        center to center.




    Virtex 1759 BGA Blind Pin Padstack:
            finished hole diameter         0.25  mm
            land pad                       0.56  mm
            plane relief                   0.85  mm
            --> ring width                 0.155 mm
            --> plane isolation Air Gap    0.145 mm
                from the pad
            This via connects only layers:
                Signal_1 - Signal_2 - Signal_3
            Tented

        Note that the Virtex 1759 BGA Blind Pin Padstack has
        the same plane relief diameter as is used for the rest
        of the pin vias in this geometry.  This is as large of
        a plane relief as we can get and still have good
```

connectivity of the ground plane into the center of
the FPGA. We want as much plane relief from the high
speed signals that used the Blind Pin Padstack as we
can get (while still having a good ground plane).

cf. section below for note about special versions of blind vias
to generate the needed "donuts" for the L6 ground plane a the bottom
of the blind via and pad stacks.

==========

L6 Ground plane issues :

Generating pads on the bottom layer of
the sub-lamination for blind vias and pins:

Mentor (at least our version) can create pads on signal layer
but does not seem able to create the flashes appropriate
for a negative data ground plane.

The technology file defines the span of layers for blind vias
stacks. If the bottom layer of the blind stack is a signal layer,
the fablink artwork generation process creates all pads as
expected. If the bottom layer is a power layer (e.g. our ground
plane), fablink only generates round flashes in the negative data
artwork, i.e. no pad for the blind vias. One would need to add
another signal layer for this ground layer and generate a ground
fill for this ground plane.

For a negative data ground plane with blind via pads, we need a
power relief with a pad in the middle of that relief and this
would appear as a "donut" in the negative gerber data. There is a
simple gerber definition to generate such donuts, but Mentor does
not seem to know how to generate them. Furthermore the Mentor
artwork viewer is not even able to simulate data including such
donuts.

The PCB manufacturer recommends an L1-L6 sub-lamination for the
blind pins and vias for the CMX circuit board which would include
our signal_1 = L1, signal_2 = L3, signal_3 = L5 with ground planes
at L2, L4, and L6. The PCB house thus needs a L6 ground plane
with pads for all blind vias.

Trying to generate these pads by adding a circle to the via and
pin geometries on some unused layer and including that layer in a
separate dedicated layer for L6 does not work. This method adds
concentric flashes, but a small flash on top of a big flash cannot
make a donut. More generally, any method that will only *add* a
donut on top of a relief flash will fail as well. The circular
relief flashes need to be *replaced* with a donut.

To replace the blind via and pin relief flashes we need to have just those vias and pins appear separately from the other power relief flashes in the gerber artwork file so that we can simply edit the gerber tool used. We thus need to force Mentor to use a different aperture for the ground "power" relief of all blind vias and pins. It needs to be different from the relief used for all other pins and vias. We could choose to make the blind via relief slightly different on all layers, but we instead make special versions of the geometries involved that will only be used to generate just the artwork for the L6 ground plane.

Blind pin geometries:

A special version of all blind pin geometries was created with 0.86 mm instead of 0.85 mm power relief so that these flashes can be forced to use a different aperture and thus receive a separate gerber D-code that we can edit to become "donuts". These geometries were only used to create the GND plane for Layer 6.

minipod_transmitter.with_1mm01_short_pin_power_relief

ffg1759_rev__bf19__geometry.with_0mm86_short_pin_power_relief.txt

Blind via geometries:

A special version of all blind via geometries was created with 1.01 mm instead of 1.00 mm power relief so that these flashes can be forced to use a different aperture and thus receive a separate gerber D-code that we can edit to become "donuts". These geometries were only used to create the GND plane for Layer 6.

via_std_blind.with_1mm01_short_via_power_relief

via_proc_in_blind.with_1mm01_short_via_power_relief

via_gtx_blind.with_1mm01_short_via_power_relief

We hand edited the versioned file aperture_table to add flash apertures 214 and 215 for D-codes 314 and 315 for flashes of 1.01 and 0.86mm.

We then can edit the artwork_23 file for L6 to replace the D-codes

```
  %ADD314C,1.010000*%
  %ADD315C,0.860000*%
with
  %ADD314C,1.000000X0.560000*%
  %ADD315C,0.850000X0.560000*%
```

(the second parameter specifies the hole in the middle of the flash)

Differential blind via pairs:

There is an additional difficulty to generate the correct ground plane cutouts under the differential blind via pairs.

On all other ground layers, these cutouts are generated in the negative data gerber files by adding "ovals" as short wide paths under the via pairs. These short paths are included in the CMX board geometry on layer "DAM_1". DAM_1 is then included in the default artwork definition for all ground planes that need those cutouts. The problem is that such simple wide paths would overwrite the donuts created as described above.

The solution is to replace each of these short wide paths on DAM_1 with a set of 3 shorter narrower paths forming a sideways "H" on DAM_3 and to include DAM_3 instead of DAM_1 for the artwork used to generate just the L6 Ground plane. The "H" combined with the two donuts then creates the intended overall "oval" relief plus one pad at each end.

Use textpad to extract columns of coordinates of all the "ovals" on DAM_1 found from cmx_0_pcb_ground_plane_cuts.txt and paste into excel. Use Excel to compute the end points of the "H"s, i.e. for each pair of X-Y coord that was making a 1.0mm long X 1.0mm wide $$path from DAM_1 we derive 3 pairs of X-Y coords for the 3 segments of the corresponding "H". There are four orientations to compute: vertical, horizontal, +45 degree and -45 degree.

The parallel bars of each "H" form the two outside edges of the oval. The line thickness matches the width of the gap between the pad and the relief (here is it 1/2 of 1.00 mm relief minus 0.56 mm pad, or 0.22 mm). The perpendicular cross bar of the "H" is in the middle with a thickness twice the airgap (here 0.44 mm). These three simple lines partially overlap the donuts (not a problem) and also completely fill out the gap between the pair of donuts to form the overall cutout, as desired.

We hand edited the versioned file aperture_table to add path apertures 216 and 217 for D-codes 316 and 317 for paths of 0.22 mm and 0.44 mm.

In hindsight: the 0.44mm path for the crossbar could have been replaced with two overlapping 0.22 mm paths. Furthermore it may not have been necessaryto use a special new 0.22 mm width as there is a significant overlap between the "H" and the "donuts". It may well have been possible to create the "H" using only our already existing 0.20 mm path width. The 0.22mm and 0.44mm "H" may still be the most straightforward method.

```
  Additional ground cutouts to blind vias:
  ---------------------------------------

    We also need cutouts under the DC block capacitors between the Avago
    receivers and the Virtex 6 GTX differential inputs.

    Including a set of paths on DAM_1 in the cap0201 component geometry
    for the DC block capacitor was not successful as the artwork output
    for the ground planes did not include those contributions to DAM_1.
    Maybe a different layer would be more successful or the DAM_1 layer
    may need to be declared with additional properties.

    The method used was to pull the coordinates x,y and angle from the
    comps file for all DC block capacitors (C1001-C1072) and use textpad
    and excel to recreate the same 3+2 $$path that was in the geometry,
    but now both on DAM_1 and DAM_3 under each cap and insert them
    in the board geometry.


=========================================================================


Trace Widths Used for Routing the CMX Card:
-------------------------------------------

   The following trace widths are used for "Normal" applications:
  --------------------------------------------------------------


    Normal CMOS signal routing where space permits:

       0.20 mm traces on 0.6 mm centers

       To break out by 45 degrees they stager by
       0.3 mm on the 0.6 mm center to center run.

       use via_0mm65 vias spaced 1.2mm center to center


    Normal CMOS signal routing where things are tight:

       In the BGA escape we need to use  0.13mm  traces for
       the optimum layout.   Details: the BGA Vias are  0.61mm
       diameter and are spaced 1mm center to center.  This
       gives  0.39mm  for the escape trace and its clearance
       on both sides.  This 0.39mm is used as a 0.13mm escape
       trace and a 0.13mm clearance on both sides.

       Using  0.16 mm  wide traces on  0.5 mm  centers works
       out well for buses that come out of the FPGA and for
       the vertical busses for the TTC decoder signals and
       the on card bus signals.
```

```
LVDS transceiver DS91M040:

          Signals - 0.20 mm trace
   Power & Ground - 0.20 mm trace  to one via_0mm65
                              centered 0.8mm from pad edge
      Bypass Caps - 0.60 mm trace   via_0mm65

Translator 74AVCAH164245

          Signals - 0.20 mm trace
                    straight IN 0.7mm to via_0mm65
                    OUT 0.4mm bend to 0.05mm grid
                    via_0mm65  0.9mm from pad edge

   Power & Ground - 0.25 mm trace  to via_0mm65  centered
                                       0.7mm from pad edge
      Bypass Caps - 0.60 mm trace


Bypass Capacitor 0603 size connections

   0.60 mm trace to via_0mm65 centered 0.5mm from pad edge


Normal Bypass Capacitor 0805 size connections

   0.75 mm  trace to via_0mm65 centered 0.7mm from pad edge
   In the power supply section may use 1.0mm trace width
   for the 0805 ceramic capacitors.


Power Bypass Capacitor 0805 size connections

   1.0 mm  trace to via_1mm1 centered 1.0mm from pad edge
                          or centered 0.9mm from pad edge


Tant D pads      2x  1.20 mm   1mm1 via   CL on pad edges
                     1.1mm or 1.2mm from pad edge to via center

Tant B pads    1.20 mm trace  1mm1 via   CL on pad edges
                       0.9mm from pad edge to via center
                 or two 0.75 mm traces to two  via_0mm65

Al Electrolytic F pads   2x  1.20 mm   1mm1 via   edge on pad edges

Transient Suppressor pads    1.20 mm   1mm1 via   in center

Fuse Holder pads      2x 4x  1.20 mm   1mm1 via

0.20mm width differential pair on 0.5mm center to center
with a unit cell pitch of 1.5mm from one pair to the next.
Thus you can fit 8 of these differential pairs in 12mm.

0.25mm width differential pair on 0.6mm center to center.

0.35mm width for the "analog" traces in the DC/DC converters.
```

```
  Special "Key" Trace Widths:
  ---------------------------

     60 Ohm single ended on the Top layer:  0.12 mm width
     60 Ohm single ended on  a  Mid layer:  0.12 mm width

    6.4 GHz Differential on the Top layer:
    6.4 GHz Differentail on  a  Mid layer:

            LVDS signals on the Top layer:
            LVDS signals on  a  Mid layer:

     Differentail Clocks on the Top layer:
     Differential Clocks on  a  Mid layer:

       For all of these 50 Ohm differential traces:

                  0.14mm width   0.4mm spacing center/center
                  0.5mm spacing cent/cent is an alternative


     Notes:  We want the open space between a differential pair
             to be about twice the width of one of the traces in
             the differential pair.  I.E. the center to center
             spacing is 3 times the width of one of the traces
             (or a little bit more - not less).

             We can not use 0.13mm width as a "Key" trace width
             because we need this for the BGA escape routing.


=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=

Differential Trace Layout:
--------------------------

All 100 Ohm differential traces on the CMX will be layed out
using a "key" trace width to indicate that they are a 100 Ohm
differential pair.   This key layout pattern is:

                       Trace Width:  0.14 mm
    Trace Spacing Center to Center:  0.40 mm
         Open Space between Traces:  0.26 mm

This is fine for horizontal and vertical traces.  What about
differential trace routing at an angle ?   CMX could use:


  Starting from the Horz or Vert parallel traces,
  Stager by  0.20 mm  to start the trace segments at an angle:

                         Slope:  1
     Center to Center Distance:  0.4243 mm
     Open Space between Traces:  0.2843 mm
      Extra Length at the Bend:  0.3414 mm
```

```
  Starting from the Horz or Vert parallel traces,
  Stager by  0.10 mm  to start the trace segments at an angle:

                        Slope:  1
     Center to Center Distance:  0.3536 mm
     Open Space between Traces:  0.2136 mm   <-- Too Small
      Extra Length at the Bend:  0.3121 mm

                        Slope:  0.5
     Center to Center Distance:  0.4025 mm
     Open Space between Traces:  0.2625 mm
      Extra Length at the Bend:  0.1894 mm

                        Slope:  0.3333
     Center to Center Distance:  0.4111 mm
     Open Space between Traces:  0.2711 mm
      Extra Length at the Bend:  0.1316 mm

                        Slope:  0.25
     Center to Center Distance:  0.4123 mm
     Open Space between Traces:  0.2723 mm
      Extra Length at the Bend:  0.1000 mm
```

The pair of traces in a differential pair need to be the same length. This is especially important on the 6.4 Gbps GTX traces where:

- the bit length is about 156 psec
- a trace 1 mm long takes about 6.6 psec (assume 1/2 c)
- the skew in a GTX transmitter output pair is 2 psec typical 8 psec maximum.
- the 20%-80% rise and fall time is 120 psec typical

We assume that the differential signals are isochronous at the component pins then there is a skew in getting these signals started into the differential trace pair. For example:

- Coming out of the BF GTX pins, after the via pair, on the Red layer, in the now parallel traces, from points directly across from each other, the longer trace back to the FPGA is about 0.638 mm longer than the shorter trace.
- Coming out of the BF GTX pins, on the Green layer, in the now parallel traces, from points directly across from each other, the longer trace back to the FPGA is about 1.206 mm longer than the shorter trace.
- In the typical escape from the MiniPOD, to where the traces are parallel, from points directly across from each other, the longer trace back to the MiniPOD is about 1.7mm to 2.2mm longer than the shorter trace.

- In a bend with a stager of 0.20mm going to a 45 degree trace, from points in the parallel traces that are directly across from each other the outer trace is about 0.34mm longer than the inner trace.

- In a bend with a stager of 0.10mm going to a trace with a slope of 0.25 or less, from points in the parallel traces that are directly across from each other the outer trace is about 0.19mm to 0.10mm longer than the inner trace.

From reading lots of application notes, and from looking at many examples of commercial cards with high speed differential traces, it is clear that we need to take some care with matching trace lengths on both sides of a differential signal. We used the following guide lines for adjusting the high speed differential trace lengths on the CMX card. These guide lines are:

- First adjust the trace lengths by modifying the circuit at the net list level, e.g. change which GTX Translator is connected to which MiniPOD channel or add a polarity swap to get a better length match within a differential pair. In general this step appears to get the trace lengths within about 1.6 mm of being equal.

- Next adjust the topology of how the traces enter the MiniPOD BGA to get a better length match, e.g. change which side of the BGA the traces enter from, enter on the other side of the MiniPOD BGA pins, add a loop to the shorter trace within the BGA foot print.

- As the last step add a serpentine section to the shorter trace. We are using the following rules to make the serpentines:

  Add the serpentine at the MiniPOD end of the trace.

  On a vertical or horizontal trace the serpentine is:

  A perpendicular step out of 0.2 mm for a length of 0.5 mm.

  Return to the normal trace path for 0.5 mm before stepping out again.

  Round the 4 corners of each step out with an arc of 4 segments and a radius of 0.10 mm.

  Each of these step outs will add 0.234 mm of trace length.

  On a 45 degree diagonal trace the serpentine is:

  A perpendicular step out of 0.2121 mm for a length of 0.5657 mm.

0.2121 mm is 3 grid dots diagonally with a grid of 0.05 mm.
0.5657 mm is 4 grid dots diagonally with a grid of 0.10 mm.

Return to the normal trace path for 0.5657 mm before stepping out again.

Round the 4 corners of each step out with an arc of 4 segments and a radius of 0.10 mm.

Each of these step outs will add 0.250 mm of trace length.

Add serpentine until the short trace comes within about 0.3 mm of the longer trace. Do not make the short trace longer than the originally longer trace. Stopping the serpentine about 0.3 mm short of a match allows for the possibility that the added electrical delay of the serpentine is greater than its added geometric length.

Note that all of the GTX traces have their 45 degree corners rounded with arcs of 2 segments at a radius of either: 0.40 mm, 0.30 mm or 0.16 mm. The 0.16 mm radius is needed only for corners adjacent to short segments, i.e. segments 0.3 mm in straight length or 0.2828 mm diagonally. When 0.16 mm radius needs to be used the other side of the differential line may use a 0.30 mm radius if that gives the best looking differential layout. The 0.40 mm radius is used only in open areas with long straight traces.

==========

Differential Via Layout:

- We will use a standardized via layout pattern for all of the 100 Ohm Differential traces.
- All of the CMX's 100 Ohm differential traces are routed as 0.14 mm trace width on 0.4 mm centers. This is a "key trace width" to identify the 100 Ohm differential traces to the bare pcb house.
- For the 6.4 GHz 100 Ohm Differential traces we will use a special blind via (via_gtx_blind) that only goes through the first 5 physical layers of the pcb (Signal_1, Signal_2, Signal_3, and the top 2 ground planes).
- For the 100 Ohm Differential traces that are spaced 0.4mm we should use Differential Vias that are spaced 1.0mm center to center.
- The ground plane is removed in an oval that is a line 1.0 mm wide and runs between the centers of the two via.

- Also see the section above about the L6 ground plane.

- The Area Fills are removed in a rectangle that is 1mm by 2mm, i.e. this rectangle has the same outer dimensions as the removed oval of ground plane.

- We may let the ground plane fill in on the very bottom ground plane layer of the CMX card as this is far enough away from the differential blind via pair that it does not upset their transmission line characteristics.

- It is good to put a pair (or a quad) of ground rivet vias near the Differential Via pair. In one pattern there are two ground rivets colinear with the two via and spaced at total of 3.4 mm center to center. The intent of the ground rivets in the differential via layout is to provide a local symmetric return path for any common mode current that is flowing with the differential signal.

=-=

Details from Looking at Examples of 6 GHz Routing

Page 293 of the Xilinx GTX Transceiver User's Guide shows some examples of GTX signal routing. These traces and pads appear to be:

```
   BGA Pin Pad Array Land Dia  0.48mm

   BGA Via Array Land Dia      0.54mm
   BGA Via Array C to C        1.0

   Routing Via Land Dia        0.42mm
   Routing Via C to C          1.0

   Trace Width                 0.11mm  or  0.12mm
   Trace C to C                0.45
```

Traces to 10 GHz optical transceiver on PCI Express card

6 GHz PCI Express traces and vias

Xilinx Demo 623 Board (was in mils - converted to mm)

```
   BGA Via Array Land Dia      0.51mm
   BGA Via Array C to C        1.0

   Routing Via Land Dia        0.46mm
   Routing Via C to C          1.27
```

Drill Sizes: The only drill that they use that goes through only layers 1 through 6 (i.e. their blind vias) is 0.20mm diameter. Their smallest drill that goes through all layers is 0.25mm which by the hole counts must be used for all of their normal small vias.

Summary:

Blind Via	Land 0.46mm	Drill 0.20mm
Through Via	Land 0.51mm	Drill 0.25mm

Both of these vias appear to use a 0.76mm plane relief --> air gaps of 0.15mm and 0.125mm

Trace Width	Surface	0.10mm	to	0.11mm
Trace C to C		0.25mm	to	0.26mm

Trace Width	Inner	0.13mm
Trace C to C		0.43mm

==========

At 6 Gbps What Size Imperfections Make a Difference ?

We have 6 G bits per second data flow to the MiniPODs. So this is basically a waveform like a 3 GHz sin wave but we need to include the 3rd and 5th harmonics. So we need transmission lines with good flat characteristics up through 15 GHz.

In open space 15 GHz is 20 mm wave length. The transmission lines on the card are about 1/2 the speed of light so on these lines a wavelength is about 10 mm.

To be a good flat line we must keep any imperfections down to a physical size of less then 1/20th of a wavelength or so. Thus we care about bumps that are 0.5mm in size.

So for work on CMX lets wake up when we see bumps on the scale of 1/2 of that, i.e. 0.2mm in size.

==========

Blind vias for 6 Gbps:

We do need some vias in the 6 Gbps 100 Ohm differential traces. All of these signals are on layers: Signal_1, Signal_2, and Signal_3.

Can we use just one type of bind via that can connect to any of these 3 signals layres or do we need two types of blind vias: one to connect Signal_1 with Signals_2 and another to connect Signal_1 wtih Signals_3 ?

The issue is using a blind via that physically passes through layers Signal_1,2,3 to connect signals between Signal_1 and Signal_2, i.e. in this case will the stub running to Signal_3 cause trouble at 6 Gbps ?

How long physically is this stub likely to be ?

- Let's be generous in this length calculation because we are interested in the lowest frequency at which this stub may cause trouble.

- The card will be about 2.8mm thick (110 mils). So each layer is about 0.13mm thick.

- To this lets add the thcikness of the copper conductor. 1 oz copper is about 0.036mm thick. 1/2 oz copper is about 0.018mm thick.

- The stub will go through a dielectric layer then a ground plane then another dielectric layer then layer signal_3. So physically the stub will be about 0.30mm long.

- We know that at a frequency where 0.30mm is 1/4 of a wavelength that this stub will case a short circuit.

- If the important Fourier components of our 6 Gbps GTX signals approach this frequency then this stub will cause us trouble.

- In the pcb signals on these 100 Ohm differential traces will travel at about 1/2 the speed of light.

- At 1/2 the speed of light, 125 GHz has a wavelength of 1.2mm (i.e. a 1/4 wavelength of 0.30mm).

- 125 Ghz is a factor of 8 or so above the frequencies that we care about for our 6 Gbps signals. Thus it's not clear whether or not this stub will cause a significant transmission line effect in our application.

- We clearly care about frequencies up through 15 GHz. 15 GHz on our transmission lines (at 1/2 half the speed of light) has a wavelength of 10 mm. So this 0.30 mm long stub is about 3% of a wavelength long.

- In any case we still must consider the lumped capacitance effects of this stub with will drive down the Zo of the differential via pair.

- As a final consideration of the via stub, think about the situation where you do not use a blind via. In this case the stub is the full thinkness of the card minus 2 layers. This is a stub about 2.5mm long. This is a 1/4 wavelength stub for our 15 GHz 10mm wavelength signals. ---> We must use blind vias.

==========

Design Rules used for Routing the CMX Card:

We will start on 10-Apr-2013 with Net Rules for the Default Net_Type:

	Pin	Via	Trc	Fill
Pin	0.5			
Via	0.1	0.3		
Trc	0.22	0.25	0.25	
Fill	0.4	0.4	0.5	0.7

==========

Drill Holes:

See also the file fill_generation_notes.txt for more information about drill holes for component pins and plain drill holes.

The CMX circuit board has a significant number of drill holes in the area where traces are routed and components mounted. Many of these drill holes are for size 4-40 machine screws. 4-40 screws are used to mount: stiffener bars, head sinks, and front panel MDR connectors. Because of the limited clearance height on the back side of the pcb we will use button head allen type screws in most/all of these 4-40 screw applications.

4-40 Button Head Allen SS Machine Screw:

diameter of the threaded section is about 2.8 mm
head diamter is about 5.3 mm
thickness of the head is about 1.5 mm

```
  4-40 Hex SS Machine Nuts:

     about  6.3 mm across flats      6.35 mm = 1/4" across flats
     about  7.0 mm point to point    7.33 mm = 6.35 / cos 30 deg.

  Number 4 Flat Washer Plated:

     diameter is about  7.2 mm
     thickness is about


- We will use  3.0 mm  drill holes in the CMX for these
  screws.

- We will relieve the power and ground planes from these
  4-40 screws with a circle of diameter  4.0 mm    that is
  from the edge of the drill hole to the closest metal in
  the plane is  0.5 mm

- No routing trace should get closer than  1.0mm  to the
  edge of the drill hole (i.e. closer than 0.5mm to the edge
  of the plane relief).   High speed or critical signals
  should perhaps stay back further from the drill holes.

- When a flat washer is  not  used all components should
  stay back at least  4.5 mm  from the center of the
  drill holes for the 4-40 screws,  i.e. there is a
  keepout circle of radius  4.5 mm.

- Because of the very limited clearance height we do not
  have room to use a flat washer under the head of most
  of these 4-40 button head screws.

    VME reccommended back side stub height is 1.0 mm.

    Back side distance to the separation plane  4.07 mm

    But actually less than this because we mill off
    the back side of the card to fit into the card guides.

- We will use a standard component pin pad-stack geometry
  for these 4-40 screws in CMX called  STD_4_40_SCREW_PIN.

- The  STD_4_40_SCREW_PIN  pad-stack is defined in only
  one place.  It is in the  Heat_Sink_BF_Geom.txt  file.


=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=
```

```
Area Fill Generation:
---------------------

The details of the Area Fill generation are given in a separate
file named,  "fill_generation_notes.txt".

 - CMX has 55 Area Fill Shapes.

 - These shapes are used to make 67 Fills.

 - The desigh net rules and the fill tool size must be
   adjusted while making these 67 Fills.

 - There are about  139  Excluder Shapes that are all
   used on 3 different layers.  These Excluders are
   kept in the file, "exclude_fills_basic_setup.txt"
   and must be added to the Traces file before the
   Area Fills are made.


=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=-=

Gerber Plot Generation:              Rev. 17-Oct-2013
-----------------------


  -->  Recall that the  Aperture Table  and the  Artwork Format  are
       Mentor Design Object type files  and  thus you must explicitly
       save them before exiting FabLink.

  -->  Recall that the  Gerber Artwork  files in the .../mfg/
       directory are written at the instant that you click
       "creat artwork" - any old files of this type are
       overwritten at that instant.


Assume that the Gerber Format has been setup and saved.
Gerber Data is in mm 3.3 format.
If necessary use:  Right Click  -->  Artwork  -->  Change Artwork Format

        Image Scale:  1
        Units:  mm
        Mode:  Absolute
        Plot Offsets:  Manual with  X=0.0  Y=0.0
        G_Code:  Allow
        Zero Suppression:  None
        Interpolation:  Linear  with  8 Segments
        Output Format:  3 Significant and 3 decimal
        Data Record Length:  80
        Header String:  none
        Sub-Header String:  none
        Trailer String:  none
        Machine Stop Code:  M02
        XY-Modal:  not checked
        Open Shutter Modal:  not checked
        View Artwork Format:  not checked
        Command Block End Character:  *
```

Verify that you are using the proper version of the Drill_Holes
section of the geometry for the CMX-0 pcb that has the copper
for the ...

Aperature Table:

NOTE: Only delete and remake the Aperture Table if you need to.
----- Once we have the Aperture Table setup the way that we
want it for the CMX then do NOT delte and remake it.

Right Click -->
Artwork --> Change Aperature Table --> Delete All Apertures

Right Click -->
Artwork --> Change Aperature Table --> Fill Aperature Table

Select the Apertures for ALL Aizes
Select NO ReSize and NO ReScale
Flash Complex Padstacks: not checked
Replace the table

Report the Aperture Table (from Report Pull Down Menu)
Include the ArtWork Format: yes
Save and Display the Report
Save Report to .../Work/Text/
Replace the existing Report

Currently there are about 188 apertures.

May/Will need to Edit the Power Apertures:

After the Aperture Table is filled it is necessary to edit the
14 Power Apertures (aka thermal reliefs) to get the desired
layout. To edit a Power Aperture

Right Click --> Artwork -->
Change Aperture Table --> Change Power Aperture

For each Power Aperture select the Aperture Position and then
set the: Tie Width, Air Gap, and Rotation and then click OK.
Direct editing of the versioned aperture_table.apertt_x
file is also possible.

Note that the outer diameter of each Power Aperture is driven
by its "power plane relief" diameter in its Geometry. We must
set the Air Gap to get the desired pad size and set the Tie Width
to get the desired amount of Copper connection. This version of
Mentor lets us control the Tie Rotation.

Before editing the Power Apertures are the following:

Raw Power Apertures from the "Aperture Fill"

aperture_table.apertt_20 27-Aug-2013 9:57

Pos	Diameter	Dcode	This Must Be
102	1.00	202	via_0mm65
103	1.60	203	via_1mm1
104	0.87	204	GTX gnd rivet vias only by MiniPODs
111	1.85	211	front panel 2x8 conn ground pins
112	2.80	212	DC/DC Conv Gnd pins & CF_Socket screws
113	1.19	213	Gnds under LVDS trans & Clk 10x Fanout
114	2.00	214	SFP ground pin center back
117	1.05	217	MiniPOD larger pins
118	2.50	218	MiniPOD mounting screws
120	0.95	220	grounds NB6L611 clock buffer
122	0.85	222	grounds under FPGA BGAs
123	3.50	223	TTCDec mounting screws
124	3.00	224	power connector center pin grounds
125	1.65	225	backplane connector ground pins

The remaining screw up on 27-Aug-2013 is that
aperture 112 is used for two not compatable
purposes.

On 17-Oct-2013 needed to add the Power Aperture for
the 3.80 mm basic diameter wrap_3mm0: 3.00 mm pad
gives a 1.00 mm ring width (with a 1.00 mm drill)
and a 0.40 mm Air Gap.

On 17-Oct-2013 also needed to add the 0.45 mm and
0.55 mm Circular Flash for the new Virtex SMD Pad Lands
and their Solder Mask.
This is Aperture 212 & 213.

On 29-Oct-2013 also needed to add the 0.86 mm and 1.01 mm
circular flashes for the relief of blind vias and pins
to generate the ground plane for stackup L6.
This is Aperture 214 & 215.

On 30-Oct-2013 also needed to add a 0.22 mm and 0.44 mm
trace for the "H" relief underneath GTX differential via pairs
to generate the ground plane for stackup L6.
This is Aperture 216 & 217.

After editing the Power Apertures are the following:

aperture_table.apertt_21 30-Oct-2013 Hand Edited

Power Apertures Desired for CMX-0

Pos	Outer Relief Diameter	Geom Air Gap	New-Current Air Gap	New-Current Tie Width	Rotate	Function
102	1.00	0.175	0.14	0.40	45	via_0mm65
103	1.60	0.25	0.20	0.64	45	via_1mm1
104	0.87	0.135	0.10	0.35	45	GTX ground rivet vias
111	1.85	0.175	0.14	0.75	45	front panel 2x8 conn
112	2.80	0.25	0.20	1.15	45	DC/DC Conv Gnd pins
113	1.19	0.24	0.20	0.50	45	Gnd LVDS trans & Clk 10x
114	2.00	0.25	0.20	0.80	45	SFP Gnd pin centr back
117	1.05	0.20	0.16	0.45	45	MiniPOD larger pins
118	2.50	-0.50	0.05	1.00	45	MiniPOD mountng screws 0.25 relief to drill
120	0.95	0.175	0.14	0.40	45	Gnd NB6L611 clock buff
122	0.85	0.120	0.10	0.35	45	gnds under FPGA BGAs
123	3.50	-0.70	0.05	1.40	45	TTCDec mounting screws 0.25 relief to drill
124	3.00	0.50	0.40	1.20	45	pwr conn centr Gnd pin
125	1.65	0.275	0.22	0.75	45	bckplane conn Gnd pins
210,	2.90	0.16	0.14	1.15	45	CompactFlash Screw Gnd
211,	3.80	0.40	0.40	1.00	45	Wrap_3mm0

In all cases this gives the same or slightly larger Land diameter than in the associated via's Signal/Pad layers and it gives generous Tie Width.

The default sizes that I made are:

Air Gap equals 80% of the geometries air gap.

Tie Width equals 40% of the relief diameter.

Gerber Data Generation:

Use the geoms_421_for_all_other version of the geometries which uses the nominal power relief thus the standard aperture for all blind pins and vias

Use the "Gerber_Ground_Upper" Technology file and then:

Right Click --> Artwork --> Creat Artwork Data

Gerber Data is Gerber 274X format
Stroke the Area Fill, Flash the Polygon
ASCII Data, for the BOARD, ALL ArtWork Numbers
NO Tear Drops, REMOVE Unused Pins, REMOVE Unused Via's
NO Output UnPlated Holes
NO ReSize, NO ReScale
Both the GTX and the non-GTX Blind pins and vias are set "Long" so all blind pins and vias will get ground plane relief.

Right Click --> Artwork --> Creat Artwork Data

All settings are the same except create Gerber Data for just ArtWork Numbers 1 i.e. just the Top pcb layer, and use the option:
Output ALL Pins, Output ALL Via's

Now use the "Gerber_Ground_Middle" Technology file and then:

Right Click --> Artwork --> Creat Artwork Data

All settings are set to how they were initially but now only the GTX Blind Vias and Pins are "long".
Create just ArtWork Number 14 i.e. just the "Middle" type of Ground Plane that has relief for only the GTX type of Blind pins and vias.

Now use the "Gerber_Ground_Lowest" Technology file and then:

Right Click --> Artwork --> Creat Artwork Data

All settings are set to how they were initially but now none of the Blind Vias and Pins are "long".
The ground plane will fill in around all blind pins and vias.
Create just ArtWork Number 15 i.e. just the lowest layer type of ground plane that does not have relief for any Blind Pins & Vias.

Right Click --> Artwork --> Creat Artwork Data

All settings are the same except create Gerber Data for just ArtWork Number 12 i.e. just the Bottom pcb layer, and use the option:
Output ALL Pins, Output ALL Via's

```
   Switch to the geoms_420_for_artwork_23 version of the geometries
   which uses a different power relief thus a different aperture
   for all blind pins and vias

   Now return to the  "Gerber_Ground_Upper"  Technology file and then:

      Right Click  -->  Artwork  -->  Creat Artwork Data

         All settings are set to how they were initially
         but now only the GTX Blind Vias and Pins are "long".
         Create just ArtWork Number 23   i.e. just
         the "Layer 6" type of Ground Plane  that has relief
         for all Blind pins and vias *AND* uses a separate
         D-code for all flashes blind pin and vias *AND*
         uses a modified style of "H" relief under the
         gtx differential vias.

         Edit artwork_23 to replace the D-code definitions for 314&315
            %ADD314C,1.010000*%
            %ADD315C,0.860000*%
         with
            %ADD314C,1.000000X0.560000*%
            %ADD315C,0.850000X0.560000*%
          (the second parameter specifies the hole
           in the middle of the flash)
         and Save as artwork_23_edited


Recall what is in each of thr Gerber artwork file:

  Gerber File  1   SIGNAL_1    Layer  1  in the PCB Stackup  Top
  Gerber File  2   SIGNAL_2    Layer  3  in the PCB Stackup
  Gerber File  3   SIGNAL_3    Layer  5  in the PCB Stackup
  Gerber File  4   SIGNAL_4    Layer  7  in the PCB Stackup
  Gerber File  5   SIGNAL_5    Layer  9  in the PCB Stackup

  Gerber File  6   SIGNAL_11   Layer 11  in the PCB Stackup
                   Bulk_2V5, GTX_AVTT,...

  Gerber File  7   SIGNAL_12   Layer 12  in the PCB Stackup
                   Bulk_3V3, GTX_AVCC,...

  Gerber File  8   SIGNAL_8    Layer 14  in the PCB Stackup

  Gerber File  9   SIGNAL_6    Layer 16  in the PCB Stackup
  Gerber File 10   SIGNAL_7    Layer 18  in the PCB Stackup
  Gerber File 11   SIGNAL_9    Layer 20  in the PCB Stackup
  Gerber File 12   SIGNAL_10   Layer 22  in the PCB Stackup  Bottom


  Gerber File 13   GROUND Plane  Upper
                   Relieve GTX and non-GTX  blind pins and vias
                        Layers:  2,4,8   in the PCB Stackup

  Gerber File 14   GROUND Plane  Middle
                   Relieve only GTX  blind pins and vias
```

```
                Layers:  10,13,15,17,19   in PCB Stackup

Gerber File 15   GROUND Plane  Lowest
                 Relieve none of the  blind pins and vias
                             Layer 21  in the PCB Stackup


Gerber File 16   Board Dimensioned Fabrication Drawing
                 BOARD_OUTLINE, SIGNAL_1, PAD_1, DRAWING_1, SILKSCREEN_1

Gerber Files 17 & 18   Silk Screens   Top then Bottom

Gerber Files 19 & 20   Solder Masks   Top then Bottom

Gerber Files 21 & 22   Solder Paste Stencils   Top then Bottom
                       (aka Solder Paste Masks)


Gerber File 23   GROUND Plane  just for Layer 6
                 Relieve GTX and non-GTX  blind pins and vias
                 Uses an "H" plane relief under the GTX
                 deifferential via pairs Layers:  6   in PCB Stackup
```

Release File Name		Mentor File Name	Content
cmx_artwork_1		artwork_1	Layer 1 Trace Top Copper
cmx_artwork_2		artwork_2	Layer 3 Trace
cmx_artwork_3		artwork_3	Layer 5 Trace
cmx_artwork_4		artwork_4	Layer 7 Trace
cmx_artwork_5		artwork_5	Layer 9 Trace
cmx_artwork_6		artwork_6	Layer 11 Power Fill
cmx_artwork_7		artwork_7	Layer 12 Power Fill
cmx_artwork_8		artwork_8	Layer 14 Power Fill
cmx_artwork_9		artwork_9	Layer 16 Trace
cmx_artwork_10		artwork_10	Layer 18 Trace
cmx_artwork_11		artwork_11	Layer 20 Trace
cmx_artwork_12		artwork_12	Layer 22 Trace Bottom Copper
cmx_artwork_13		artwork_13	Layers 2,4,8 Gnd Plane
cmx_artwork_14	(*)	artwork_23_edited	Layer 6 Gnd Plane
cmx_artwork_15		artwork_14	Layers 10,13,15,17,19 Gnd Pln
cmx_artwork_16		artwork_15	Layer 21 Gnd Plane
cmx_artwork_17		artwork_16	Overall Assembly Drawing
cmx_artwork_18		artwork_17	Silkscreen Top
cmx_artwork_19		artwork_18	Silkscreen Bottom
cmx_artwork_20		artwork_19	Solder Mask Top
cmx_artwork_21		artwork_20	Solder Mask Bottom
cmx_artwork_22		artwork_21	Solder Paste Stencil Top
cmx_artwork_23		artwork_22	Solder Paste Stencil Bottom

```
     (*) note where we have inserted artwork_23 into a more natural location
              and shifted the numbering below that point


  Gerber Data Viewing:

     Right Click  -->  Artwork  -->  Simulate Artwork Data

        Note that currently the default FabLink grid is 0.005 mm
        and thus its hard to measure anything.  This is clearly
        left over from an English project and needs to be changed.



=======================================================================


Hand Edit the Final Gerbers:
----------------------------

  Had to hand edit the GND plane for layer 6 to force pads on all
  blind pin and vias as the sub-lamination will be L1-L6.

     Edit artwork_23 to replace the D-code definitions for 314&315
        %ADD314C,1.010000*%
        %ADD315C,0.860000*%
     with
        %ADD314C,1.000000X0.560000*%
        %ADD315C,0.850000X0.560000*%
      (the second parameter specifies the hole in the middle of the flash)
     and Save as artwork_23_edited


=======================================================================



Drill File Generation:              Rev. 26-Aug-2013
----------------------


  -->  Recall that the  Drill Table  and the  Drill Format  are
       Mentor Design Object type files  and  thus you must
       explicitly save them before exiting FabLink.

  -->  Recall that the  Excellon Drill files  in the .../mfg/
       directory are written at the instant that you click
       "creat drill file" - any old files of this type are
       overwritten at that instant.


  Assume that the Drill Format has been setup and saved.
  Drill Data is in mm 3.3 format.
```

Drill Table:

NOTE: Only delete and remake the Drill Table if you need to.
----- Once we have the Drill Table setup the way that we want it for the CMX then do NOT delte and remake it.

Use the "Drill Generation" Technology file and then:

Right Click -->
Drill --> Change Drill Table --> Delete All Drills

Right Click -->
Drill --> Change Drill Table --> Fill Drill Table

Select Replace the Drill Table

Report the Drill Table (from Report Pull Down Menu)

Currently there are about 22 drills.

Right Click -->
Drill --> Creat Drill Data

This is now a lot more complicated menu because we have some drills that go only through the top 5 or 6 layers for the blind vias.

It now also appears that this must be done in 2 steps, i.e. separate steps for "Plated Holes" and for "Unplated Thru-Holes"

Note that from Mentor's point of view the mechanical mounting holes for the front panel and for the board stiffeners are Unplated.

Generate the Plated Holes:

Excellon, ASCII, NO Mirror, Board,

Drill Hole Types: Plated_Holes, By Pin/Via Rules

Physical_1 to Physical_3 YES
Physical_1 to Physical_13 YES

i.e. click Generate All

Click "OK" at the bottom

In the .../mfg/ directory this should make the files: drill_1_3 and drill_1_13

Generate the UnPlated Holes:

Excellon, ASCII, NO Mirror, Board,

Drill Hole Types: UnPlated Thru-Holes

Click "OK" at the bottom

In the .../mfg/ directory this should make the file: drill_unplt

Report the Drill Table (from Report Pull Down Menu)
Include the Drill Format
Save and Display the Report
Save Report to Design with .../Work/Text/ filename
Replace the existing Report

Look at the Simulation of the Drill Data and find:
based on 16-Oct-2013

Drill_1_13

Drill Position	Drill Size	Count	Plated	Function
2	0.3	7137	yes	small vias bga pins
3	0.6	1761	yes	bigger vias backplane conn
4	0.7	136	yes	mdr 68 pin front panel conn
5	0.9	16	yes	2x8 front panel connector
6	1.0	32	yes	AWG22 WRAP vias & SFP Cage pin
8	1.1	36	yes	SFP Cage pins
10	1.2	40	yes	SFP Cage pins
11	1.3	95	yes	DC/DC Converter pins
14	2.0	10	yes	MiniPOD mounting screw pins
16	2.3	2	yes	CF_Socket mountng screw pins
17	2.7	4	yes	m2.5 mounting screw pins
18	3.0	38	yes	4-40 mounting screw pins

Drill_1_3

Drill Position	Drill Size	Count	Plated	Function
1	0.25	967	yes	blind vias

Drill_Unplated

Drill Position	Drill Size	Count	Plated	Function
7	1.0	10	no	CF_Socket Header_2x20 TTCDec
9	1.1	10	no	LED alignment
12	1.55	17	no	SFP MiniPOD CANBus Proc Conn
13	1.75	2	no	CF_Socket
15	2.0	3	no	Power Conn alignment
19	3.18	2	no	Backplane Pin Receptacle

Viewing Drill Data:

Right Click --> Drill --> Simulate Drill Data

Note that currently the default FabLink grid is 0.005 mm and thus its hard to measure anything. This is clearly left over from an English project and needs to be changed.

=-=

The actual PCB stackup that is used to manufacture the bare CMX PCBs is given in:

http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/manufacturing/

for_production/cmx_stackup_fr4_14jan2014.pdf

=-=

Appendix W: Heat Sinks

The mechanical drawings for the heat sinks are in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/heat_sinks/

A current snapshot of the detailed description is included below while the source material is in cmx_ab_heat_sinks.txt found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
              CMX  Heat-Sinks  FPGA and MiniPOD
            ---------------------------------------

                                        Original Rev. 18-Feb-2013
                                         Current Rev. 25-Apr-2014


The CMX card requires heat sinks for two component types:
the Virtex FPGAs and the MiniPOD optical components.
These two applications will require different types of
heat sinks and will be described separately.


Virtex FPGA Heat Sinks:
-----------------------

The Virtex FPGAs on the CMX card are in the Xilinx FFG1759
package.

 - This package has a 42.5 mm square metal top thermal contact.

 - The absolute maximum junction temperature of the Virtex
   FPGAs used on the CMX card is 85 deg C.

 - The expected thermal resistance from the junction to the
   top metal thermal contact lid is about 0.1 Deg C per Watt.
   There is a parallel junction to board thermal resistance
   of about 2.0 deg C per Watt.

 - The heat dissipation in the CMX Virtex FPGAs is estimated
   to be  > 7 Watts    < 30 Watts.

 - The surface of the top metal thermal contact lid is between
   2.80 and 3.50 mm above the upper surface of the pcb.
   I do not know how parallel we can assume that the FFG1759
   lid will be to the CMX circuit board.

 - To be within specifications, the maximum height of any
   component on a VME card is  13.716mm.  If we assume
   the maximum 3.50mm mounting height for the FFG1759 this
   implies that the heat sink can be at the most  10.2 mm
   tall   ( 0.402 inches tall ).   This is not enough height
   to use a heat sink with a built in fan
```

- The expected air flow velocity in the VME card crate
  is at least 200 feet/minute or 1 meter per second.

- I will assume that the air inlet temperature is 30 deg C
  or less.

- One must control the force of the heat sink against the
  top metal thermal contact lid of the FFG1759 package.
  A rational force is 30 pounds. Numbers range from 5
  to 70 pounds. Typically you need 300 kPa (43 lb/sq_in)
  to get full thermal connection with a thermal grease TIM.
  The contact lid of the FFG1759 is about 2.8 sq_in which
  implies 120 lb of clamp force for full thermal contact.

- There is not enough space on the back side of the card to
  include a stiffener aka force spreader under the BGA
  package. Thus we are limited in how much force we may
  use to clamp the heat sink to the Virtex FPGA.

- Springs are used on the top side of the heat sink to
  control the force of the heat sink against the lid of
  FFG1759 package.

- Extra attachment bolts are used out, near the perimeter
  of the heat sink, that do not apply clamping force, but
  rather just control / limit the movement of the heat sink
  relative to the card.

- The bolts that apply clamping force to the heat sink are
  located symmetrically around the FPGA package so that the
  heat sink will remain flat against the FFG1759 lid.

- If done right the expected thermal resistance in the
  joint between the FFG1759 lid and the heat sink is
  0.1 deg C per Watt.

- The lowest expected mounting height of the FFG1759
  (2.80mm) allows enough space between the circuit board
  and the bottom of the heat sink to mount all of the
  capacitor types that need to be close to the FPGAs.
  Specifically the expected capacitor heights are:
  0.87mm for the 100 and 220 nFd,   1.40mm for the 4.7 uFd
  2.10mm for the 33 uFd tantalum. The bottom of the heat
  sink needs to be milled to provide clearance for any
  taller components that it covers.

- The heat flow out of the silicon will be on two main paths:

    junction to top lid through interface to heat sink
    then from the heat sink to ambient

  and a parallel path of:

    junction to board then board to ambient

I have manufacturer's numbers for all of these thermal resistances except for the board to ambient. The board to ambient thermal resistance obviously depends on the details of the board design and the air flow around the board.

For the CMX, its board to ambient thermal resistance is probably pretty low because of the 10 full coverage Ground layers and because some of these layers are close to the surface of the card. This thermal resistance probably not more than 3 deg C per Watt. The 10 ground planes are 1/2 oz which gives an overall ground thickness of 5 oz or about 7 mils of copper.

- The Xilinx white paper 258 indicates that a typical heat sink design will result in *about* 25% of the heat going out through the board and about 75% of the heat going out through the package lid and heat sink.

- What is the temperature of the air coming out of the heat sink with this 30 Watt load and with 30 deg C air going into the heat sink ?

  The heat capacity of air is about 36 Joules per cubic foot deg C i.e. 36 Watts will rise 1 cu_ft 1 deg C in 1 second.

  The cross section of the air flow through the heat sink is about 0.013 sq ft. With 200 linear ft/min flow through the heat sink this gives about 2.5 cu_ft / min or about 0.04 cu_ft / sec flowing through the heat sink.

  There is about 75% of 30 Watts or 22.5 Watts going into the heat sink. This is enough heat to rise 1 cu_ft per second of air 0.625 deg C. But we have only 0.04 cu_ft per second flowing through the heat sink which gives an air temperature rise of about 15.6 deg C.

- What is the power limit without a heat sink but running vertical in the crate with 250 LFM air flow ?

  Without a heat sink but with 250 linear feet/min air flow the FFG1759 package has a junction to ambient thermal resistance of 4.7 deg C per Watt. This is in parallel with the 2 + 3 deg C / Watt thermal resistance for heat flowing out through the circuit board. This gives an overall thermal resistance of about 2.42 deg C / Watt junction to ambient.

  With a 30 Watt load and 30 deg C input air this would give 103 deg C silicon temperature.

  With a 22 Watt load and 30 deg C input air this would give 83 deg C silicon temperature.

With a 16 Watt load and 30 deg C input air this would give 69 deg C silicon temperature.

- What is the power limit without a heat sink and running flat on the bench without forced air flow ?

  Without a heat sink and without forced air flow the FFG1759 package has a junction to ambient thermal resistance of 7.8 deg C per Watt. This is in parallel with the 2 + 7 deg C / Watt thermal resistance for heat flowing out through the circuit board. The 7 deg C / Watt board to ambient comes from the board being flat on the bench. This gives an overall thermal resistance of about 4.2 deg C / Watt junction to ambient.

  With the 7 Watt quiescent heat load and 30 deg C ambient air this gives a silicon temperature of 59 deg C

  With a 9.5 Watt heat load and 30 deg C ambient air this gives a silicon temperature of 70 deg C.

- Some of the possible errors in the above design estimates:

  The BF heat sink is down stream from the hot air that could come out of the TP heat sink and thus BF FPGA silicon temperature may be hotter than indicated above.

  The heat sink is close to the pcb and thus has limited air flow under it. The published thermal resistance data for the heat sink assumed air flow all around it. About 18% of the heat sink's surface area is the surface on its bottom side next to the pcb which may have limited air flow.

  The board to ambient thermal resistance is only an estimate and needs to be studied or measured.

  The heat sink may work slightly better than the manufacturer's data because the heat is passed to the sink over 42.5mm x 42.5mm rather than over 1 sq inch.

  There are many more sources of error in these estimates.

- A stock heat sink extrusion with good fin design for the CMX Virtex application is QATS types: ATS-EXL1-254-R0. The ATS-EXL1-254-R0 is $51.71 ea in small quantity.

- Specifications of the ATS-EXL1-254-R0 material:
  100.0mm wide
  10.0mm height overall
  2.0mm base thickness --> 8.0mm tall fins
  2.5mm fin center to center aprox.
  ?mm width of a fin
  ?mm width of the gap between fins
  40 fins in the 100mm width, edge fins are full width
  5 deg C per Watt thermal resistance for a 76mm
  long section and 200 linear feet/min air flow.
  31.0 sq inch per inch of length total surface area
  calculated from perimeter 33.2 sq_in / inch

- The final decision is to use ATS Part No: ATS-EXL1-254-R0
  Heat Sink Extrusion for the BF and TP Virtex FPGAs.
  This is a 100mm x 254mm x 10mm extrusion.

- The final drawings of the BF and TP Virtex FPGA Heat Sinks
  and the details of mounting these heat sinks are in:

  http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/heat_sinks/

  m1_base_function_fpga_heat_sink.pdf
  m2_topological_fpga_heat_sink.pdf
  m20_fpga_heat_sink_mounting.pdf

- After manufacture in the MSU Physics Machine Shop the CMX
  Virtex heat sinks were black anodized.

- The details of mounting these Virtex heat sinks onto the CMX
  card and the hardware, springs, and thermal compound used to
  mount them are given in the Final Assembly document.

MiniPOD Heat Sinks:

- The MiniPOD heat sink from Avago is 17mm x 20mm mounts
  on top of the MiniPOD and has 20 prongs that stick up
  into the air flow.

- Each of these 20 prongs has a 2mm x 2mm cross section and
  is 10 mm long. 80 sq_mm per prong. (20 x 80 sq_mm) +
  (17mm x 20mm) = 1940 sq_mm total exposed surface on the
  Avago MiniPOD heat sink.

- I have not identified exactly what manufacturer and part
  number the Avago MiniPOD heat sink is but from looking
  at similar parts it probably has a thermal resistance in
  the range of 20 to 25 deg C / Watt at 200 LFM air flow.

- The Avago heat sink uses a spring clip mount and there
  are no specific mounting instructions that I know of.

- Avago data sheet specification:

```
  Maximum Operating Case Temperature:   70 deg C
       Module Top Surface Load Limit:    3 Kg
    Transmitter 2.5 Volt Current Max:  400 mA
    Transmitter 3.3 Volt Current Max:  160 mA
            --> Transmitter Heat Max:  1.6 Watts
       Receiver 2.5 Volt Current Max:  525 mA
       Receiver 3.3 Volt Current Max:   90 mA
               --> Receiver Heat Max:  1.6 Watts
```

- So with 1.6 Watts of heat and 30 deg C cooling air
  and a maximum case temperature of 70 deg C we need
  a case to ambient thermal resistance of 25 deg C / Watt
  or less.

- We need to use some kind of heat sink that is in the range
  of 20 to 25 deg C / Watt thermal resistance. Obviously
  because of its height, the Avago supplied heat sink can
  not be used on the CMX card.

- Our MiniPOD heat sink design fits down over the sides of
  the MiniPODs and attaches to the MiniPOD with thermal epoxy.

- As placed on the CMX there is enough space for an 18mm
  wing to the East and enough space for a 4mm bar on the
  North and South side. This the heat sink stock material
  needs to be at least 18 + 18 + 22 = 58mm East-West
  and 4 + 4 + 18 = 26mm North-South.

- The heat sink sits on the bottom edge of the side skirt
  and thus can be at the most 8mm high.

- The aluminum extrusion bar stock that was used to make
  the CMX MiniPOD heat sinks is: Alexandria Industries
  Extrusion Part Number: MM12854

  This material is 38mm wide and comes in 6 ft bars.

- To make the heat sinks the bar stock is cut into 28mm
  lengths and then wire EDM is used to cut the fancy shaped
  hole in the center that fits down over the MiniPOD. This
  is a nice snug fit on the shoulders of the MiniPOD

- The final drawings of the MiniPOD Heat Sink is in:

    http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/drawings/heat_sinks/

      m21_minipod_heat_sink_blank.pdf
      m22_minipod_heat_sink_hole.pdf

- The finished heat sink is anodized black and then attached
  to the MiniPOD using Wakefield Part Number: DeltaBond 155
  thermal epoxy.

Appendix X: Final Assembly

Photos of the CMX card can be found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/photos/

A current snapshot of the detailed description is included below while the source material is in cmx_ab_final_assembly.txt found in
http://www.pa.msu.edu/hep/atlas/l1calo/cmx/hardware/details/

```
          CMX  Final Assembly and Initial Power Up
        ---------------------------------------------


                                              Original Rev.  5-Dec-2013
                                               Current Rev. 25-Apr-2014


This note describes the "Final Assembly" steps that are
required for each CMX card.  This final assembly work is
done here at MSU.  A separate later section of this note
describes the procedure for the "Initial Power Up" of each
CMX card.

All work on the CMX cards should be done at an anti-static
work station while wearing a grounding wrist strap.

Do not unnecessarily flex the CMX circuit board.  This is
especially important before the front panel and stiffener
bars have been installed.


CMX Final Assembly:
-------------------


1. Write the Serial Number on the CMX card.  Serial numbers
   will start with SN #00  for the initial CMX card without
   either of the Virtex FPGAs on it.  Serial numbers are
   expected to run through SN #23.   The intent is that all
   cards with serial number => 1  will be available for
   Physics use.


2. Start an entry in the CMX Trailer Sheet file for the
   CMX card that you are now starting final assembly on.


3. Inspection before starting the Mechanical Final Assembly:

   - The purpose of this examination is to verify that this
     CMX card is in good physical condition and thus it is
     OK to proceed with this Mechanical Final Assembly.
```

- Verify that the edges and corners of the card are not damaged.

- Verify that the CMX card look flat when it is not under stress. We do not want a card that is warped to be flattened by the front panel and stiffener bars.

- Verify that the upper and lower card edges have been milled, from the back side, to the nominal 62 mil thickness.

- Verify that the connectors, SFP Cages and LEDs along the front panel edge of the card look straight and in the correct positions to fit with the front panel.

- Verify that 8 press in backplane connectors look fully inserted and correctly aligned. Verify that the 3 pin backplane power connector looks correctly installed.

- Check the back side of the card for damaged components. Specifically check the tallest back side components which are the 0805 ceramic capacitors. None of these should be cracked or broken off.

- Check the top side of the card for damaged components. Carefully examine the tallest components and the components nearest the edges. Look for folded over pins on the TSSOP packages. Look for contamination under the BGA packages. Verify that the various connectors on the top side of the card are in the correct orientation (2mm HM connectors, Meg Array connectors for the MiniPODs, TTCDec Samtec connectors, and CAN-Bus CPU connectors).

4. Mechanical Final Assembly:

- Attach the Rear Guide Pin Receptacle Block:

  . Press the two splined pins of the Guide Pin Receptacle into the CMX card using our small arbor press. The splined pins stick out of the bottom side of the card so you must use a platen under the card to support it.

  . Verify that this guide pin receptacle is fully pressed into the card and then lock it in place by applying one or two drops of super glue to the splines on these pins from the back side of the card.

  . Let this glue cure with the back side of the card facing up in a well ventilated area.

- Attach the Front Panel and Stiffener Bars:

  . Loosely screw the Upper and Lower Brackets to the CMX card using 10 mm M2.5 Cheese Head screws.

. Very loosely attach the Upper and Rear Stiffener Bards to the circuit board using 3/8" 4-40 Button Head screws.

. Attach the Rear Stiffener Bar to the Upper Stiffener Bar using a 7/16" 4-40 Flat Head screw. Fully tighten this screw. This screw head fits down behind the Guide Pin Receptacle and you will not be able to access it once the stiffener bars are screwed down against the circuit board.

. Loosely attach the Lower Stiffener Bar using 3/8" 4-40 Button Head screws in all locations except for the screw that runs through into the Rear Stiffener Bar. In that location use a 5/8" 4-40 Button Head screw.

. Loosely attach the Upper and Lower Stiffener Bars to the Upper and Lower Brackets using 5/16" 4-40 Flat Head screws.

. Loosely attach the front panel to the CMX card via the J10 and J11 connectors using 1/4" 4-40 Button Head screws.

. Slip the VME Insert/Eject Handles into place. Note that the Upper and Lower Handles are different. Loosely attach each handle to the circuit board with a 6 mm M2.5 Cheese head screw. Loosely attach each handle through the front panel to its bracket using a 12 mm M2.5 Cheese Head screw. Note that the threaded area in the handle for this screw has been drilled to an M2.5 body drill size.

. All of the Front Panel and Stiffener Bar mechanical parts have now been mounted on the circuit board. Now in multiple passes begin tightening all of these screws. Verify that the circuit board remains flat and does not warp as all of these screws are slowly tightened pass after pass. Verify the the VME Insert/Eject Handles are square to the pcb as these screws are tightened. Recall that the screw that holds the Rear Stiffener Bar to the Upper Stiffener Bar must have already been fully tightened.

. The final step in the front panel assembly is to install the two MTP feedthrough optical connectors. They snap into the front panel when inserted from the exterior surface. Typically the corners of these feedthrough connectors need to be scraped clean with an exacto-knife to allow them to fit into the hole in the front panel. We are mounting these feedthrough connectors with their metal clip up away from the circuit board.

- Attach the Flash Card Socket:

. Install two M2 x 10mm screws and nuts to hold the Flash Card socket in place. Tighten these far enough so that the compression of the FC socket plastic will keep them from coming loose. There are pockets on the top side of the FC socket to receive these M2 hex nuts.

- Attach the Virtex Heat Sinks:

  . Before starting the steps to attach the Base Function FPGA Heat Sink (and possibly the Topological FPGA Heat Sink) make a final careful examination of the whole area that will be covered by these heat sinks. Many bypass capacitors and other components will be "permanently" hidden once these heat sinks are in place. Carefully examine the FPGAs themselves and the BGA area under the FPGA. Verify that the FPGA is mounted flat and parallel to the surface of the pcb and that no foreign matter is trapped in the BGA pins under the FPGA.

  . Install the four 3/4" 4-40 Button Head screws and three 1/2" 4-40 Button Head screws that are used to attach each Virtex Heat Sink to the circuit board. The 3/4" screws must have already been ground down in length by 65 mils. These shortened 3/4" screws are used in the positions with the compression springs. The 1/2" length screws are used in three corners for motion limit control

    These screws are installed using special thin nuts with a nylon lock collar (McMaster 90101A004). The screw threads MUST be lubricated with 50 wt oil before these nuts are installed. These stainless screws will gall if they are not lubricated before installing these lock nuts. No washers are used under these screw heads or nuts because there is no space for such washers.

    Tighten these screws enough so that the nuts will hold them in place. Be careful not to over-tighten these screws or to let the screw head or nut cut into the circuit board. To provide something like a washer, there is copper on the circuit board where the screw head and nut will press together. Check for burrs on the screw heads and nuts before using them. Carefully tighten these parts using a nut driver while holding the screw head with a nut driver.

  . Test fit the heat sink to verify that it will fit over the 7 screws and rest squarely on the FPGA heat spreader. Note the area on the bottom of the heat sink that will actually be in contact with the heat spreader on top of the FPGA.

  . Clean the top of the FPGA and the bottom of the heat sink. Any foreign material in this area will interfere with good heat transfer.

  . Apply the heat sink compound. There are at least 2 theories on the best way to do this. 1) one blob in the dead center with no trapped air but will take a long time to squish down 2) try to spread on a thin even layer which will without doubt trap some air when the heat sink

and FPGA are clamped together. Trapped air --> almost no heat transfer. Large excess amounts of heat sink compound do nothing to transfer heat, are a mess, and can leak out.

On these parts the scheme that appears to work best is to apply 5 small blobs to to the top of the FPGA; one in the center and 4 nearer the corners. Note that the fancy heat sink compound that we obtained for this application makes a good enough seal between the FPGA and its heat sink that it is difficult to remove the heat sinks once it is installed. It is easy to rotate the heat sink but it will not pull off from the FPGA. Don't try pulling hard or the FPGA may pull off from the circuit board. A synthetic heat sink thermal compound is used in CMX card assembly. It is Wakefield Part Number: 126-2.

. Assembly the heat sink down over its 7 screws and onto the FPGA. The 4 clamping screws closest to the FPGA each receive a compressing spring (currently a Jones Spring Part Number: C06-026-010 which will provide about 4.8 lbs of clamp force each at a 5.4 mm compressed height) and a thin nut with a nylon lock collar. Again there is no vertical space available for washers. One must hold the screw heat with an allen key when tightening these lock nuts over the springs with a nut driver. Obviously these nuts must be tightened in a series of small steps to keep the pressure event, the heat sink flat against the FPGA, and not to warp or flex the circuit board. The current target is that the tops of these 4 nuts should be just even with the top of the heat sink fins when they are tightened far enough. It may take some time for the heat sink compound to evenly squeeze out from between the heat sink and the top of the FPGA. Thus the apparent compressed height of the springs may change for some time.

. Once the 4 clamping screws are in place then the 3 movement limit control nuts may be installed. Again we are using a thin nut with a nylon lock collar for this application. These nuts are installed with a nut driver while holding the screw head with an allen key. Run these nuts down on their screws until they are about 0.5 mm short of touching the top surface of the heat sink. Their purpose is to limit the movement of the heat sink if it gets banged and thus give some protection to the FPGA and its BGA connections.

. A post assembly inspection of a Virtex heat sink should verify that it is flat and parallel to the circuit board, that the circuit board is still flat and not warped, and that no foreign material is trapped under the heat sink. Both the upper and lower nuts on the 3 movement limit control screws should be just short of actually touching the surface of the heat sink.

- Attach the MiniPODs with their Heat Sinks:

  . Assume that the MiniPOD Heat Sinks have already been attached to the MiniPODs with thermo epoxy (Wakefield part number #155).

  . Make a final inspection of the area of the CMX circuit board where this MiniPOD is going to be installed. Once this MiniPOD and its Heat Sink are installed this area of the circuit board will be "permanently" covered. Check that the Meg Array connector on the CMX looks straight and that nothing is trapped under its BGA foot print. Check for damaged capacitors bypass and DC-Blocking in the area that will be covered. Check the small 0201 capacitors that are around each of the Receiver MiniPODs.

  . Remove the covers on the CMX and MiniPOD Meg Array connectors. Verify that everything is clean and free of foreign material in these connectors before they are put together.

  . The Meg Array document fci_specification_gs-20-033.pdf describes how to rock these connectors as they are being pressed together. Do not put force on the heat sink. Do not flex the CMX card. Do not allow the optical cover on the MiniPOD to open. The two Meg-Array connectors should fit fully together with the application of a rational force.

  . Install two M1.6 x 8mm screws into each MiniPOD from the bottom of the circuit board to hold the MiniPOD in place.

- Attach a "Pig Tail" optical cable to the MiniPOD and run it to the Front Panel MTP Connector Housing

  . Practice making both of these connections with test/demo parts before working with the real production parts.

  . We want to do this optical assembly work in a clean room area.

  . Clean the top area of the MiniPOD and the MTP connector housings with compressed air before removing any of the dust covers.

  . Remove the dust cover (rubber optical cover) from the top of the MiniPOD. Install the MiniPOD end of the optical pig tail cable and then replace the rubber dust cover verifying that it is full pressed into the MiniPOD. The sealing flaps on the rubber dust cover need to be directed outward to allow it to fit fully down in place. The optical cable routes out through the center area of the Heat Sink where a fin has been removed for this purpose.

. Route and clamp the optical cable in the path on the CMX card that has been designed for it. Once the optical ribbon cable is plugged into the MTP connector then attach optical ribbon cable to the circuit board at places along this route using RTV.

. Remove the dust covers from the MTP end of the optical pig tail cable. Install the MTP cable connector into the MTP feedthrough housing. Do not remove the MTP housing dust cover from the exterior side of the CMX Front Panel.

5. Electrical Final Assembly:

- The exact set of steps to be performed during the Electrical Final Assembly depend on a number of things, e.g. does this CMX card have a Topological FPGA installed on it. One needs to be familiar with the contents of the file:

  cmx_ab_board_jumpers.txt

  and understand what jumpers have been installed by default during the CMX card assembly process. At the time of this writing there are some aspects of Electrical Final Assembly that are still questions, e.g. the desired dynamic range of the various voltage and current monitor readout circuits. In general the following notes apply to the standard type of CMX circuit board without a Topological FPGA.

  Much of the Electrical Final Assembly work consists of installing 0805 size SMD resistors. The resistors that are now being installed were not installed during the production process either because their value was not known at that time or because they are a one of a kind part and we wanted to limit the number of spools in use during the main assembly process. To make these resistors easy to install, in most cases, their SMD land pattern has only one solder blob on it from the production process. The installation of these resistors is facilitated if the various required resistor values are available in a labeled tray.

- Install the Hi/Low Voltage Monitor Power OK Resistors

  . There are 24 of these resistors. Note that these parts have been called Res_x.yzk_Ohm_0805 in the Mentor comps file and raw Mentor BOM file. The SMD pattern for these 24 resistors has only one solder blob.

. Install the following parts all of which are on the back side of the circuit board immediately under U1861 & U1862.

	Rx	Ry	Rz
BULK_2V5 OK Lim	R1861 2000 Ohm	R1862 49.9 Ohm	R1863 475 Ohm
BULK_3V3 OK Lim	R1864 2800 Ohm	R1865 49.9 Ohm	R1866 475 Ohm
TP_Core OK Lim	R1867 475 Ohm	R1868 49.9 Ohm	R1869 475 Ohm
GTX_AVCC OK Lim	R1870 887 Ohm	R1871 49.9 Ohm	R1872 825 Ohm
GTX_AVTT OK Lim	R1873 680 Ohm	R1874 49.9 Ohm	R1875 475 Ohm
BF_Core OK Lim	R1876 475 Ohm	R1877 49.9 Ohm	R1878 475 Ohm
BSPT_Core OK Lim	R1879 680 Ohm	R1880 49.9 Ohm	R1881 475 Ohm
BULK_5V0 OK Lim	R1882 4530 Ohm	R1883 100 Ohm	R1884 475 Ohm

. These resistor values in the voltage dividers will result in the following nominal Hi/Low Voltage Monitor trip points:

	Center of OK Range	Low Trip	Hi Trip	Voltage Tolerance
BULK_2V5 OK Lim	2.531 V	2.405 V	2.658 V	+- 5.0 %
BULK_3V3 OK Lim	3.334	3.167	3.500	+- 5.0 %
TP_Core OK Lim	1.002	0.952	1.053	+- 5.0 %
GTX_AVCC OK Lim	1.037	1.007	1.068	+- 2.9 %
GTX_AVTT OK Lim	1.208	1.148	1.268	+- 5.0 %
BF_Core OK Lim	1.002	0.952	1.053	+- 5.0 %
BSPT_Core OK Lim	1.208	1.148	1.268	+- 5.0 %
BULK_5V0 OK Lim	4.906	4.439	5.374	+- 9.5 %

. This set of resistors provides about 1.0 mA of standing current in all dividers except for the GTX_AVCC supply which has about 0.59 mA standing current in its divider.

. This setup of the Hi/Low Voltage Monitor dividers requires a total of 9 resistor values.

. The most critical supply on the CMX card is the GTX_AVCC bus. This 1.030 Volt bus has a +- 30 mV tolerance, i.e. +- 2.9%.

Base Function FPGA GTX_AVCC feed resistance:

We anticipate a load of about 1.68 Amps on this supply from the Base Function FPGA. The resistance of the fill routing and filter inductor to the BF FPGA should be about 2.6 mOhm + 6.4 mOhm = 9 mOhm --> 15 mV drop.

Topological FPGA GTX_AVCC feed resistance:

We anticipate a load of about 2.13 Amps on this supply from the Topological FPGA. The resistance of the fill routing and filter inductor to the BF FPGA should be about 5.3 mOhm + 6.4 mOhm = 12 mOhm --> 25 mV drop.

Thus we will probably tune the output of the GTX_AVCC supply to about 1.040 Volts. From the data sheet the Virtex 6 GTX_AVCC Absolute Maximum is 1.100 Volts.

. A special connection is needed when the TP_CORE supply is not going to be used. Even without the TP_CORE DC/DC running we need to have the Hi/Low Voltage Monitor provide an all supplies are OK signal (for all 8 monitored voltages). The cleanest way to obtain this is:
do not install R1867, R1868, R1869
jumper the R1867-R1868 node to the R1864-R1865 node
jumper the R1868-R1869 node to the R1865-R1866 node
i.e. have the TP_CORE monitor watch the BULK_3V3 supply.

- Install the DC/DC Converter Output Voltage Set Resistors

. There are 7 of these resistors. The SMD pattern for these 7 resistors has only one solder blob.

. Install the following 7 parts all of which are on the back side of the circuit board under the associated DC/DC Converter.

. These resistors together with the variable trim pot that is associated with each converter control the output voltage from that converter.

Converter	Nominal Output Voltage	Install Resistor Refer Desig	Install Resistor Value Ohms	Expected Adjstmt Range Low Limit	Expected Adjstmt Range High Limit	Trim Pot Ohms
DCDC1 BULK_2V5	2.500	R1504	2.10k	2.402	2.645	500
DCDC2 BULK_3V3	3.300	R1554	953	3.083	3.586	500
DCDC3 TP_Core	1.000	R1604	53.6k	0.963	1.051	20k
DCDC4 GTX_AVCC	1.030	R1654	16.5k	0.991	1.075	5k
DCDC5 GTX_AVTT	1.200	R1704	9.76k	1.116	1.307	5k
DCDC6 BF_Core	1.000	R1754	53.6k	0.963	1.051	20k
DCDC7 BSPT_Core	1.200	R1804	9.76k	1.116	1.307	5k

. For details see page 7 of the CMX schematics.

. For details about the output voltage Rset control resistor in these TI DCDC Converters:
  see the PTH04T240 data sheet page 12.
  see the PTH04T220 data sheet page 11.
  see the PTH05T210 data sheet page 8.

- Install the DCDC Converter Input Current Monitor Scale Set Resistors

. These 14 resistors control the scale of the output voltage from the Hi-Side Current Monitors that watch the input current to each of the DC/DC Converts.

Converter	Install Resistors Reference Designators	Install Resistors Value Ohms	Sense Resistor mOhms	LT6105 Volts Out per Amp In	Vout =1.5V --> F.S. Amps
DCDC1 BULK_2V5	R1502 R1503	115	5	0.200V	7.5 A
DCDC2 BULK_3V3	R1552 R1553	115	5	0.200	7.5
DCDC3 TP_Core	R1602 R1603	115	5	0.200	7.5
DCDC4 GTX_AVCC	R1652 R1653	115	10	0.400	3.75
DCDC5 GTX_AVTT	R1702 R1703	115	10	0.400	3.75
DCDC6 BF_Core	R1752 R1753	115	5	0.200	7.5
DCDC7 BSPT_Core	R1802 R1803	115	10	0.400	3.75

. See the Linear Technology LT6105 data sheet for details about the current sense amplifier output voltage vs series sense resistor voltage drop relationship. See pages 1 and 11. Basically,

  Vout = sense drop * (Rout / Rin) with a 1 mA max on Vout.

It is not absolutely clear how hi of a voltage the LT6105's Vout pin can pull to. It appears that in all of the modes that we will use this part that its Vout will pull to at least + 1.5 Volts.

The Rout/Rin gain of 40.00 indicated above assumes that the 4.7k Rout resistor is shunted by about 216.2k Ohm in the voltage divider that feeds the Virtex System Monitor. Without this 216.2k Ohm shunt the Rout/Rin gain gain is about 40.87

. For all 7 DCDC Converts we have installed an Rout e.g. R1507 that is 4.70k Ohm (not 4.99k).

. Recall that the full scale input to the CAN-Bus uProcessor is 4.096 Volts and that it is an 8 bit converter, i.e. only the upper 8 bits of this converters 10 bit output have any significance. The LSBit of this 8 bit value represents about either 80 mA or 40 mA depending on the scale indicated in the table above.

. Recall that the full scale input to the Virtex System Monitor is 1.000 Volts and that you basically have a 10 bit converter. These Current Monitor voltage signals go through a resistor divider attenuation of 0.5 before they go into the to the Virtex System Monitor Analog Inputs. The LSBit of this 10 bit value represents about either 9.8 mA or 4.9 mA depending on the scale indicated in the table above.

. For details see pages 4, 5, and 35 of the CMX schematics.

- Install the one of a kind resistors in the Select I/O VRef_P supply

. There are 3 of these resistors. The Select I/O VRef_P supply is located just above the Base Function MiniPODs. These 3 resistors are located on the back side of the circuit board.

. Install the following 0805 1% resistors:

R1922	3.74k Ohm	Select I/O VRef_P Voltage Set Range
R1923	11.8k Ohm	Select I/O VRef_P OpAmp Gain Set
R1925	10 Ohm	Select I/O VRef_P Series Isolate

. With these resistor values the range of the VRef_P Supply output voltage should be adjustable via trim pot R1921 from +0.75 Volts up to +1.75 Volts. In any case the output of the VRef_P supply is clamped at about 2.4 Volts by zener diode U1923.

. The 400 Backplane Processor Input signals are 2.5 Volt CMOS signal levels. The intent is to have a VRef_P supply for these Processor Input signals that is adjustable by +- 0.500 Volt either side of their nominal 1.250 Volt center threshold.

. For details see page 6 of the CMX schematics.

- Install the 2 EDS Strip Resistors.

. These resistors are located on the Top side of the circuit board. Both of them are right next to the EDS Strips.

R631 is located just East of the Can-Bus uProcessor
R632 is located just East of Converter DCDC7

. Install the following 0805 1% resistors:

R631	1 Meg Ohm	EDS Strip Ground Resistor
R632	1 Meg Ohm	EDS Strip Ground Resistor

- Install the Scale Setting Resistors for the Virtex System Monitor Readout

. There are 24 resistors that are used to scale the analog signals that are sent to the Base Function Virtex System Monitor ADC Mux Inputs. These are 0805 SMD resistors R1941 through R1964.

. Install the following 0805 1% or 0.1% resistors. They are located on the top and bottom sides of the circuit board just under the J13 monitor connector.

Refer Desig	Value	Monitored Quantity	Gain	SysMon Input	LSB Scale
R1941	100k Ohm	BF_Core V	0.50	4	1.955 mV
R1942	100k Ohm				
R1943	100k Ohm	BF_Core I	0.50	3	9.775 mA
R1944	100k Ohm				
R1945	100k Ohm	GTX_AVTT V	0.50	1	1.955 mV
R1946	100k Ohm				
R1947	100k Ohm	GTX_AVTT I	0.50	7	4.888 mA
R1948	100k Ohm				
R1949	100k Ohm	GTX_AVCC V	0.50	11	1.955 mV
R1950	100k Ohm				
R1951	100k Ohm	GTX_AVCC I	0.50	8	4.888 mA
R1952	100k Ohm				
R1953	100k Ohm	TP_Core I	0.50	14	9.775 mA

R1954	100k Ohm				
R1955	300k Ohm	BULK_3V3 V	0.25	12	3.910 mV
R1956	100k Ohm				
R1957	100k Ohm	BULK_3V3 I	0.50	10	9.775 mA
R1958	100k Ohm				
R1959	300k Ohm	BULK_2V5 V	0.25	9	3.910 mV
R1960	100k Ohm				
R1961	100k Ohm	BULK_2V5 I	0.50	13	9.775 mA
R1962	100k Ohm				
R1963	100k Ohm	Select I/O	0.50	15	1.955 mV
R1964	100k Ohm	VRef_P V			

. The LSB Scale is based on assuming that the System Monitor ADC has a 1 Volt Full Scale Input and will be used to produce 10 bit outputs, i.e. the LBS of the raw converter is about 1 Volt / 1023 = 0.978 mV per LSB.

- Install resistors to scale the BULK_5V0 CAN-Bus monitor signal:

. The BULK_5V0 input to the CAN-Bus uProcessor ADC is by default above the 4.096 Volt level that this ADC can correctly digitize. The solution is to attenuate this BULK_5V0 monitor signal before it enters the CAN-Bus ADC. This will be accomplished by:

. Remove the 100 Ohm resistor that is installed at location R1915 just above the J13 monitor connector on the top side of the circuit board. Install a 1.00k Ohm resistor.

. Install a 2.80k Ohm resistor parallel to C1885 on the top side of the circuit board just under connector J13.

. The BULK_5V0 monitor signal to both the J13 connector and to the Channel #7 input to the Can-Bus ADC is now attenuated by a factor of 0.7368 When read by the CAN-Bus ADC the BULK_5V0 monitor signal will now have a scaler factor of about 1/0.7368 x 4.096 Volts divided by 255 counts = 21.80 mV per count (assuming an 8 bit ADC value from the CAN-Bus uProcessor). That is, every LSB from the ADC implies 21.80 mV of BULK_5V0 supply.

. Pin #29 on connector J13 still allows monitoring of the BULK_5V0 supply but it now has a scale factor of 0.7368 built into what you read there with a DVM. E.G. if the DVM reads 3.684 Volts on J13 pin 29 it means that BULK_5V0 supply is 5.000 Volts.

- Install the Main Power Input Fuse - F1

  . Because it may need to carry up to 20 Amps under normal operating conditions a standard (i.e. large) 1/4" x 1 1/4" ceramic cartridge type fuse and holder are used for the F1 - Main Power Input Fuse on the CMX circuit board.

  . The holder for the F1- Main Power Input fuse is mechanically attached to the Rear Stiffener Bar about 3.7" up from the lower end of this bar.

  . The backplane +5V power enters the CMX card via the bottom pin on the backplane J9 connector and arrives at 4 vias labeled WRP1:WRP4 in the SE corner of the circuit board just inside the stiffener bars. Wires are installed to connect these 4 vias to the lower terminal on the F1 Fuse Holder. Use the specified #22 AWG wire to make these connections. The insulation covered section of these 4 wires is about: 48, 52, 56, and 60 mm long. Tin the end that is to be soldered into the via. Use liquid flux on the via tunnel. Use an appropriate soldering iron to properly solder these high heat load connections. Tuck the slack in these wires down against the Rear Stiffener Bar and glue it to the circuit board if necessary.

  . The power from the F1 fuse is routed up to the BULK_5V0 bus along the top edge of the circuit board via 4x #22 AWG wires. Along the top edge these wires are soldered into vias: WRP5:WRP8. These wires should be tinned and soldered into these vias before they are routed down to the F1 fuse. These vias should be fluxed and the wire soldered into them with an appropriate Wattage iron. The insulation covered section of these 4 wires is about: 380, 410, 475, and 535 mm long.

  . Once these 4 wires have been soldered into the vias route them vertically across the top of the card in a way that minimize the air flow restriction. Glue these 4 wires in place along this path. The path takes these wires under the MSU silkscreen as they run across to the Rear Stiffener Bar. Do not glue these wires to the Rear Stiffener Bar because we may need to remove this bar for some future card repair. Only after these wires are routed and glued in place should they be trimmed to length and soldered into the top of the F1 fuse holder.

- Clock Generator and Crystal Oscillator Final Setup:

  . Remove 12 terminator / pull-down resistors:
    R455, R456,
    R459, R460, R461, R462,
    R463, R464, R465, R466,
    R469, and R470.

  . Install a 200 Ohm 1206 resistor on the bottom side of the circuit board from R459 pin 2 to R460 pin 2.

. Install a 200 Ohm 1206 resistor on the bottom side of the circuit board from R463 pin 2 to R464 pin 2.

. Install a 120 MHz crystal Oscillator in location U371 aka Crystal #1. This oscillator is for the G-Link output from the Base Function FPGA.

. Crystal Oscillator location U373 aka Crystal #2 is left open at this time.

- Setup the correct TTCDec Chip-ID Jumpers

. For correct operation of the TTCDec Mezzanine card its CHIP_ID(2) must be set HI. At the time of main assembly all TTCDec CHIP_ID Jumpers are set LOW. See drawing 12 in the CMX web circuit diagrams.

. Remove the 4.7k Ohm jumper resistor from locations JMP14.

. Install a 4.7k Ohm 0603 resistor in location JMP15.

- Setup the CMX Card Serial Number Jumpers

. This set of jumpers is on the back side of the card up near the BSPT FPGA. These jumpers must be set on each CMX card to match that card's actual Serial Number, i.e. the serial number that you write on the card during final assembly.

. Install as required zero Ohm jumpers JMP101 through JMP105 to match the card's serial number. Install a zero Ohm jumper to pull that bit LOW. If a jumper is not installed then that bit is pulled HI by a Pull-Up in the BSPT FPGA.

- Setup the 82C250 Can-Bus Interface Chip Drive Level

. The CAN-Bus interface chip is a Philips NXP 82C250. It is Reference Designator U272. Pin #8 on the 82C250 CAN-Bus interface chip controls its mode and transmitter output current.

. On the CMX card R501 pulls 82C250 pin #8 towards Ground. R502 pull this pin towards +5 Volt. Both R501 and R502 are on the back side of the CMX card. They are located near the Backplane Power connector.

. To allow the 82C250 CAN-Bus interface chip to actually talk to the backplane CAN-Bus connection:

Remove both the R501 and R502 resistors.

Install a Zero Ohm Jumper in location R501

to pull the 82C250 pin #8 to Ground.

Leave location R502 open with nothing installed.

. Doing this will put the 82C250 in the same mode that is used by the other L1Calo cards.

- Setup the Front-Panel Access Signal Select Jumpers

. At main assembly jumpers are installed so that the two Front Panel Access Signals both come from the BSPT FPGA. If Front Panel Access signal are wanted from the BF or TP FPGAs them the correct jumpers in the range R365 through R370 must be installed to make this selection. These are 47 Ohm 0603 resistors.

- Not Installed SMD Components:

. When Final Assembly is finished, for a standard application CMX card we currently expect to see the following SMD component locations still open

Ref Num	Side (1=top 2=bot)	X (mm)	Y (mm)	Rotate (degree)	
JMP4	2	263.00	323.00	0	Jumpers that
JMP11	2	298.00	43.00	90	are not
JMP13	2	301.00	43.00	90	Normally
JMP14	2	304.00	43.00	90	Installed
JMP17	2	307.00	43.00	90	
JMP19	2	310.00	43.00	90	
JMP21	2	313.00	43.00	90	
JMP23	2	316.00	43.00	90	
JMP25	2	319.00	43.00	90	
JMP27	2	322.00	43.00	90	
JMP31	2	183.00	196.00	0	
JMP34	2	187.00	188.00	0	
JMP35	2	183.00	192.00	0	
JMP38	2	187.00	208.00	0	
JMP41	2	134.00	91.00	0	
JMP44	2	138.00	83.00	0	
JMP45	2	134.00	87.00	0	
JMP48	2	138.00	103.00	0	
JMP52	2	263.00	301.40	0	
JMP54	2	263.00	311.40	0	
JMP56	2	263.00	306.40	0	
JMP59	2	322.00	346.50	0	
JMP62	2	45.00	74.00	90	
JMP63	2	309.00	20.50	90	
JMP66	2	262.00	278.00	0	
JMP68	2	268.00	278.00	0	
JMP72	2	53.50	74.00	90	
JMP73	2	61.00	80.00	90	

JMP76	2	59.00	73.50	0	
JMP79	2	121.90	294.00	90	
JMP81	2	42.00	74.00	90	
JMP85	2	99.40	26.90	0	
R256	1	272.00	44.50	0	TTCDec Clk Sel
R366	2	258.00	84.00	0	FP Access 1
R368	2	277.00	84.00	0	FP Access 2
R369	2	258.00	95.00	0	FP Access 1
R370	2	277.00	95.00	0	FP Access 2
R455	1	162.90	26.00	0	U371 Term
R456	1	167.20	26.00	180	
R459	2	196.90	36.10	180	U375 Term
R460	2	202.10	36.10	0	
R461	1	196.90	35.90	0	
R462	1	202.10	35.90	180	
R463	2	221.90	36.10	180	U377 Term
R464	2	227.10	36.10	0	
R465	1	221.90	35.90	0	
R466	1	227.10	35.90	180	
R469	1	247.90	37.00	0	U379 Term
R470	1	252.20	37.00	180	
SR1	1	112.00	208.05	0	Connections to
SR2	1	112.00	205.85	0	Spare IC Foot
SR3	1	118.00	208.05	0	Print SU1
SR4	1	118.00	205.85	0	
SR5	1	112.00	188.05	0	
SR6	1	112.00	185.85	0	
SR7	1	118.00	188.05	0	
SR8	1	118.00	185.85	0	
SR10	1	107.00	204.65	0	
SR11	1	107.00	202.45	0	
SR12	1	107.00	200.25	0	
SR13	1	107.00	198.05	0	
SR14	1	107.00	195.85	0	
SR15	1	107.00	193.65	0	
SR16	1	107.00	191.45	0	
SR17	1	107.00	189.25	0	
SR20	1	123.00	204.65	0	
SR21	1	123.00	202.45	0	
SR22	1	123.00	200.25	0	
SR23	1	123.00	198.05	0	
SR24	1	123.00	195.85	0	
SR25	1	123.00	193.65	0	
SR26	1	123.00	191.45	0	
SR27	1	123.00	189.25	0	
SR31	1	263.00	312.00	0	Spare
SR32	1	267.80	327.50	90	Connections

SR33	1	277.10	327.50	90	to BSPT
SR34	1	263.00	309.30	0	FPGA U351
SR35	1	263.00	306.60	0	
SR36	1	263.00	303.90	0	
SR37	1	287.00	327.50	90	
SR41	1	137.00	25.00	0	Spare
SR42	1	137.00	22.50	0	Connections
SR43	1	151.00	27.50	0	to CAN-Bus
SR44	1	151.00	25.00	0	uProcessor
SR45	1	151.00	22.50	0	Connector
SR46	1	151.00	20.00	0	J16
SR51	1	258.00	113.00	0	Auxillary
SR52	1	258.00	110.00	0	Connections
SR53	1	258.00	104.00	0	to the
SR54	1	258.00	100.00	0	FPGA Access
SR55	1	258.00	92.00	0	Connector
SR56	1	258.00	89.00	0	J14
SR57	1	258.00	82.00	0	
SR58	1	277.00	82.00	0	
SR59	1	277.00	89.00	0	
SR60	1	277.00	92.00	0	
SR61	1	277.00	100.00	0	
SR62	1	277.00	104.00	0	
SR63	1	277.00	110.00	0	
SR64	1	277.00	116.00	0	
SR71	1	89.00	250.00	90	Spare
SR72	1	87.00	246.00	90	Connections
SR73	1	85.00	250.00	90	to Monitor
SR74	1	83.00	246.00	90	Conn J13
SU1	1	115.00	196.95	0	Spare IC
U373	1	180.00	20.00	0	Crystal Osc.

6. Inspection Before Initial Power Up:

- Shorts checks:

  . Short check to ground the 5 Volt input bus to the card by probing one of the labeled Ground Vias, e.g. WRP35 or WRP 36, to the 5 Volt input F1 Fuse Block.

  . Shorts check to ground the output of all 7 of the DC/DC Converters across the top side of the card. Do this by probing across the Tantalum output capacitors at the lower side of each DC/DC Converter.

- Set all power supply output voltage trim pots to full CCW. This is to set them at their minimum output voltage. These are 5 turn trim pots located to the East of each DC/DC Converter and one in the VREF_P supply just above the Transmitter MiniPODs. 8 trim pots total to set CCW.