



ATLAS NOTE

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Hardware test results for the CMX PRR, Version 2.0

CMX project team

Abstract

This document describes the results of the interface tests on the CMX prototypes for the CMX production readiness review.

Tests on the CMX services are presented as well as on the real-time and read-out path tests. Extensive tests of the backplane interface, LVDS IO and low speed and high speed optical links are presented. Tests with dedicated stress data patterns and pseudo-random data as well as long term tests demonstrate the reliability of the data interfaces and that they meet the requirement on the error rate in the L1 trigger system. The successful completion of the data interface tests either in loopback tests or in tests with the appropriate hardware components on the receiver side have shown that the data interfaces are capable of reliable data transmission that fulfill the requirements of the L1 trigger system. The layout and design of the CMX prototype boards is sufficient and the test results indicate that no design changes are necessary for the fabrication and assembly of the full production CMX boards.

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1 Introduction

This document describes the results of the interface tests on the CMX prototypes for the CMX production readiness review. The details on the CMX specifications can be found in another document here [1].

Tests on the CMX services consist of tests on

- reading back the correct geographical addresses.
- the configuration of the firmware via the compact flash card slot.
- VME interface to the base function FPGA (Section 2).
- I²C interfaces to operate with the XILINX System ACE controller, TTCrx chip on the TTCDec card, and SFP and MiniPOD optical components (Section 2).

The real-time and read-out path tests were done for the following interfaces:

- backplane interface in a full crate of JEMs and CPMs with two CMX's where the data validity window was probed and long-term tests were executed to find an upper limit on the bit and event error rate with fixed data patterns and pseudo-random data (Section 3).
- LVDS IO with the RTM were tested in loopback mode (Section 4).
- front panel LVDS IO connections to the ATLAS CTP were tested with simple stress patterns and pseudo-random data in long term tests and bathtub curves were obtained by varying the delay settings on the CTP (Section 4).
- high speed optical links at 6.4 Gpbs between the base function FPGA MiniPods and the Topo FPGA MiniPods were tested in loopback tests using Xilinx IBERT cores. The same optical links are also used to connect to L1Topo and this connection was tested with the available L1Topo prototype (Section 5).
- low speed optical links at 1.0 Gbps from two Topo and two base function SFP outputs were tested using Xilinx IBERT cores and received on four base function SFP inputs. First tests of the low speed optical links to a ROD in the test crate have also been performed (Section 6).

The correct operation of the general services, especially the VME interface to the FPGAs, was necessary to perform all other test, since these are initiated and controlled by reading and writing registers in the firmware. Throughout all interface tests the operation was found to be reliable. In a dedicated test with writes of random data and subsequent read back and comparison of the values confirmed the reliable operation.

The full crate backplane interface tests with two prototype CMX's in a full JEM or CPM crate showed that the capability of the firmware to adjust the delay settings of the incoming data and clock lines was good enough to adjust the timing settings over a large range and to scan the size of the data validity window. In tests with dedicated stress data patterns and pseudo-random data, the width of the data validity window was found to be large enough to probe at least one edge of the validity window. The width of the window itself was found to be sufficient to have a stable operation with a comfortable margin. In long term tests over a few hours at a stable operation point it was shown that no error occurred. The resulting upper limit on the event error rate surpasses the requirement on the error rate in the L1 trigger system by far. No power or heat issues have occurred throughout the tests in the full crates for the duration of the tests.

The other interface tests aimed at the reliability of the data interfaces to the other L1 systems, such as to another CMX card, to the L1Topo, to the CTP and to the RODs. All interfaces were first successfully

tested in loopback mode. Data and stress patterns were sent between interfaces on the CMX that can be configured to send or receive data.

At CERN all data interfaces were tested also with the appropriate hardware components on the receiver side. This is the CTP for the LVDS IO interfaces, a ROD card for the low speed optical transmissions and the L1Topo prototype card for the high speed optical transmission. In cases where the timing can be adjusted, such as the CMX-to-CTP on the CTP side, the timing window was also scanned to probe the width of that window. The reliable data transmission was successfully confirmed in these tests and bit or event error ratios were determined in long term tests. The ratios and the corresponding error rates were found to meet the requirement on the error rate in the L1 trigger system.

In the following sections the interface tests are described in detail and each section concludes that the interfaces meet the performance requirement that is necessary for a reliable data transmission within the requirements in the L1 trigger system. Tests on the CAN bus interface for the DCS monitoring were not performed, yet, but should not have substantial impact.

2 Services

The access and reliability tests of the CMX services consists of checks that the correct geographical address were read back correctly, the firmware can be configured via the compact flash slot, tests to the VME interface to the base function FPGA and tests to the I²C interfaces to operate with the XILINX System ACE controller, TTCrx chip on the TTCDec card, and SFP and MiniPOD optical components. The I²C interface is provided via a control register and a status/data register which in turn are accessible via the VME interface. For the TTCrx chip this is described for example here [2].

In the CERN test crate the geographical address of the prototype CMX's were read back correctly and it was confirmed that the address was zero for the left slot and one for the right slot. The configuration of the firmware through the compact flash slot was also verified on one of the prototypes.

The VME interface was tested with a set of read/writeable test registers at addresses 0x28 – 0x2E and 0x60 – 0x7E. A loop of 100 read/writes with random data at time were performed and in total 10000 accesses were performed without errors.

The I²C interface to the TTCrx chip, the SFP and the MiniPODs was tested by a series of read and writes of known data. Useful data such as the delay setting of the Dskew clocks were set and read back successfully. No errors have been observed in these tests.

3 Full crate backplane tests

3.1 Background information

The Virtex 6 Select I/O blocks have the ability to delay signals arriving on the GPIO pins by up to 31 taps each corresponding to a delay of approximately 78 ps, therefore giving a maximum delay of 2.4 ns. The delay can be applied on each data line and clock line independently. This allows us to explore a 4.8 ns data validity window with respect to the phase of the forwarded clock (as the forwarded clock is sent by the JEMs and CPMs in the middle of the period where data is expected to be stable). Given that the theoretical maximum data window is 6.25 ns, it is not possible to get a full picture of the data eye. However, the 4.8 ns range is sufficient to be able to judge if the data transmission will be reliable.

The SumET and the Jet FPGA in all JEMs were configured with an updated firmware that has 55 pre-configured data patterns (numbered 0-54). Each pattern consist of 256 events and 4 event slices per event. Separate firmware was used to provide pseudo-random patterns. The CPMs were all configured with updated firmware that contained the same 55 pre-configured patterns and the pseudo-random generator in the same firmware.

The CMX firmware has an ability to

- Count events received from the last counter reset for each source module. The counter is 32-bit allowing for measurements up to 107 s.
- Check for parity errors and count parity errors from each processor module (counters are also 32-bit). The error counter increments at most once per event, whenever a parity error has been detected in any of the four 24-bit slices corresponding to given event.
- Continuously perform on every 48-bit half-event word received a bitwise check of received data against the contents of a programmable spy memory. A flag indicating if an error occurred is supplied for each bit.
- On a per-source module basis a count (32-bit) till a first detected bit error (a deviation from the expected pattern) is performed.

In addition during all tests described below, the FPGA outputs connected to the LVDS transceivers (two CTP cables and three RTM cables) are driven with a repeating predefined pattern aiming to stress the internal ground reference of the FPGA. The 80 Mbps pattern is 255 events long and contains long coherent silences in the '0' state as well as '1' state, high and low coherent pulses as well as switching data. The length of this pattern is an attempt to create beats against the 256 events long backplane pattern. Since the predefined data patterns from the source modules are 256 events long, if there is a transition on the LVDS outputs that causes a problem for the backplane data reception, it will be explored within approx 1 ms. The drive current on these FPGA outputs is set to 12 mA which is much higher than we expect to use in the final system (preliminary tests suggest that drive current of 6 mA is sufficient to maintain error-free transmission at 80 Mbps). The voltage translators driving the LVDS transceivers are turned off, so that no activity will actually be generated on the LVDS cables. No other interfaces (MiniPod, SFP) are used in these tests.

3.2 General setup and test procedures

The two prototype CMX SN-01 and CMX SN-03 were used for the full crate test in the ATLAS service cavern (USA15). Two series of tests were performed in either the JEP0 crate with 16 JEMs (channel 0-15) or into the CP0 crate with 14 CPMs (channel 1-14, channel 0 and channel 15 are unused). CMX SN-01 was used in CMM/CMX position 1 corresponding to the right slot (referred to as CMX 1, slot 20 in the crate) and CMX SN-03 was used in the CMM/CMX position 0 (referred to as CMX 0, slot 3 in the crate). In a JEM crate CMX 0 receives data from the SumET FPGA and CMX 1 receives data from the Jet FPGA. Only for the last tests both CMX's were placed in the CMM/CMX position 0, CMX SN-01 was moved into the JEP1 (JEP system crate) crate and CMX SN-03 remained in the position 0 of the CP0 crate.

The test procedure consists of the following four steps:

- The first test was to estimate the data validity window for each data signal received from the source modules. Here we cycled through all predefined patterns. For each pattern we delay all data lines by the same number of taps and 32 tap settings were explored.

We then returned all data taps to zero and successively incremented the clock tap. The error flags for each data bit, delay setting and pattern were collected and are presented as a 2D-histogram where the bit number is on the y -axis and the delay setting is presented on the x -axis. The delay on the data lines are represented by negative delay settings, while the delay on the source clock is represented by positive delay settings. An example can be found in Figure 1 and the same figure for each pattern is shown in Figures 2-6. For each bit and delay setting the histogram entry is

either zero or one, since only data comparison errors are flagged, not counted. The result from all 55 patterns are added up to find the narrowest validity window from the delay setting where not error has been recorded in any pattern as shown in Figure 7. The number of entries (on the color-coded z -axis) reflect the number of patterns in which an error occurred for a given bit and delay setting, so that the maximum value is 55 (corresponding to the 55 possible patterns).

- The second test conducted was a long duration run where predefined patterns were periodically changed and tap settings were held at a fixed delay setting for clock and data lines, which was found to be in the middle of the valid delay window. The data are regularly read out and the counters are reset to avoid overflows. For the final result the data from each cycle and each pattern is added up and it is presented as a 2D-histogram with the bit number on the y -axis and the number of bit errors on the x -axis. A successful test is indicated by entries at zero errors for all bits and all 55 patterns. The duration of the test can be converted into a bit error ratio and then converted into an event error rate which is compared to the requirement in the L1 trigger system. An example is shown in Figure 8. For each bit the error is either zero or one and the number of entries correspond to the number of patterns and cycles (for the figure 55 patterns and 10 cycles were used).
- The third test consisted of estimation of the 'bathtub curve' using the pseudo random data. Here again the data lines were delayed by a common tap value (from 0 to 31) and then returned to 0 while clock tap value was scanned from 0 to 31. The pseudo-random generation was not replicated on the CMX and therefore the parity was used to discover corruption of the transmission. The result is presented as a 1D-histogram with the number of parity errors versus the delay setting as shown in Figure 9. The delay on the data lines are represented by negative delay settings, while the delay on the source clock is represented by positive delay settings. The number of parity errors usually is high in the region of bad timing. The number of errors is limited by the dwell time times the 40 MHz event rate (here a dwell time of 50 s and 10 cycles were used). Then it decreases over a small range of delay settings to zero for a larger range before it increases again when the other edge is reached. The width of the parity error free region is estimated from the histogram region with zero errors and compared to the width found in the previous tests.
- The final test was a pseudo-random data run using a single tap setting. The data is regularly read out and the counters are reset to avoid overflows. For the final result the data from each cycle are added up. The result is presented as a 1D-histogram counting the number occurrences of a certain number of parity errors for all cycles as shown in Figure 10. In the best case only zero errors occurred and the number of entries correspond to the number of cycles (here 384 cycles were added up). The duration of the test can be converted into a event error ratio and then converted into an event error rate which is compared to the requirement in the L1 trigger system.

3.3 Test patterns and synchronization

The test patterns are defined as follows to create specific stress (ISI stress pattern 0-51, cross talk stress 3-49, 51) on the data lines. In the examples of the test patterns each row represents one data bit and the time runs from left to right.

- The test pattern 0 creates one high signal pulse on all data bits for one event slice followed by a low for all other event slices, i.e. the pattern has all bits in the first event slice of the first event slice at high and low for the others event words and events creating a high pulse on all data lines followed by long silence:
1000 0000 0000 0000 0000 0000
1000 0000 0000 0000 0000 0000

1000 0000 0000 0000 0000 0000
up to 24th bit...

- Test pattern 1 is the inverted pattern:
0111 1111 1111 1111 1111 1111
0111 1111 1111 1111 1111 1111
0111 1111 1111 1111 1111 1111
up to 24th bit...

- Test patterns 2-25 switches one bit (bit number = pattern number minus two) to high in the first event slice, while the other bits are zero. The pattern is inverted for the following event slices creating a pattern where one bit switches out of phase with respect to the other bits:
0111 1111 1111 1111 1111 1111 ...
1000 0000 0000 0000 0000 0000 ...
0111 1111 1111 1111 1111 1111 ...
up to 24th bit...

- Test patterns 26-49 invert patterns 2-25:
1000 0000 0000 0000 0000 0000 ...
0111 1111 1111 1111 1111 1111 ...
1000 0000 0000 0000 0000 0000 ...
up to 24th bit...

- Test pattern 50 alternates between all bits high and low, i.e. maximal switching in phase:
1010 1010 1010 1010 1010 ...
1010 1010 1010 1010 1010 ...
1010 1010 1010 1010 1010 ...
up to 24th bit...

- Test pattern 51 has alternating highs and lows in each event slice and the pattern is inverted for the next event slice, i.e. maximal switching out of phase:
1010 1010 1010 1010 1010 ...
0101 0101 0101 0101 0101 ...
1010 1010 1010 1010 1010 ...
0101 0101 0101 0101 0101 ...
up to 24th bit...

- Test patterns 52-54 are patterns that can be used for finding the correct slice position in a set of 4 event words. For the first event of pattern 52 the data bits are all low, all high, all high and all low for each event slice respectively. The following events reverse the order in the first two slices and keeping the last two slices. Pattern 53 repeats the pattern all low, all high, all high and all low for all events. Pattern 54 has all data bits high, then all low, all low and all high for the first event and the slices are all inverted for the other 255 events:
Pattern 52:
0110 1010 1010 1010 1010 ...

0110 1010 1010 1010 1010 ...
0110 1010 1010 1010 1010 ...
up to 24th bit...

Pattern 53:

0110 0110 0110 0110 0110 ...
0110 0110 0110 0110 0110 ...
0110 0110 0110 0110 0110 ...
up to 24th bit...

Pattern 54:

1001 0110 0110 0110 0110 ...
1001 0110 0110 0110 0110 ...
1001 0110 0110 0110 0110 ...
up to 24th bit...

These patterns are not a realistic representation of physics data, but are designed to explore scenarios where data transmission could be least reliable, in an electrical environment in which all lines are active and all slots drawing power.

The pseudo-random data is realized as an array of 47-bit LFSR (linear feedback shift register) running in parallel in the JEM firmware and as a single 95-bit LFSR, which advances a full word after each event, in the CPM firmware. Databit 23 represents the odd-parity of the random data word.

All patterns were send synchronously from all source modules to both CMX's. For the JEM this was achieved by using the BC reset for synchronization to the first event of the pattern in the playback. On the CPMs the synchronization was achieved by sending a reset signal to each CPM that was not synchronous. The reset sets the playback to the first event. This was done by the test software after capturing and retrieving a set of 256 events from the CMX and finding the first event of pattern 0. While reading of the events from the CMX and checking of the patterns in the test software, the event loop on the CPMs keeps running independently, so that the reset occurs almost randomly. If the first event of the pattern is not at the first event in the spy memory, a reset of the event loop was initiated to the corresponding CPM. This procedure is repeated until the events that are received from all 14 CPM modules are synchronous with respect to the first event in pattern 0. A change in the pattern does not stop the event loop, so that the synchronization remains throughout all the patterns. For both, the JEM and the CPM tests, the comparison between the received data and the spy memories on the CMX is reset to the first event (or programmable to start at any start address in the spy memory) by the BC reset signal.

3.4 JEM crate

For the first test in the JEM crate the dwell time for each delay tap setting was set to 0.1 s corresponding to a total run time of 6 min and the possible validity windows was explored. For the first run 1395868943 data pattern 22, 25 and 54 did not match in the JEM firmware to the patterns that were loaded into the CMX spy memories. These differences were consequently flagged as errors for these patterns. Looking at Figures 11 and 12 the valid data window is still visible when looking at summed error entries above 3. The valid window exhibits two features: The window is not centered around the zero delay setting, so that only one edge of the window can be probed. This is contrary to the expected behavior from the firmware configuration which is suppose to place the clock edge in the middle of the data eye. The second feature is that the data window moves for CMX 0 (left side of the crate, receiving data from the

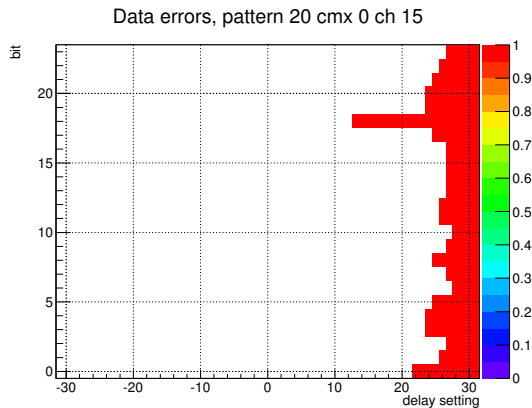


Figure 1: Example of a data error histogram for CMX 0, channel 15 for each bit versus the delay setting and using pattern 20. The error flags for each data bit, delay setting were collected and are presented as a 2D-histogram where the bit number is on the y -axis and the delay setting is presented on the x -axis. Negative delay settings correspond to delay on the data lines, positive delay settings correspond to delays of the source clock. Only ones and zeros are expected for each entry corresponding to an occurrence of any error or no error during the dwell time, respectively.

Table 1: Overview of the test performed in the JEP0/1 crate

run	CMX	time [s]	cycles	patterns	delay	total time [h]	figure
1395868943	0/1	0.1	1	all patterns	scan	0.10	11 12
1396273108	0/1	0.1	1	all patterns	scan	0.10	13 14
1396277853	0/1	0.1	1	all patterns	scan	0.10	15 16
1396279431	0/1	5.0	1	all patterns	scan	4.81	17 18
1396303792+	0/1	50.0	10	all patterns	0/0	7.64	19 20
1396010274+	0/1	50.0	11	random	scan	9.63	21 22
1396049227+	0/1	50.0	384	random	10/10	5.32	23 24
1396964926	0	0.1	1	all patterns	scan	0.10	25
1396970468	0	5.0	1	all patterns	scan	4.81	26

SumET FPGA), but not for CMX 1. Since the clock is source synchronous this cannot be explained by the different signal path lengths between the CMX and the JEMs and by the path length differences between data and clock lines. Both features do not invalidate the width of the valid data window, since the clock is source synchronous and the delay is always set at the receiver end.

In run 1396273108, Figures 13 and 14, the expected delay between the clock edge and the data eye edge has been removed for the SumET FPGA, to move the validity window more to the center of the delay settings. Also the bad patterns 22, 25 and 54 were corrected, so that every pattern in the firmware and in CMX spy memories match. Still bit pattern 25 was not switching bit 23 out of phase. This bug does not invalidate the results, since the validity window is evaluated from the overlap of all test patterns. When comparing different patterns the width of the window seems to be similar for all the bits, so that the narrowest window can still be evaluated from the sum over the other correct patterns. Shorts and opens would have been also detected by those patterns and by the parity checks on pseudo-random data. This bug has been removed in later runs from run number 1396964926 on.

From the Figures 13 and 14 one can see that the validity window for CMX 0, which receives the data from the SumET FPGAs, has moved, so that the other edge becomes visible. A refined adjustment of the

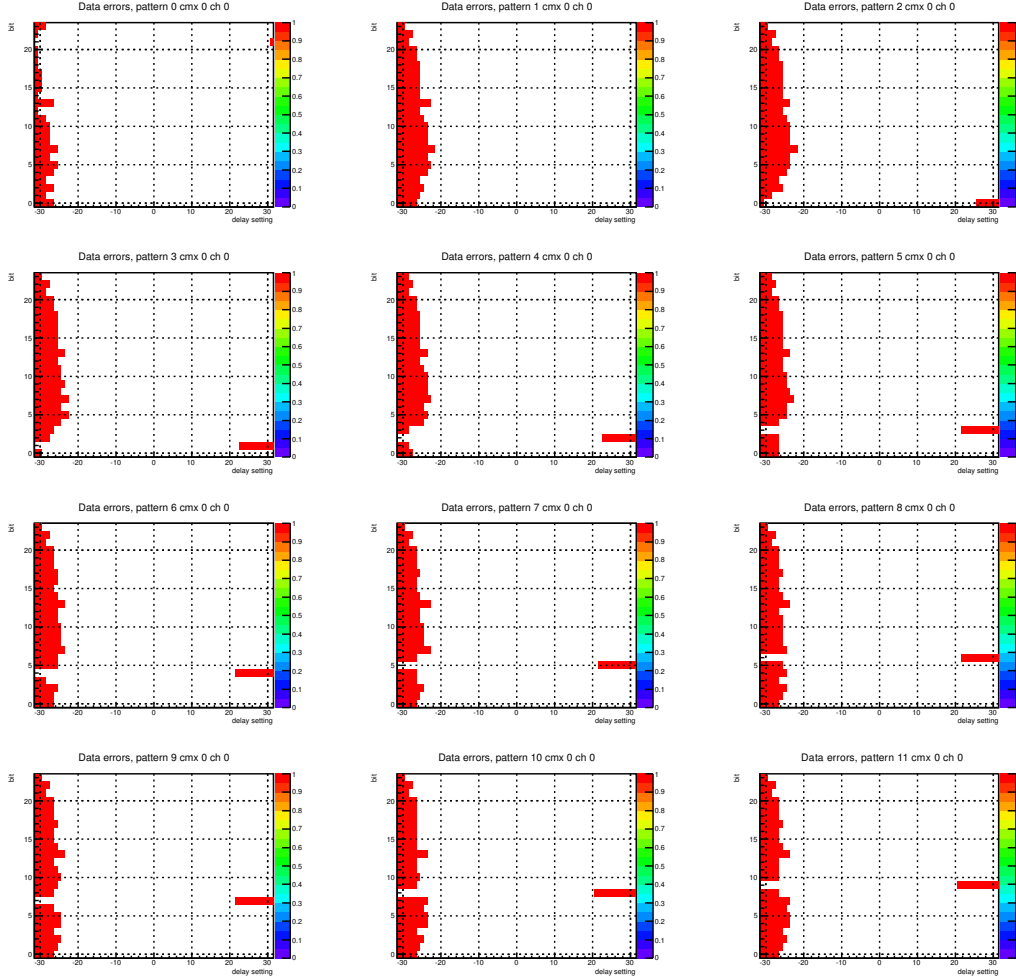


Figure 2: Example for data error histograms for CMX 0, channel 0 for each bit versus the delay setting for patterns 0-11. The error flags for each data bit, delay setting and pattern were collected and are presented as a 2D-histogram where the bit number is on the y -axis and the delay setting is presented on the x -axis. Negative delay settings correspond to delay on the data lines, positive delay settings correspond to delays of the source clock. Only ones and zeros are expected for each entry corresponding to an occurrence of any error or no error during the dwell time, respectively.

delay to 1.5 ns on both, SumET FPGA and JET FPGA, has been made, so that the validity window for both CMX's are almost centered around zero delay as seen in Figures 15 and 16.

For run 1396279431 the dwell time was increased to 5 s per tap delay setting, so that the total run time for a full loop over all 63 tap delays and 55 patterns sums to 4.8 h. Figures 17 and 18 show that the validity window is very similar to the previous runs and is roughly 30 taps for CMX 0 and 40 taps for CMX 1 for each bit. This corresponds to a window width of 2.3 ns and 3.1 ns, respectively. No errors were observed in the center of the window during the full dwell time.

The center of the validity window was found to be around delay setting 0 (corresponding to no additional delay on neither the clock nor the data lines). A longer run (1396303792) was taken at this delay setting with 10 cycles through all 55 patterns and a dwell time of 50 s per cycle and setting. The total time for this run was 7.6 h. The accumulated error counts are shown for each CMX, channel and bit in Figures 19 and 20. No errors were observed during the full dwell time. The upper limit on the bit

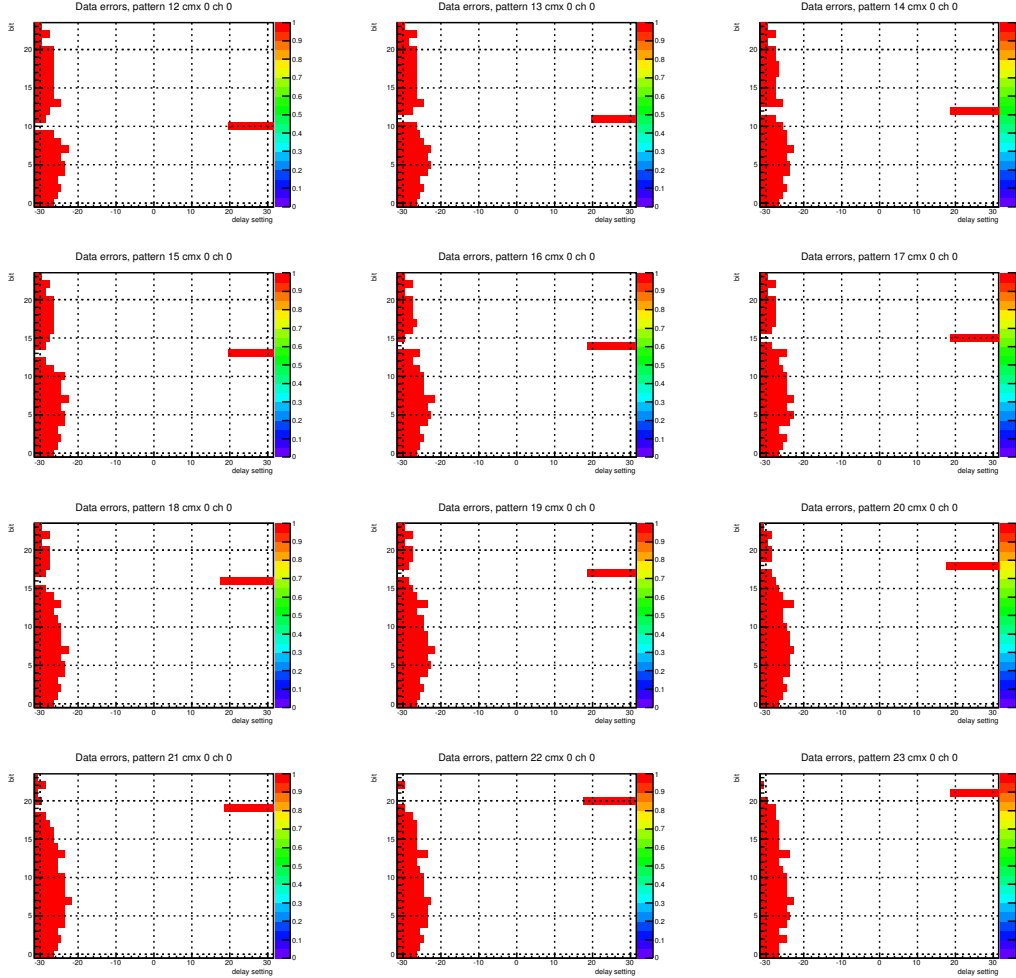


Figure 3: Example for data error histograms for CMX 0, channel 0 for each bit versus the delay setting for patterns 12-23. The error flags for each data bit, delay setting and pattern were collected and are presented as a 2D-histogram where the bit number is on the y -axis and the delay setting is presented on the x -axis. Negative delay settings correspond to delay on the data lines, positive delay settings correspond to delays of the source clock. Only ones and zeros are expected for each entry corresponding to an occurrence of any error or no error during the dwell time, respectively.

error ratio (BER) is 23×10^{-14} .

The JEM FPGAs were configured for the runs 1396010274 and 1396049227 with a different firmware that produced pseudo-random data with odd parity. For run 1396010274 the parity errors for 11 cycles were recorded while the delay settings we scanned. The dwell time for each delay setting was 50 s resulting in a total dwell time of 9.6 h. Figures 21 and 22 show the parity errors versus the delay setting summed over all 11 cycles. The center of the validity window has moved due to the changed timing in the new firmware configuration and only one side of the window can be seen. The systematic shift of the window edge for CMX 0 is still observed in the pseudo-random data tests. The width of the validity window was found to be at least as large as in the scans with the pre-programmed patterns. The parity error counts saturate at 22×10^9 errors counts corresponding to 40 MHz events per seconds over 50 s dwell time and 11 cycles.

For the longer term run 1396049227 an error delay setting of 10 for both CMX's was chosen. The

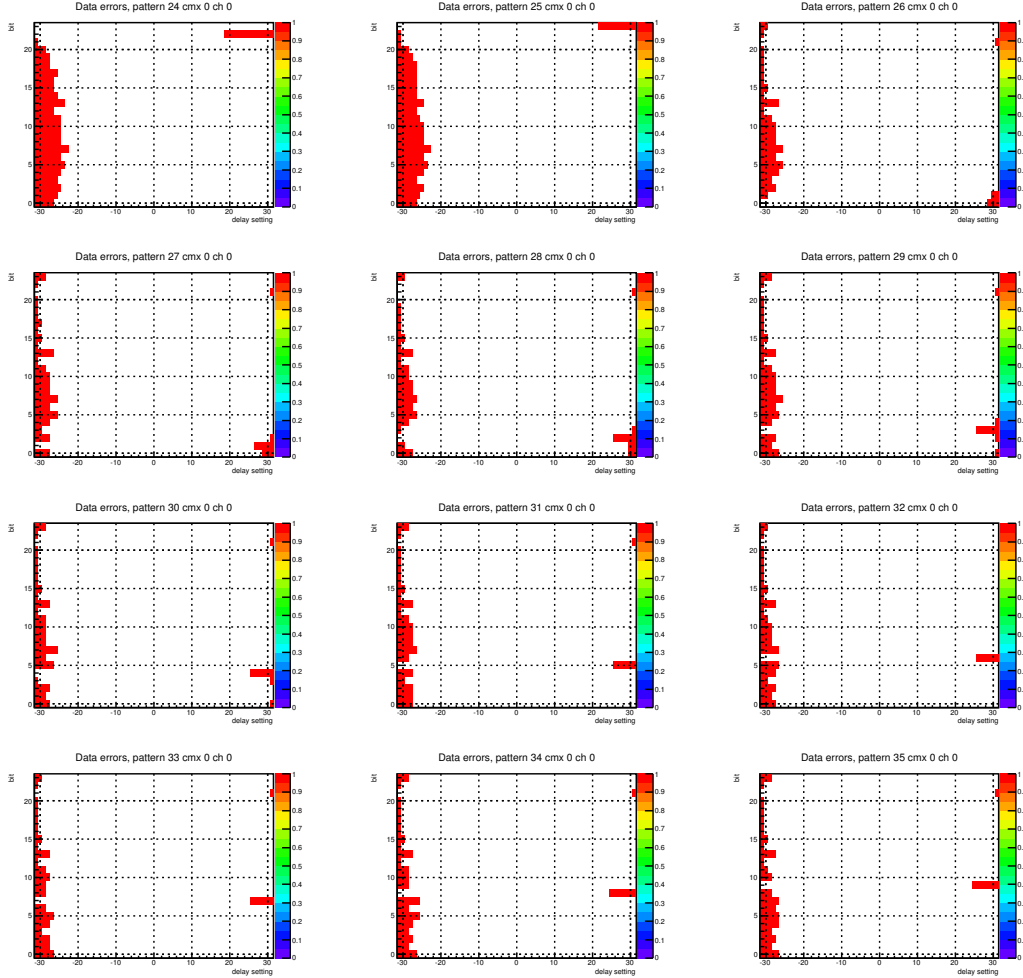


Figure 4: Example for data error histograms for CMX 0, channel 0 for each bit versus the delay setting for patterns 24–35. The error flags for each data bit, delay setting and pattern were collected and are presented as a 2D-histogram where the bit number is on the y -axis and the delay setting is presented on the x -axis. Negative delay settings correspond to delay on the data lines, positive delay settings correspond to delays of the source clock. Only ones and zeros are expected for each entry corresponding to an occurrence of any error or no error during the dwell time, respectively.

number of parity errors were counted over 384 cycles with a dwell time of 50 s per cycle. The total dwell time was 5.3 h and no parity errors were observed as shown in Figures 23 and 24. This corresponds to an upper limit of the event error rate of 131×10^{-14} .

Pattern 25 has been fixed in the firmware configuration that was used on the JEMs in runs 1396964926 and 1396970468, so that a through test on bit 23 was made. In addition the CMX 1 from the JEP0 crate was moved to the CMX 0 position in the JEP1 crate, so that CMX SN-01 is receiving now the signals from the SumET FPGAs. Figure 25 shows the bit errors per data line for a quick run with a dwell time of 0.1 s per delay setting. Figure 26 shows the bit errors per data line for a repeated run with a dwell time of 5 s per delay setting. In both cases only data from CMX 0 is received. The previously observed behaviour did not change, the validity window from the SumET FPGAs still moves systematically when going from module to module. The positions and the widths of the windows remain unchanged. It also confirms that data bit 23 on all channels are not affected by particular defects such as shorts or opens and

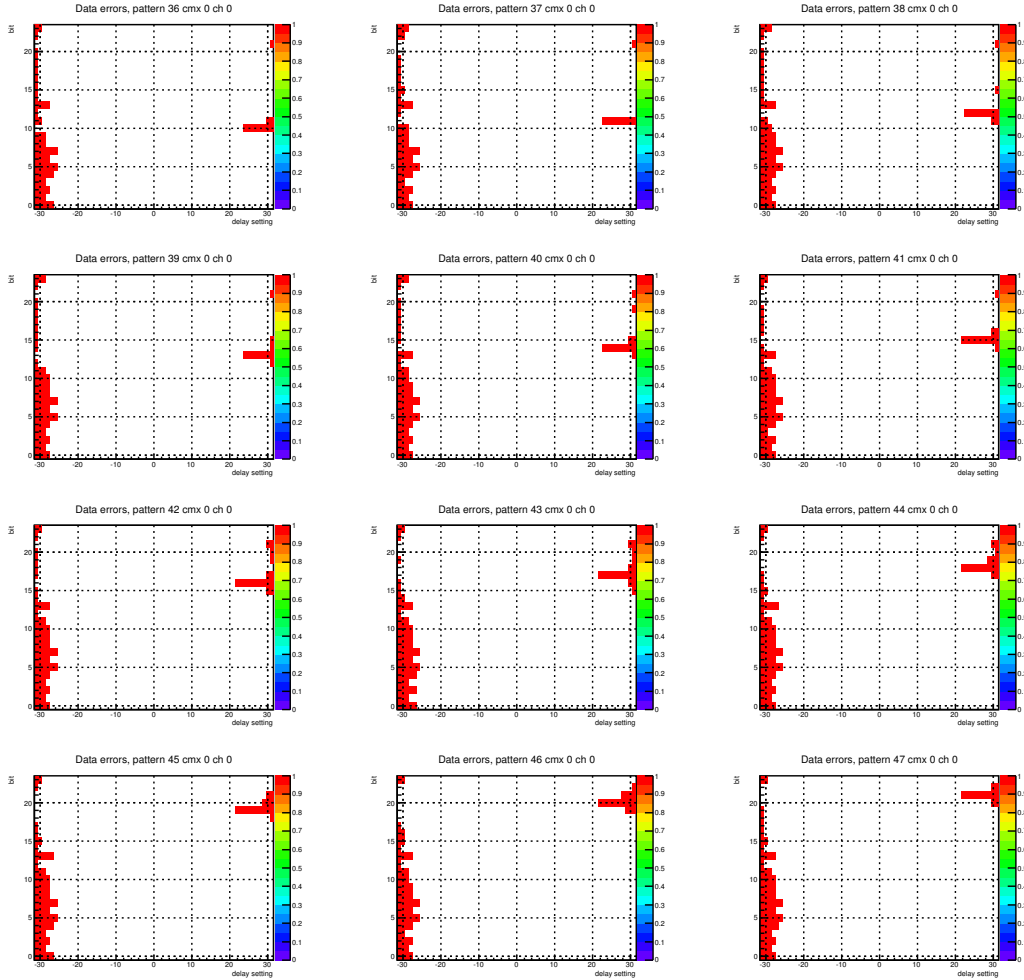


Figure 5: Example for a data error histogram for CMX 0, channel 0 for each bit versus the delay setting for patterns 36-47. The error flags for each data bit, delay setting and pattern were collected and are presented as a 2D-histogram where the bit number is on the y -axis and the delay setting is presented on the x -axis. Negative delay settings correspond to delay on the data lines, positive delay settings correspond to delays of the source clock. Only ones and zeros are expected for each entry corresponding to an occurrence of any error or no error during the dwell time, respectively.

the timing behavior is similar to the other data lines.

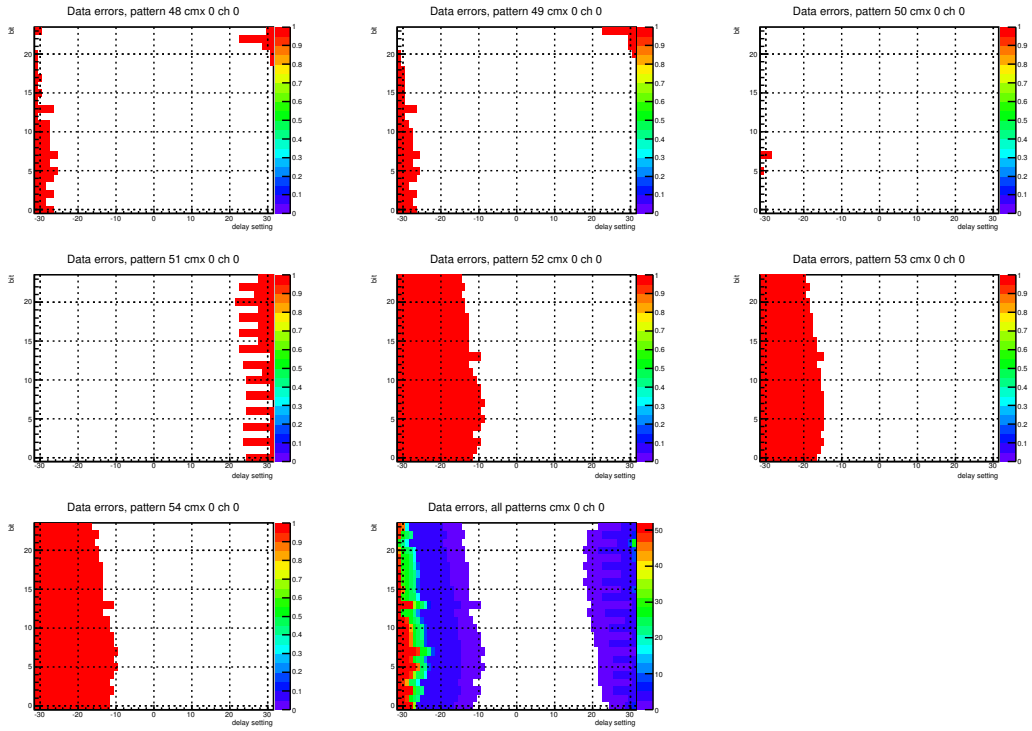


Figure 6: Example for a data error histogram for CMX 0, channel 0 for each bit versus the delay setting for patterns 48-54 and the sum over all 55 patterns. The error flags for each data bit, delay setting and pattern were collected and are presented as a 2D-histogram where the bit number is on the y -axis and the delay setting is presented on the x -axis. Negative delay settings correspond to delay on the data lines, positive delay settings correspond to delays of the source clock. Only ones and zeros are expected for each entry corresponding to an occurrence of any error or no error during the dwell time, respectively. For the sum over all patterns, the number of entries (color-coded on the z -axis) corresponds to the number of patterns for which an error occurred. From the sum over all patterns the width of the data validity is determined from the region where no errors occurred.

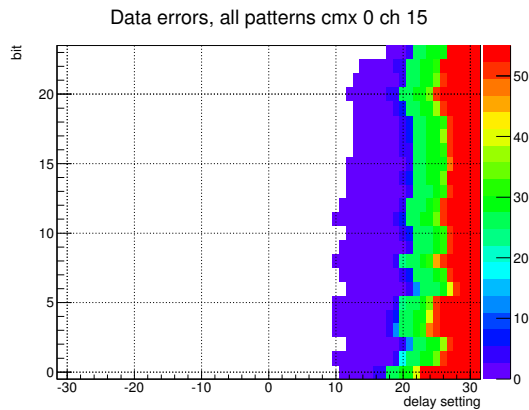


Figure 7: Example for a data error histogram for CMX 0, channel 15, for each bit versus the delay setting and summed over all 55 patterns. The error flags for each data bit, delay setting and one pattern were collected and are presented as a 2D-histogram where the bit number is on the y -axis and the delay setting is presented on the x -axis. Negative delay settings correspond to delay on the data lines, positive delay settings correspond to delays of the source clock. Only ones and zeros are expected for each entry and pattern corresponding to an occurrence of any error or no error during the dwell time, respectively. The number of entries (color-coded on the z -axis) corresponds to the number of patterns for which an error occurred. The width of the data validity is determined from the region where no errors occurred.

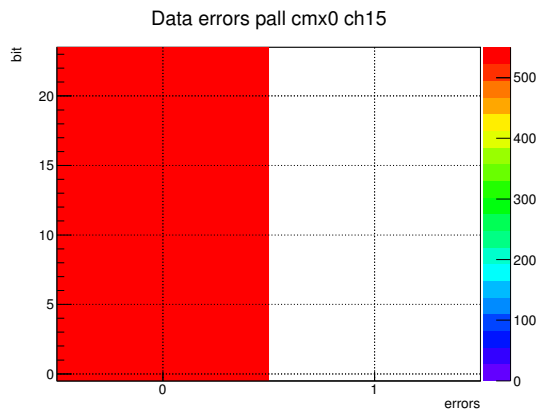


Figure 8: Example for a data error histogram for CMX 0, channel 15 during 10 cycles over all 55 patterns at delay setting 10. The error flags for each data bit and pattern were collected and are presented as a 2D-histogram where the bit number is on the y -axis and the number of errors is presented on the x -axis. For each bit the error is either zero or one and the number of entries correspond to the number of patterns and cycles. For a successful test only zeros are expected for each entry corresponding to no error during the dwell time. The total dwell time is converted into an event error rate and compared to the requirement in the L1 trigger system.

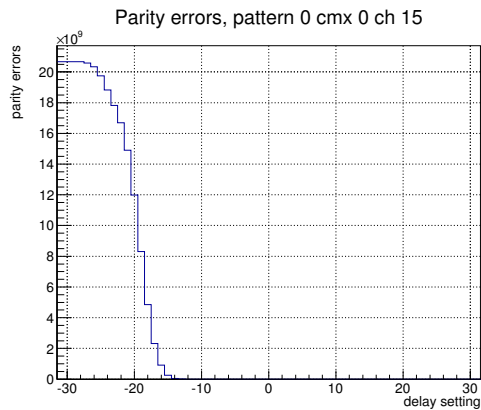


Figure 9: Example for a parity error histogram for CMX 0, channel 15 during 10 cycles versus all delay settings using the pseudo-random data. The number of errors is limited by the dwell time times the 40 MHz event rate (here 10 cycles with a dwell time of 50 s were used). The delay on the data lines are represented by negative delay settings, while the delay on the source clock is represented by positive delay settings. The width of the parity error free region is estimated from the histogram region with zero errors and compared to the width found in the previous tests.

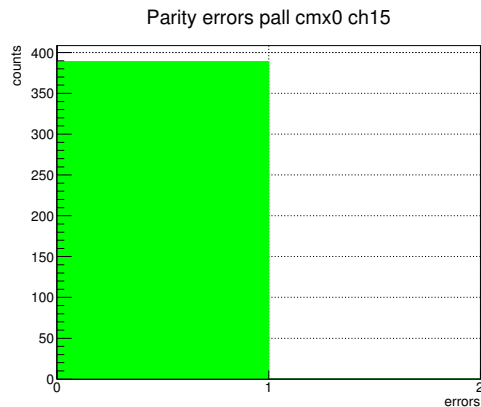


Figure 10: Example for a parity error histogram for CMX 0, channel 15 during 384 cycles for the pseudo-random pattern at delay setting 10. In the best case only zero errors occurred and the number of entries correspond to the number of cycles. The duration of the test can be converted into a event error ratio and then converted into an event error rate which is compared to the requirement in the L1 trigger system.

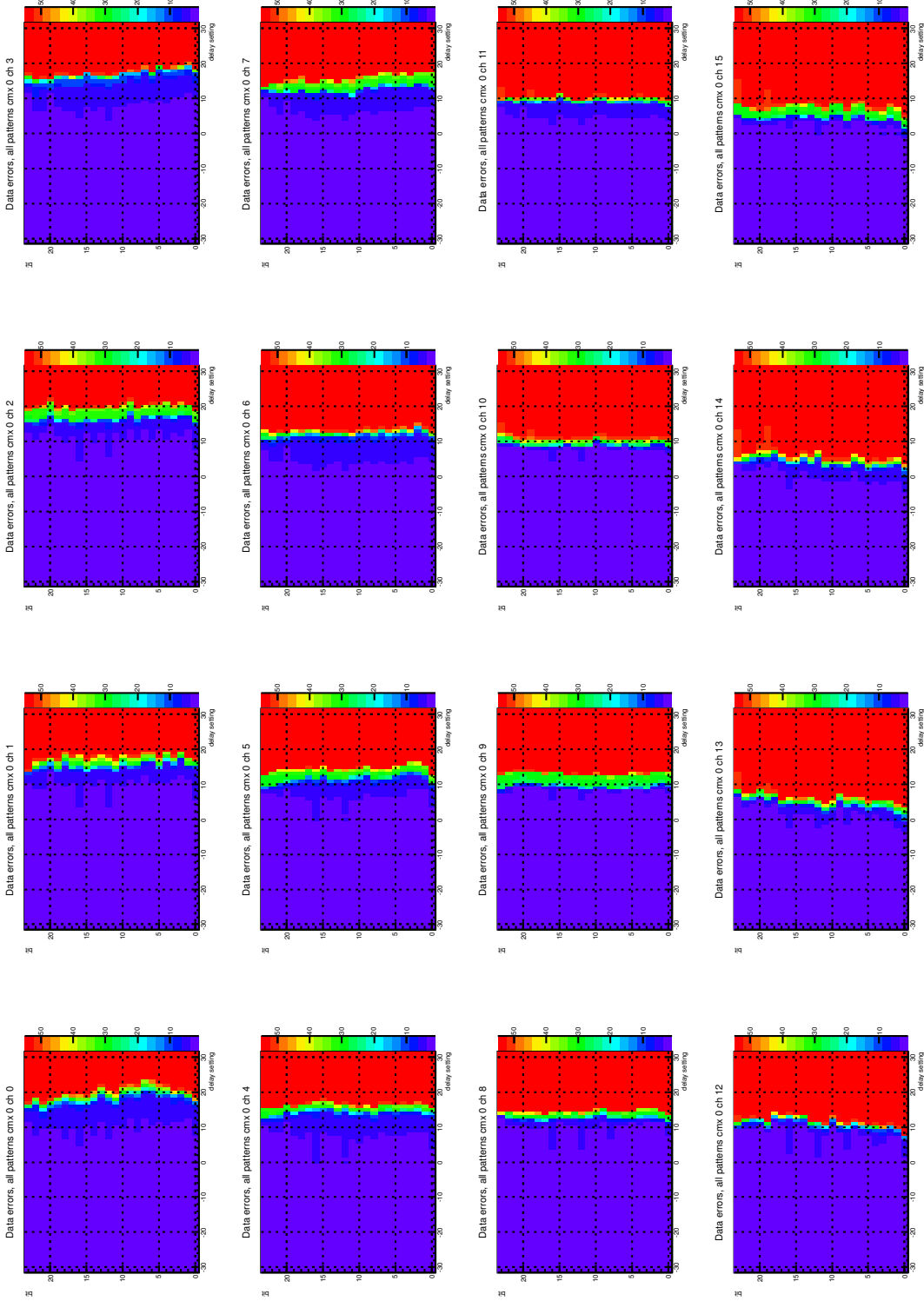


Figure 11: Summary of the data errors for CMX 0 for all channels and each bit versus the delay setting and summed over all patterns for run 1395868943. The number of errors was at least 3 because three patterns were not matching in the JEM firmware and the CMX spy memory. The edges of the valid timing window are still visible and the non-matching patterns have been fixed in the subsequent tests.

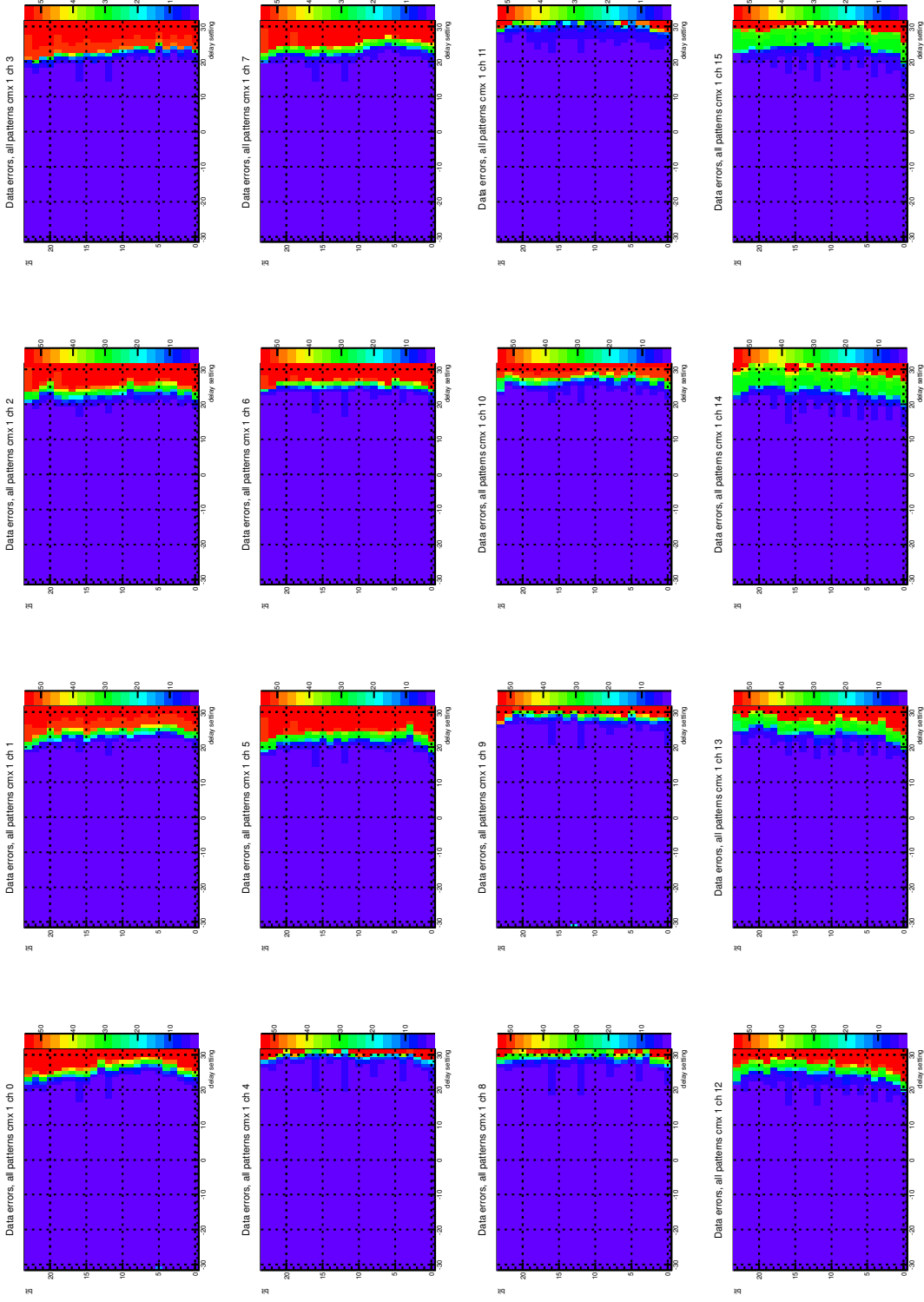


Figure 12: Summary of the data errors for CMX 1 for all channels and each bit versus the delay setting and summed over all patterns for run 1395868943. The number of errors was at least 3 because three patterns were not matching in the JEM firmware and the CMX spy memory. The edges of the valid timing window are still visible and the non-matching patterns have been fixed in the subsequent tests.

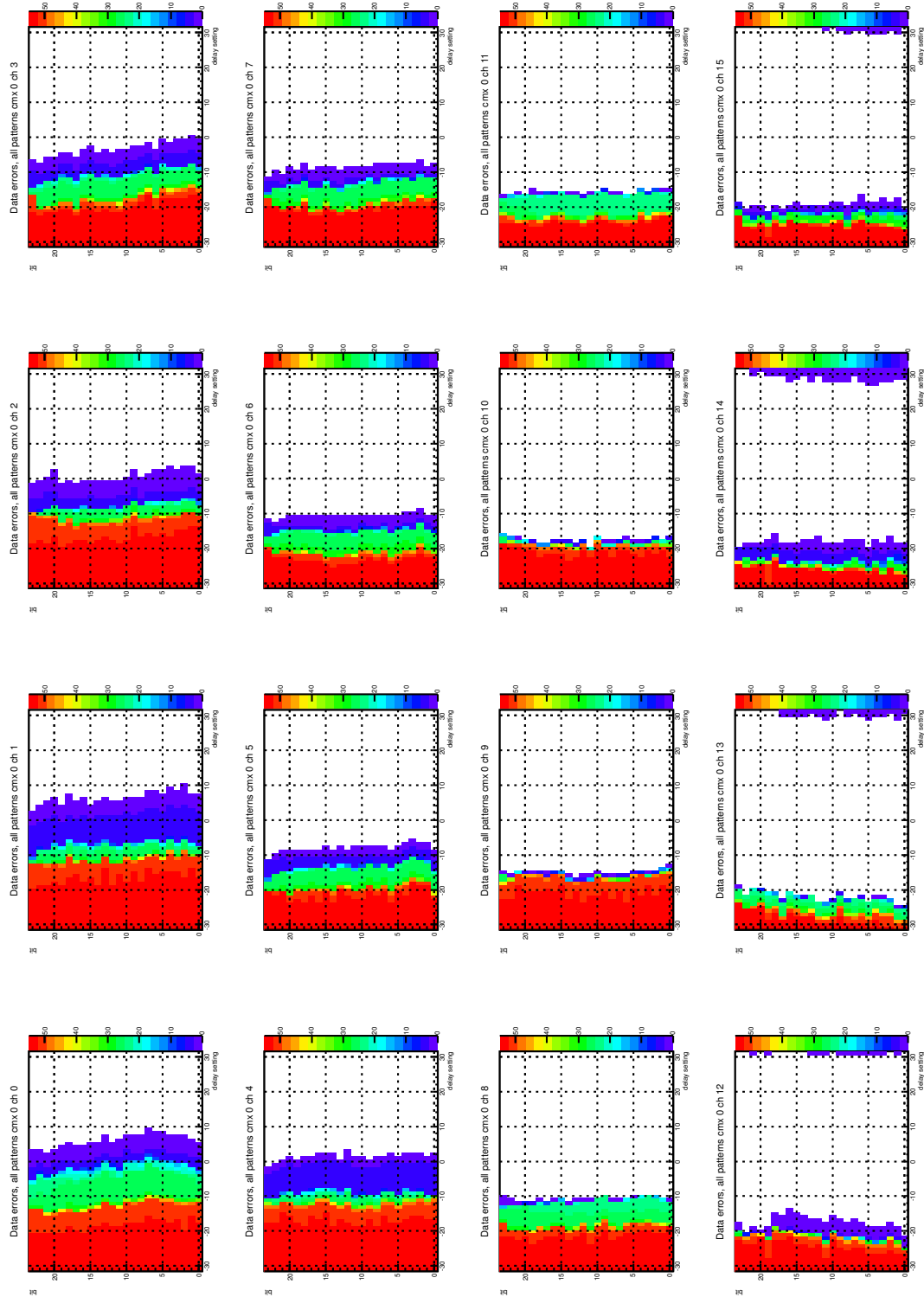


Figure 13: Summary of the data errors for CMX 0 for all channels and each bit versus the delay setting and summed over all patterns for run 1396273108.

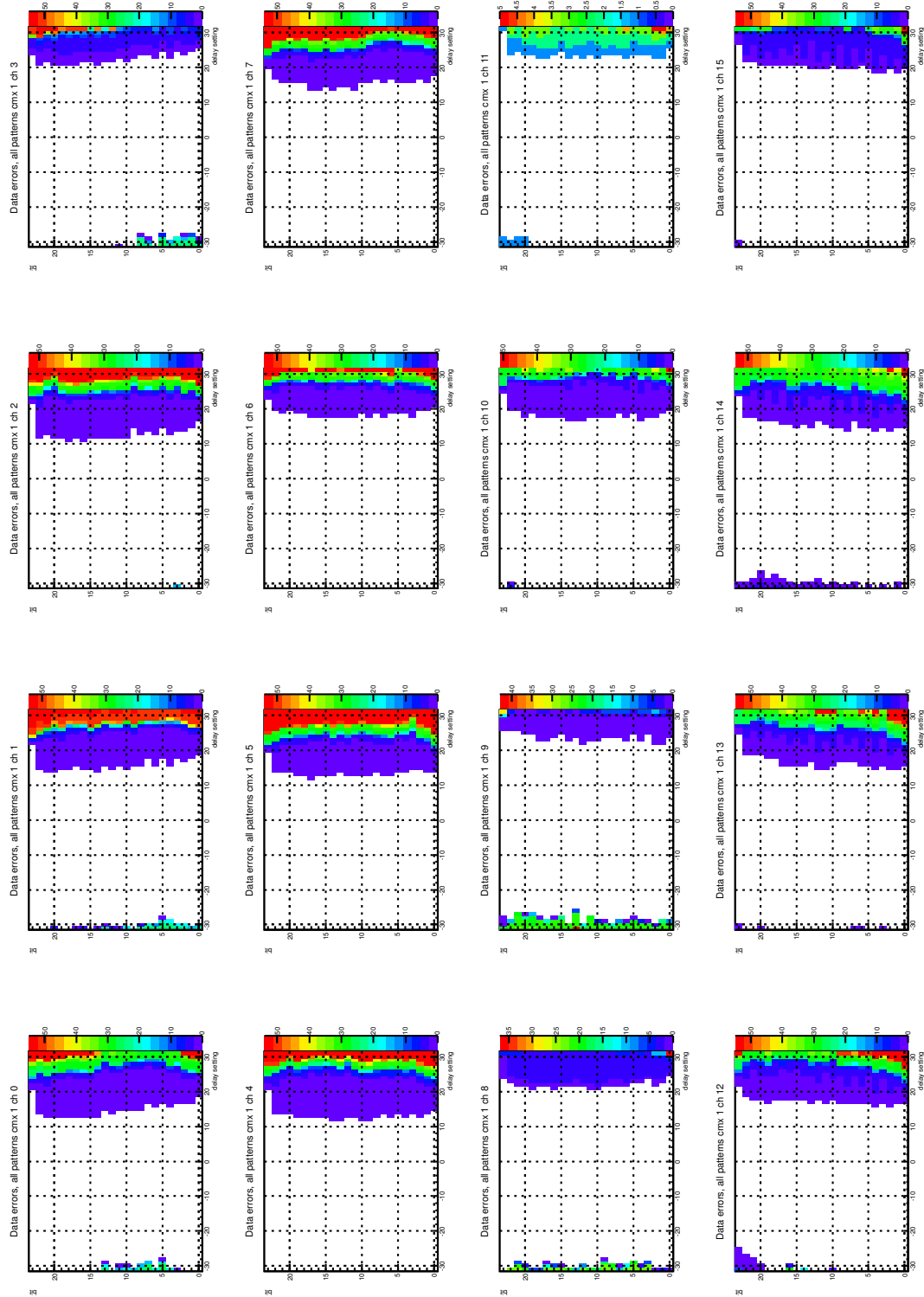


Figure 14: Summary of the data errors for CMX 1 for all channels and each bit versus the delay setting and summed over all patterns for run 1396273108.

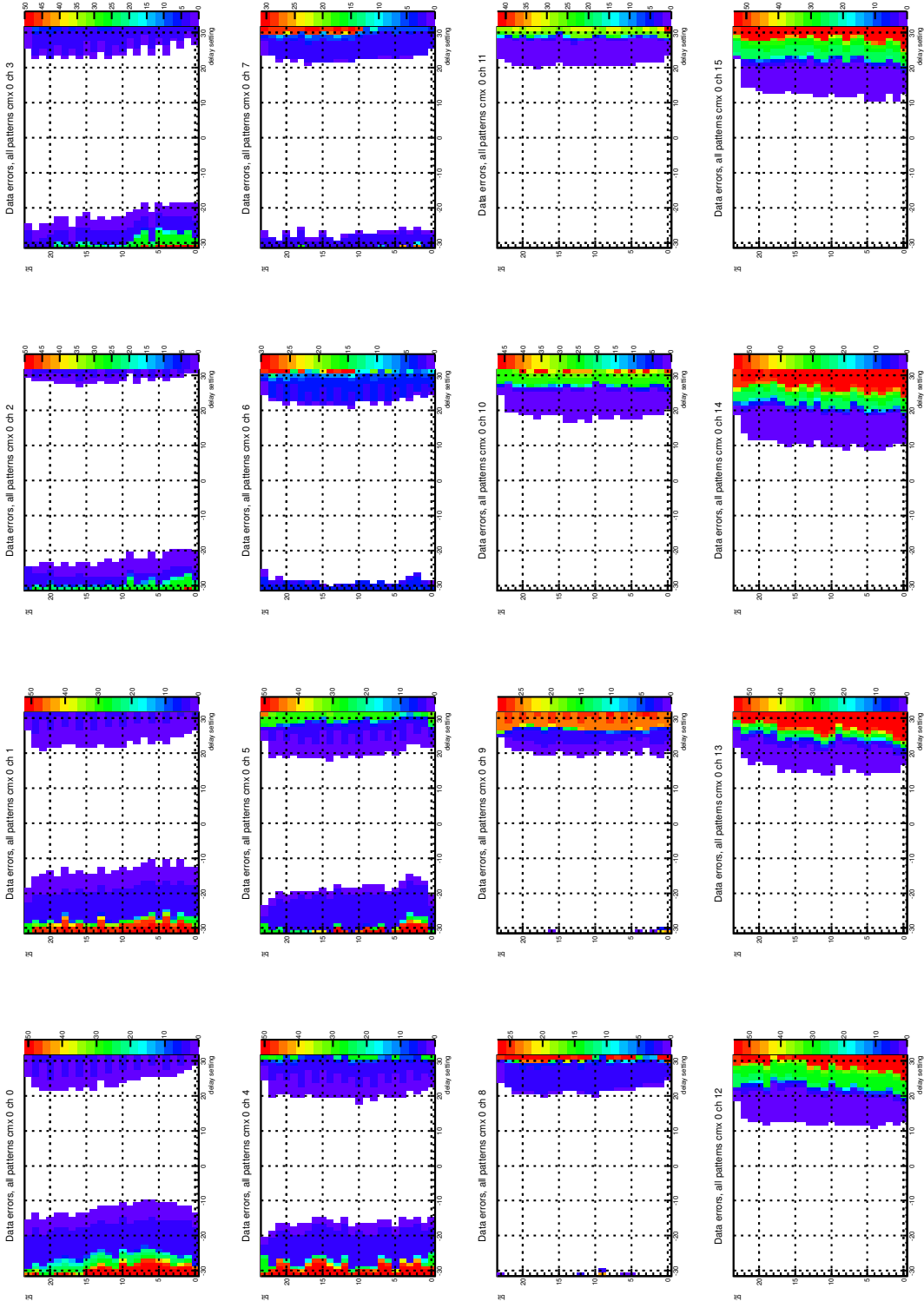


Figure 15: Summary of the data errors for CMX 0 for all channels and each bit versus the delay setting and summed over all patterns for run 1396277853.

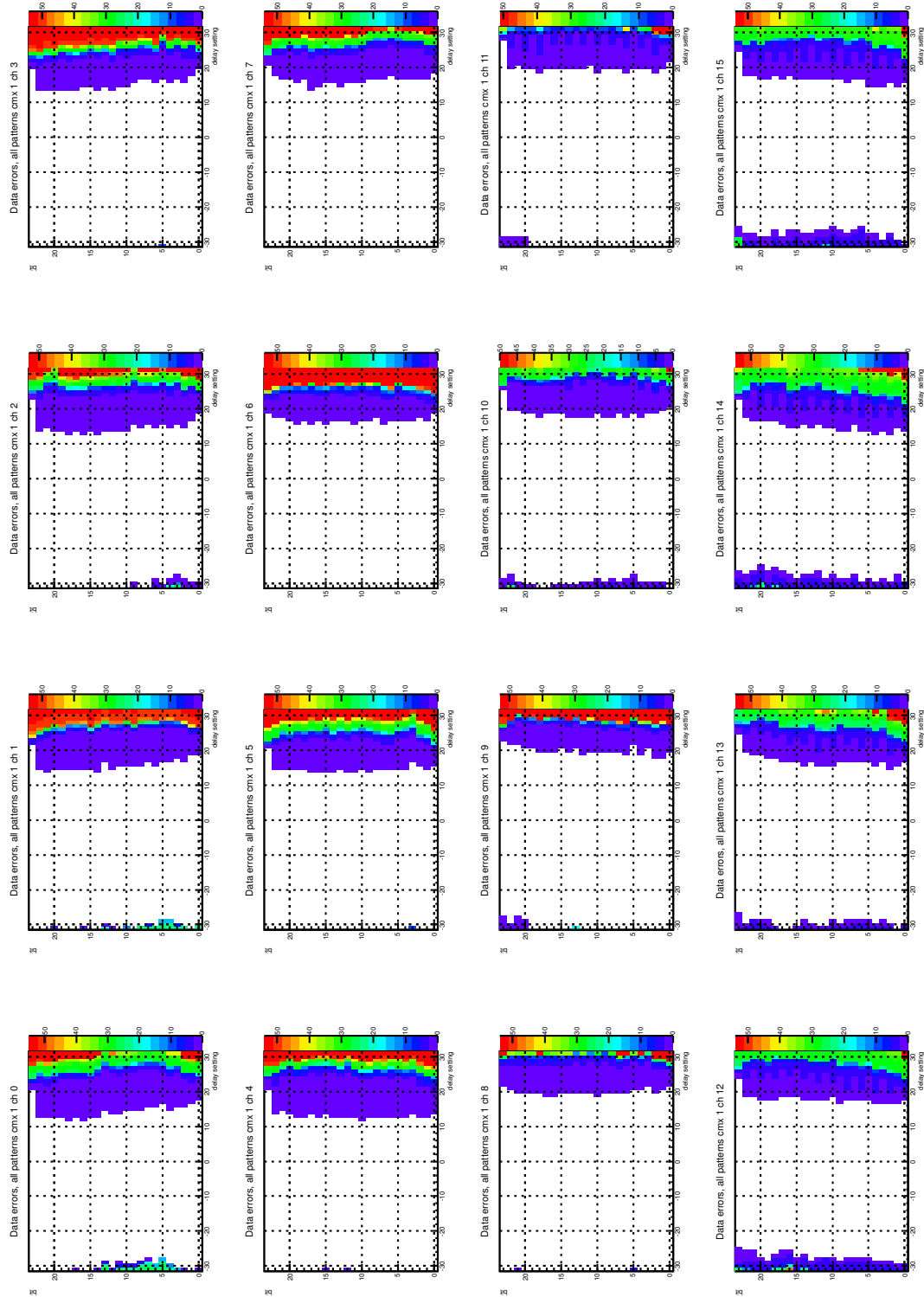


Figure 16: Summary of the data errors for CMX 1 for all channels and each bit versus the delay setting and summed over all patterns for run 1396277853.

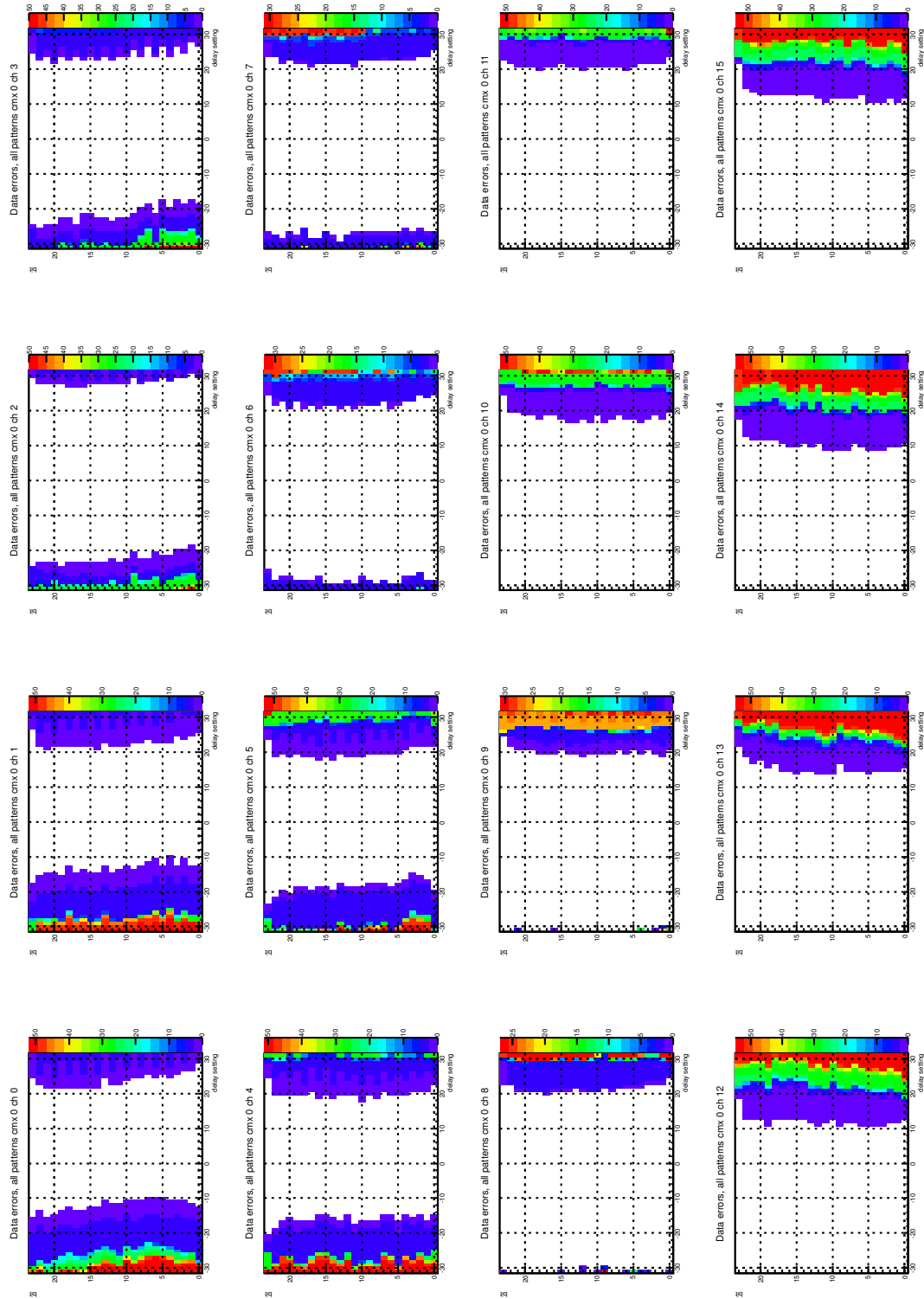


Figure 17: Summary of the data errors for CMX 0 for all channels and each bit versus the delay setting and summed over all patterns for run 1396279431.

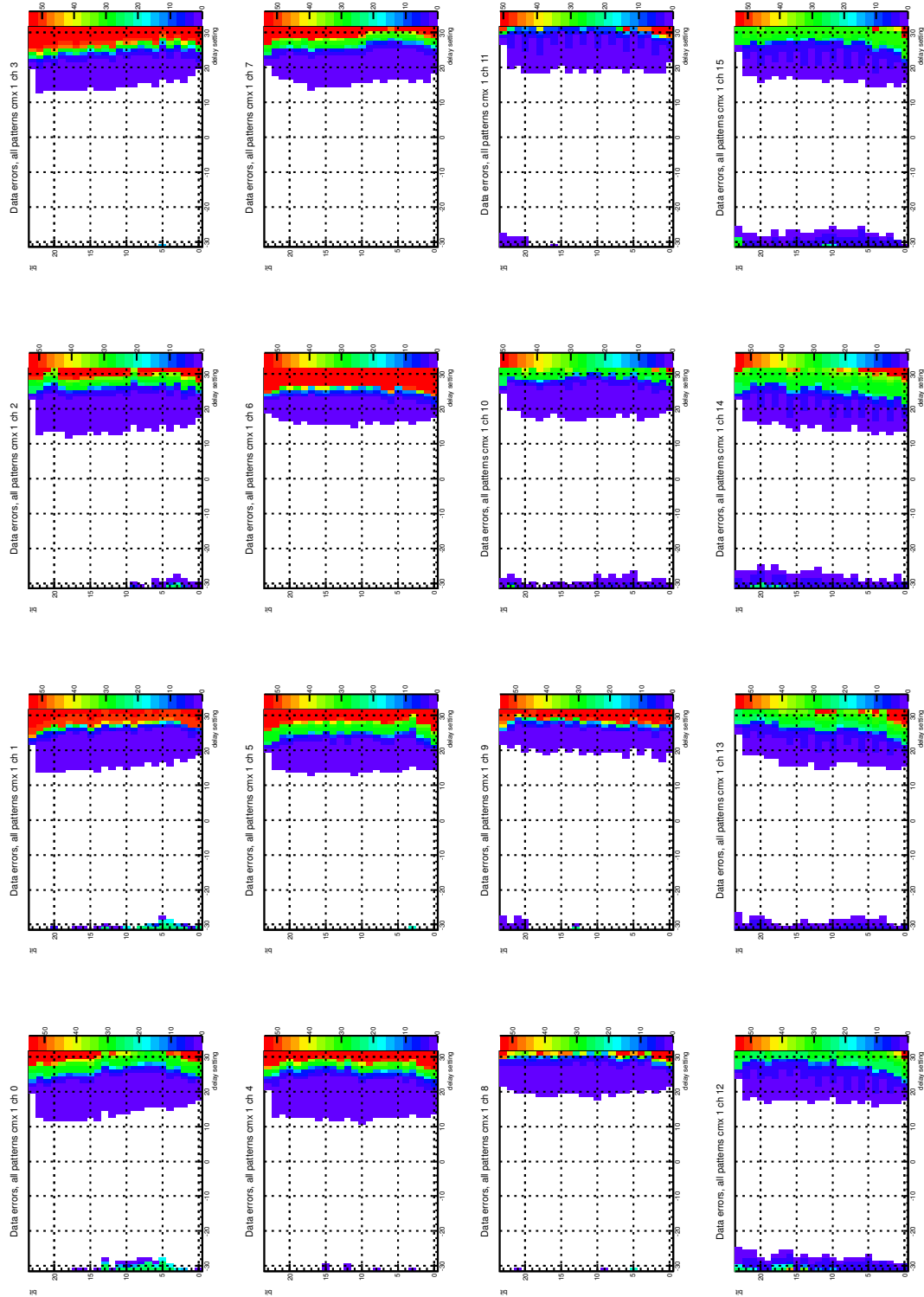


Figure 18: Summary of the data errors for CMX 1 for all channels and each bit versus the delay setting and summed over all patterns for run 1396279431.

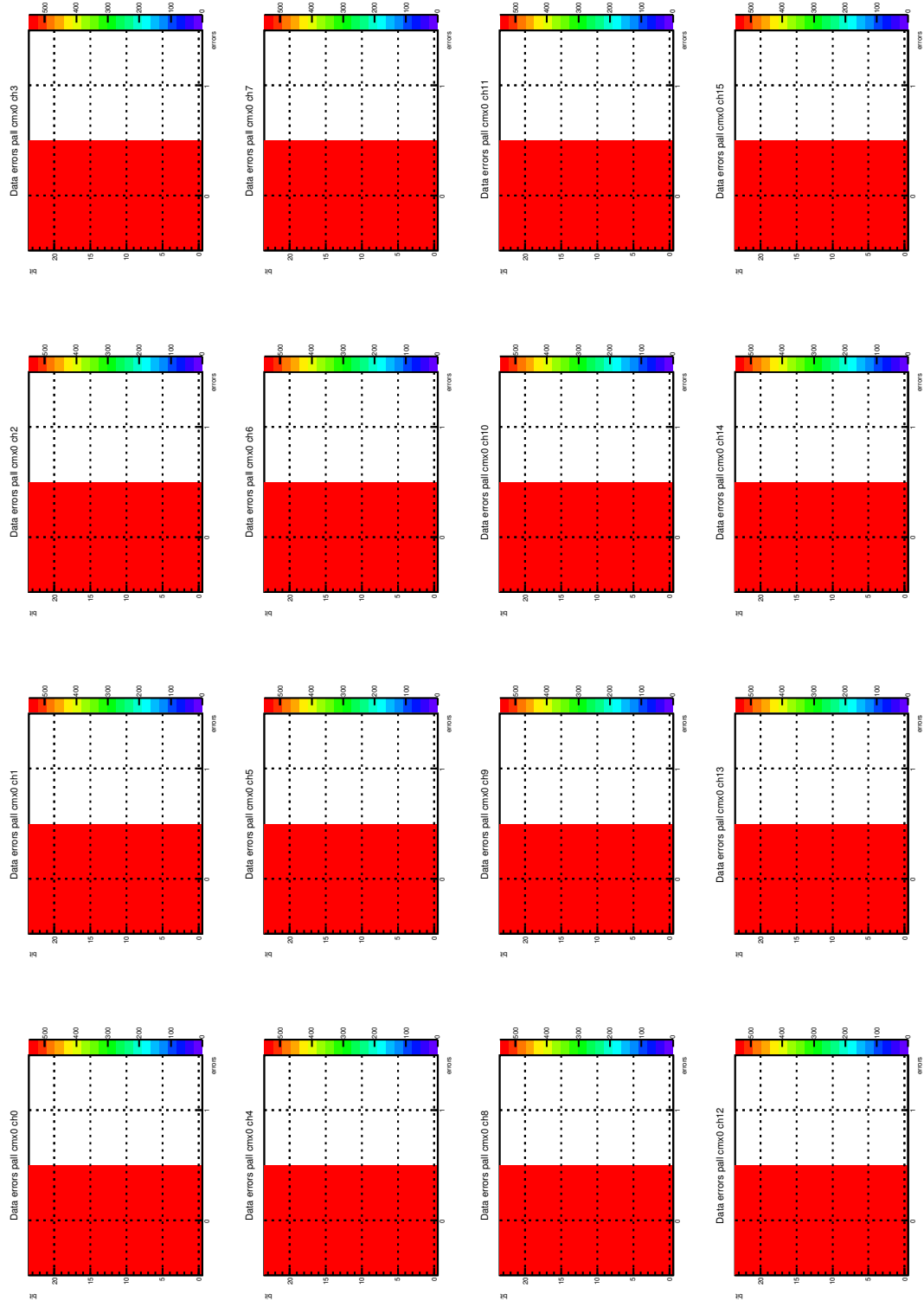


Figure 19: Summary of the data errors for CMX 0 for all channels at fixed delay setting 0 and summed over all patterns for run 1396303792.

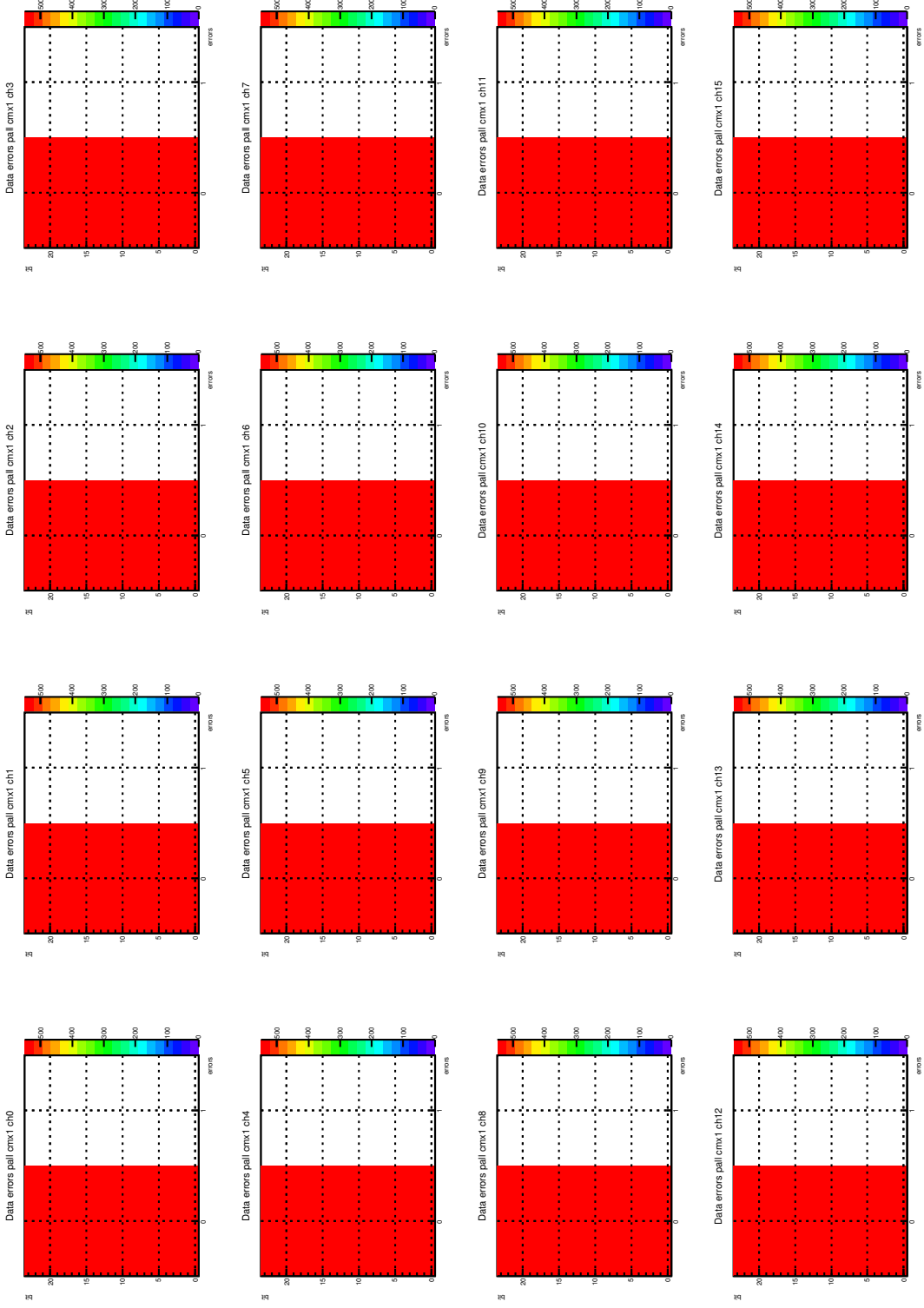


Figure 20: Summary of the data errors for CMX 1 for all channels at fixed delay setting 0 and summed over all patterns for run 1396303792.

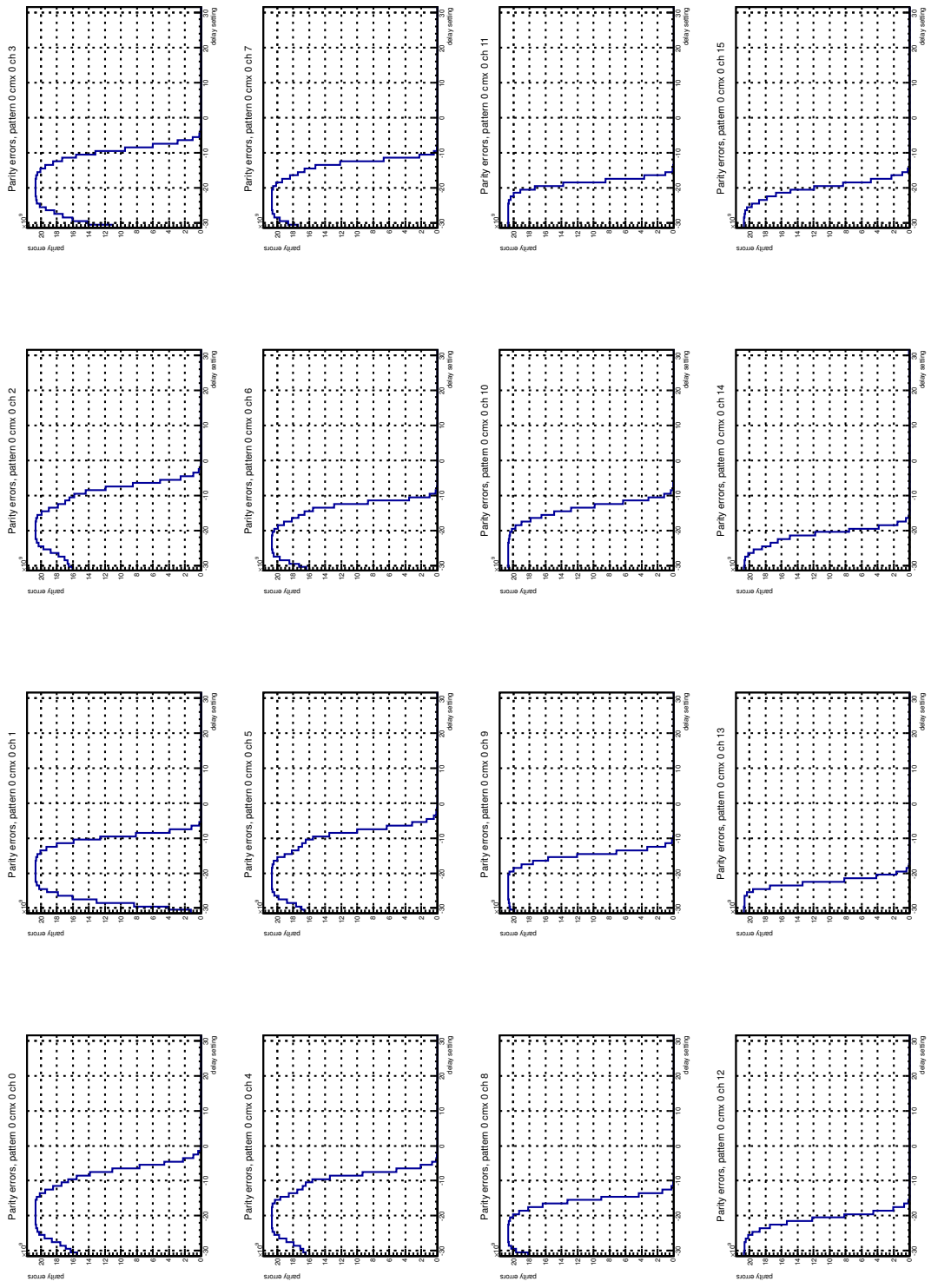


Figure 21: Summary of the parity errors for CMX 0 for all channels and each bit versus the delay setting and summed over all patterns for run 1396010274.

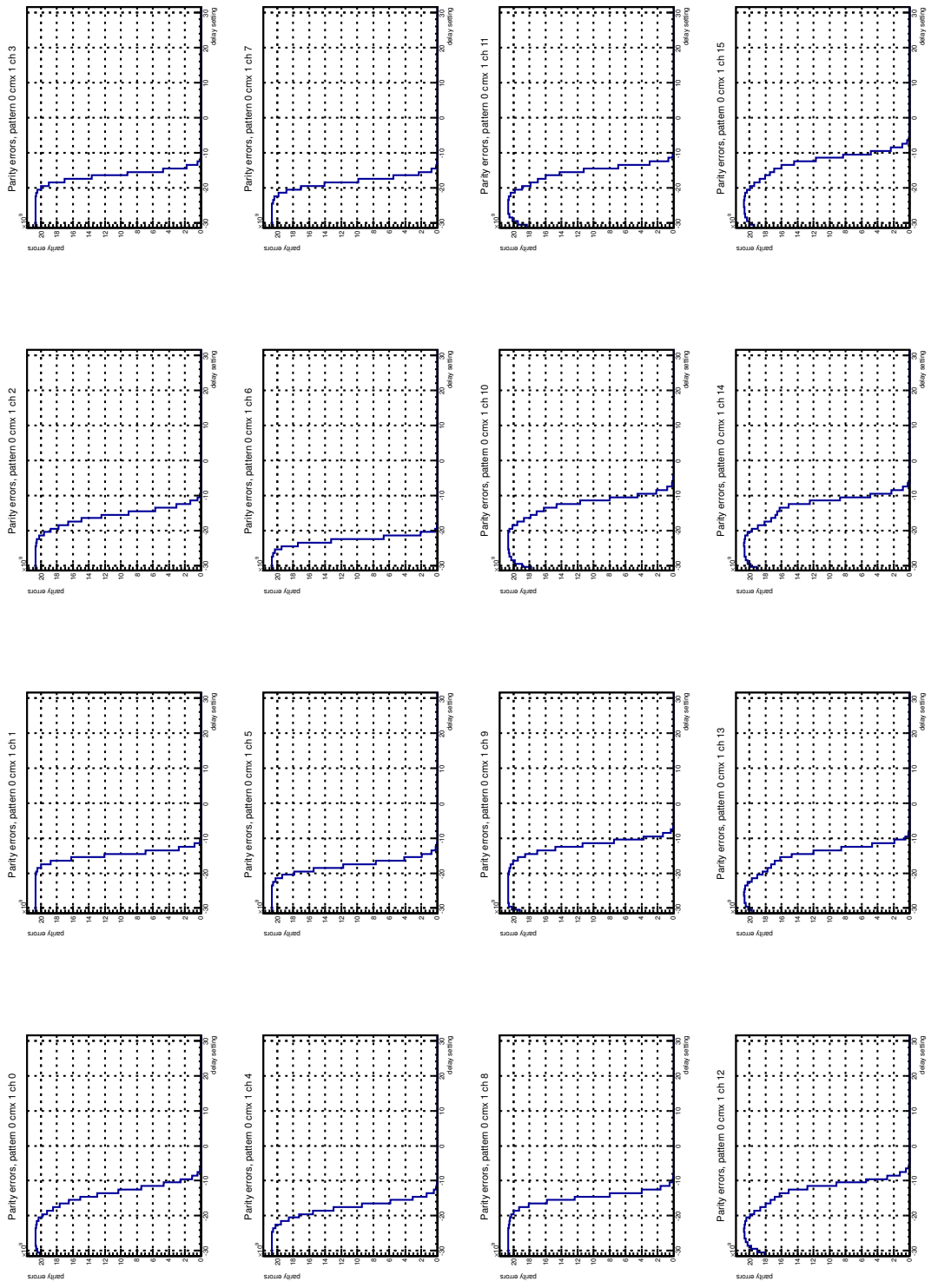


Figure 22: Summary of the parity errors for CMX 1 for all channels and each bit versus the delay setting and summed over all patterns for run 1396010274.

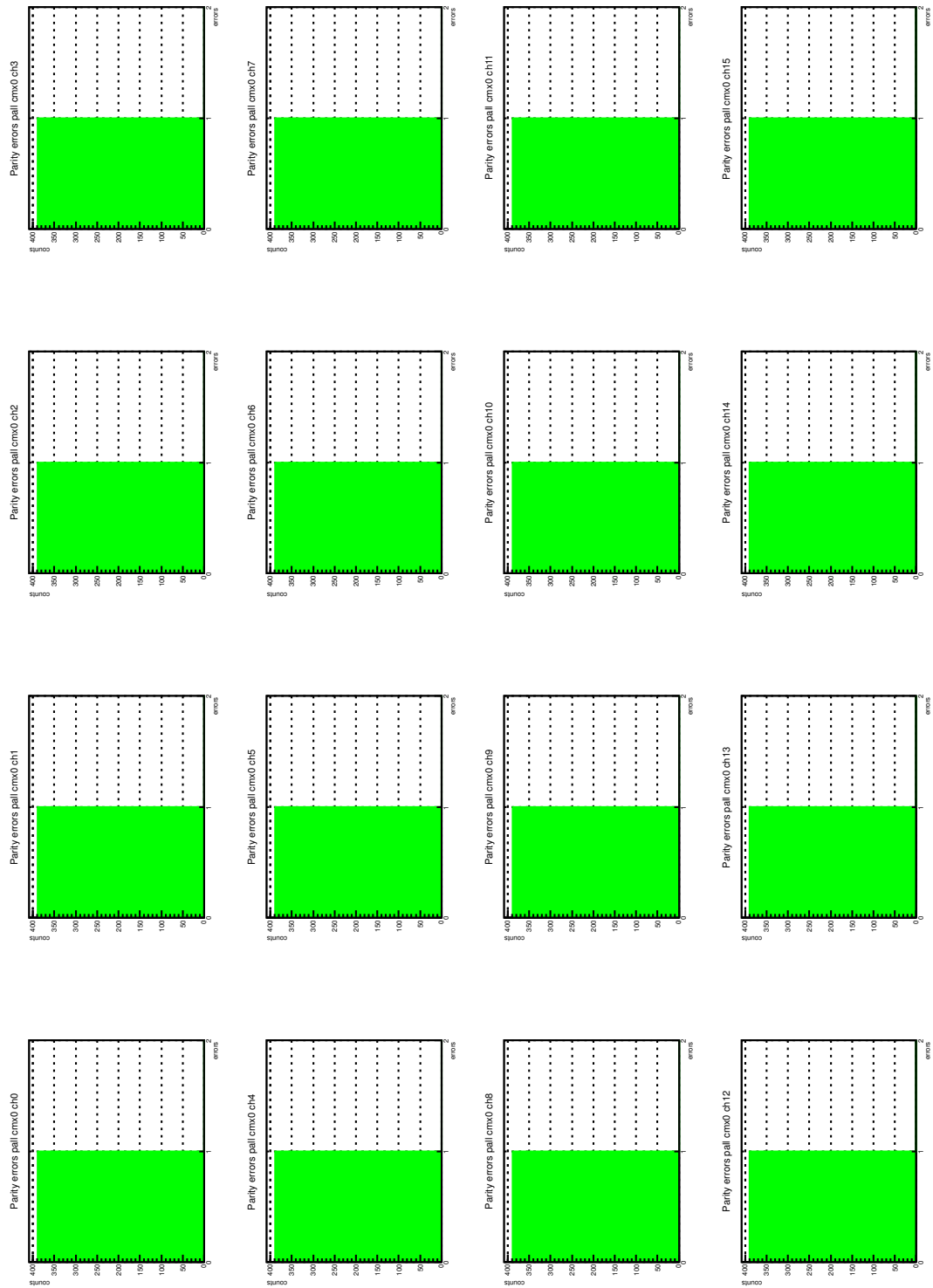


Figure 23: Summary of the parity errors for CMX 0 for all channels versus the delay setting and summed over all patterns for run 1396049227.

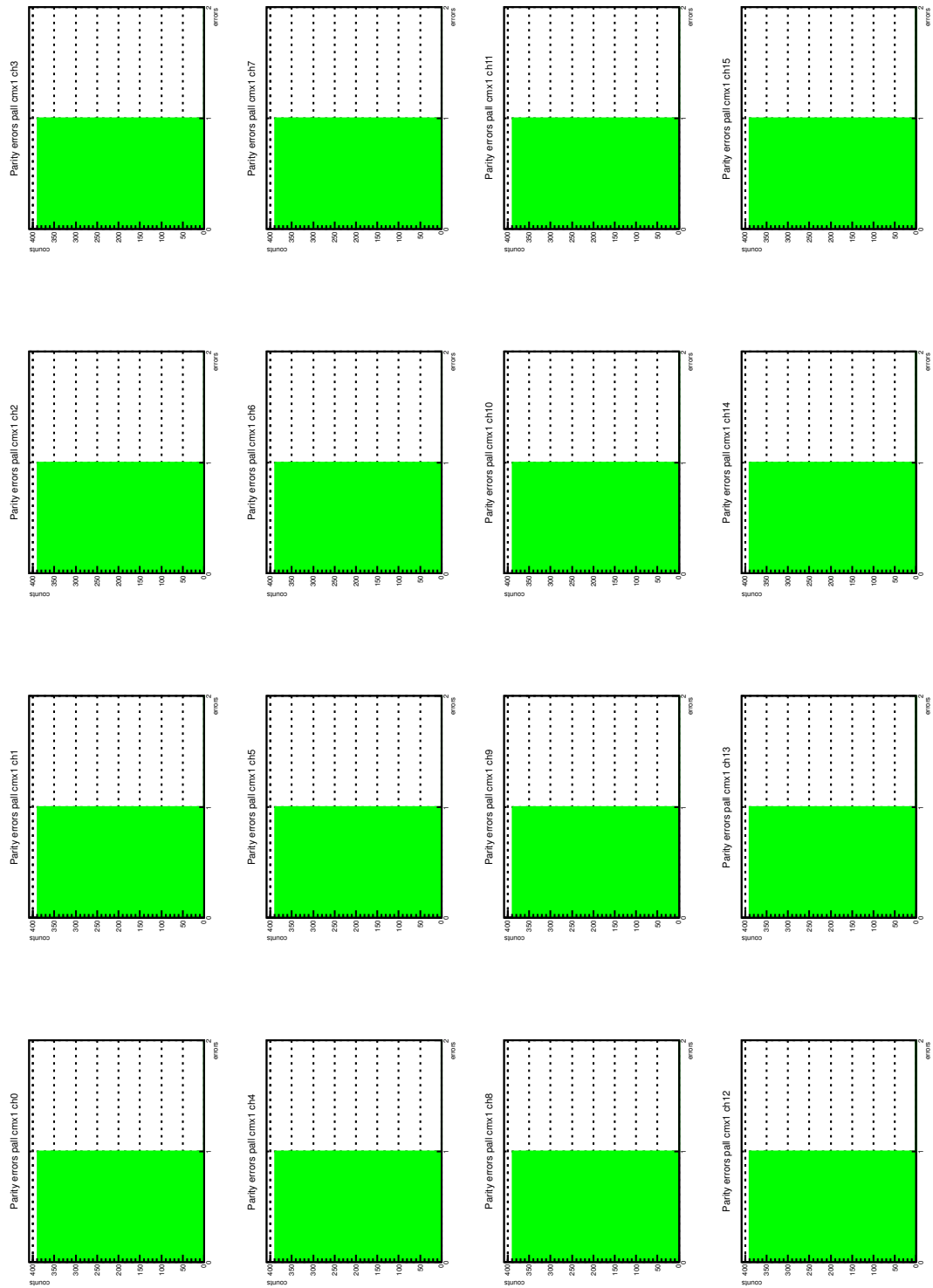


Figure 24: Summary of the parity errors for CMX 1 for all channels versus the delay setting and summed over all patterns for run 1396049227.

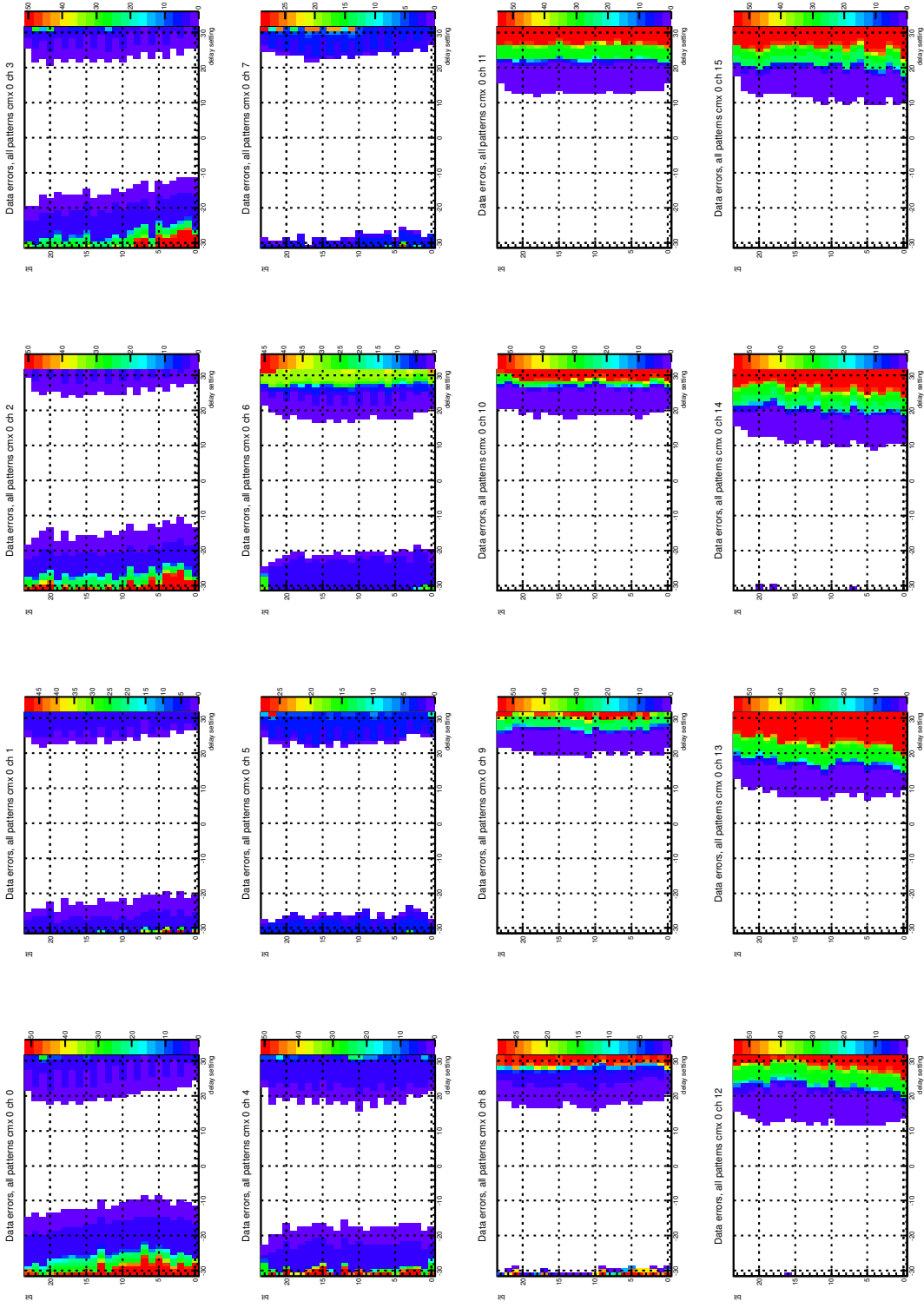


Figure 25: Summary of the data errors for CMX 0 for all channels and each bit versus the delay setting and summed over all patterns for run 1396964926.

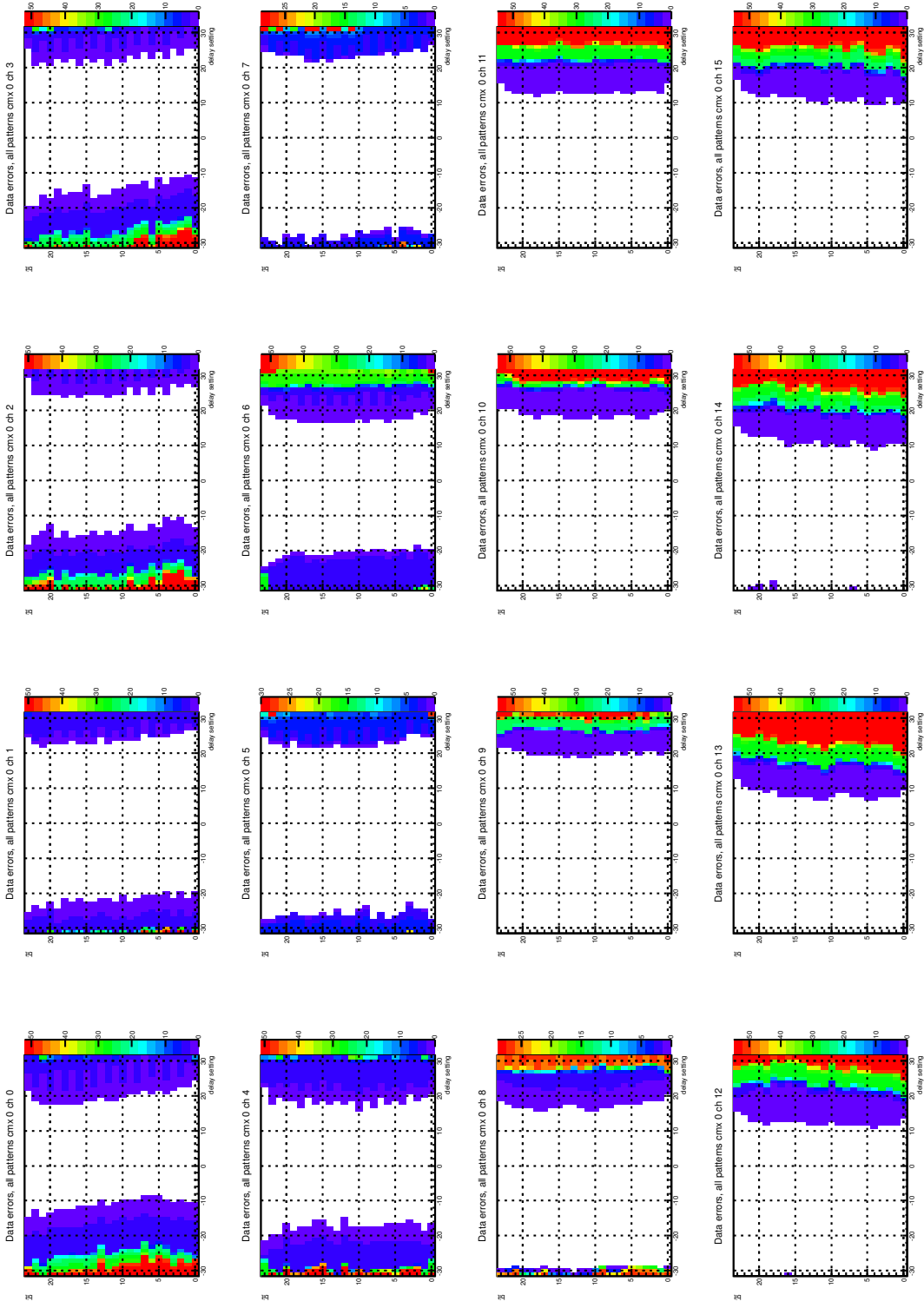


Figure 26: Summary of the data errors for CMX 0 for all channels and each bit versus the delay setting and summed over all patterns for run 1396970468.

3.5 CPM crate

Table 2: Overview of the test performed in the CP0 crate

run	CMX	time [s]	cycles	patterns	delay	total time [h]	figure
1396388038	0/1	5.0	1	all patterns	scan	4.81	27 28
1396406084+	0/1	50.0	8	all patterns	-10/-10	6.11	29 30
1396625660	0/1	0.1	1	all patterns	scan	0.10	31 32
1396629697	0/1	5.0	1	all patterns	scan	4.81	33 34
1396650911+	0/1	50.0	23	all patterns	-10/-10	17.57	35 36
1396647710	0/1	50.0	1	random	scan	0.88	37 38
1396716630+	0/1	50.0	1265	random	-10/-10	17.57	40 41
1396949335+	0	85.0	1	random	scan	1.49	39

The same set of tests that was performed in the JEP0/1 crate was done in the CP0 crate. First a scan over all delay settings using all patterns was performed. The errors for each data line were recorded during the scan and from this the center and width of the valid timing window was found. Then for a good delay setting a longer dwell time was chosen and again all patterns were tested. The procedure was repeated with the pseudo random data. The same firmware configuration was used for the patterns and the pseudo random data.

A main difference to the tests with the JEMs is that the firmware configuration of the CPMs cannot synchronize the start of the pattern via the BC reset signal. For the first tests in runs 1396388038, 1396406084 only the CMX were synchronized and then the comparison patterns that are loaded into the CMX were modified to match the different beginnings of the incoming events. From run 1396625660 on the firmware configuration of the CPMs was able to perform a reset of the event loop triggered by writing to a reset register. With a series of resets all 14 CPM modules were synchronized with respect to the first event in pattern 0.

The first run 1396388038 using a dwell time of 5 s per delay setting and pattern (4.8 h total run time) shows that the data validity window is at least 40 taps (= 3.1 ns) wide, since only one edge of the window can be seen (see Figures 27 and 28). For both CMX's the validity window only exhibits module-to-module variations and the variations depending on the position of the CPM module to the CMX for CMX 0 is not present here. A longer run 1396406084 (50 s dwell time for all patterns, 8 cycles) with a total run time of 6.1 h at delay setting -10 on both CMX showed no error (Figures 29 and 30).

The effect of the synchronous start of the patterns can be seen in Figures 31 and 32 for run 1396625660. For this and all subsequent runs the start address was synchronised using the procedure described above. In this short run with a dwell time of 0.1 s there is no significant difference in the width or position of the validity window with respect to run 1396388038. Run 1396629697 (see Figures 33 and 34) repeats run 1396388038 with a total run time of 4.8 h and again there is no significant change in the validity window between the two runs.

Run 1396650911 extends run 1396406084 by 23 more cycles using all patterns at delay setting -10 for both CMX's (see Figures 35 and 36). The total run time is 17.6 h. The total accumulated run time is 23.7 h and no errors have been found. This translates into an upper limit on the BER of $7.3 - 9.9 \times 10^{-14}$ for a data rate of 160 Mbit/s.

The parity errors have been recorded for run 1396647710 while scanning all delay settings (see Figures 37 and 38). The dwell time was set to 5 s per delay setting. Since the firmware configuration has not been changed when providing random data, the validity window size and position has not significantly changed. All channels on both CMX show the expected behavior of the parity error counts which drops to zero in the region of good timing and saturate at the total event counts in the region with bad timing

(2×10^9 events are expected for a dwell time of 50 s). The only exception is channel 1 (from CPM 0) on CMX 0 which shows a large error count in the transition region between the error free and error saturated region. In the figures this large error count creates an overflow while producing the histogram, hence it shows a negative count. This behaviour is understood from the clocks used for counting: While the 80 MHz clock is used for the comparison and flagging the error, the counts are increased by the 40 MHz clock. If the clocks are moved too close to each other the system enters a meta-stable timing region where it can happen that the count is increased twice per event error. This does not have any influence on the width or position of the validity window. Later a new firmware configuration was used in which a protection against double counting the errors was implemented and the results from run 1396949335 in Figure 39 (using only CMX 0) with an accumulated dwell time of 85 s (total run time 1.5 h) shows the expected behavior.

For run 1396716630 the delay settings were chosen to the -10 on both CMX's and 1265 cycles with random data and a dwell time of 50 s were used. The total run time corresponds to 17.6 h and no errors have been found (see Figures 40 and 41). The upper limit on the event error rate is 40×10^{-14} .

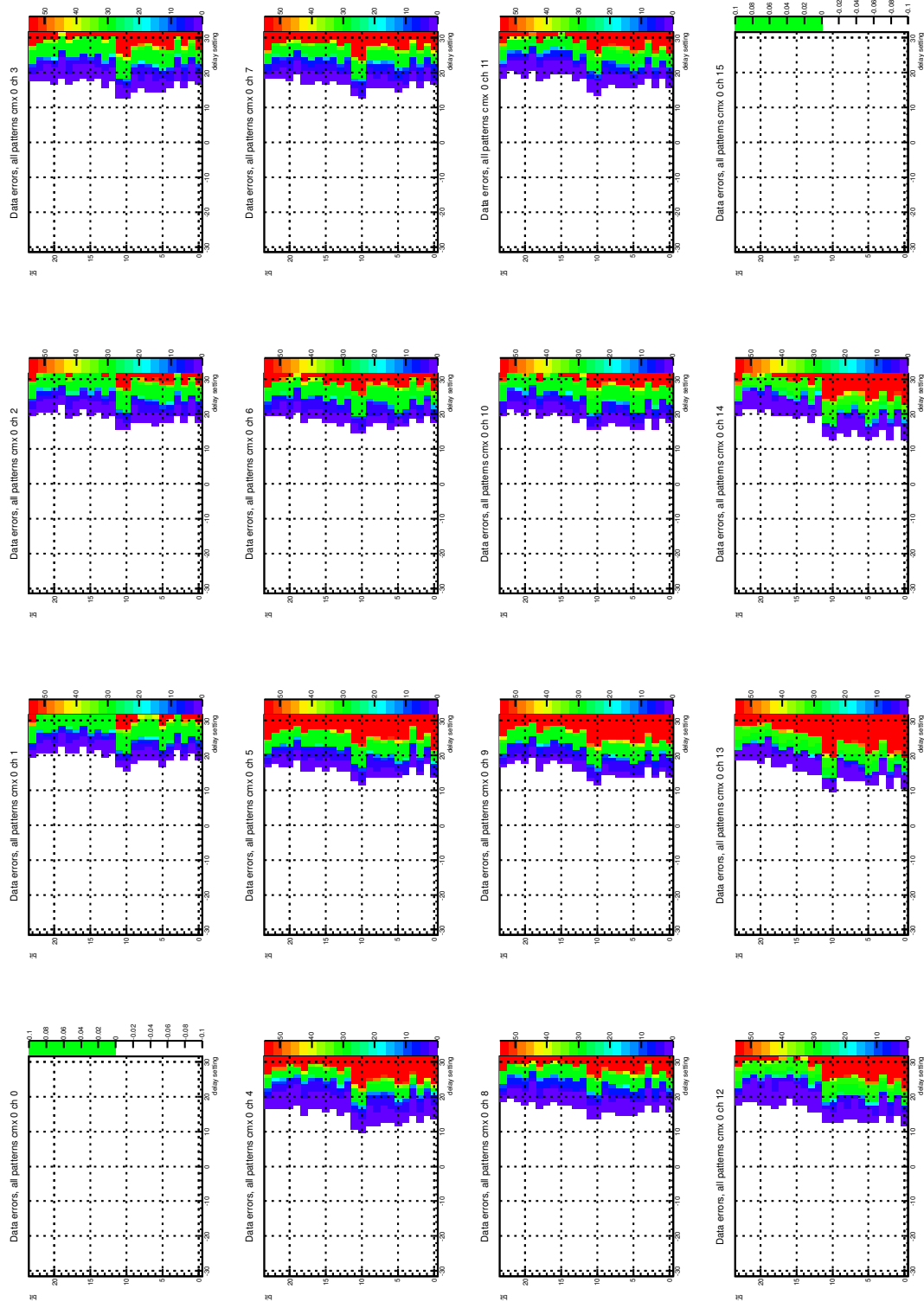


Figure 27: Summary of the data errors for CMX 0 for all channels and each bit versus the delay setting and summed over all patterns for run 1396388038.

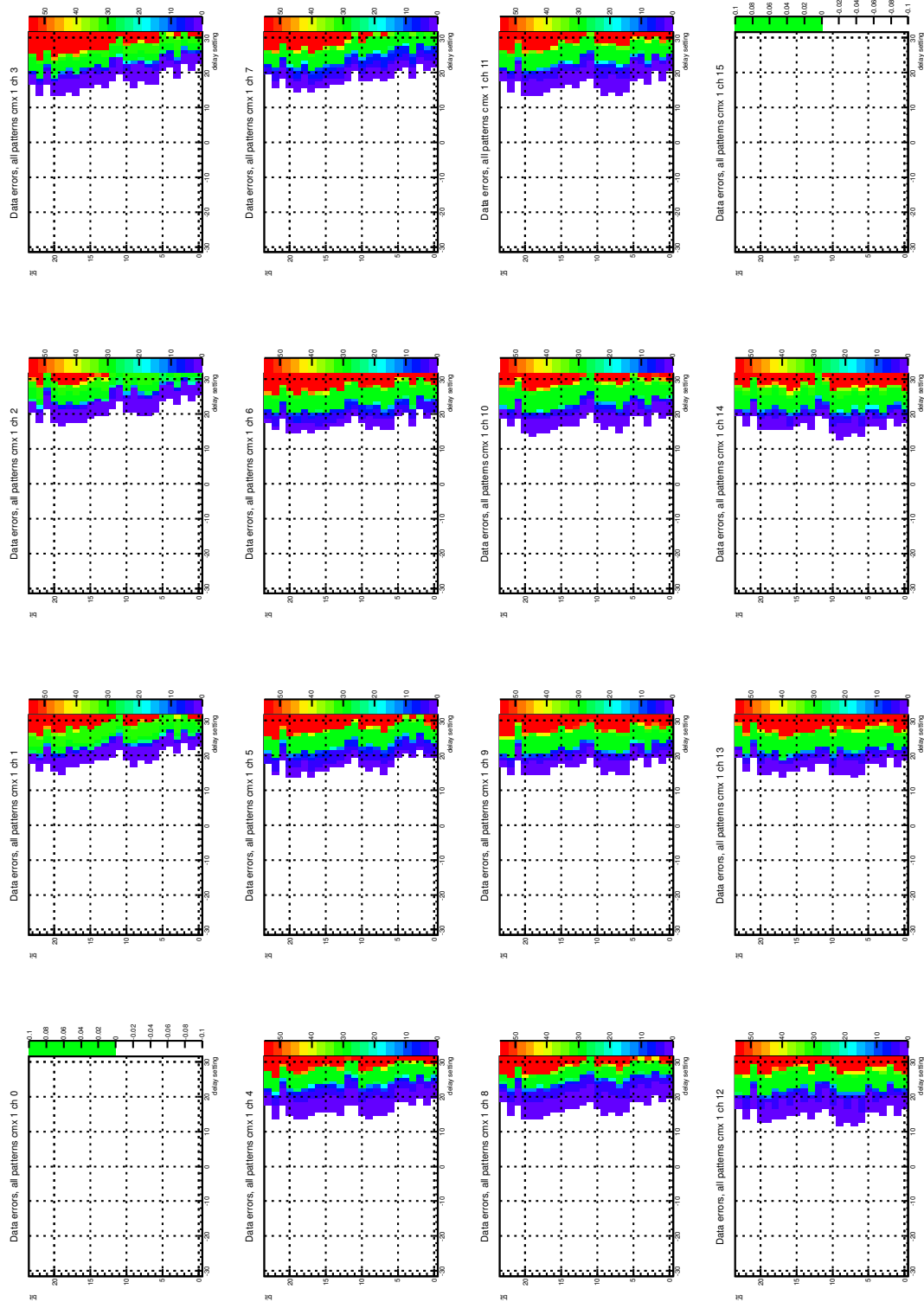


Figure 28: Summary of the data errors for CMX 1 for all channels and each bit versus the delay setting and summed over all patterns for run 1396388038.

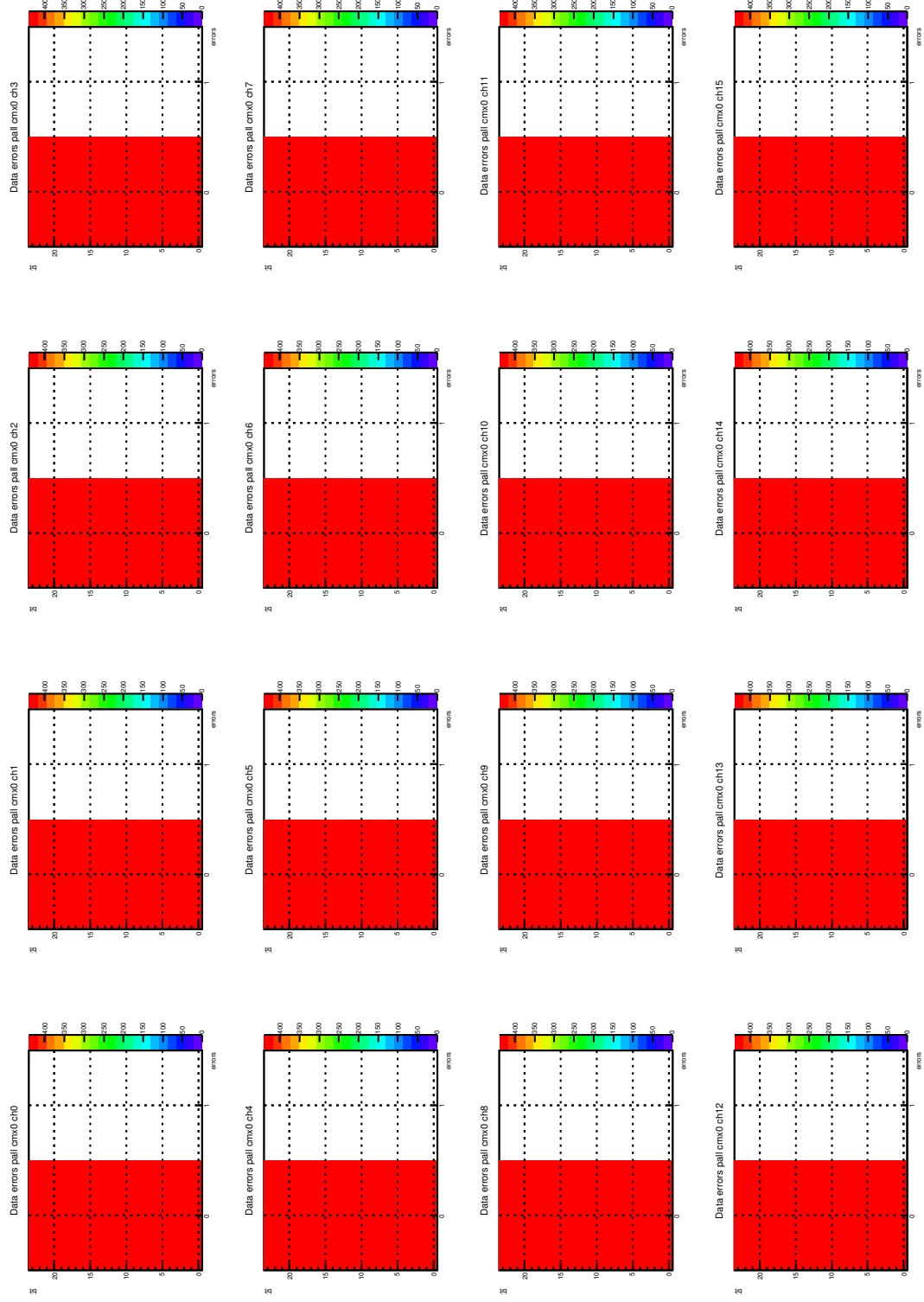


Figure 29: Summary of the data errors for CMX 0 for all channels at fixed delay setting -10 and summed over all patterns for run 1396406084.

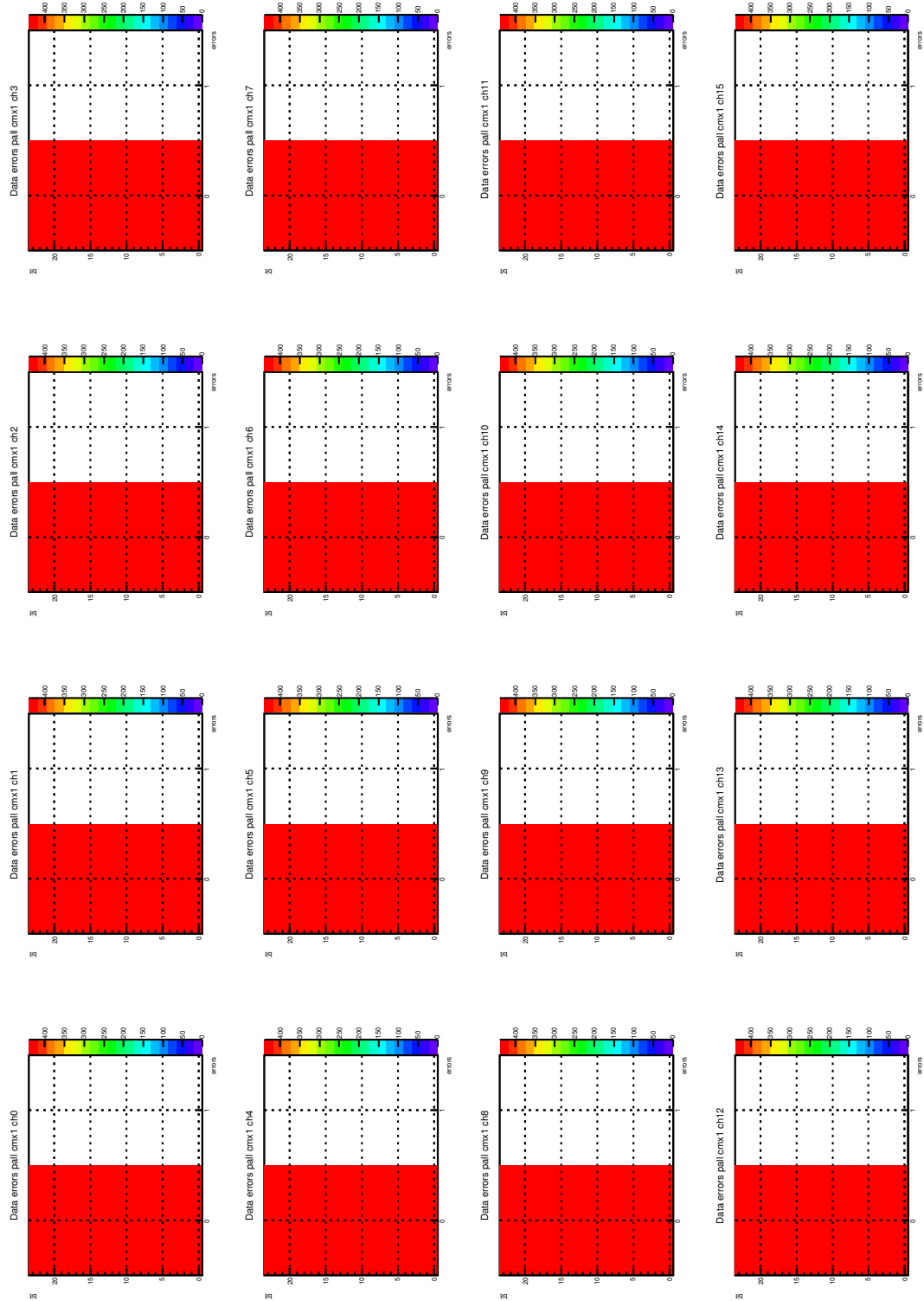


Figure 30: Summary of the data errors for CMX 1 for all channels at fixed delay setting -10 and summed over all patterns for run 1396406084.

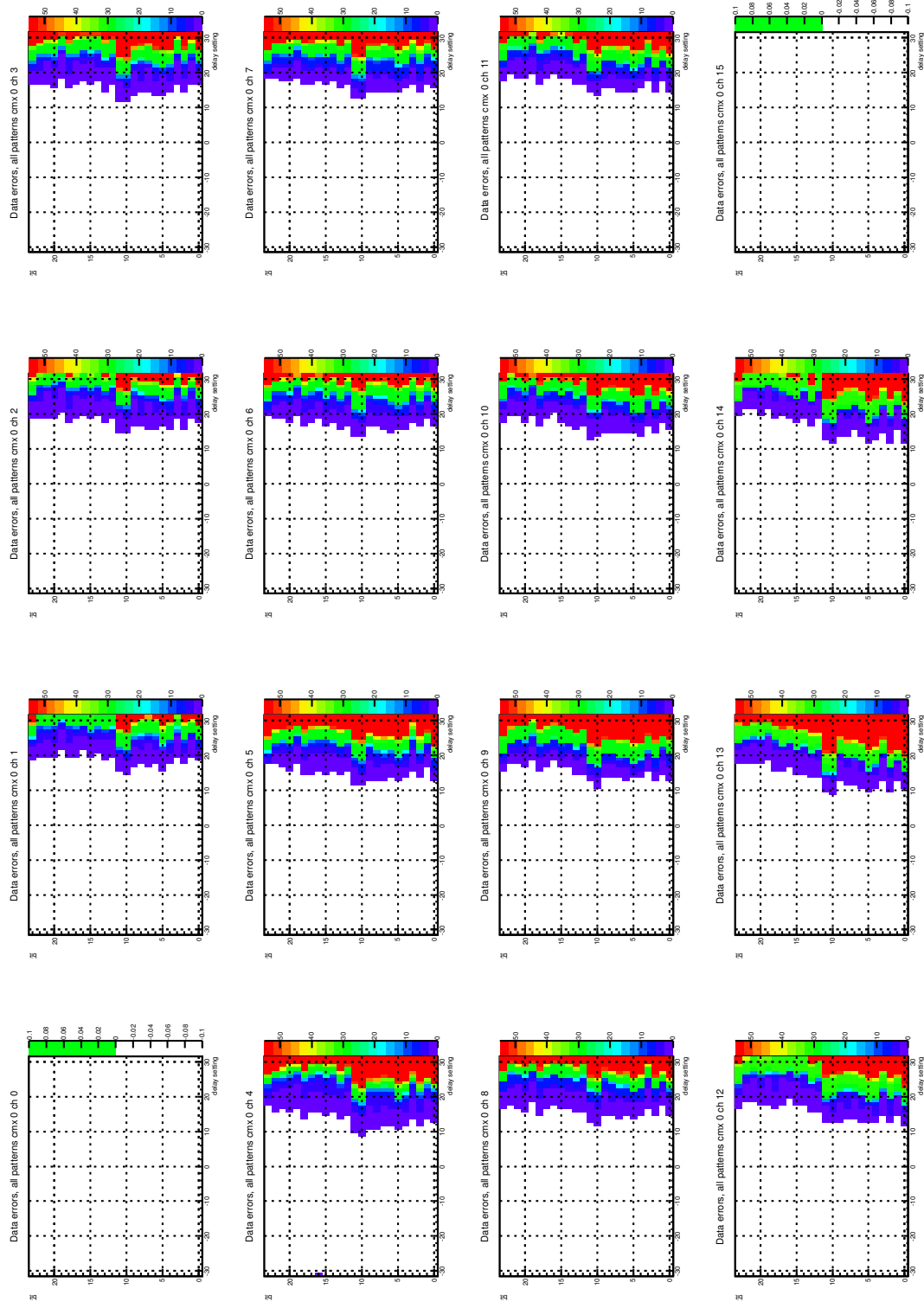


Figure 31: Summary of the data errors for CMX 0 for all channels and each bit versus the delay setting and summed over all patterns for run 1396625660.

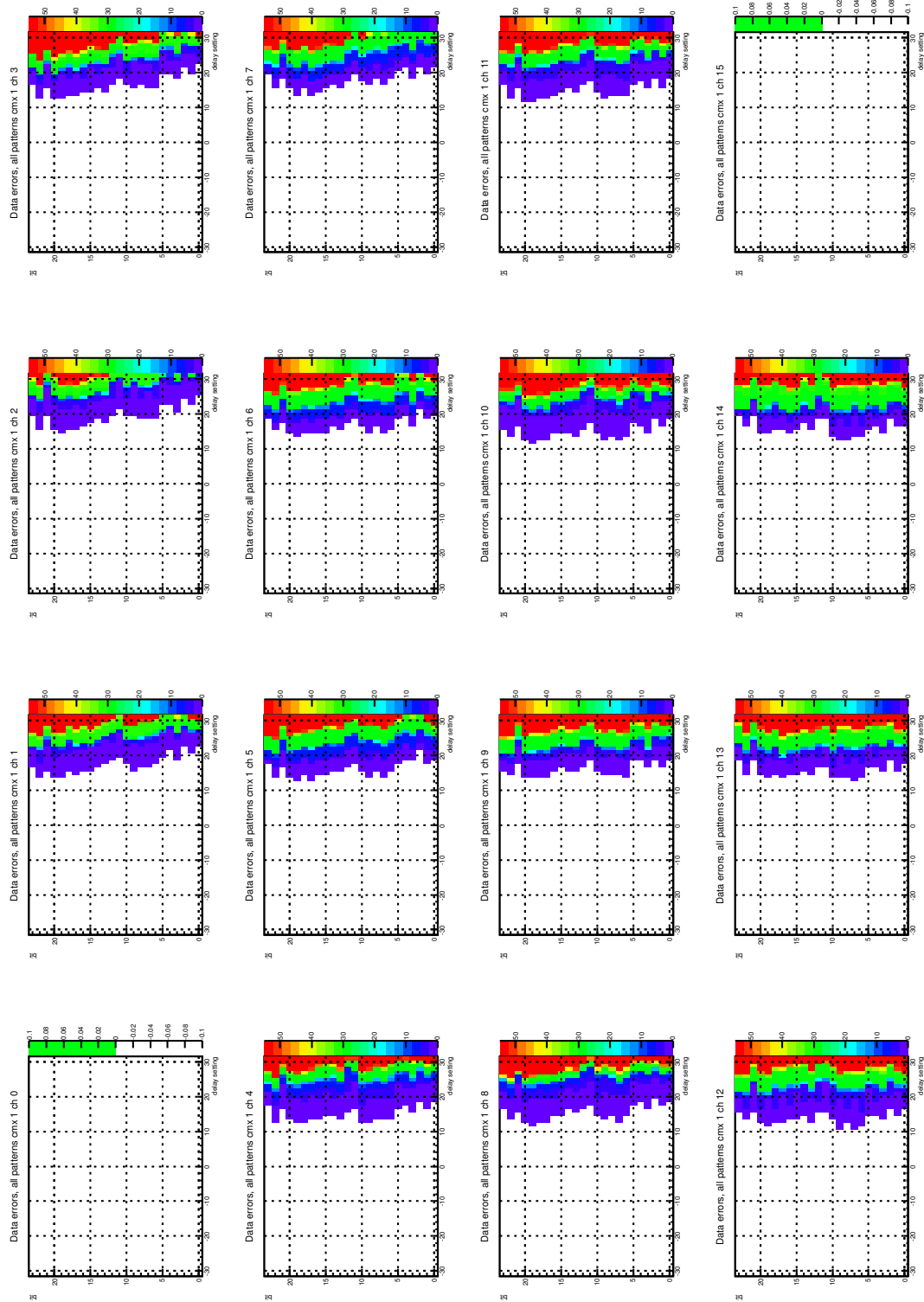


Figure 32: Summary of the data errors for CMX 1 for all channels and each bit versus the delay setting and summed over all patterns for run 1396625660.

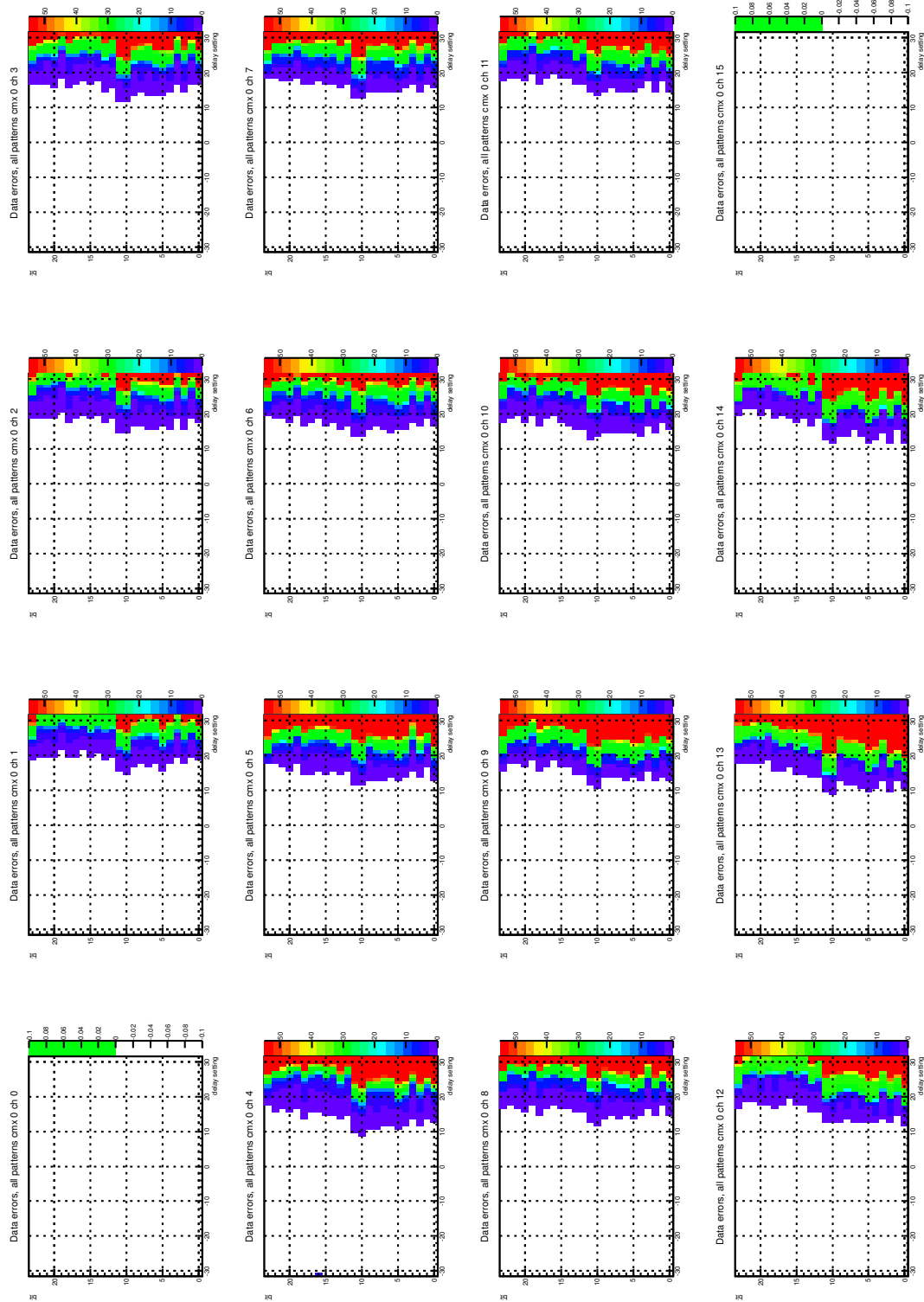


Figure 33: Summary of the data errors for CMX 0 for all channels and each bit versus the delay setting and summed over all patterns for run 1396629697.

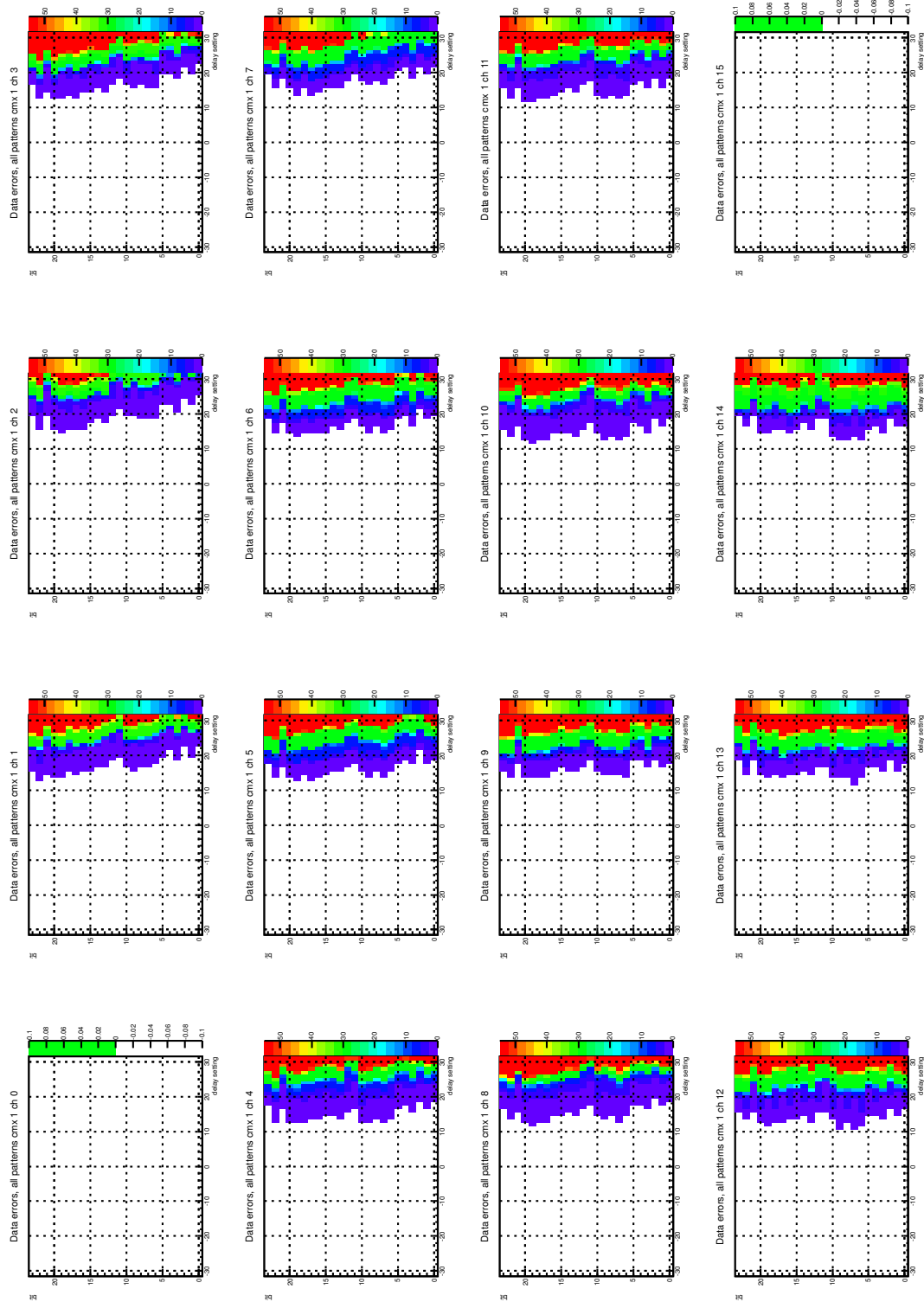


Figure 34: Summary of the data errors for CMX 1 for all channels and each bit versus the delay setting and summed over all patterns for run 1396629697.

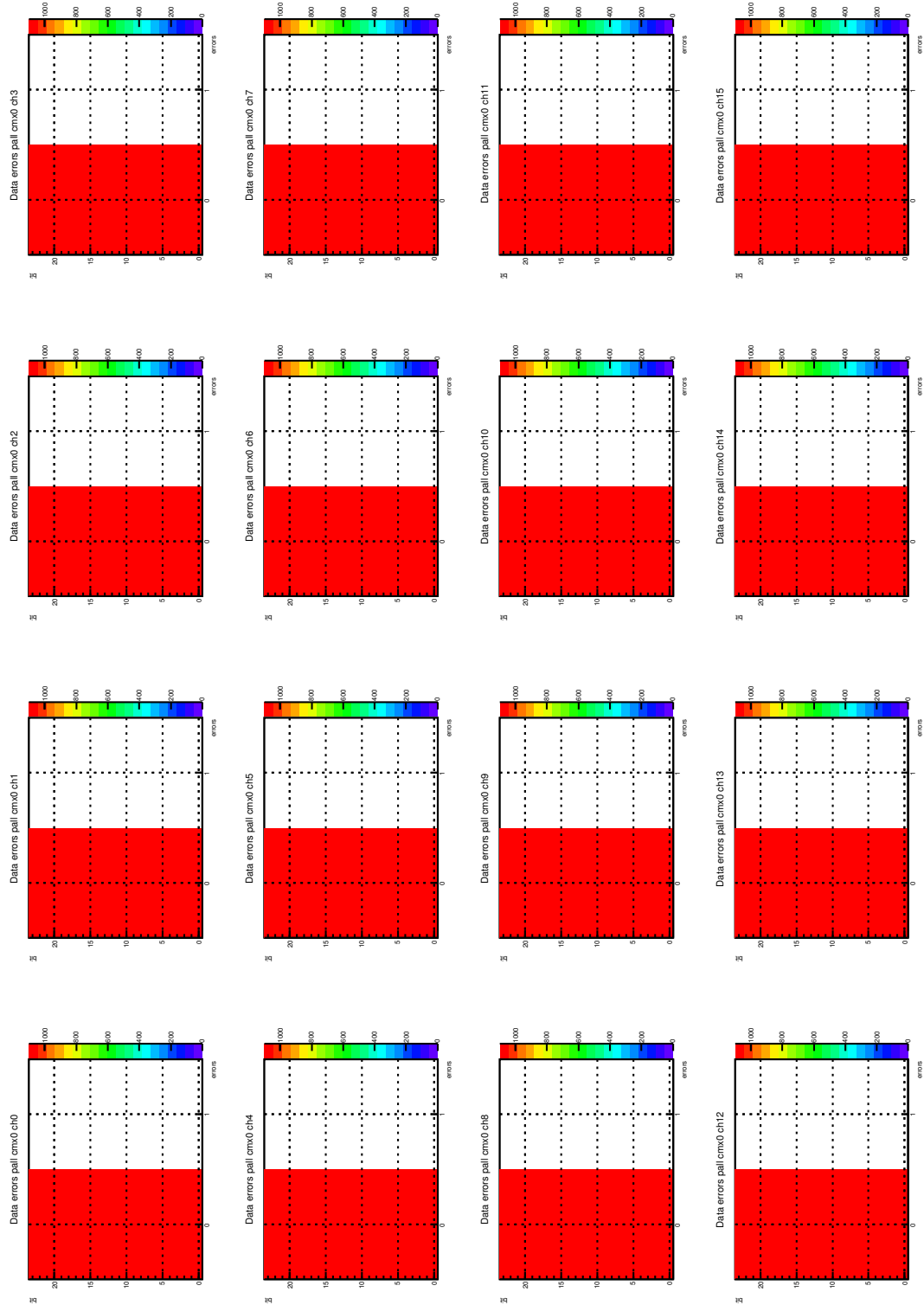


Figure 35: Summary of the data errors for CMX 0 for all channels at fixed delay setting 0 and summed over all patterns for run 1396650911.

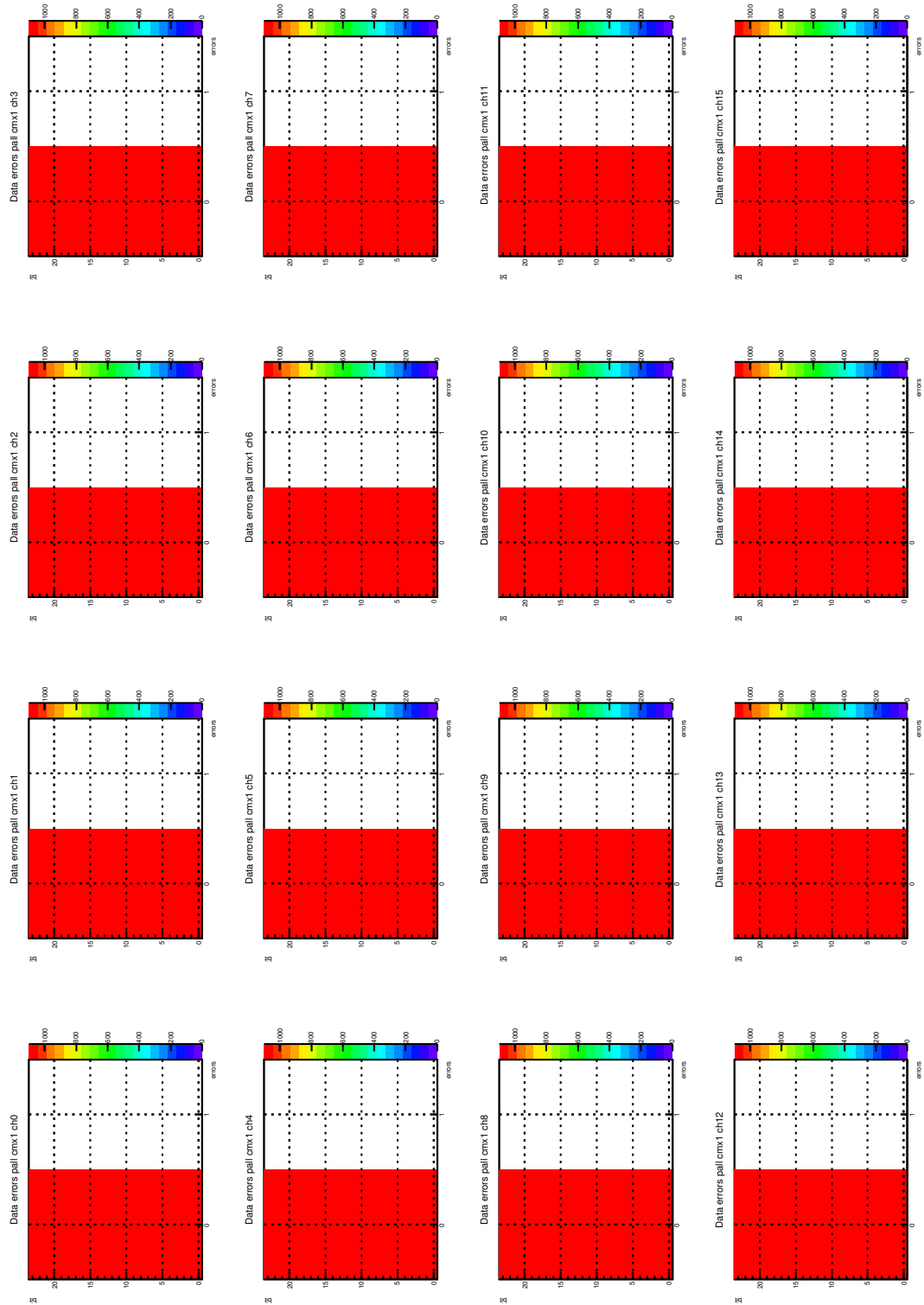


Figure 36: Summary of the data errors for CMX 1 for all channels at fixed delay setting 0 and summed over all patterns for run 1396650911.

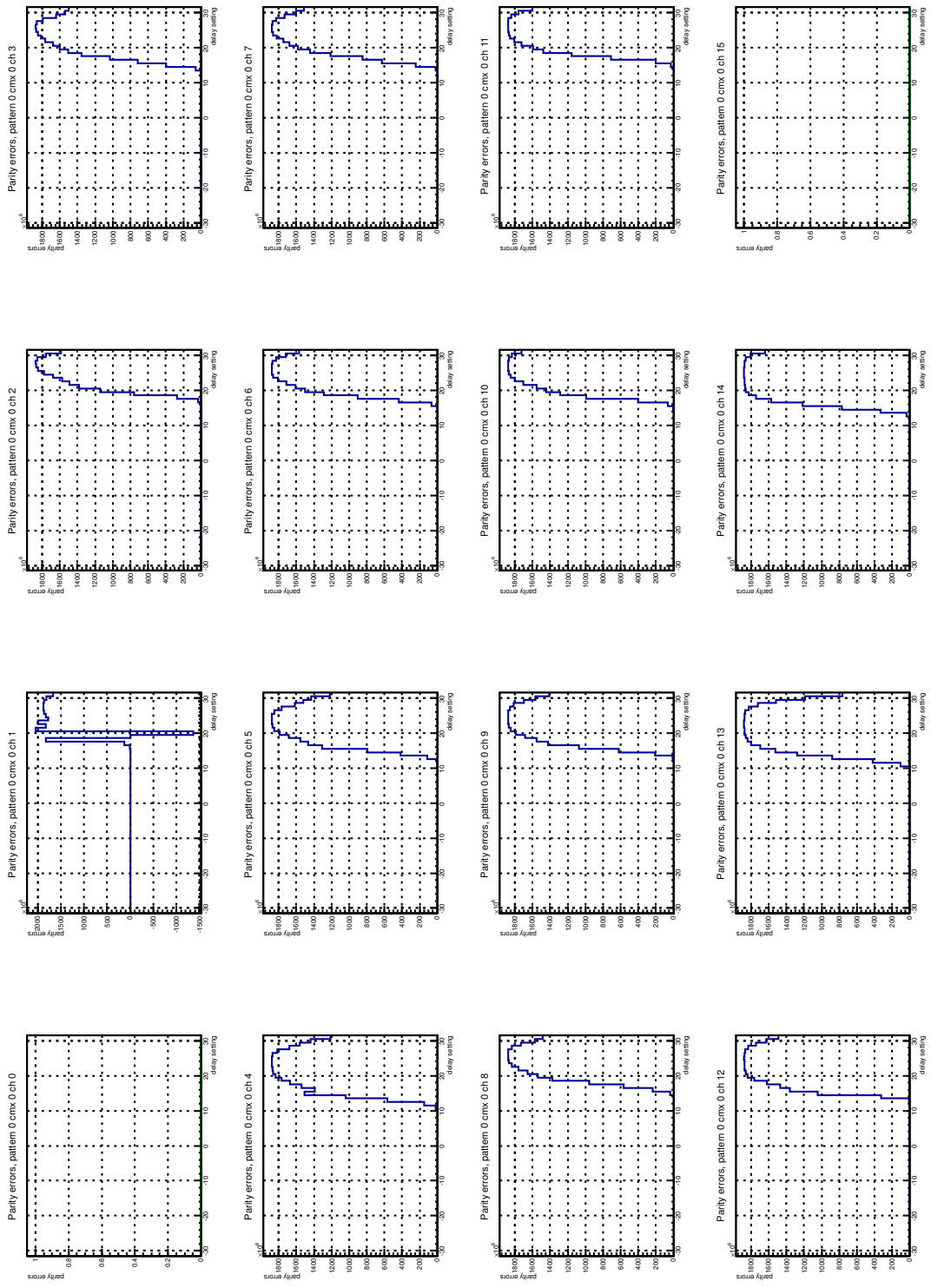


Figure 37: Summary of the parity errors for CMX 0 for all channels and each bit versus the delay setting and summed over all patterns for run 1396647710.

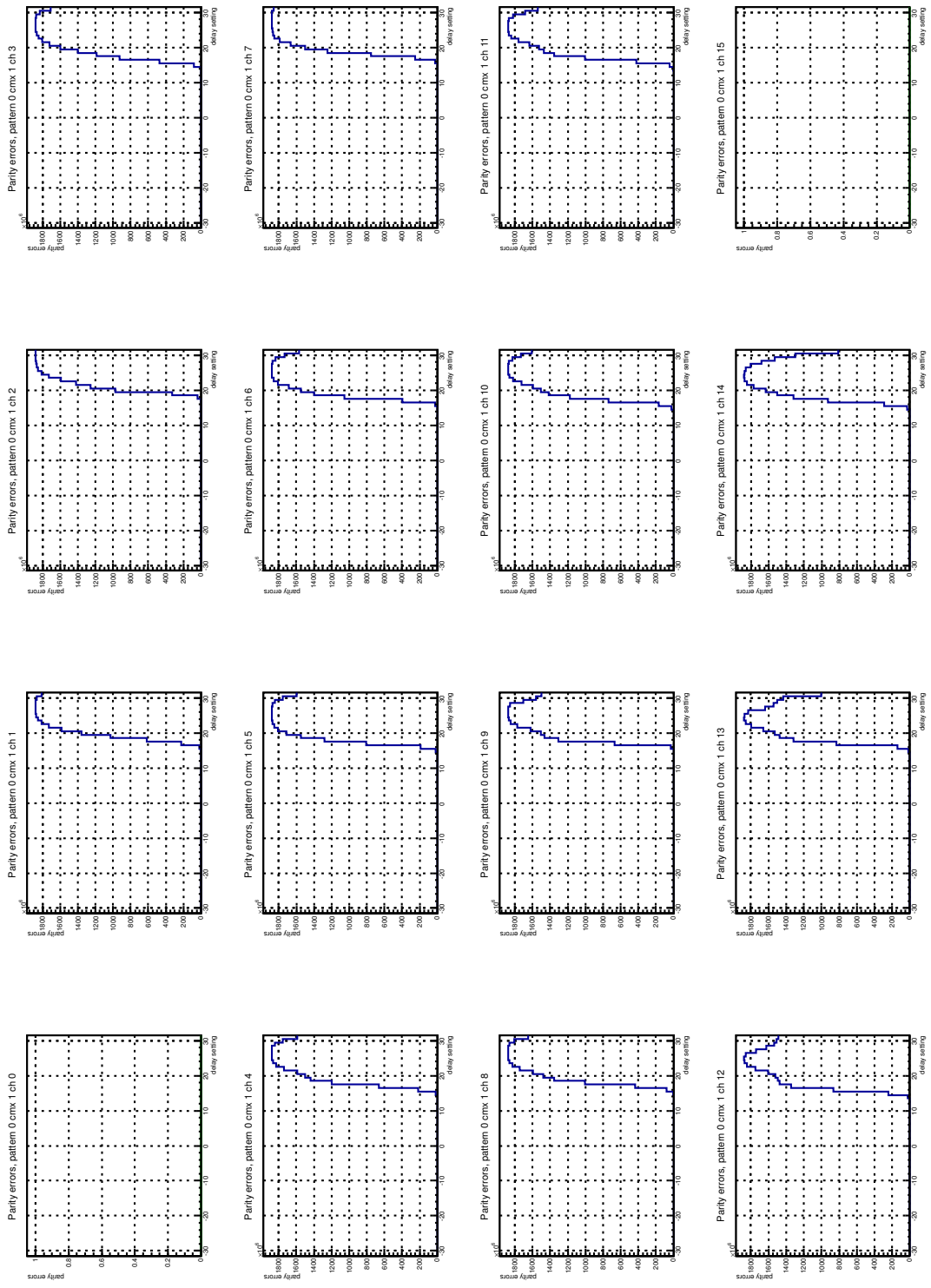


Figure 38: Summary of the parity errors for CMX 1 for all channels and each bit versus the delay setting and summed over all patterns for run 1396647710.

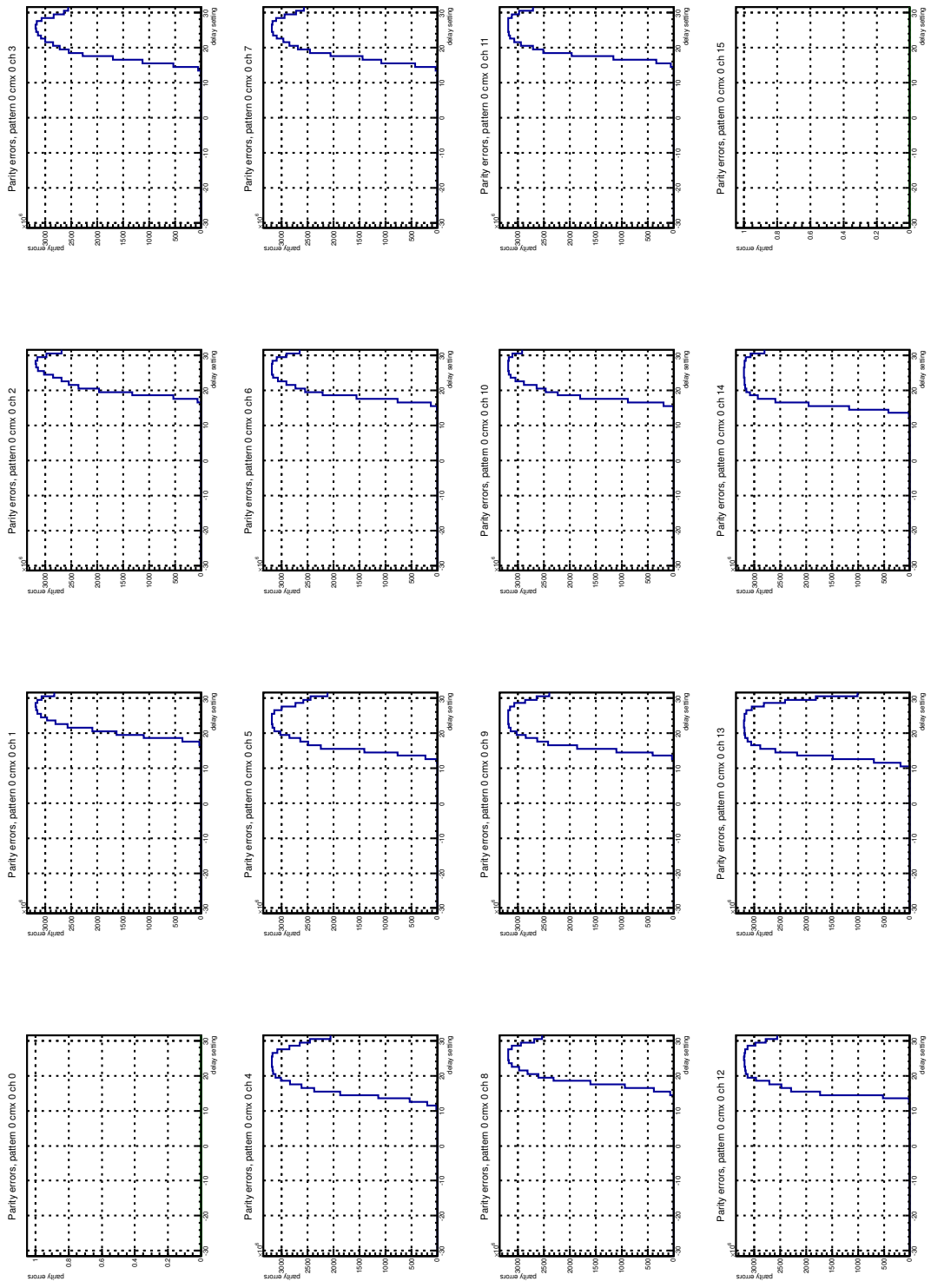


Figure 39: Summary of the parity errors for CMX 0 for all channels and each bit versus the delay setting and summed over all patterns for run 1396949335.

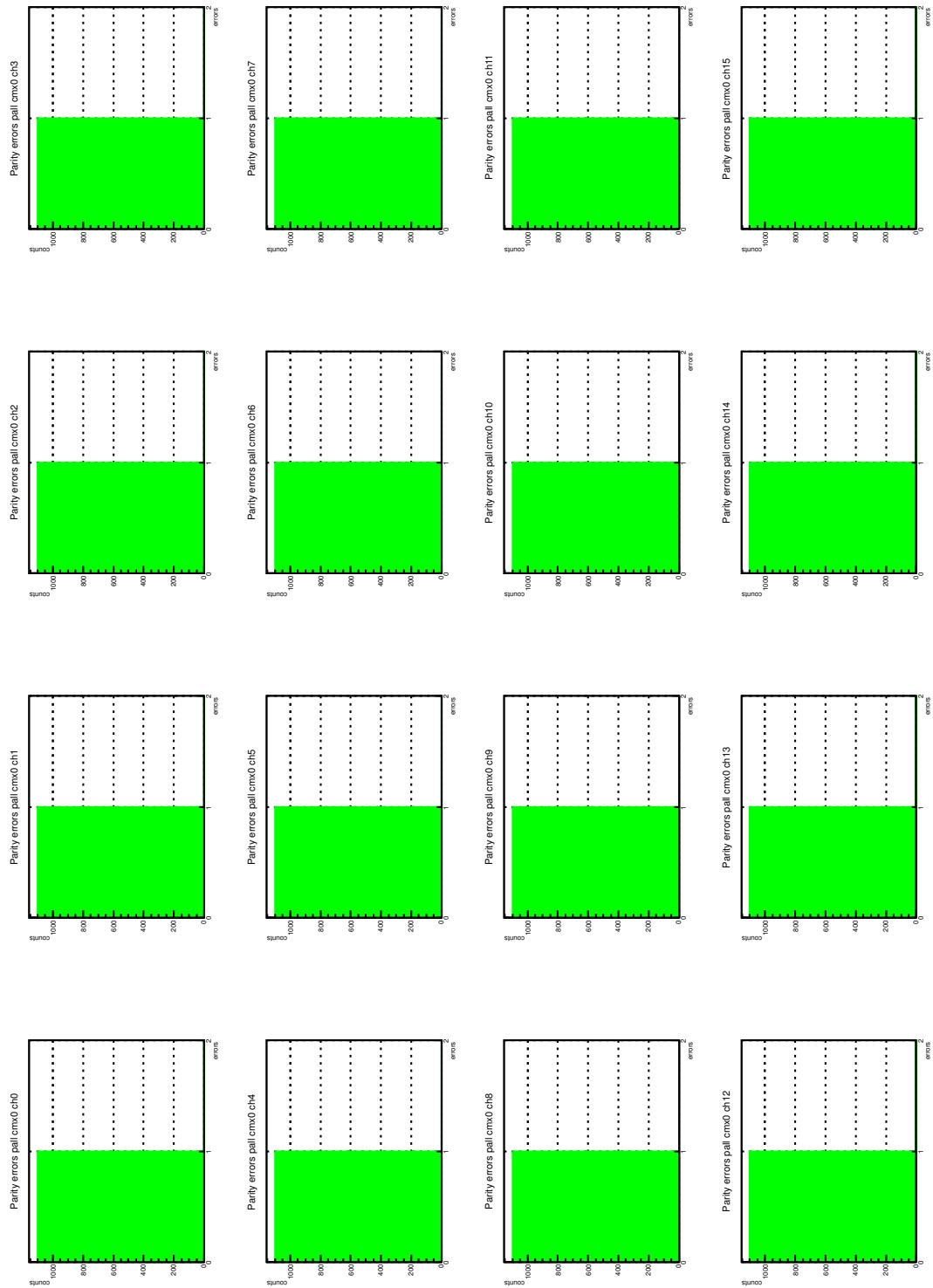


Figure 40: Summary of the parity errors for CMX 0 for all channels versus the delay setting and summed over all patterns for run 1396716630.

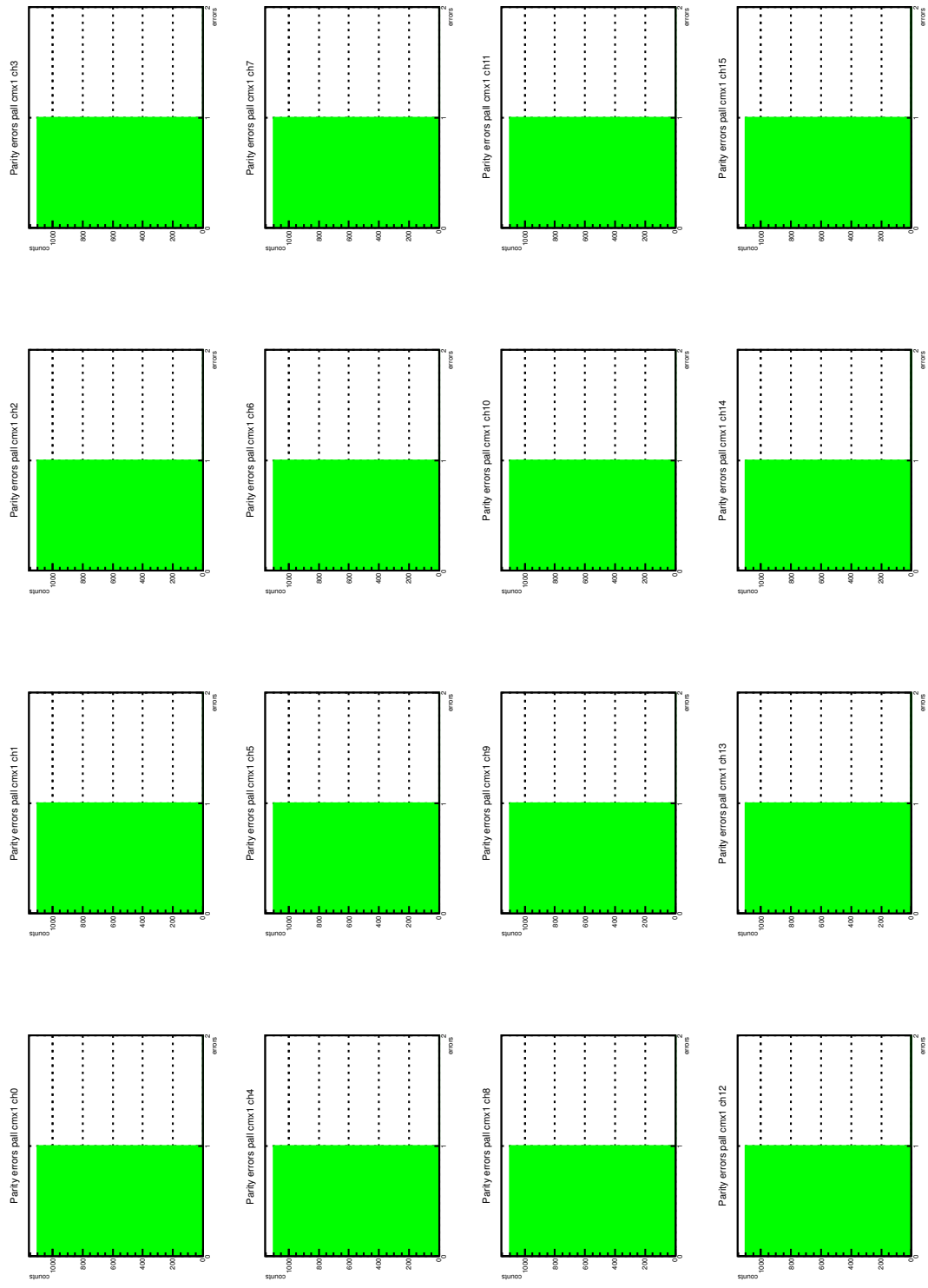


Figure 41: Summary of the parity errors for CMX 1 for all channels versus the delay setting and summed over all patterns for run 1396716630.

3.6 Conclusion

The two prototypes CMX SN-01 and CMX SN-03 have been tested in full crate tests in the JEP0 crate with 16 JEMs and in the CP0 crate with 14 CPMs. Generally, no power or heat issues have occurred throughout the tests in the full crates for the duration of the tests. The data validity window was probed for both CMX's and in both crates. The width of the timing window has been determined with data stress patterns using event-by-event comparisons. The window was also probed with random data using parity checks. In short runs (\approx min) and longer runs (\approx h) a valid window was found for all data bits. Although differences in the location of the window were found for JEMs and CPMs and not always the full width could be probed, the width was determined to be at least 30-40 taps corresponding to a window width of 2.3 ns and 3.1 ns, respectively. The differences in the location of the window were within the adjustable delay setting window, so that for each module a good operation point can be found. This window is wide enough to guarantee stable operation. In long term tests over a few hours at a good delay setting no data errors have been found in tests with patterns and no parity errors have been found for random data. In the JEM crate tests with a duration between 5.3 h and 7.6 h have been performed and in the CPM crate the tests had a duration between 17.6 h and 23.7 h. This corresponds to an upper limit on the BER of $7.3 - 22 \times 10^{-14}$ (best of each crate test) for a data rate of 160 Mbit/s. Assuming the worst case that any bit error in one of the 400 backplane lines of all 6 CMX modules can trigger an event, an event error rate of 0.03 - 0.09 Hz is expected. This surpasses the requirement on the error rate in the L1 trigger system by far.

4 LVDS IO tests

4.1 Standalone tests in loopback configuration

Each of the CMX's cable IO's can be independently configured as an input or as an output by appropriately configuring the LVDS transceivers and voltage translators connected to the Base and Topo function FPGA's single ended I/O pins. In addition the front panel cable I/O (CTP connectors 1 and 2) can be independently configured to send the cable data to one or both FPGA's or to transmit data from a selected FPGA. This capability allows for extensive stand-alone loopback tests.

For this test the CMX's voltage translators and LVDS transceivers were configured such that the CTP1 connector was driven by the Base function FPGA. Data received on the CTP2 connector was forwarded to both Base and Topo function FPGAs. The rear transition module (RTM) connectors 1 and 2 were configured as outputs and connector 3 was configured as input.

The data sources (CTP 1, RTM 1, 2) were configured to transmit a fixed stress pattern at 80 Mbps/line. The pattern respects even parity on per-event basis. In the pattern there are periods of silence in logic '0' on all bits with pulses of logic state '1', periods of silence in logic state '1' with pulses of logic '0' and periods of switching data. The pattern is cyclical with 255 event period. One of the lines on each output cable was set up as 40 MHz clock line with rising edge in the middle of the data window. The output IO buffers on the FPGA were configured to provide 6 mA drive current. The FPGA inputs were configured as DDR input buffers. Data capture and error checking was performed using the forwarded clock eliminating the need for tuning the clock phase. Xilinx Chipscope cores were utilized to detect parity errors.

Cables used in the test were the 9 m cable connecting CTP 1 connector to CTP 2 and the 2 m cable connecting connector RTM 1 or 2 to RTM 3.

The test was run for approximately 10 minutes sending data from RTM 1 and receiving on RTM 3 and for approximately 1 hour sending data from RTM 2 and receiving on RTM 3 and simultaneously sending data from CTP 1 and receiving on CTP 2. During that time no parity errors were detected. Efficacy

of error detection was confirmed by unplugging the cable and verifying that the Chipscope cores were triggered.

4.2 Data transmission to the CTP

In this test CMX SN-01 was deployed in the JEP-01 crate in the logical slot 0 (left side of the crate). From this location a cable is routed to the CTP. Both CMX's CTP connectors were configured as outputs with data provided by the Base function FPGA. The FPGA was configured to provide data in two modes selectable via VME input: a cyclical stress pattern and pseudorandom data. In each case the data rate is 40 Mbps/line. A 40 MHz clock is forwarded on one of the lines however it is not actually used by the CTP for the data capture.

The random data is generated using an array of 47-bit LFSRs (one LFSR per bit, running in parallel) and preserved odd parity. The stress pattern has a period of one orbit (3564 events) and comprises:

- Walking 1's
- Walking 0's
- Pulse of logic state '1' surrounded by logic state '0' on all bits
- Pulse of logic state '0' surrounded by logic state '1' on all bits
- Pulse of logic state '1' surrounded by logic state '0' on a given bit while all other bits pulse logic state '0' surrounded by logic state '1'
- Pulse of logic state '0' surrounded by logic state '1' on a given bit while all other bits pulse logic state '1' surrounded by logic state '0'
- Maximally switching data, all bits in-phase (F's and 0's)
- Maximally switching data, even bits out of phase with odd bits (A's and 5's)

The stress pattern does not respect a defined parity.

The CTP has the ability to check the incoming data against a pre-defined pattern. This comparison is software-driven and so can be performed only at a frequency of several Hertz, however every bit is checked. The CTP also detects parity errors. Utilizing CTP's TDC's one can measure phase of the transitions on each incoming data line with respect to the LHC clock received on the CTP. One can also adjust phase of the incoming signals in steps of 0.5 ns.

The pre-defined pattern test was run for approximately two hours using the CTP 2 connector and approximately one hour for the CTP 1 connector. During these runs 121 million events were checked for the CTP 2 connector and 48 million events for the CTP 1 connector. Pseudo-random transmission was also checked for approximately half an hour for both output connectors. Neither of these test revealed any errors. It has to be noted that the logic states received by the CTP are reversed from the intended ones, which is easily alleviated by FW adjustment.

The characteristics of the data transmission were studied using the infrastructure available on the CTP. Figures 42 and 43 show parity error count when scanning the delay values for all data lines. The region where data transmission is not reliable is appropriately 5 ns wide.

Tables 3 and 4 show phases of the transitions in the incoming signals. Note that the width of the region where data transmission is not stable in Fig. 42 and 43 can be explained by the relative phase differences of the incoming signals and not by signal jitter.

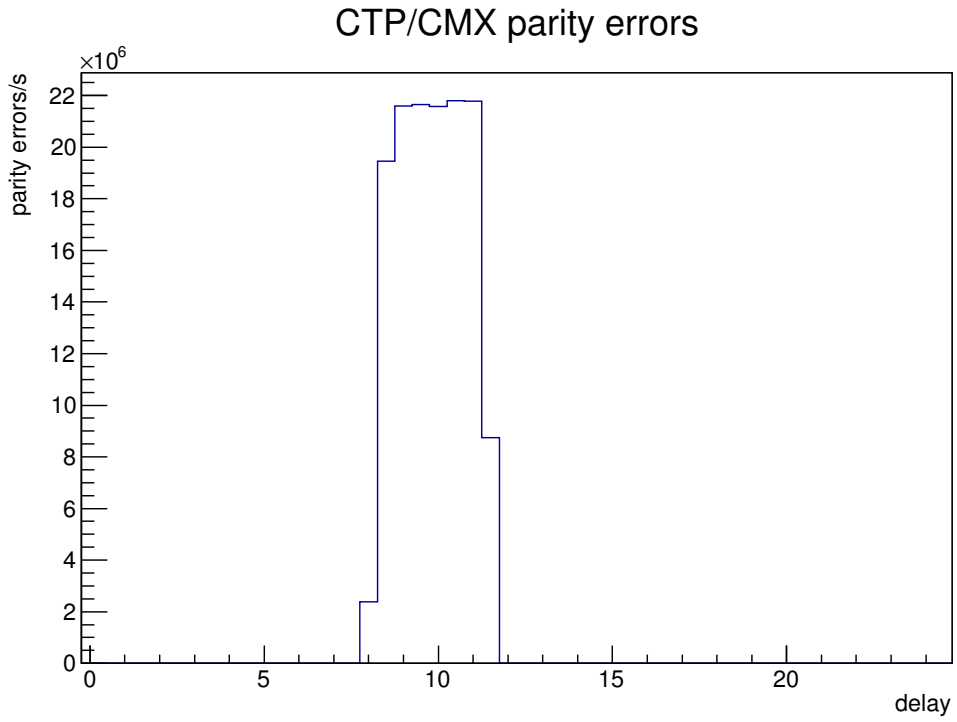


Figure 42: Parity error count versus delay setting for data received from CMX’s CTP 1 connector. Delay unit is ns. Dwell time was set to 0.5s

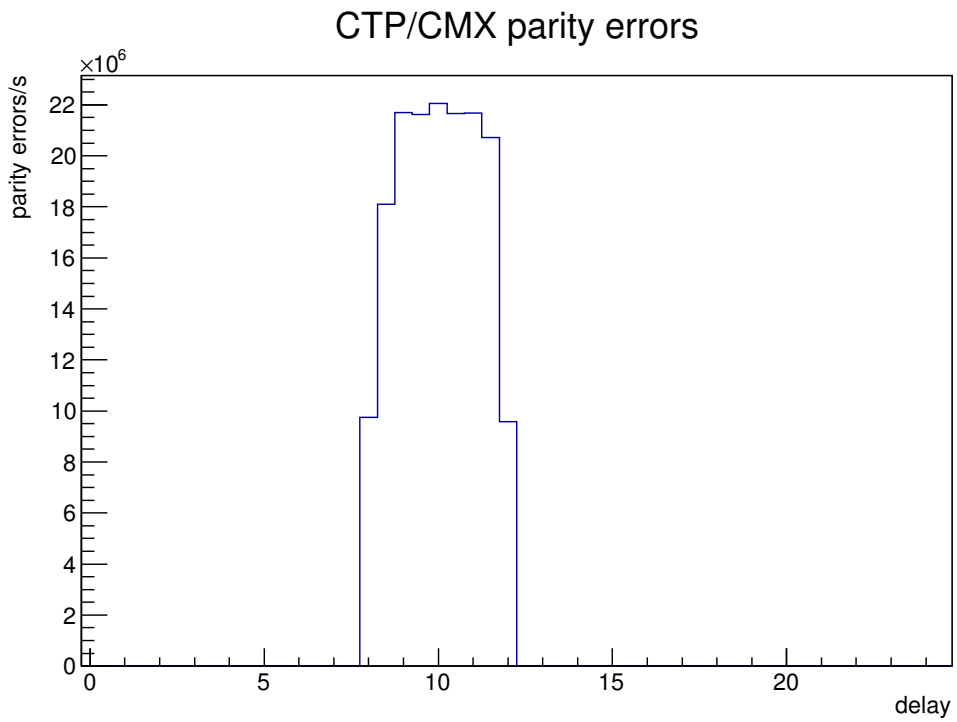


Figure 43: Parity error count versus delay setting for data received from CMX’s CTP 2 connector. Delay unit is ns. Dwell time was set to 0.5 s

signal number	signal name	TDC phase (ns)	TDC phase RMS (ns)
0	SIG00	11.43	0.14
1	SIG01	13.10	0.13
2	SIG02	11.87	0.16
3	SIG03	12.26	0.15
4	SIG04	11.54	0.16
5	SIG05	11.13	0.18
6	SIG06	11.62	0.19
7	SIG07	11.16	0.15
8	SIG08	12.67	0.15
9	SIG09	12.11	0.13
10	SIG10	11.23	0.13
11	SIG11	12.46	0.15
12	SIG12	12.05	0.18
13	SIG13	12.92	0.19
14	SIG14	12.82	0.18
15	SIG15	12.77	0.19
16	SIG16	11.47	0.14
17	SIG17	11.83	0.22
18	SIG18	12.13	0.17
19	SIG19	12.72	0.12
20	SIG20	12.12	0.17
21	SIG21	10.90	0.17
22	SIG22	12.67	0.12
23	SIG23	11.87	0.14
24	SIG24	11.14	0.17
25	SIG25	12.09	0.13
26	SIG26	11.03	0.16
27	SIG27	10.55	0.15
28	SIG28	10.54	0.17
29	SIG29	10.61	0.19
30	SIG30	13.43	0.26
31	CLK	3.13	0.05
32	PAR	13.63	0.11

Table 3: Phase of transition and its RMS for each signal received from CMX's CTP 1 connector

signal number	signal name	TDC phase (ns)	TDC phase RMS (ns)
0	SIG00	12.74	0.15
1	SIG01	12.40	0.20
2	SIG02	13.15	0.17
3	SIG03	12.27	0.17
4	SIG04	12.79	0.15
5	SIG05	12.75	0.16
6	SIG06	13.00	0.17
7	SIG07	11.22	0.12
8	SIG08	12.34	0.16
9	SIG09	11.42	0.15
10	SIG10	12.12	0.16
11	SIG11	12.01	0.18
12	SIG12	13.39	0.16
13	SIG13	12.36	0.17
14	SIG14	11.68	0.18
15	SIG15	12.44	0.16
16	SIG16	11.76	0.14
17	SIG17	12.49	0.18
18	SIG18	12.99	0.15
19	SIG19	12.21	0.17
20	SIG20	11.80	0.14
21	SIG21	10.72	0.14
22	SIG22	11.91	0.17
23	SIG23	12.86	0.11
24	SIG24	12.36	0.10
25	SIG25	11.80	0.12
26	SIG26	10.85	0.13
27	SIG27	9.89	0.14
28	SIG28	10.82	0.17
29	SIG29	10.99	0.16
30	SIG30	13.57	0.20
31	CLK	3.21	0.10
32	PAR	14.12	0.13

Table 4: Phase of transition and its RMS for each signal received from CMX's CTP 2 connector

4.3 Conclusion

LDVS IO tests performed in standalone simultaneous loopback tests between the CTP connectors and the RTM connectors showed no errors with stress pattern test for at least one hour. Tests of both CTP connectors to a CTP in USA15 at 40 MHz with stress patterns for 1 – 2 h and with pseudo-random data for 30 mins have not revealed any data or parity errors, respectively. Scanning the delay settings on the CTP revealed an error free region of 5 ns.

5 High speed optical link tests

5.1 Loopback tests

For the tests of the high speed links we used the CMX SN01 – the board with two FPGAs. Two transmitter Minipods (MP) 1 and 2 are connected to the Base function and three receiver MPs 3, 4, 5 are connected to the Topo function FPGA. In what follows we describe results of the tests where all of the high speed paths have been tested in stand-alone tests in loopback configuration and tests where the L1Topo prototype was used as the receiver. In all of the tests thus far Xilinx IBERT cores were utilized.

An IBERT core is a programmable FW configuration designed to test FPGAs serial interfaces. Using this core each MGT TX(RX) can be configure to transmit (receive) one of the standardized pseudo-random bit sequences. MGT parameters and can be tuned and data transmission fidelity can be monitored using Chipscope environment that communicates with the IBERT core on the FPGA via JTAG interface. CMX's FPGA allow for maximally twelve GTXs to be included in the IBERT core.

In all the the tests described here PRBS-7 bit pattern was used. The GTX TXs were configured to provide 590 mV swing with no pre-cursor and post-cursor emphasis. The GTX RXs in the loopback tests were configured with default recommended internal termination and AC-coupling schemes. The linear filter was set to value of 0 and the digital feedback equalizer was not used. The Minipod configurations were not adjusted from their power-up configuration.

Figures 44, 45 and 46 show IBERT GUI screen captures for loopback tests where data was sent from MP2 to MP5, MP1 to MP3 and MP2 to MP4 respectively. In each case in the optical path between the transmitter and the receiver MP there were in order: short fiber bundle pigtail, Avago barrel, 6 ft fiber bundle, Avago barrel and pigtail. The test duration varied between half an hour for the MP2 to MP5 test and six days for MP2 to MP4 test achieving BER measurement down to 3E-16.

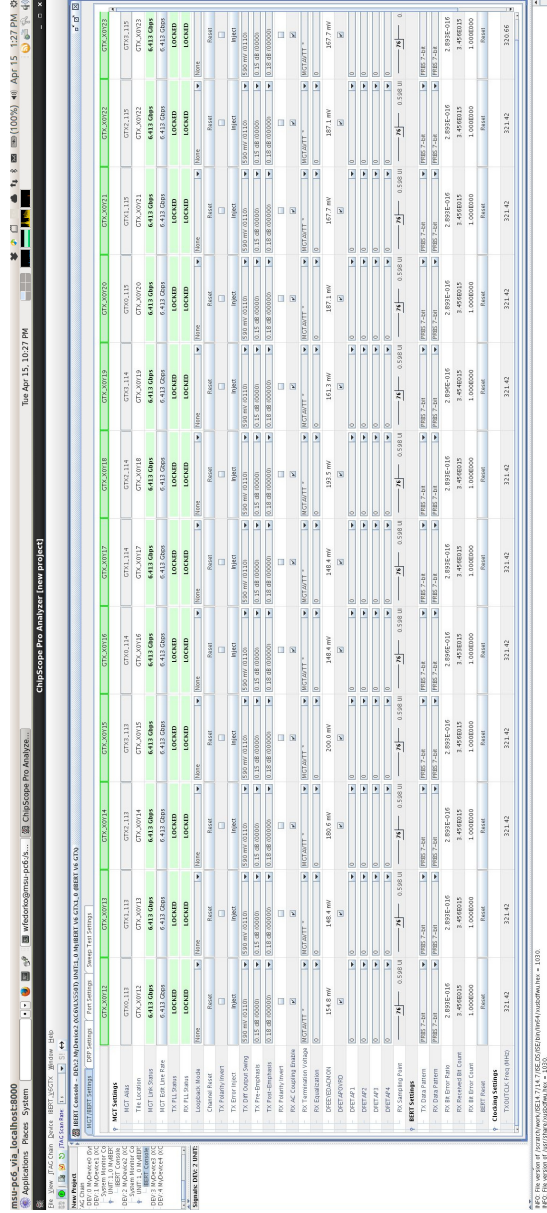


Figure 46: Screen capture of the IBERT interface for the test of MP2 to MP4 data transmission showing receiver set up, number of sent bits and error counts on each channel. Note that the count of 1 error bit is due to purposefully inserted bit error.

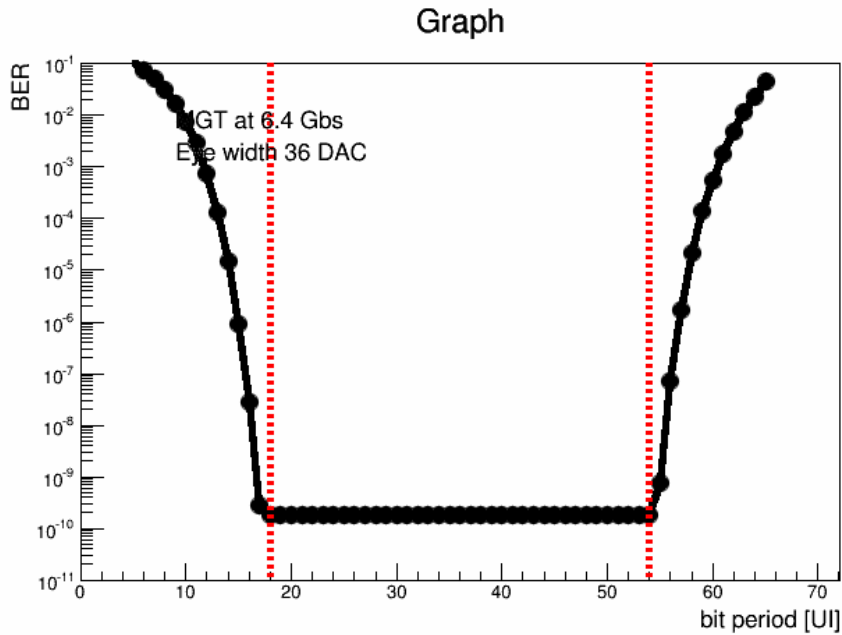


Figure 47: A typical bathtub BER curve for one of the data channels between CMX and L1TOPO processor.

5.2 Tests with L1Topo

Test of data transmission to L1Topo was performed in a similar fashion to the loopback test. IBERT cores were set up on both CMX and one of the L1Topo FPGAs. Both MP1 and MP2 were tested in turn with transmission over 10 m and 2 m fiber bundle respectively (and a pigtail-barrel at either end) for approximately half an hour achieving BER measurement of 3×10^{-14} . For both tests the same MP was used on L1Topo. No errors were observed during these tests. A bathtub curve was measured for all the channels and in all cases it was found to be more than 50% open. A typical bathtub obtained in this test is shown in Fig. 47.

An additional test of data transmission was performed using a realistic optical path between the CMX and L1Topo. In that test the following optical components were used between CMX's transmitter MP and L1Topo receiver MP in order: pigtail, Avago barrel, 1.5 m fiber bundle with breakout, LC barrel, passive splitter, rebundler, LC barrel, 10 M fibre bundle, Avago barrel, pigtail. Only four fibers out of the breakout entered the passive splitter and so data integrity was tested for eight outgoing data streams. The test was run for approximately half an hour without any bit errors observed achieving BER measurement of 1×10^{-14} . The bathtub curve were measured for each of the eight channels, a typical one is shown in Fig. 48.

The tests described here show that high fidelity data transmission over the optical lines can be achieved between the CMX and L1Topo processor. Additional tests are planned utilizing a realistic data format.

5.3 Conclusion

The high speed optical links have been tested in loopback tests between the transmitter Minipods that are connected to the Base Function and Topo Function FPGA. In all tests a Xilinx IBERT core was used to determine the BER of 3×10^{-16} in test up to a duration of six days. In tests with the L1Topo realistic

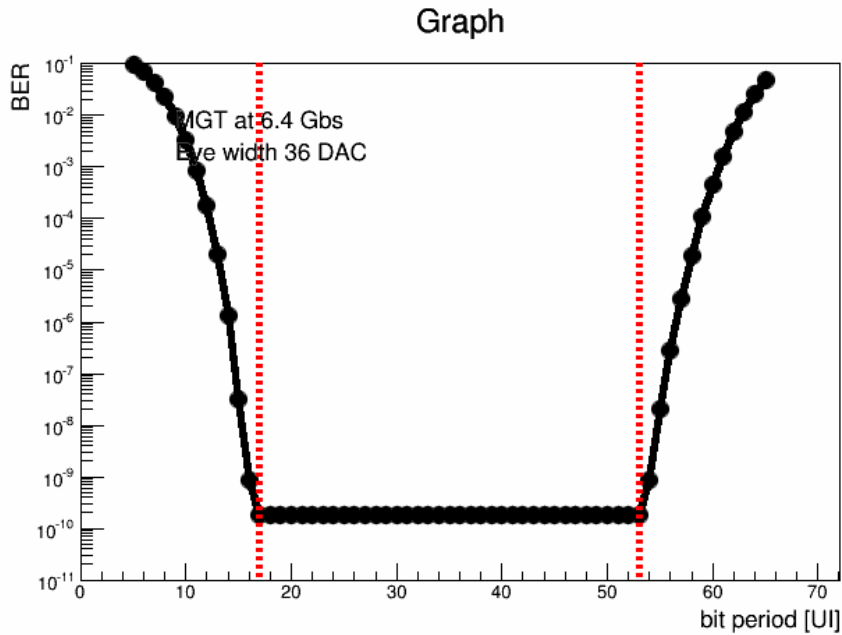


Figure 48: A typical bathtub BER curve for one of the data channels between CMX and L1Topo processor when a realistic optical path with a splitter is used

fiber lengths and connections with e.g. passive splitters and barrel connectors were used. Bathtub curves with an opening of more than 50% and BER between $1 - 3 \times 10^{-14}$ were observed.

6 Low speed optical link and G-Link protocol tests

6.1 Background information

The Low Speed Optical components are being used on the CMX card to transmit the DAQ and ROI information from the Base Function (BF) and Topological Processor (TP) FPGAs to the ROD card. On the CMX card these components are labeled SFP1 through SFP4. The actual SFP fiber optic module which is used on the CMX card is the Avago AFBR-57M5APZ optical transceiver. It was decided to use the Avago component on the CMX card because the Infineon part used on the CMM card is no longer available in the market. In addition, the CMX card does not use the HP G-Link chip to encode its ROI and DAQ information. The required functionality of the HP G-Link chip is implemented by a combination of Virtex FPGA resources and a GTX transmitter running at 960 Mbits/s. The reference clock to the GTX transmitters is a dedicated 120 MHz crystal for the G-Link operation. In the tests described only a 100 MHz clock is used, only in later test the target clock will be used. The CMX G-Link reference frequency is intentionally not following the 40.08 MHz clock.

6.2 Test procedures

The tests of the LSO components were divided into several steps. Initial hardware steps were conducted with an Integrated Bit Error Ratio Tester (IBERT) core and Chipscope Pro Analyzer. This tool was customized and used to evaluate and monitor the functionality of transceivers. Each transceiver in the IBERT design is equipped with a pattern generator (PRBS 7-bit) and a pattern checker. The pattern generator transmits data out through the transmitter, while the pattern checker takes the incoming data

in though the receiver and checks it with internally generated data. Also, the design has an access to the dynamic reconfiguration port (DRP) attributes of transceivers and is accessible in real time through the JTAG chain. It can also perform a test to optimize the transceivers channels and plot the data as shown in Figures 49 and 50. In the current setup two transmitters connected to the TF FPGAs send out the data to the two receivers on the BF FPGA while two transmitters connected to the Base send out data to the other two RX's on the BF FPGA. For this tests the line rate was set to 1 Gbps, and the TX and RX PLL status is locked. The RX bit error ratio was found to be less than 1.5×10^{-13}

BERT Config - DR11_MDR1042_OCNAL550D_INTEL_0_MBERT_V6_C1V1_0_0BERT_V6_G10											
MGT/BERT Settings Post Settings Sweep Test Settings											
MGT Link Status	GTX_X00728	GTX_X00729	GTX_X00730	GTX_X00731	GTX_X00732	GTX_X00733	GTX_X00734	GTX_X00735			
MGT Error Line Pair	1.0 Chps	1.0 Chps	1.0 Chps	1.0 Chps	No Link	No Link	No Link	No Link	No Link	No Link	No Link
TX Full Status	LOCKED	LOCKED	LOCKED	LOCKED	LOCKED	LOCKED	LOCKED	LOCKED	LOCKED	LOCKED	LOCKED
RX Full Status	LOCKED	LOCKED	LOCKED	LOCKED	LOCKED	LOCKED	LOCKED	LOCKED	LOCKED	LOCKED	LOCKED
Loopback Mode	None	None	None	None	None	None	None	None	None	None	None
Channel Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset
TX Polarity Invert	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
TX Error Invert	Invert	Invert	Invert	Invert	Invert	Invert	Invert	Invert	Invert	Invert	Invert
TX DMT Output Swing	590 mV / 0.110	590 mV / 0.110	590 mV / 0.110	590 mV / 0.110	590 mV / 0.110	590 mV / 0.110	590 mV / 0.110	590 mV / 0.110	590 mV / 0.110	590 mV / 0.110	590 mV / 0.110
TX Pre-Emphasis	0.15 dB / 000000	0.15 dB / 000000	0.15 dB / 000000	0.15 dB / 000000	0.15 dB / 000000	0.15 dB / 000000	0.15 dB / 000000	0.15 dB / 000000	0.15 dB / 000000	0.15 dB / 000000	0.15 dB / 000000
TX Post-Emphasis	0.18 dB / 000000	0.18 dB / 000000	0.18 dB / 000000	0.18 dB / 000000	0.18 dB / 000000	0.18 dB / 000000	0.18 dB / 000000	0.18 dB / 000000	0.18 dB / 000000	0.18 dB / 000000	0.18 dB / 000000
RX Polarity Invert	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
RX AC Coupling Enable	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
RX Termination Voltage	HIGHZ/PTT *	HIGHZ/PTT *	HIGHZ/PTT *	HIGHZ/PTT *	HIGHZ/PTT *	HIGHZ/PTT *	HIGHZ/PTT *	HIGHZ/PTT *	HIGHZ/PTT *	HIGHZ/PTT *	HIGHZ/PTT *
RX Equalization	0	0	0	0	0	0	0	0	0	0	0
DFE/DFE/DACHON	200.0 mV	200.0 mV	200.0 mV	200.0 mV	19.3 mV	32.3 mV	12.9 mV	45.2 mV			
DFE/AF/DFD	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
DFE/AF1	0	0	0	0	0	0	0	0	0	0	0
DFE/AF2	0	0	0	0	0	0	0	0	0	0	0
DFE/AF3	0	0	0	0	0	0	0	0	0	0	0
DFE/AF4	0	0	0	0	0	0	0	0	0	0	0
RX Sampling Pair	76	76	76	76	76	76	76	76	76	76	76
RX Sampling Rate	0.598 U	0.598 U	0.598 U	0.598 U	0.598 U	0.598 U	0.598 U	0.598 U	0.598 U	0.598 U	0.598 U
TX Data Pattern	PRES7-SR	PRES7-SR	PRES7-SR	PRES7-SR	PRES7-SR	PRES7-SR	PRES7-SR	PRES7-SR	PRES7-SR	PRES7-SR	PRES7-SR
BERT Settings											
TX Data Pattern											

Figure 49: Screenshot of the low Speed Optical components test showing TX and RX PLL status.

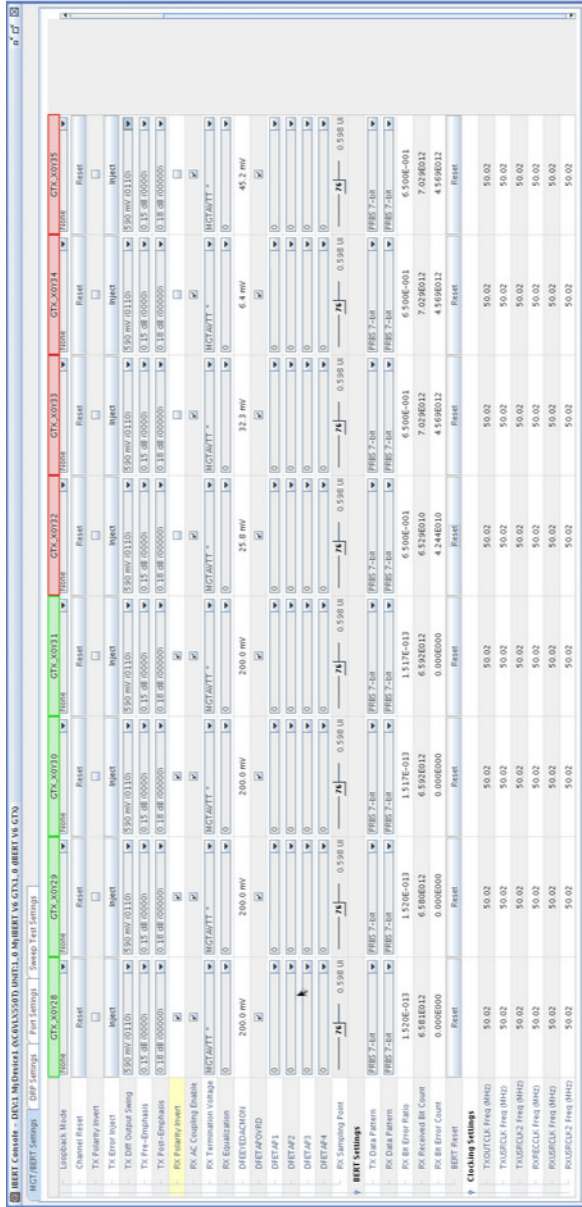


Figure 50: Screenshot of the low Speed Optical components test showing the BER information.

The second step only concerns the G-Link emulation with the Virtex-6 ML605 evaluation board and is mentioned only briefly here [3]. The conclusion was that the G-Link protocol is successfully implemented and tested. The scope tests of the optical output (an eye diagram) executed with the evaluation card proved that there is no problem to emulate the G-Link protocol in FPGA. The rise and fall time was measured to be below 240 ps which is good enough to fulfill the G-Link protocol requirements.

The final step concerns the G-Link communication tests. In order to conduct this test a hardware setup was used which consists of the CMX and ROD card. Two Low Speed Optical components were used to transmit the DAQ and ROI information to the ROD. Also, the CMX G-Link protocol, which encodes 20 bits of user data, was emulated in FPGA. The ROD G-Link receiver recovers the user data from the serial data stream and it also checks the framing bits to verify the link stability.

The main idea for the G-Link protocol tests is the following: on receipt of an L1A signal, the CMX G-Link firmware is obliged to extract data from its diagnostic component. The test data is connected via a shift register to one of G-Link emulated user data pins. The internal logic moves the diagnostic data into the shift registers and asserts the Data Available (DAQ) signal to the G-Link logic. Then, the Low Speed Optical components are being used to transmit the encoded data from G-Link to the RODs [4]. An odd parity bit is appended to each active G-Link line when the shift register contents have been transmitted. The logic de-asserts the DAV signal and the emulated G-Link returns to its quiescent state for at least one clock cycle. During the time period where there is no L1A signal, the CMX G-Link protocol transmits so-called fill frames to maintain the lock between the transmitter and receiver. In the current tests only the fill frames were transferred to the ROD and the lock between the transmitter and receiver was established.

6.3 Conclusion

The CMX Low Speed Optical components tests were performed with an Integrated Bit Error Ratio Tester (IBERT) core with Chipscope Pro Analyzer. The result is encouraging and indicates that the CMX Low Speed Optical components have capability to be used to transmit the DAQ and ROI information from the BF and TP FPGAs to the ROD card. Also, the G-Link emulated protocol was implemented and successfully tested in FPGA. The CMX G-Link communication tests with the ROD are in progress, but the first results are promising and indicate that the lock between the transmitters and receivers can be established. The G-Link protocol tests will be continued.

7 Summary

The results from the interface tests on the CMX prototypes for the CMX production readiness review were presented in this document. Tests were performed on the CMX services and the real-time and read-out paths which include the backplane interface, LVDS IO, and low speed and high speed optical links. Tests with dedicated stress data patterns and pseudo-random data as well as long term tests demonstrate the reliability of the data interfaces and that they meet the requirement on the error rate in the L1 trigger system.

The correct operation of the VME interface to the FPGAs has been shown in dedicated test and throughout all interface tests the operation was found to be reliable. Other services such as reading back the geographical address, configuration of the firmware from the compact flash slot and the I²C interfaces to the XILINX System ACE controller, TTCrx chip on the TTCDec card, and SFP and MiniPOD optical components are also working.

The full crate backplane interface tests with two prototype CMX's in a full JEM or CPM crate showed that the capability of the firmware to adjust the delay settings of the incoming data and clock lines was good enough to adjust the timing settings over a large range. In tests with dedicated stress data patterns

and pseudo-random data, the width of the data validity window was found to be at least 2.3 ns – 3.1 ns. The width of the window is sufficient to have a stable operation with a comfortable margin. In long term tests over a few hours at a stable operation point it was shown that no error occurred and the upper limit on the event error rate was determined to be 0.03 – 0.09 Hz, surpassing the requirement on the error rate in the L1 trigger system by far. No power or heat issues have occurred throughout the tests in the full crates for the duration of the tests.

LDVS IO tests performed in standalone simultaneous loopback tests between the CTP connectors and the RTM connectors showed no errors with stress patterns test for at least one hour. Tests of both CTP connectors to a CTP in USA15 at 40 MHz with stress patterns for 1 – 2 h and with pseudo-random data for 30 mins have not revealed any data or parity errors, respectively. Scanning the delay settings on the CTP revealed an error free region of 20 ns.

The high speed optical links have also been tested in loopback tests between the transmitter Minipods that are connected to the Base Function and Topo Function FPGA. In all tests a Xilinx IBERT core was used to determine the BER of 3×10^{-16} in test up to a duration of six days. In tests with the L1Topo realistic fiber lengths and connections were used. Bathtub curves with an opening of more than 50% and BER between $1 - 3 \times 10^{-14}$ were observed.

The low speed optical links tests were performed with IBERT cores and the Chipscope Pro Analyzer. In loopback tests with SFPs connected the Base Function and Top Function FPGA, and the SFPs connected only to the Base Function a BER of less than 1.5×10^{-13} was observed. The G-Link communication was first successfully implemented and tested in an emulation and then tested in data transfers between the CMX and a ROD card using fill frames of the G-Link protocol to verify a lock between the transmitter and the receiver.

Tests on the CAN bus interface for the DCS monitoring were not performed, yet, but should not have substantial impact on the production readiness.

The successful completion of the data interface tests either in loopback tests or in tests with the appropriate hardware components on the receiver side have shown that the data interfaces are capable of reliable data transmission that fulfill the requirements of the L1 trigger system. The layout and design of the CMX prototype boards is sufficient and the test results indicate that no design changes are necessary for the fabrication and assembly of the full production CMX boards.

References

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- [2] http://www.pa.msu.edu/hep/atlas/l1calo/cmz/firmware/fpga_bspt_fw/TTCrx_control_draft.txt.
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