CMX – prototype testing

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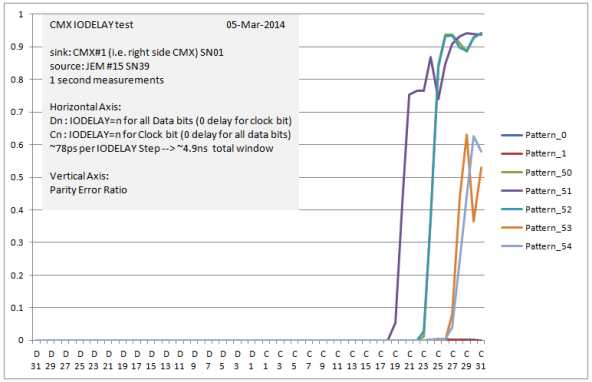
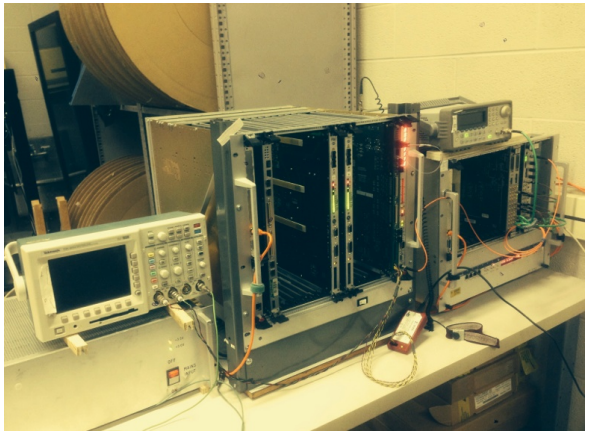
Outline of CMX tests

- 4 Prototypes produced:
  - 1 without Virtex 6 parts: SN0 (@CERN)
  - 2 with both Virtex 6 parts on: SN1 (@CERN), SN2 (@MSU)
  - 1 with only 'Base Function' (standard configuration): SN3 (@CERN, USA 15)
- Prototypes arrived mid-Feb
- RT and readout path testing commenced after final assembly and checkout.
  - MSU 2nd half of Feb
  - CERN b. 104 most of March
  - CERN USA 15 last week of March-mid April.
  - Back to CERN b.104 till now. One CMX left installed at USA15

Accomplished during MSU testing:

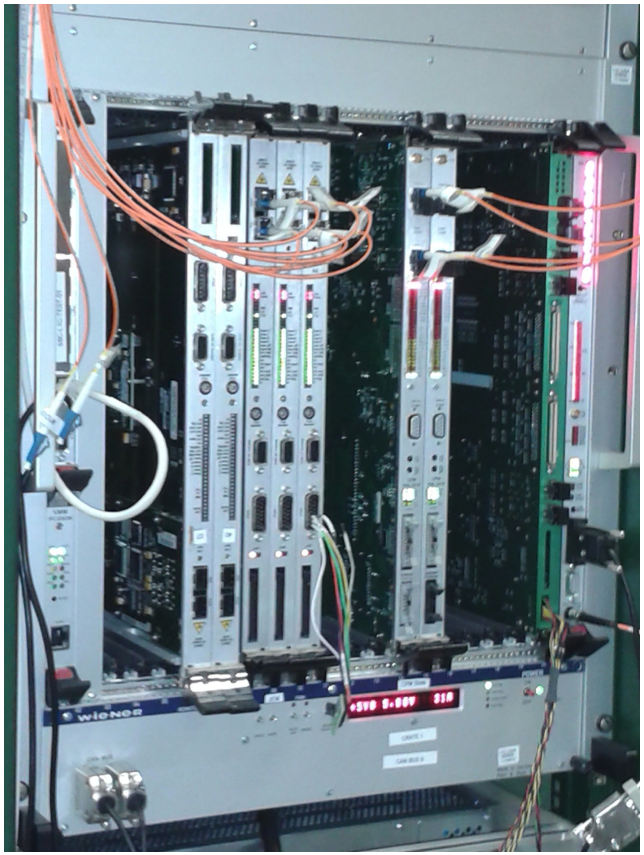
- All RT/readout interfaces tested to some level, some tests superseded/extended:
  - Backplane tests:
    - 2 JEMs
    - Static patterns
    - Pre-defined patterns
    - First IO-delay scans
    - Superseded by full crate tests at USA 15 → Duc's talk
  - 'Slow' optical link tests using IBERT → Pawel's talk
  - 'Fast' optical link tests using IBERT → later in this talk
  - LVDS link tests → later in this talk





March: preparation for full crate tests

- B 104 test rig.
- Debugging FW with on-the fly data checking
- Testing/debugging JEM FW (mostly SumET)
  - Extension of functionality: PRBS
- Testing the CPM FW
- Final preparation and debugging of the software tools



RT Data path tests: LVDS, MSU

- Pre-defined 80 Mbps DDR source-synchroneous stress patterns sent
  - Coherent pulses '1' and '0', switching data.
  - RTM 1,2 → 3
  - CTP1 (driven by BF) → CTP2
    - received on both BF and TP FPGA's
- 2.5m cable RTM
- 9.5m cable CTP
- IO pins configured for 6 mA drive strength
- Parity monitored using chipscope ~1hr no errors (~10 min RTM 1 → 3)

RT Data path tests: LVDS CMX → CTP, USA 15

- CMX configured to provide on both CTP output connectors selectable data at 40 Mbps:
  - Stress pattern, 1 orbit long:
    - Walking 1's, walking 0's
    - Coherent pulses '1', and '0'
    - Pulses on selected bits,
    - Switching data (F's and 0's, A's and 5's)
  - Pseudorandom data
    - Array of LFSRs
    - Odd parity preserved

RT Data path tests: LVDS CMX → CTP, USA 15

- CTP:
  - Can compare incoming data bit-by-bit against a known sequence (at low frequency)
  - Flag parity errors
  - Adjust timing of incoming signals
- No errors observed in stress pattern running in:
  - 121M events in data from CTP 2
  - 48M events from CTP1
- No parity errors in half hour of pseudo-random data runs

LVDS CMX → CTP Link characterisation:

transition timing

CTP 1 connector

signal number	signal name	TDC phase (ns)	TDC phase RMS (ns)
0	SIG00	11.43	0.14
1	SIG01	13.10	0.13
2	SIG02	11.87	0.16
3	SIG03	12.26	0.15
4	SIG04	11.54	0.16
5	SIG05	11.13	0.18
6	SIG06	11.62	0.19
7	SIG07	11.16	0.15
8	SIG08	12.67	0.15
9	SIG09	12.11	0.13
10	SIG10	11.23	0.13
11	SIG11	12.46	0.15
12	SIG12	12.05	0.18
13	SIG13	12.92	0.19
14	SIG14	12.82	0.18
15	SIG15	12.77	0.19
16	SIG16	11.47	0.14
17	SIG17	11.83	0.22
18	SIG18	12.13	0.17
19	SIG19	12.72	0.12
20	SIG20	12.12	0.17
21	SIG21	10.90	0.17
22	SIG22	12.67	0.12
23	SIG23	11.87	0.14
24	SIG24	11.14	0.17
25	SIG25	12.09	0.13
26	SIG26	11.03	0.16
27	SIG27	10.55	0.15
28	SIG28	10.54	0.17
29	SIG29	10.61	0.19
30	SIG30	13.43	0.26
31	CLK	3.13	0.05
32	PAR	13.63	0.11

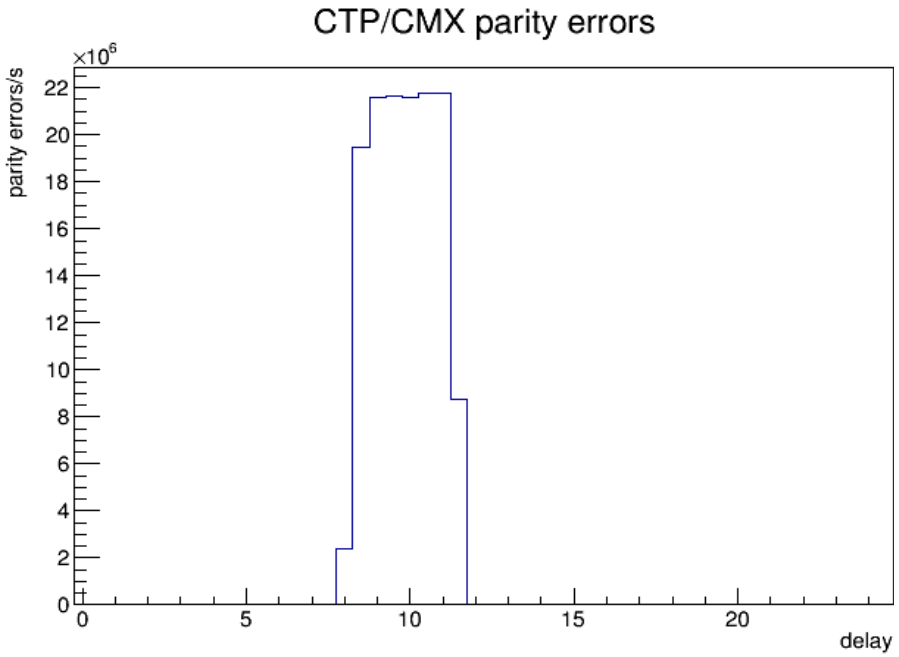
CTP 2 connector

signal number	signal name	TDC phase (ns)	TDC phase RMS (ns)
0	SIG00	12.74	0.15
1	SIG01	12.40	0.20
2	SIG02	13.15	0.17
3	SIG03	12.27	0.17
4	SIG04	12.79	0.15
5	SIG05	12.75	0.16
6	SIG06	13.00	0.17
7	SIG07	11.22	0.12
8	SIG08	12.34	0.16
9	SIG09	11.42	0.15
10	SIG10	12.12	0.16
11	SIG11	12.01	0.18
12	SIG12	13.39	0.16
13	SIG13	12.36	0.17
14	SIG14	11.68	0.18
15	SIG15	12.44	0.16
16	SIG16	11.76	0.14
17	SIG17	12.49	0.18
18	SIG18	12.99	0.15
19	SIG19	12.21	0.17
20	SIG20	11.80	0.14
21	SIG21	10.72	0.14
22	SIG22	11.91	0.17
23	SIG23	12.86	0.11
24	SIG24	12.36	0.10
25	SIG25	11.80	0.12
26	SIG26	10.85	0.13
27	SIG27	9.89	0.14
28	SIG28	10.82	0.17
29	SIG29	10.99	0.16
30	SIG30	13.57	0.20
31	CLK	3.21	0.10
32	PAR	14.12	0.13

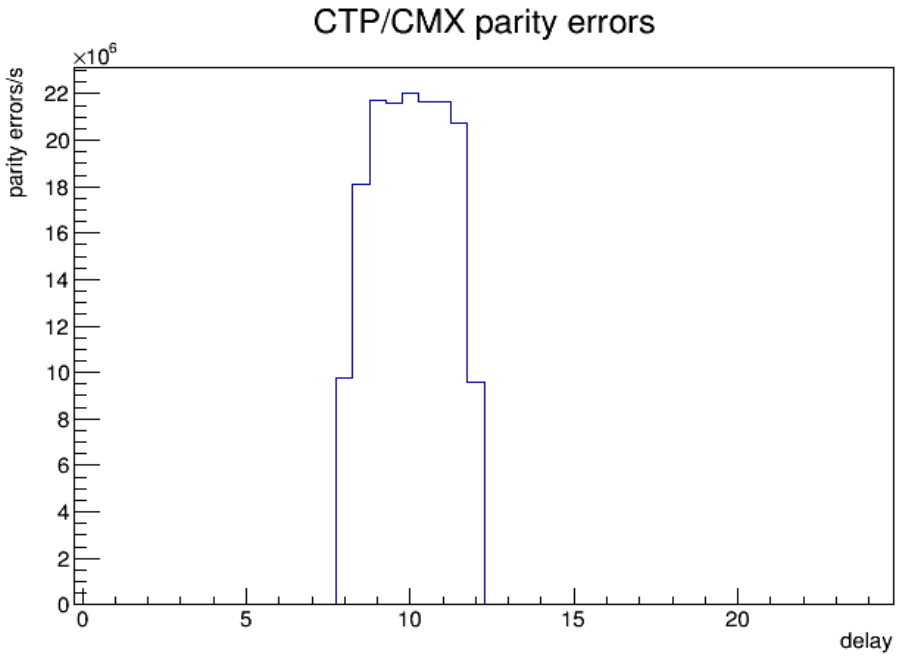
LVDS CMX → CTP Link characterisation:

'bathtub'

CTP 1 connector

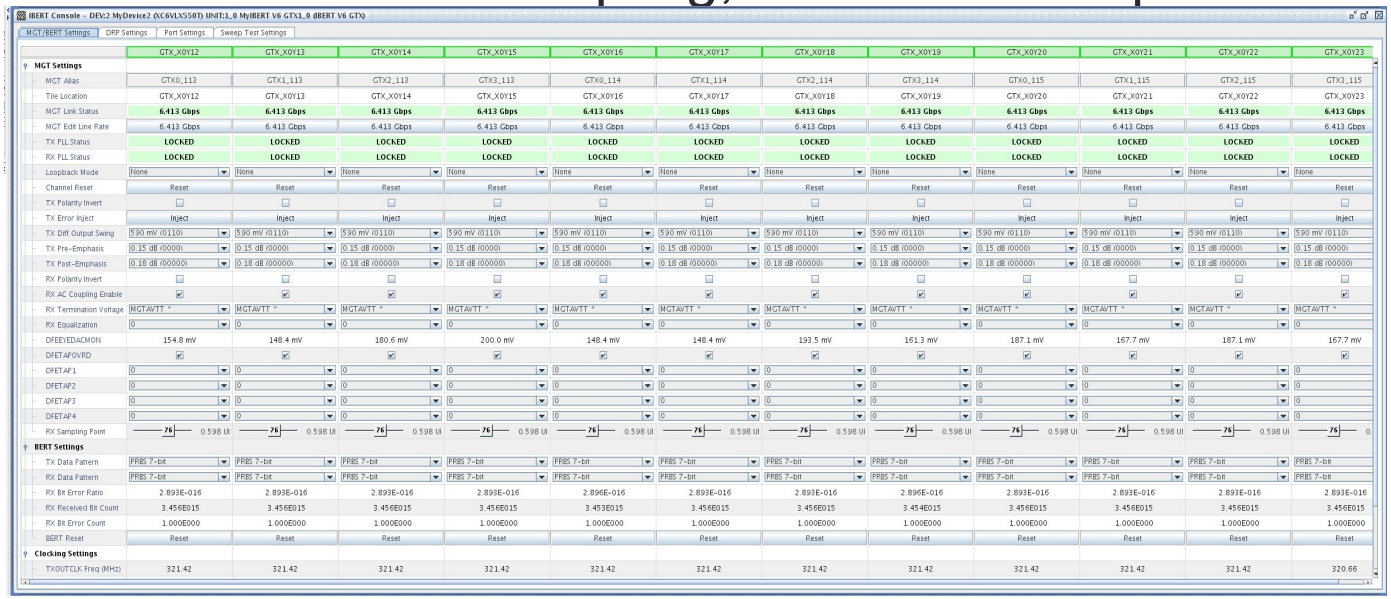


CTP 2 connector



RT Data path tests: High Speed Links MSU, CERN, loopback configuration

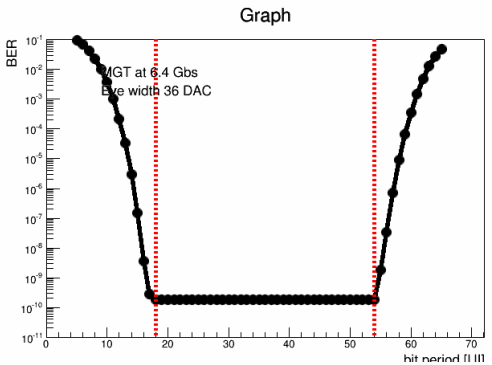
- 'IBERT' cores
  - Test a single Minipod (12 channels) pair at a time
  - Tests up to several days (shortest MP2 → MP5 30 min)
    - BER 3E-16 reached
  - Two pigtails and 6 ft fibre bundle optical path
  - Standard termination coupling, default TX/RX parameters

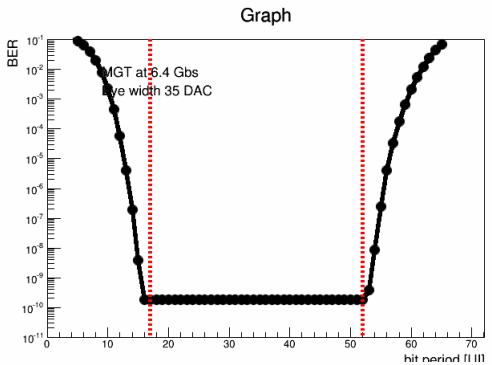


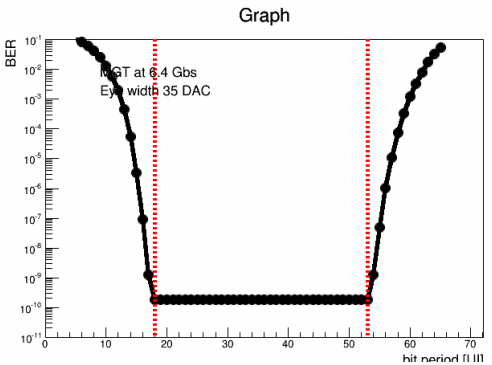
RT Data path tests: High Speed Links CERN, CMX → L1Topo

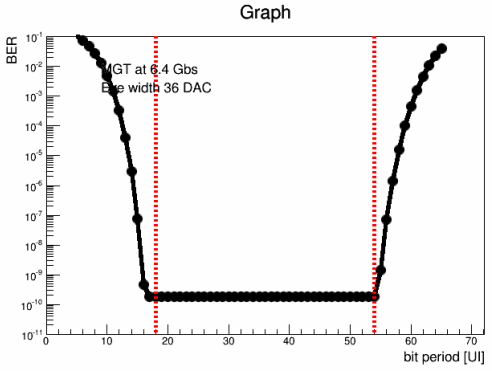
- 'IBERT' cores again
- First tests with simple optical path from both CMX's MPs
  - ~30 minutes BER 3E-14
- Transmission from one MP tested via optical path:
  - Pigtail → barrel → breakout → barrel → **splitter** → rebundler → barrel → 10m bundle → barrel → pigtail
  - No errors; BER measured to 1E-14
  - Bathtub > 50% open
- Tests pending:
  - Realistic formatted data

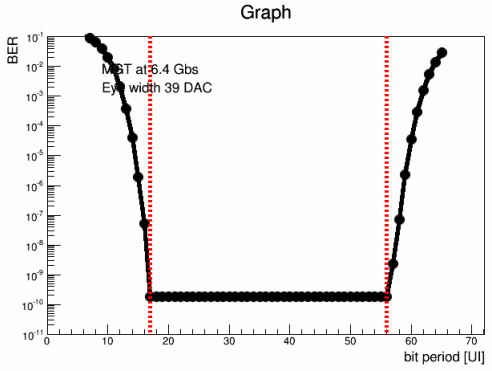
RT Data path tests: High Speed Links CMX → L1Topo, bathtubs w/splitter

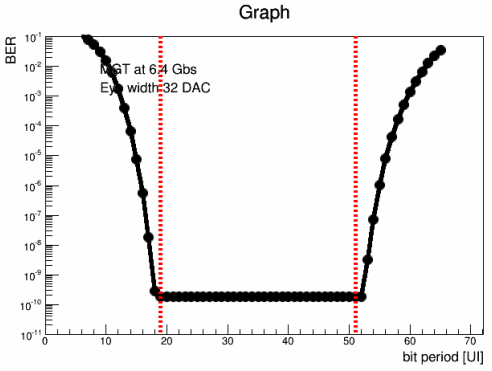


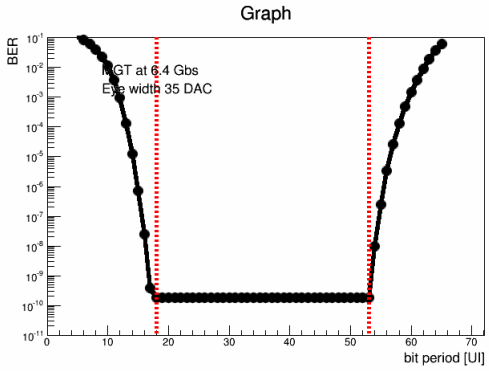


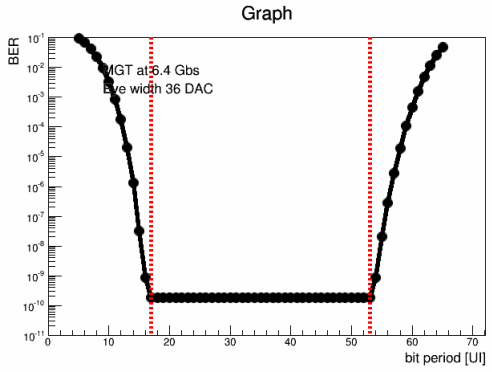












So far so good:

- All tests so far satisfactory!
- Up next:
  - Duc: Backplane test
  - Pawel 'Slow' optical interfaces