CMX backplane tests

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CMX used for backplane test

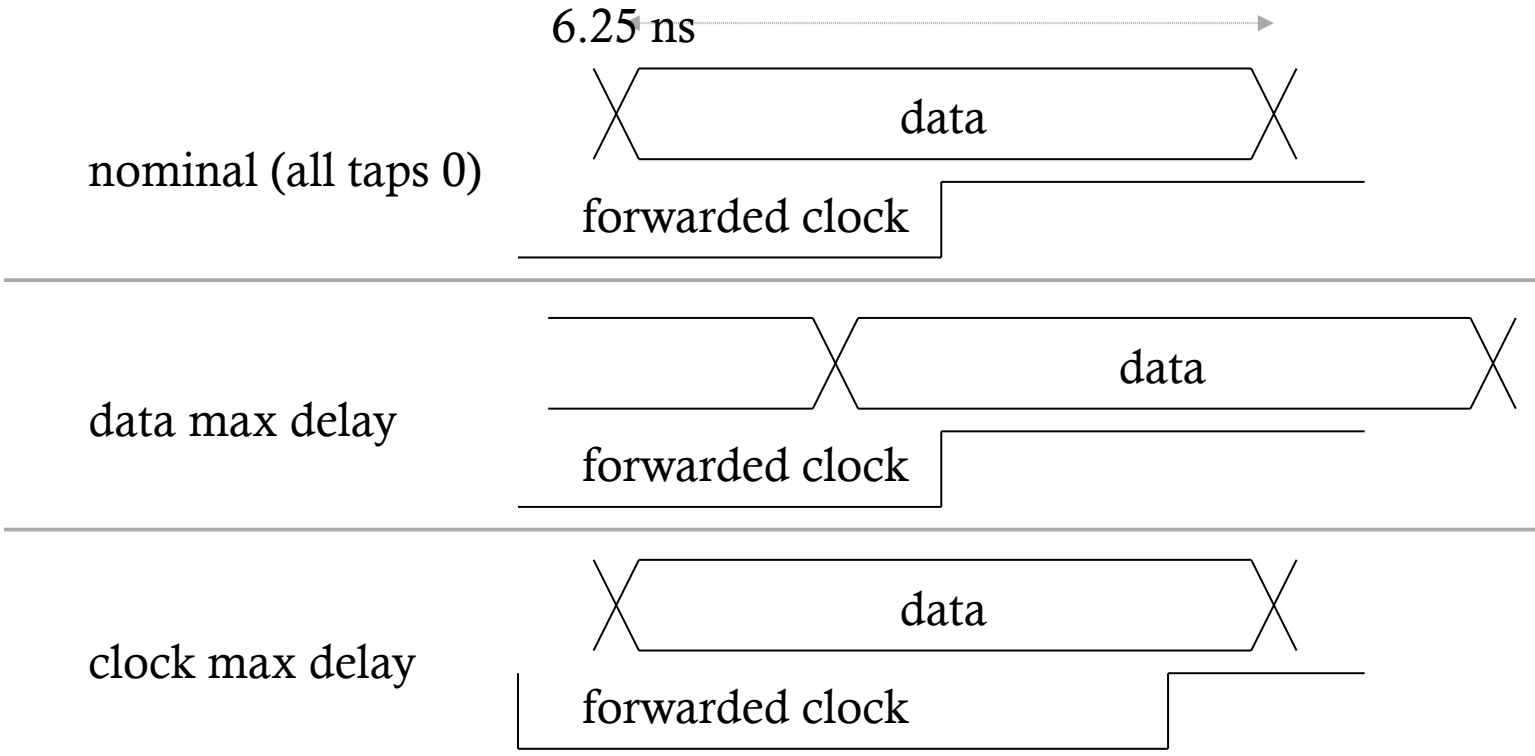
- **Two CMX boards at CERN**
  - SN01: Base and Topo FPGA
  - SN03: Base FPGA only
- **Both operated in B104 test crate with three JEMs and two CPMs**
  - Firmware and software developed and available for backplane tests
    - Debugging code, development of test procedures
- **Both CMX were tested in USA15, JEP0 crate with 16 JEMs, CP0 crate with 14 CPMs**
  - Test for powering problems, heat etc.
  - Test backplane data transmission fidelity at 160 Mbps/signal
- **Both boards are still at CERN for further tests and developments**

Test procedures

- **Test backplane data transmission fidelity at 160 Mbps/signal**
  - Data integrity: no shorts, no opens
  - Data stability: Good timing window (bathtub curve) wide enough to guarantee stable operation, flexibility to cope with different/problematic timing configurations
  - Long term data stability: long term test, determination of bit error ratio and event error ratio/rate
- **Tests using data patterns and pseudo-random data, either timing scan over data/clock delays or fix timing for long term tests**
  - Patterns designed to stress data lines, do not correspond to physics data

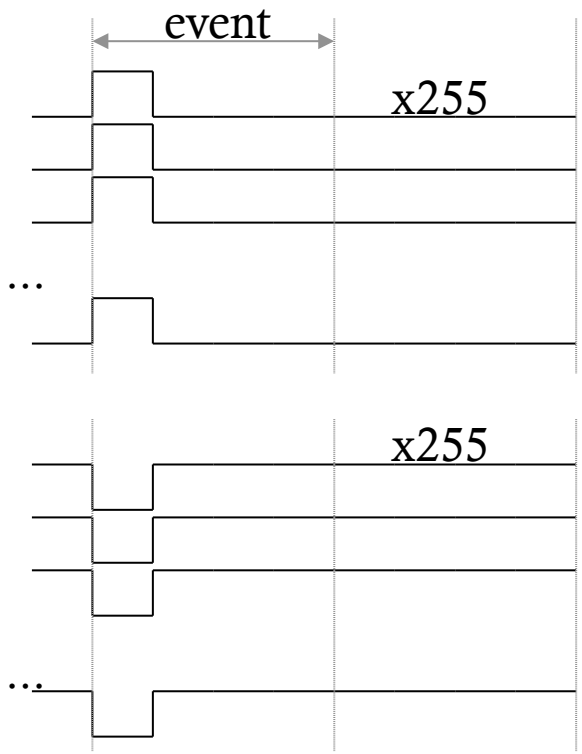
Timing shift setup

- **CMX has independent 16 x (24 [data lines] + 1 [source synchronous clock]) delay circuits in 31 taps à ~78ps, window of 4.8ns in total**
  - sufficient range, but not enough to scan the full range



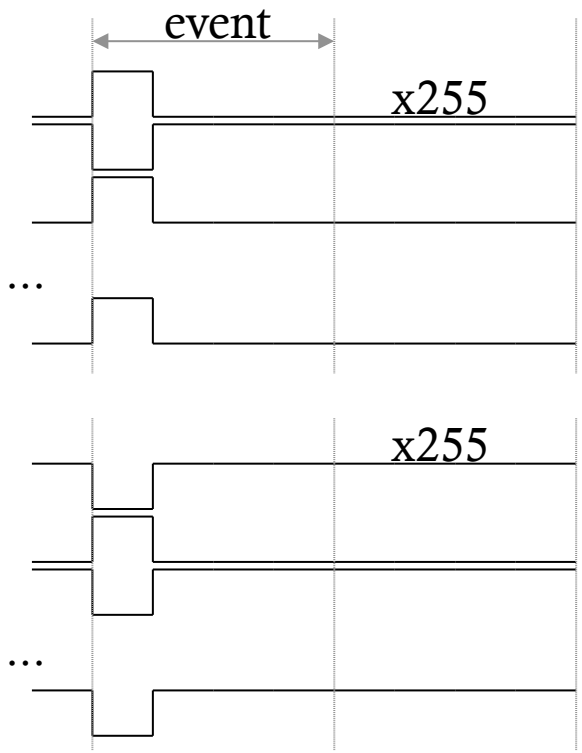
Stress patterns

- **Stress patterns with a 256 event cycle**
  - Each event has 4 event words, i.e. 24bit x4=96bits per source channel
  - Firmware configuration of JEMs (both SumET and Jet FPGA) and CPMs updated to send patterns at 160Mbps
  - Patterns do not have defined parity
  - In total 55 patterns to stress inter signal interferences/cross talk
- **Switching all bits in phase (2 patterns)**
  - Pulse all '1' for first event word, then 255 events silence '0'
  - Pulse all '0' for first event word, then 255 events silence '1'



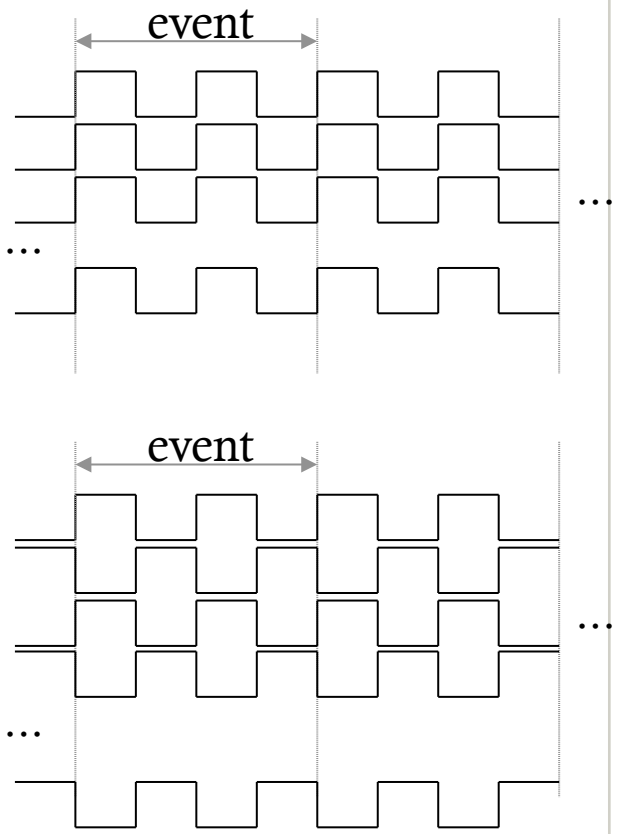
Stress patterns

- **Switching of single bits out of phase (24 + 24 pattern)**
  - Pulse '0' on selected signal bit, then 255 events silence '1' while all other pulse '1' at the same time then silence '0'. (24 patterns)
  - Pulse '1' on selected signal bit, then 255 events silence '0' while all other pulse '0' at the same time then silence '1'. (24 patterns)



Stress patterns

- **Other types of patterns (5 patterns)**
  - Max switching all bits in phase
  - Max switching even bits out of phase with odd bits
  - Special patterns to detect event word position (3 patterns)
- **Pseudo-random data**
  - JEM
    - Array of 47-bit LFSR running in parallel
    - A different firmware configuration is used
  - CPM
    - Single 95-bit LFSR, advance a full word after each event
    - Same firmware configuration for patterns and pseudo-random data
  - Generated with odd parity to check for parity errors



CMX test capabilities

- **CMX firmware compares data inputs with spy memory**
  - Pattern loaded externally into spy memory for each channel (=96 bits x 16 channels x 256 events), corresponding to one of the 55 patterns above
  - **Flags bit errors on each data bit** per input channel, ***used for pattern tests***
- **Counters**
  - **parity errors per channel,** ***used for pseudo-random data tests***
  - number of events until a bit error has been found in one channel
  - number of events
- **Special mode that fills spy memory with input data instead of comparison**
  - Used to check input data, not connected modules will not overwrite spy memories
  - Used to adjust start address with special pattern

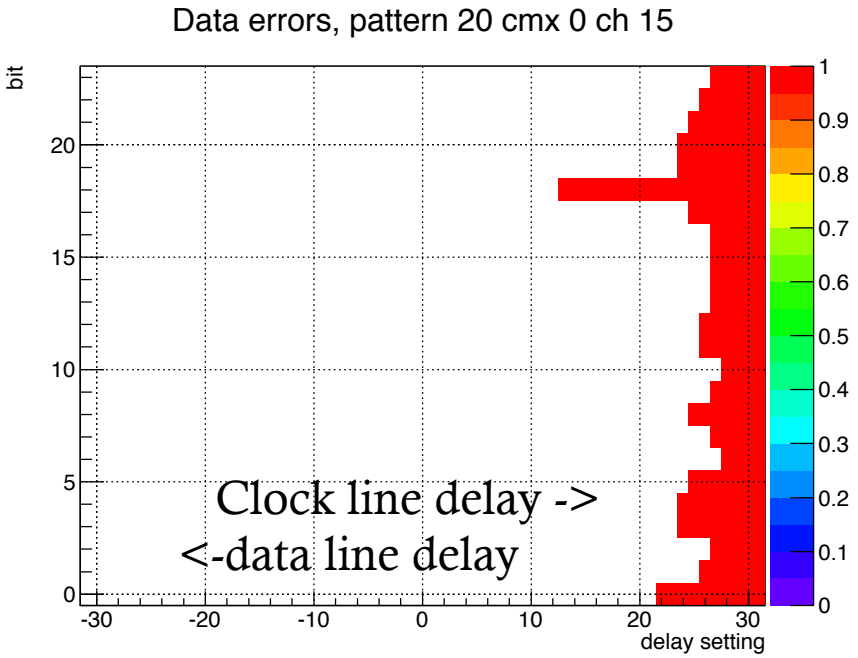
Stress pattern setup

- **Synchronization of patterns**
  - CMX comparison synchronized via BC reset signal
  - JEM pattern generation synchronized via BC reset signal, different arrival times compensated on CMX via adjustable start addresses for comparison
  - CPM synchronization via “random” resets until synchronized arrival of data at CMX is achieved
- **Additional stress test from CMX LVDS drivers**
  - No actual data is send out (translators disabled)
  - FPGA outputs normally driving LVDS lines (all -2xCTP, 3xRTM) sending a stress pattern (all in sync)
  - Long silences all at '0', all at '1', all pulsing '1', all pulsing '0', switching
  - High drive current (12 mA)
  - Aims to disturb ground reference of the FPGA potentially affecting CMOS input timing
  - 255 events long (aims to create 'beats')

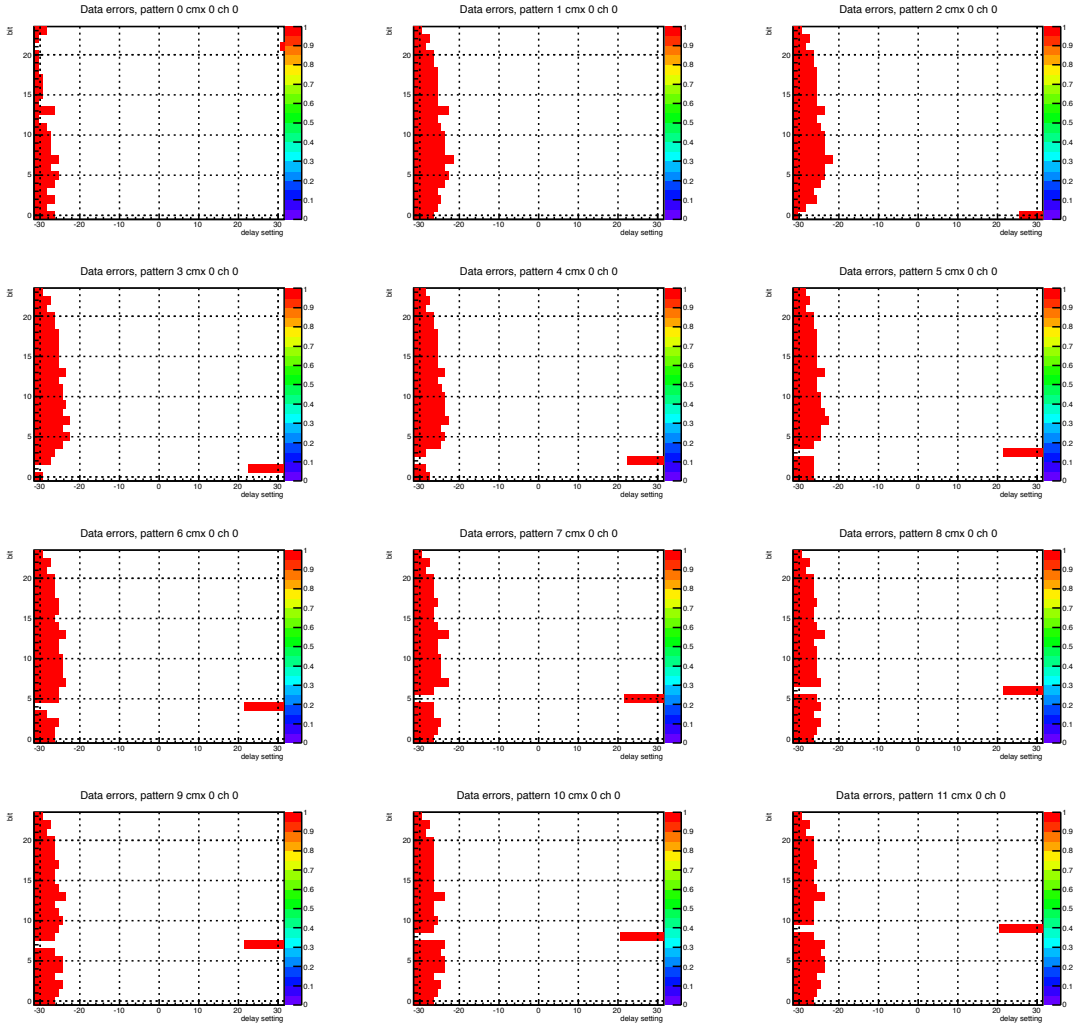
Timing scans with patterns

- **Scan over delays on the data lines and clock lines using patterns**
  - One scan [0..31], same delay setting for all data lines ("negative" delay value on the plot)
  - One scan [1..31] over clock delay ("positive" delay value on the plot)
  - Cycle through all 55 patterns
  - Record bit errors per delay setting, per data bit

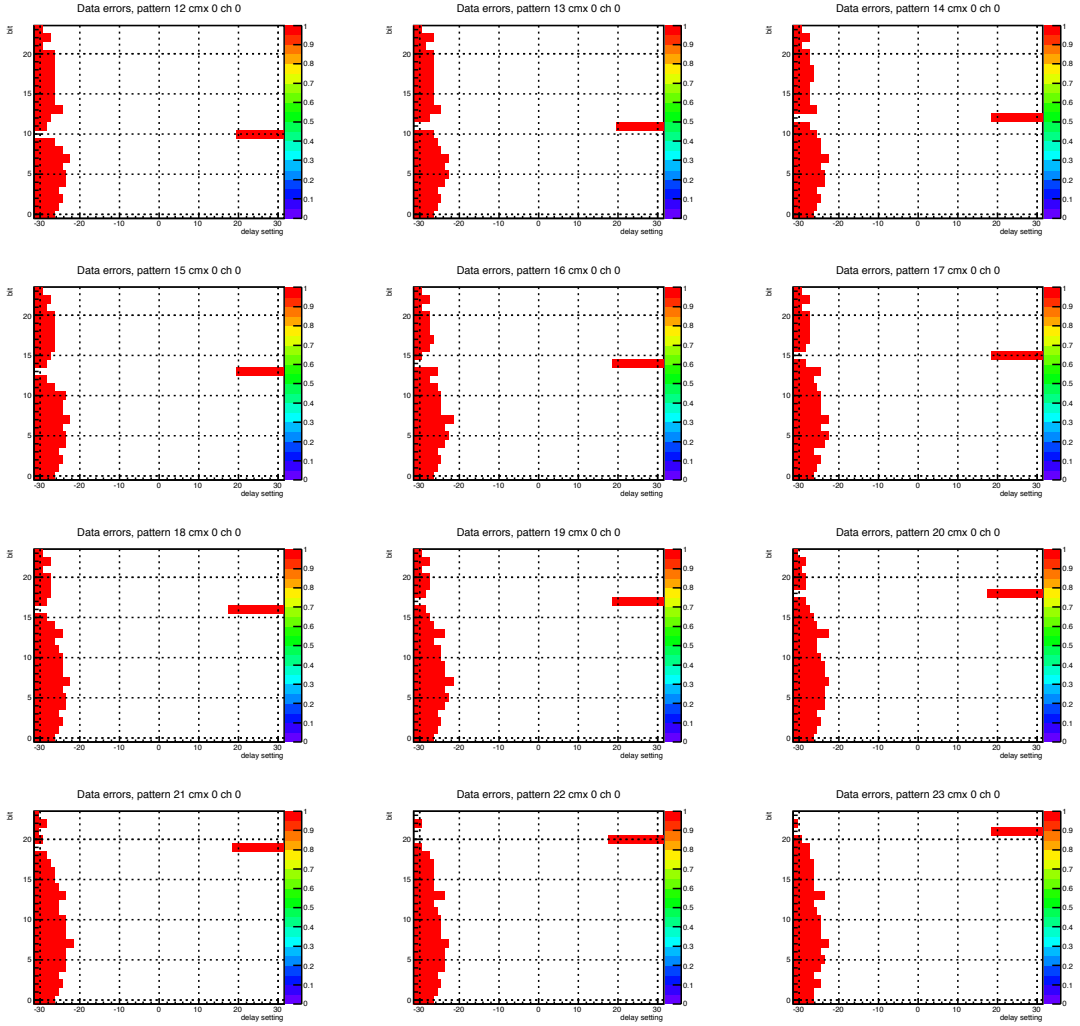
Pattern 20 (switching out of phase of bit 18)
CMX 0 (left side of crate)
Channel 15
Errors are just flagged, not counted!



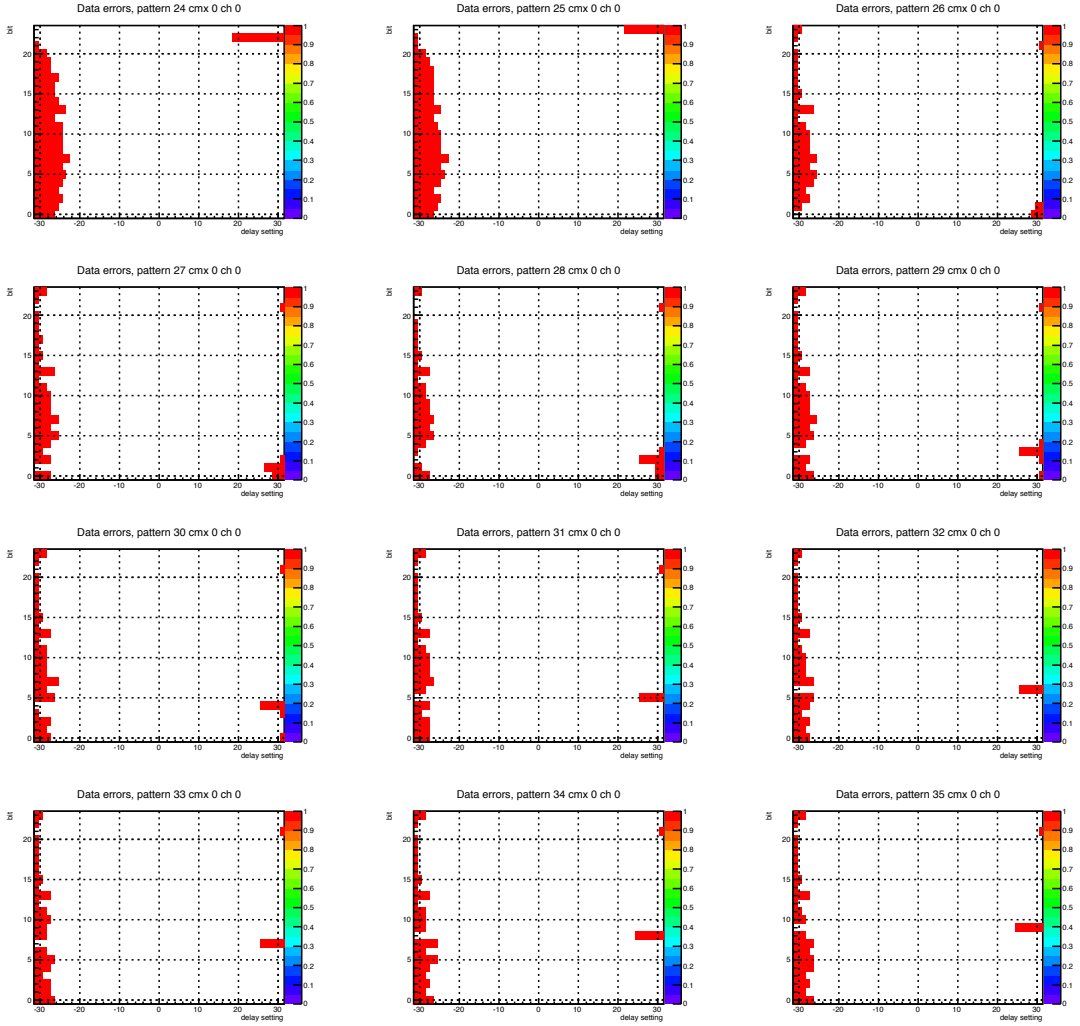
Timing scans with patterns



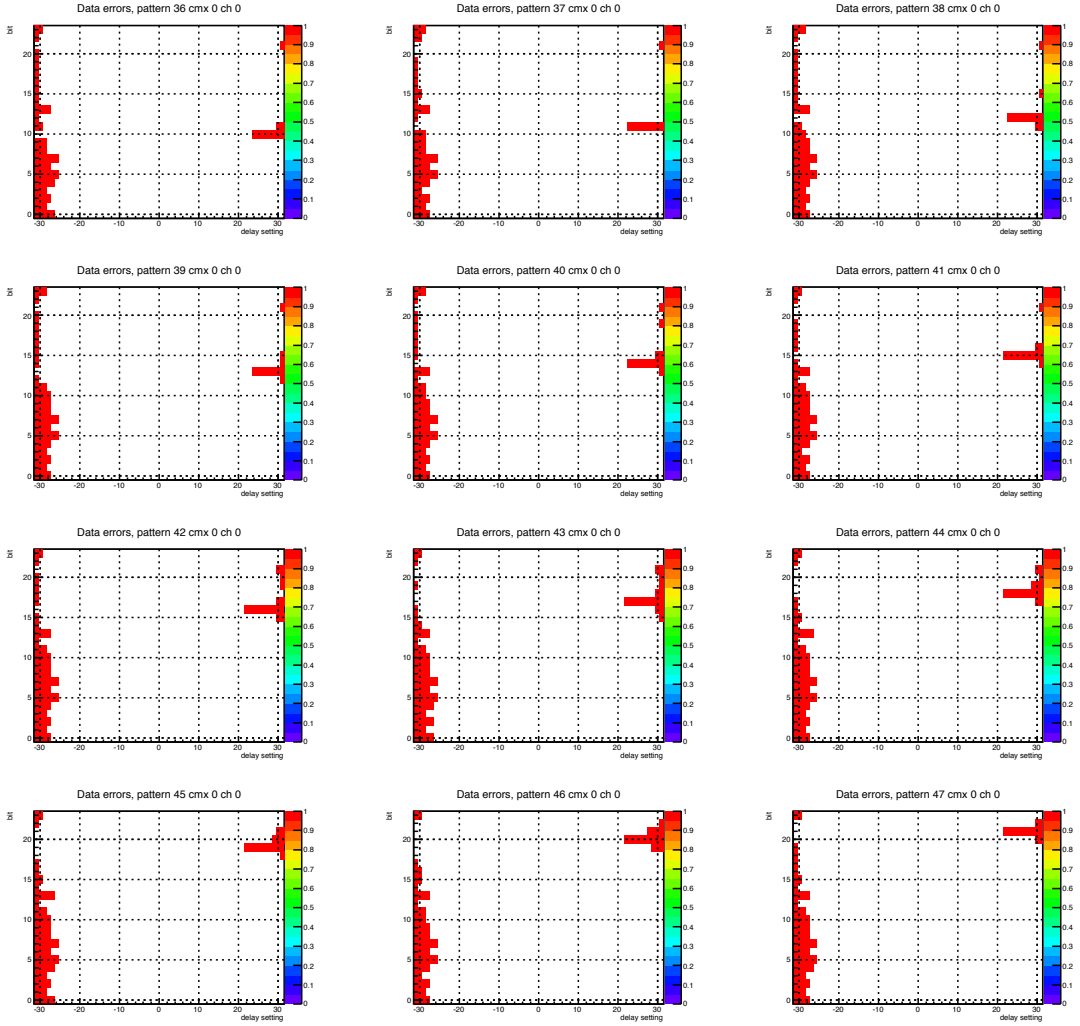
Timing scans with patterns



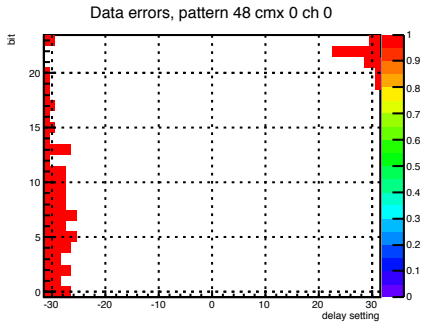
Timing scans with patterns

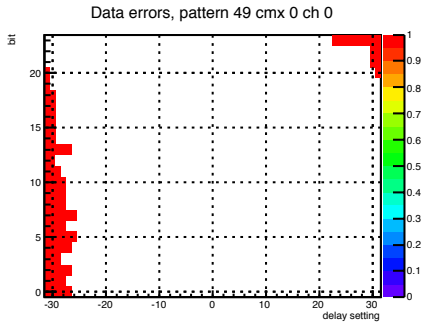


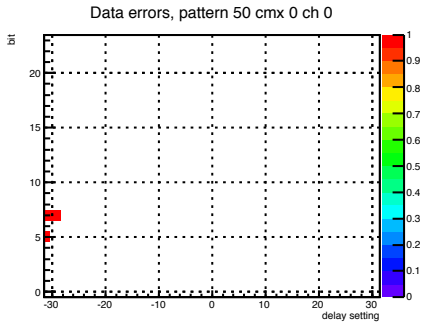
Timing scans with patterns

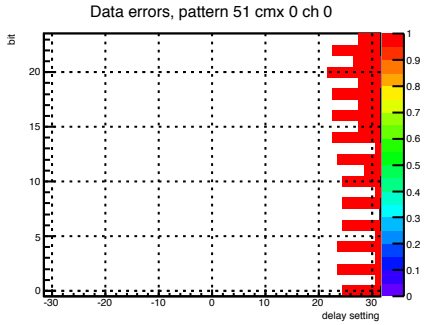


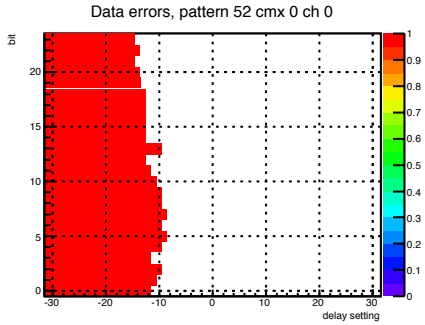
Timing scans with patterns

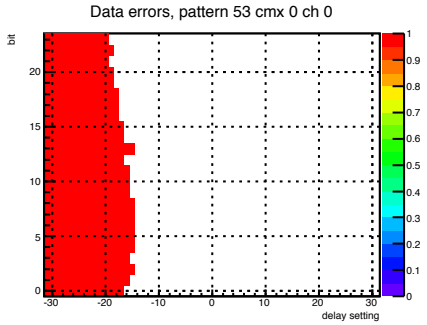


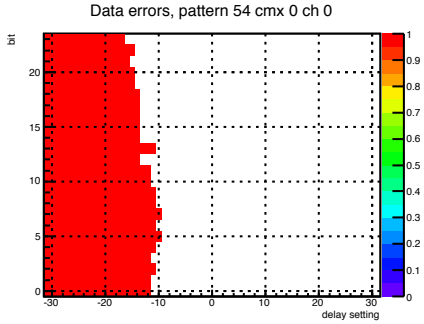


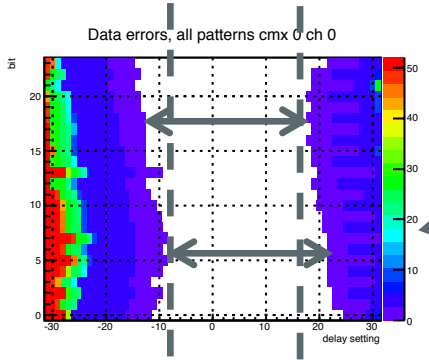












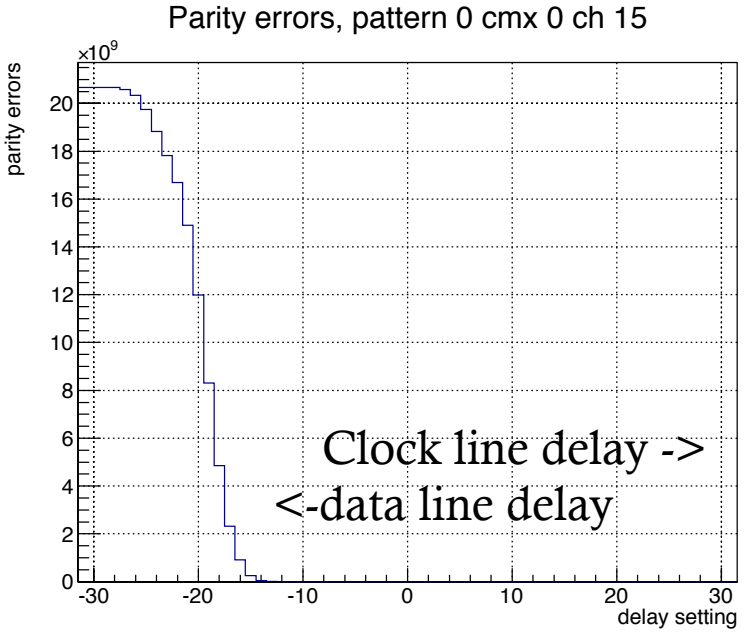
Sum over all patterns

Timing window width

Timing scans with random data

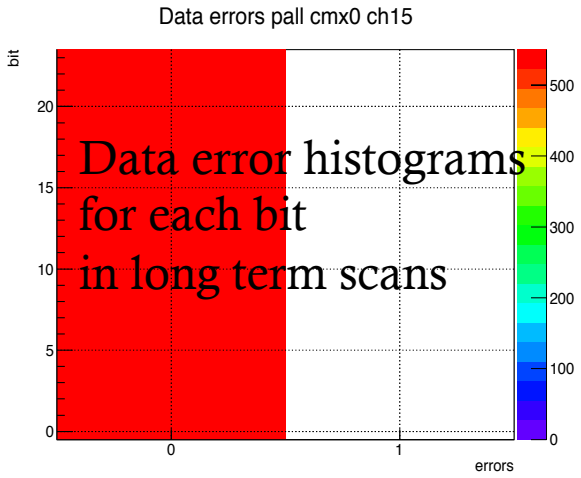
- **Scan over delays on the data lines and clock lines using pseudo-random data**
  - One scan [0..31], same delay setting for all data lines ("negative" delay value on the plot)
  - One scan [1..31] over clock delay ("positive" delay value on the plot)
  - Record parity errors per delay setting, per channel

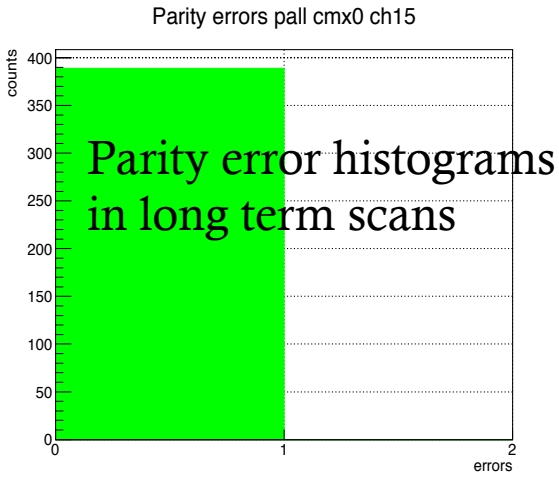
Pseudo random pattern
(different firmware on JEM)
CMX 0 (left side of crate)
Channel 15
Parity error counters do not exceed total event counts

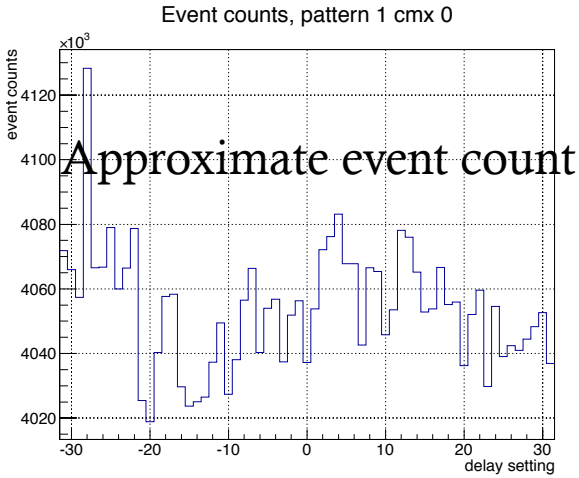


Test procedures

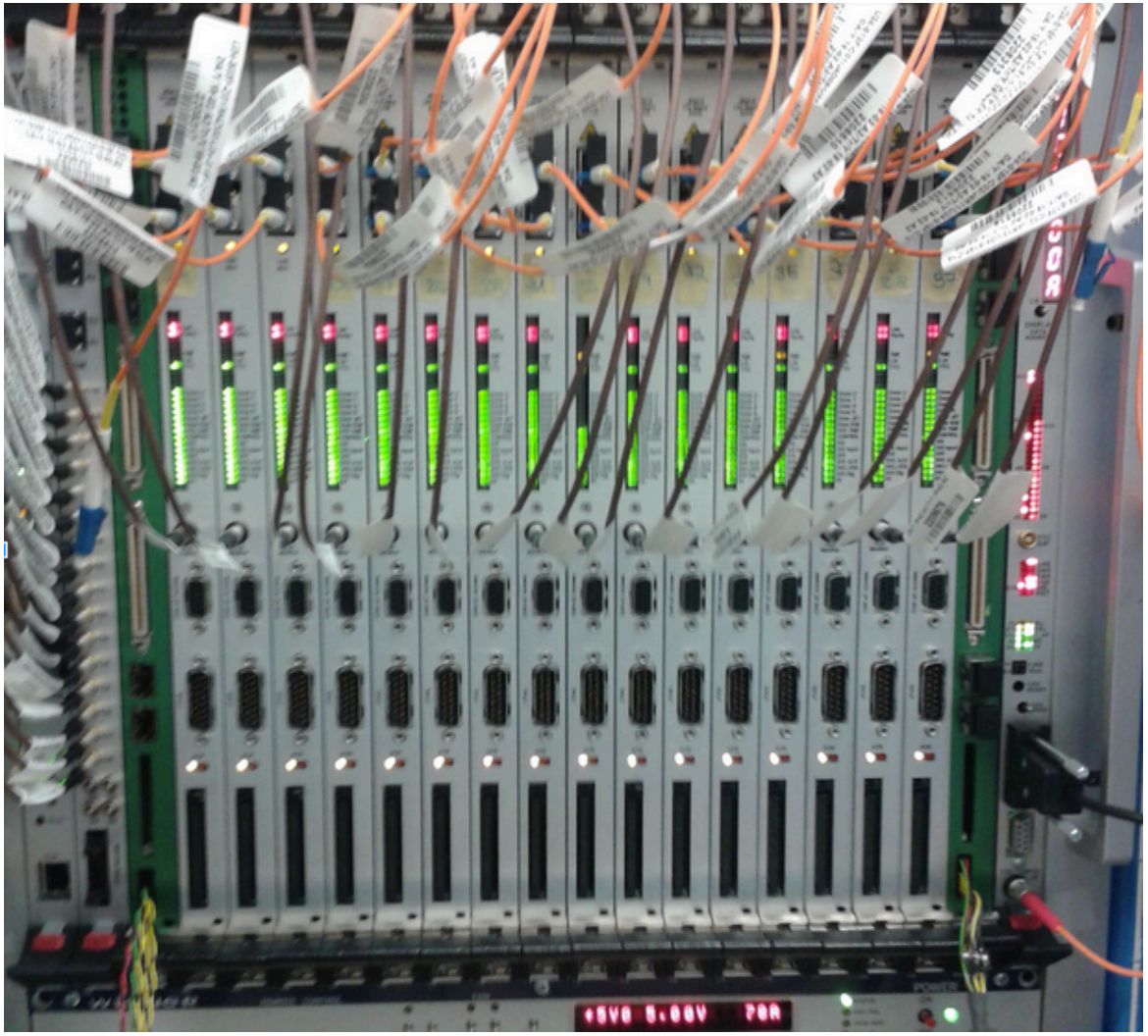
- **Timing scans with patterns and pseudo-random data**
  - Test data integrity: find error free delay settings
  - Test data stability: determine the width of the error free range, determine roughly the center for long term tests
- **Long term tests with patterns and pseudo-random data**
  - Using center of the timing window
  - Determine limit on bit error ratio as 1/(dwell time * 160 Mbps)
  - Maximum run time ~100s, for longer tests need cycles of tests with regular readout of data and reset of counters







Timing scans USA15



JEP0 crate

Full crate tests JEMs

- **Full crate tests in JEP0 crate with 16 JEMs**

NO	run	CMX	time [s]	cycles	patterns	delay	total time [h]
1	1395868943	0/1	0.1	1	all patterns	scan	0.10
2	1396273108	0/1	0.1	1	all patterns	scan	0.10
3	1396277853	0/1	0.1	1	all patterns	scan	0.10
4	1396279431	0/1	5.0	1	all patterns	scan	4.81
5	1396303792+	0/1	50.0	10	all patterns	0/0	7.64
6	1396010274+	0/1	50.0	11	random	scan	9.63
7	1396049227+	0/1	50.0	384	random	10/10	5.32
8	1396964926	0	0.1	1	all patterns	scan	0.10
9	1396970468	0	5.0	1	all patterns	scan	4.81

- CMX SN03 - CMX 0 position receives data from SumET FPGAs
- CMX SN01 - CMX 1 position receives data from Jet FPGAs
- All in JEP0 crate, except for run #8 and run #9, use JEP1 crate and CMX SN01 only in CMX 0 position

Full crate tests JEMs

- **Full crate tests in JEP0 crate with 16 JEMs**

NO	run	CMX	time [s]	cycles	patterns	delay	total time [h]
1	1395868943	0/1	0.1	1	all patterns	scan	0.10
2	1396273108	0/1	0.1	1	all patterns	scan	0.10
3	1396277853	0/1	0.1	1	all patterns	scan	0.10
4	1396279431	0/1	5.0	1	all patterns	scan	4.81
5	1396303792+	0/1	50.0	10	all patterns	0/0	7.64
6	1396010274+	0/1	50.0	11	random	scan	9.63
7	1396049227+	0/1	50.0	384	random	10/10	5.32
8	1396964926	0	0.1	1	all patterns	scan	0.10
9	1396970468	0	5.0	1	all patterns	scan	4.81

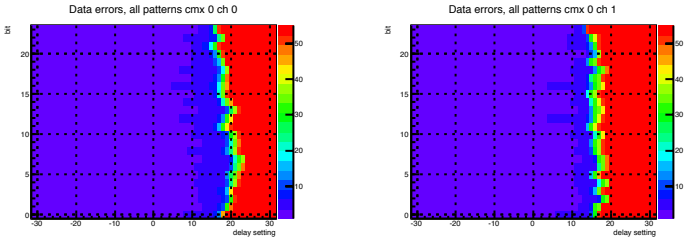
  - Run #1: patterns 22, 25, 54 mismatch in firmware and CMX spy memory, default timing setting in JEM FPGAs (clock edges shifted by 3.125 ns with respect to data edge)
  - Run #2: clock shift removed on SumET FPGA
  - Run #3: clock shift moved to 1.5ns
  - Were able to move the center of the window around delay setting 0

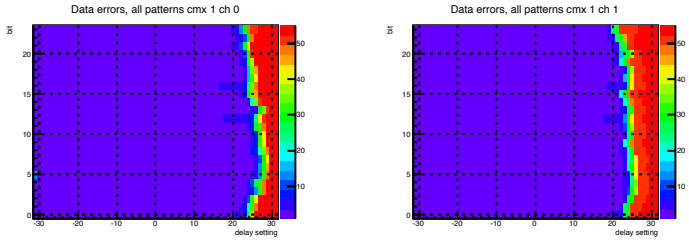
Pre-tests timing scans JEMs

CMX 0

CMX 1

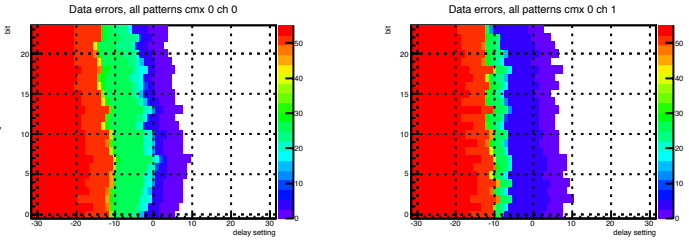
Run #1



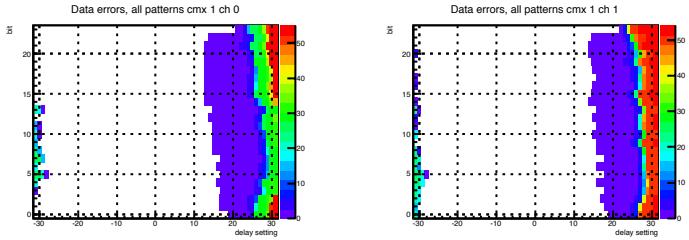


clock | data 3.125ns

Run #2

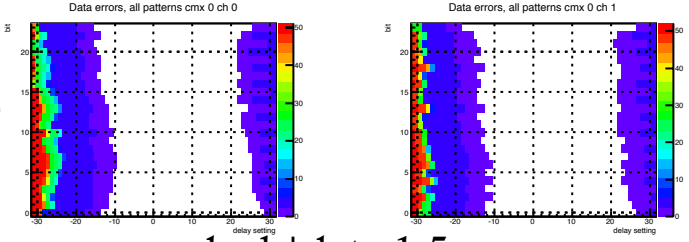


clock | data 0ns

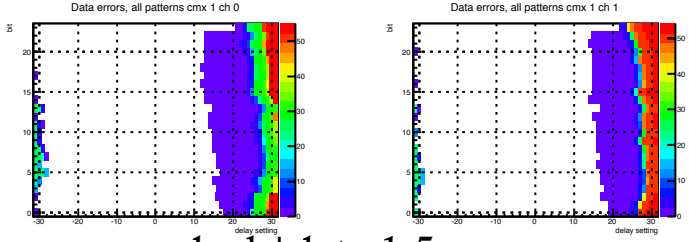


clock | data 1.5ns

Run #3



clock | data 1.5ns



clock | data 1.5ns

In all histograms: channels 0 and 1

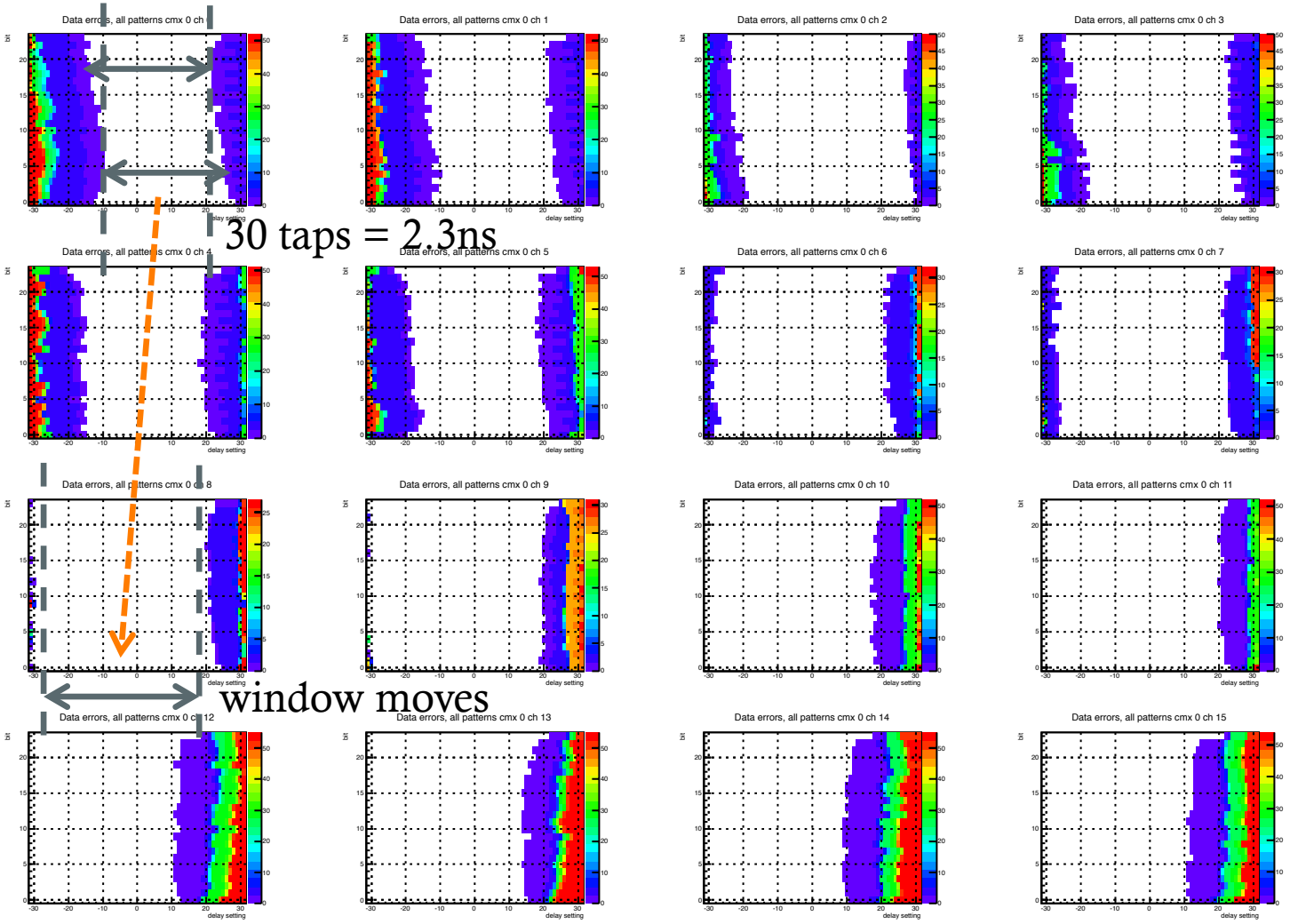
Full crate tests JEMs

- **Full crate tests in JEP0 crate with 16 JEMs**

NO	run	CMX	time [s]	cycles	patterns	delay	total time [h]
1	1395868943	0/1	0.1	1	all patterns	scan	0.10
2	1396273108	0/1	0.1	1	all patterns	scan	0.10
3	1396277853	0/1	0.1	1	all patterns	scan	0.10
4	1396279431	0/1	5.0	1	all patterns	scan	4.81
5	1396303792+	0/1	50.0	10	all patterns	0/0	7.64
6	1396010274+	0/1	50.0	11	random	scan	9.63
7	1396049227+	0/1	50.0	384	random	10/10	5.32
8	1396964926	0	0.1	1	all patterns	scan	0.10
9	1396970468	0	5.0	1	all patterns	scan	4.81

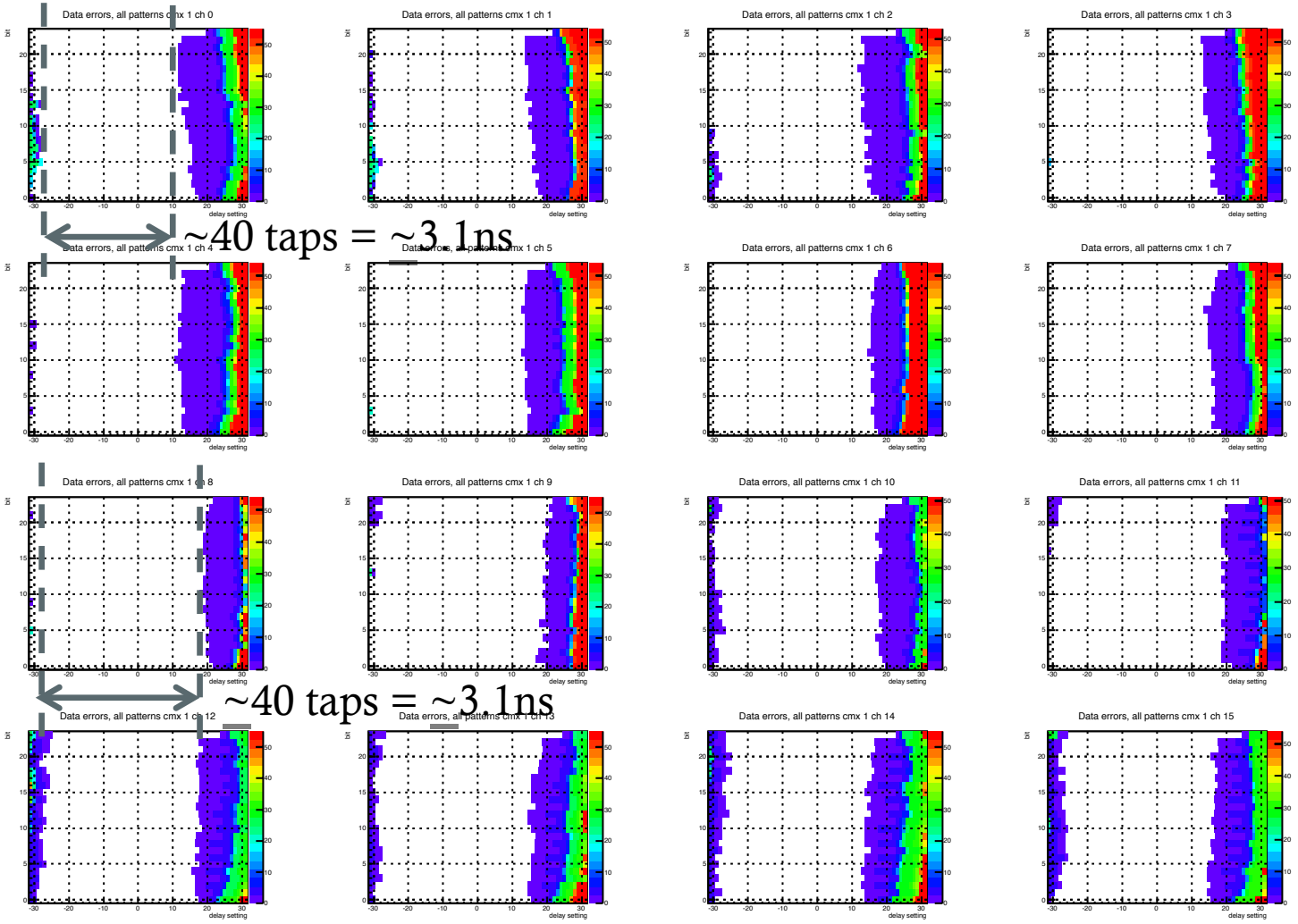
- Main results from run #4 to run #7
- For pattern and pseudo-random data different firmware configurations used, phase between data and clock possibly different, do not expect optimal delay settings to be the same

Timing scan JEMs



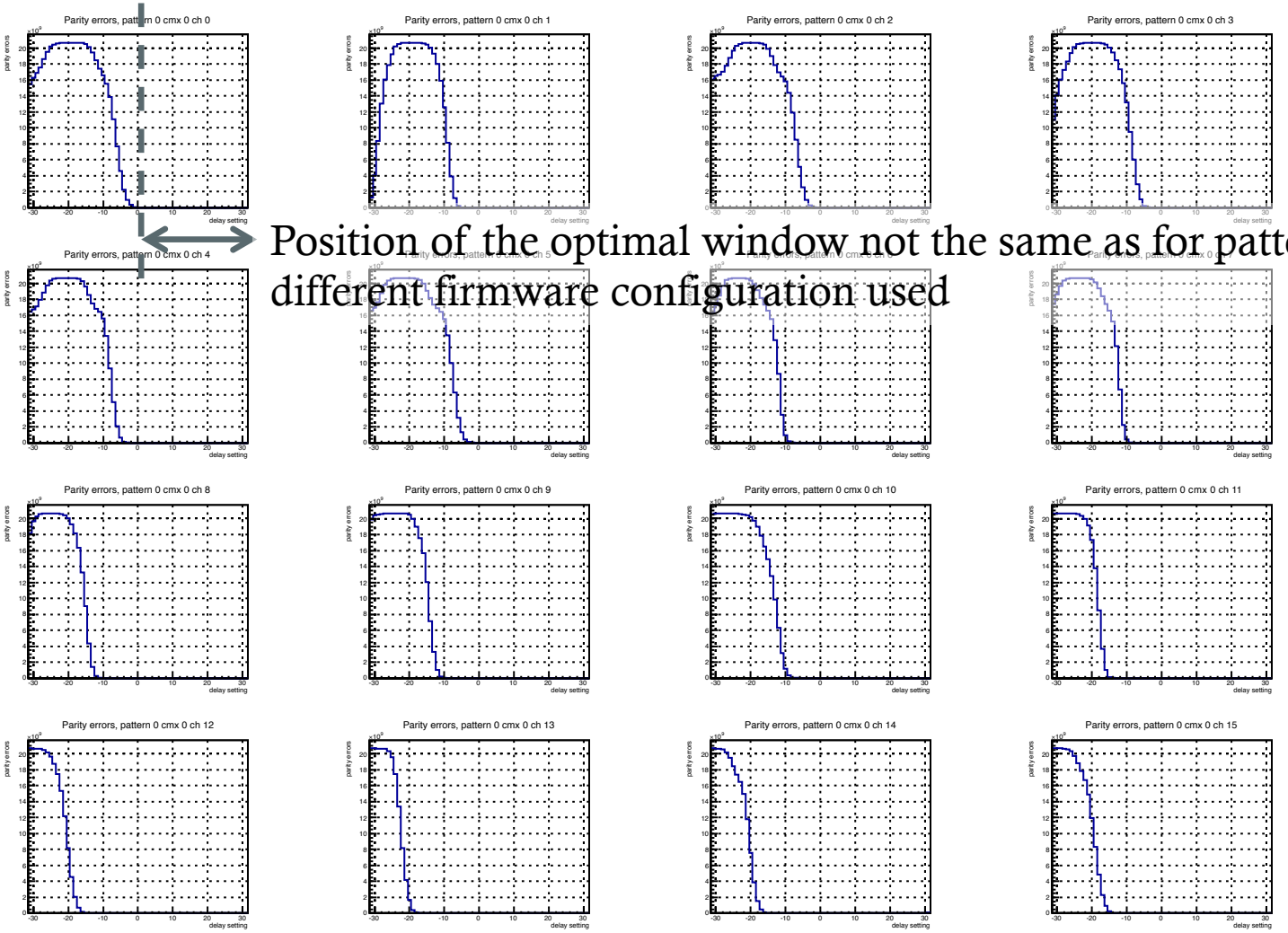
Run #4: CMX0, all patterns, 5s dwell time per scan point

Timing scan JEMs



Run #4: CMX1, all patterns, 5s dwell time per scan point

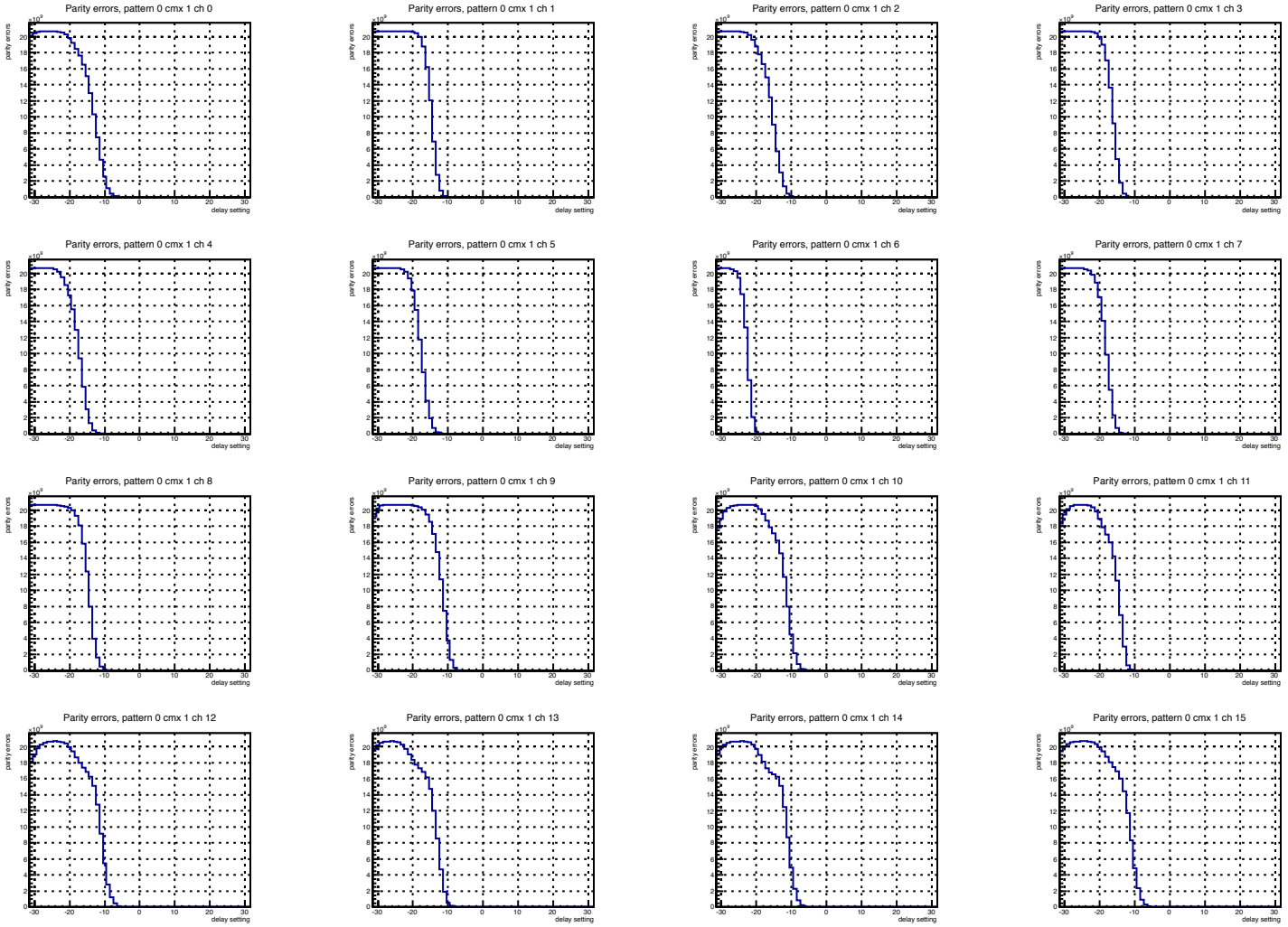
Timing scan JEMs



Position of the optimal window not the same as for patterns, different firmware configuration used

Run #6: CMX0, pseudo-random data, 50s dwell time per scan point

Timing scan JEMs



Run #6: CMX1, pseudo-random data, 50s dwell time per scan point

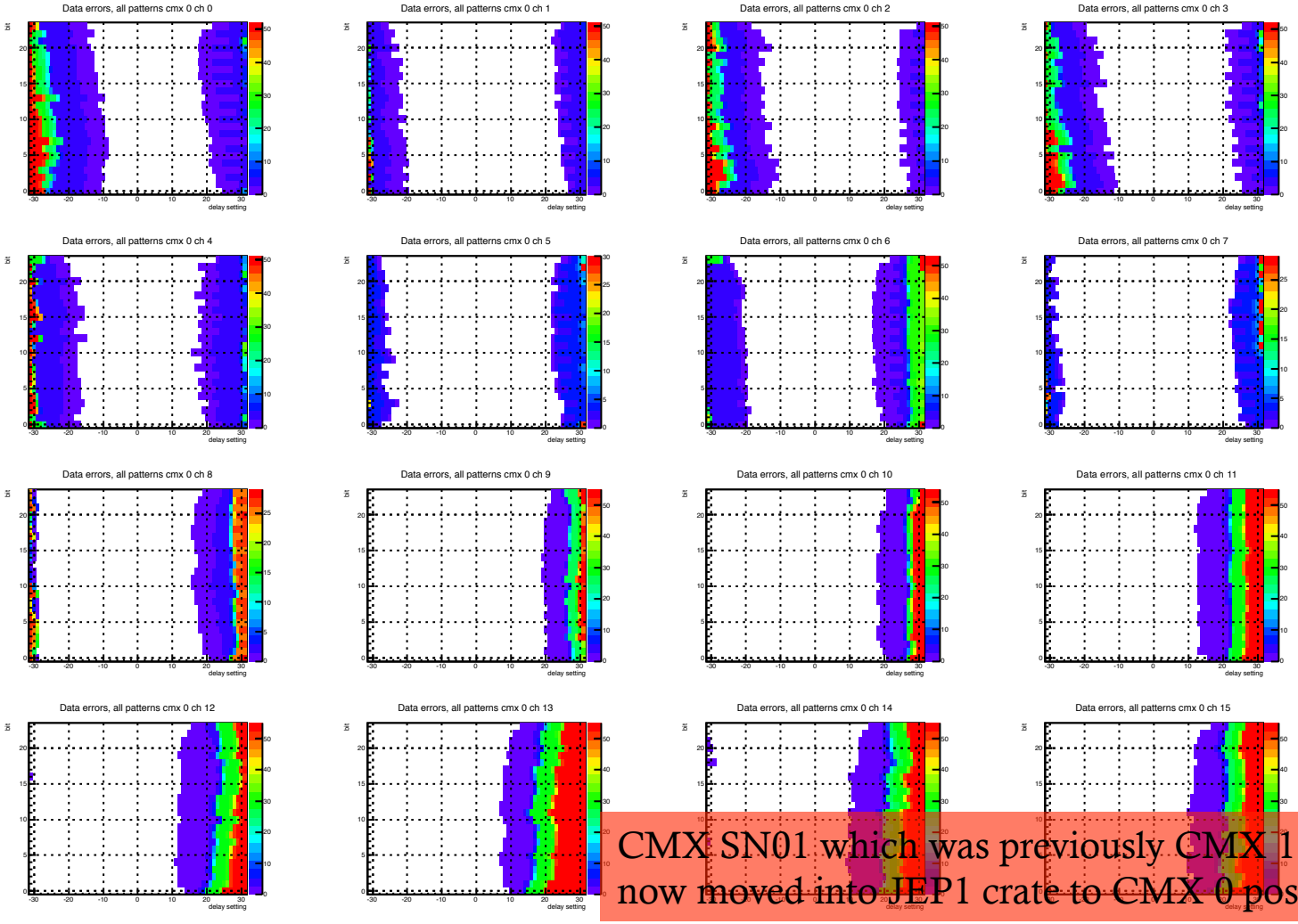
Full crate tests JEMs

- **Full crate tests in JEP0 crate with 16 JEMs**

NO	run	CMX	time [s]	cycles	patterns	delay	total time [h]
1	1395868943	0/1	0.1	1	all patterns	scan	0.10
2	1396273108	0/1	0.1	1	all patterns	scan	0.10
3	1396277853	0/1	0.1	1	all patterns	scan	0.10
4	1396279431	0/1	5.0	1	all patterns	scan	4.81
5	1396303792+	0/1	50.0	10	all patterns	0/0	7.64
6	1396010274+	0/1	50.0	11	random	scan	9.63
7	1396049227+	0/1	50.0	384	random	10/10	5.32
8	1396964926	0	0.1	1	all patterns	scan	0.10
9	1396970468	0	5.0	1	all patterns	scan	4.81

  - Run #8 and run #9
    - corrected pattern 25 to probe bit 23 in the intended way
    - CMX SN01 from CMX 1 moved to CMX 0 position in JEP1 crate
    - only one CMX, but no difference to other runs or problems uncovered
    - Systematic shift of the window still visible for CMX 0 position

Post-tests timing scans JEMs



CMX SN01 which was previously CMX 1 position, now moved into JEP1 crate to CMX 0 position

Run #9: CMX0, all patterns, 5s dwell time per scan point

Full crate tests JEMs

- **Comfortable window of at least ~2.3ns and ~3.1ns**
  - Window on CMX 0 position moves systematically from module to module
  - Difference in window sizes on CMX 0 and CMX 1 (related to the position, not to the module)
  - In tests with pseudo-random data the other edge cannot be probed
- **No power or heat issues**
- **Longest runs with 0/0 delay settings for 7.6h and all patterns**
  - Limit on bit error ratio is 23×10^{-14}, would translate into event error rate of 0.09 Hz (assuming one bit in any of the 400 data lines and 6 CMX will trigger an event)

Full crate tests CPMs

- **Full crate tests in CP0 crate with 14 CPMs**

NO	run	CMX	time [s]	cycles	patterns	delay	total time [h]
1	1396388038	0/1	5.0	1	all patterns	scan	4.81
2	1396406084+	0/1	50.0	8	all patterns	-10/-10	6.11
3	1396625660	0/1	0.1	1	all patterns	scan	0.10
4	1396629697	0/1	5.0	1	all patterns	scan	4.81
5	1396650911+	0/1	50.0	23	all patterns	-10/-10	17.57
6	1396647710	0/1	50.0	1	random	scan	0.88
7	1396716630+	0/1	50.0	1265	random	-10/-10	17.57
8	1396949335+	0	85.0	1	random	scan	1.49

  - CMX SN03 - CMX 0 position
  - CMX SN01 - CMX 1 position
  - All in CP0 crate, removed CMX SN01 later to be placed into JEP1 crate

Full crate tests CPMs

- **Full crate tests in CP0 crate with 14 CPMs**

NO	run	CMX	time [s]	cycles	patterns	delay	total time [h]
1	1396388038	0/1	5.0	1	all patterns	scan	4.81
2	1396406084+	0/1	50.0	8	all patterns	-10/-10	6.11
3	1396625660	0/1	0.1	1	all patterns	scan	0.10
4	1396629697	0/1	5.0	1	all patterns	scan	4.81
5	1396650911+	0/1	50.0	23	all patterns	-10/-10	17.57
6	1396647710	0/1	50.0	1	random	scan	0.88
7	1396716630+	0/1	50.0	1265	random	-10/-10	17.57
8	1396949335+	0	85.0	1	random	scan	1.49

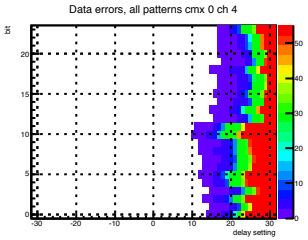
- Run #1 and run #2: unsynchronized pattern start on CPMs (no BC reset reception in firmware possible), compensated with shifted patterns stored in CMX spy memory
- Run #3: synchronized pattern start on CPMs, no difference seen in results

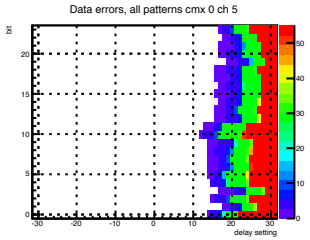
Pretests timing scans CPMs

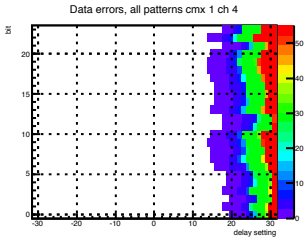
CMX 0

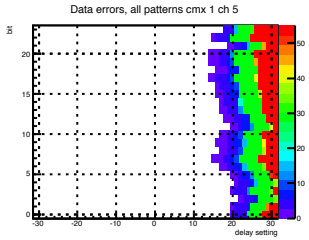
CMX 1

Run #1



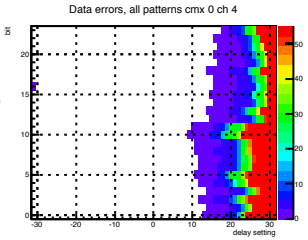


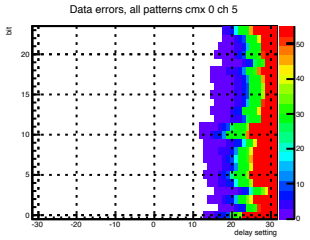


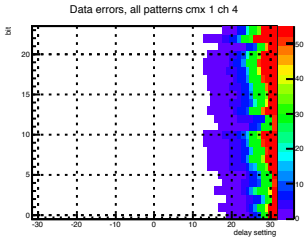


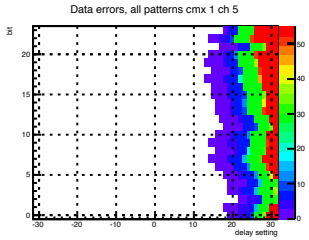
Unsynchronised patterns

Run #3









Synchronised patterns

In all histograms: channels 4 and 5

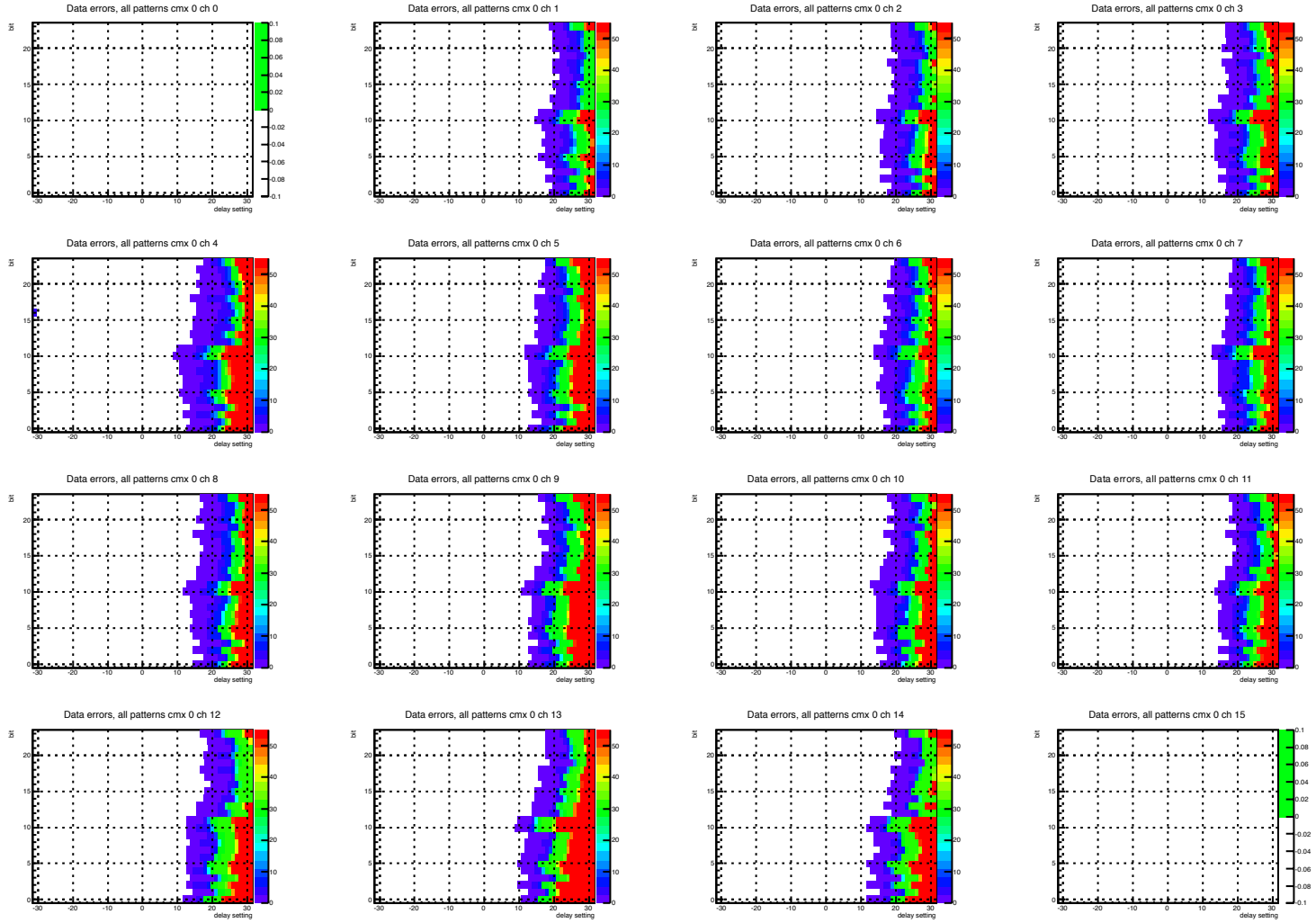
Full crate tests CPMs

- **Full crate tests in CP0 crate with 14 CPMs**

NO	run	CMX	time [s]	cycles	patterns	delay	total time [h]
1	1396388038	0/1	5.0	1	all patterns	scan	4.81
2	1396406084+	0/1	50.0	8	all patterns	-10/-10	6.11
3	1396625660	0/1	0.1	1	all patterns	scan	0.10
4	1396629697	0/1	5.0	1	all patterns	scan	4.81
5	1396650911+	0/1	50.0	23	all patterns	-10/-10	17.57
6	1396647710	0/1	50.0	1	random	scan	0.88
7	1396716630+	0/1	50.0	1265	random	-10/-10	17.57
8	1396949335+	0	85.0	1	random	scan	1.49

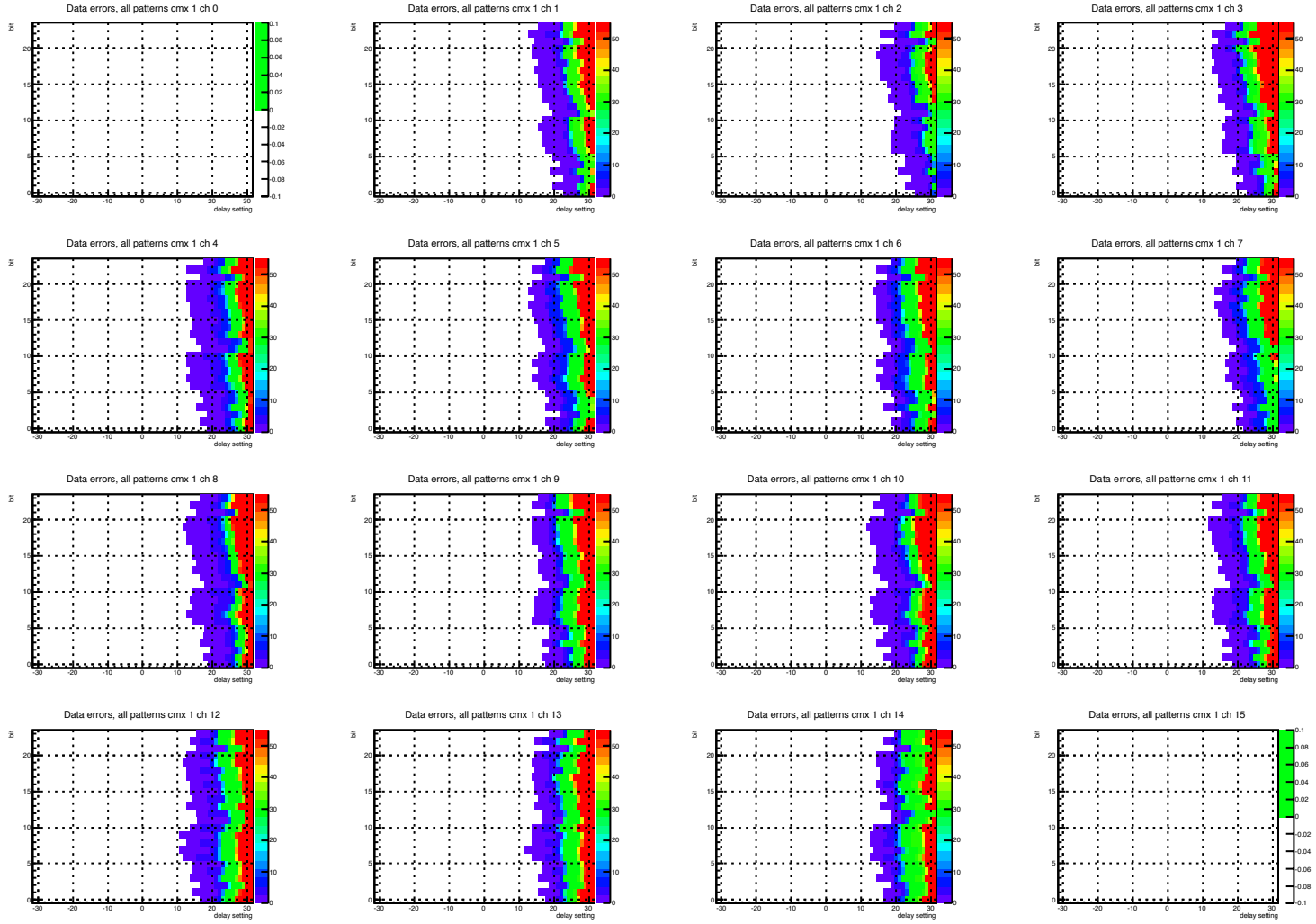
  - Main results from run #4 to run #7, for BER scan time from run #2 and run #5 were added

Timing scan CPMs



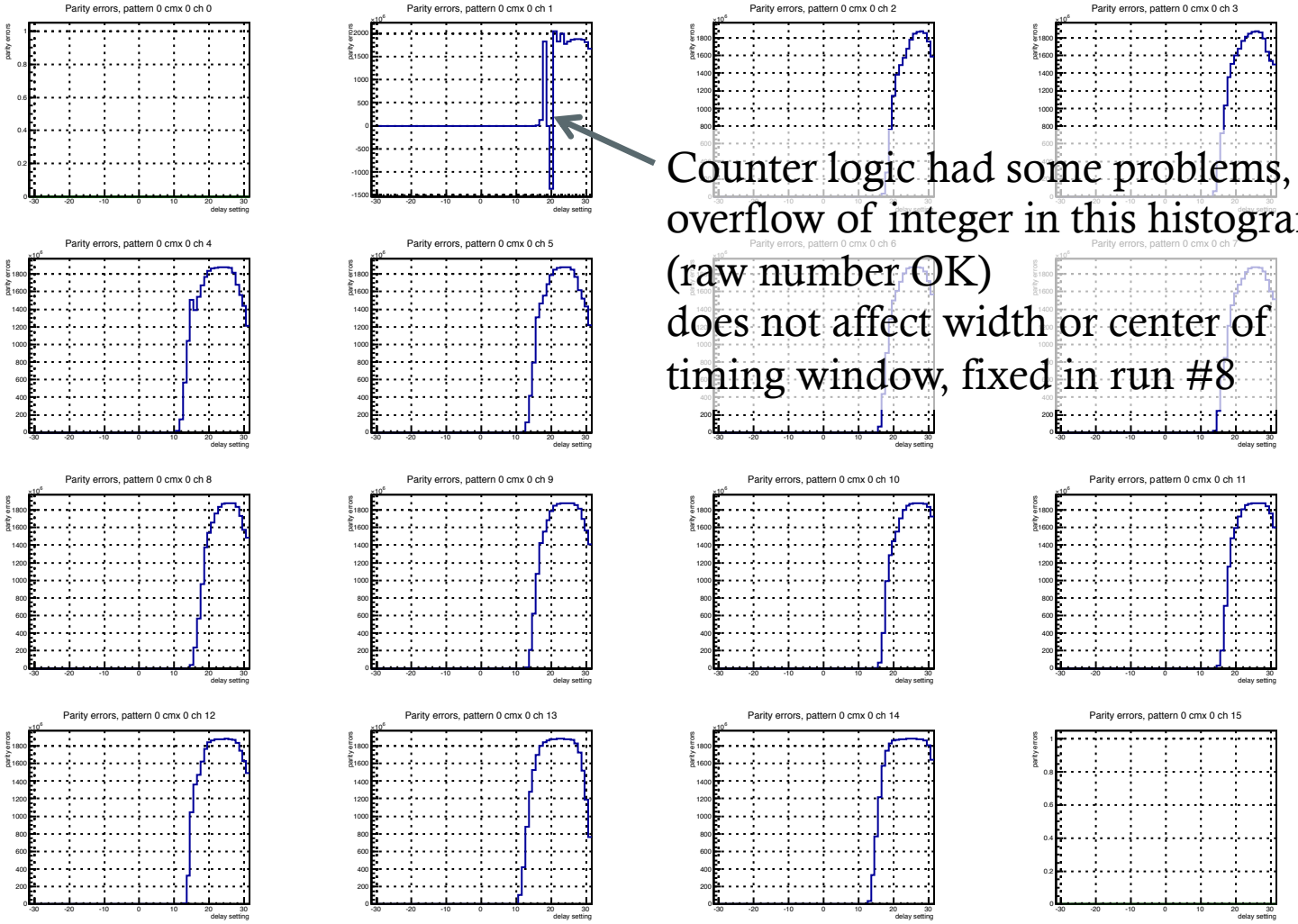
Run #4: CMX0, all patterns, 5s dwell time per scan point

Timing scan CPMs



Run #4: CMX1, all patterns, 5s dwell time per scan point

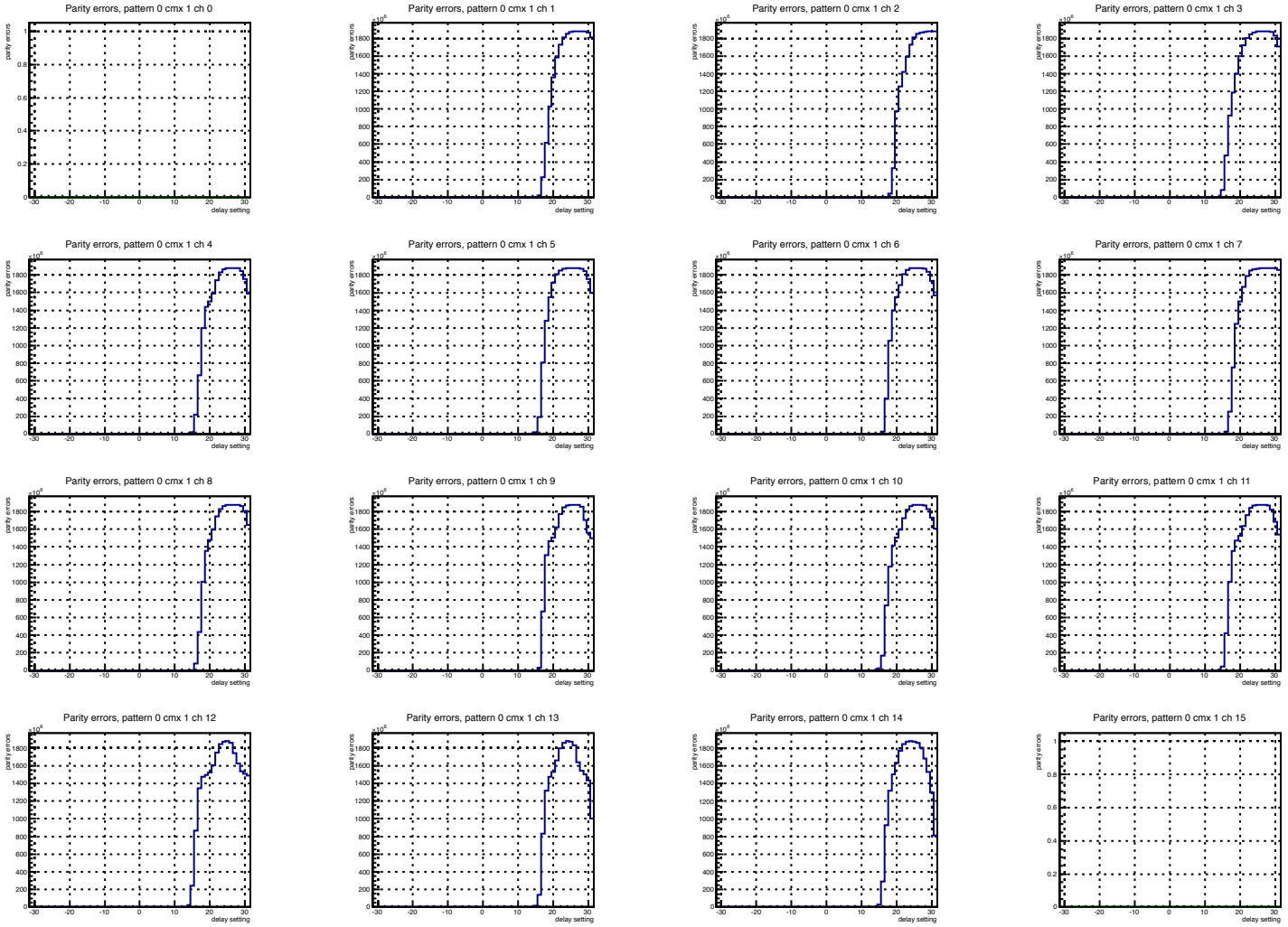
Timing scan CPMs



Counter logic had some problems, overflow of integer in this histogram (raw number OK)
does not affect width or center of timing window, fixed in run #8

Run #6: CMX0, pseudo-random data, 50s dwell time per scan point

Timing scan CPMs



Run #6: CMX1, pseudo-random data, 50s dwell time per scan point

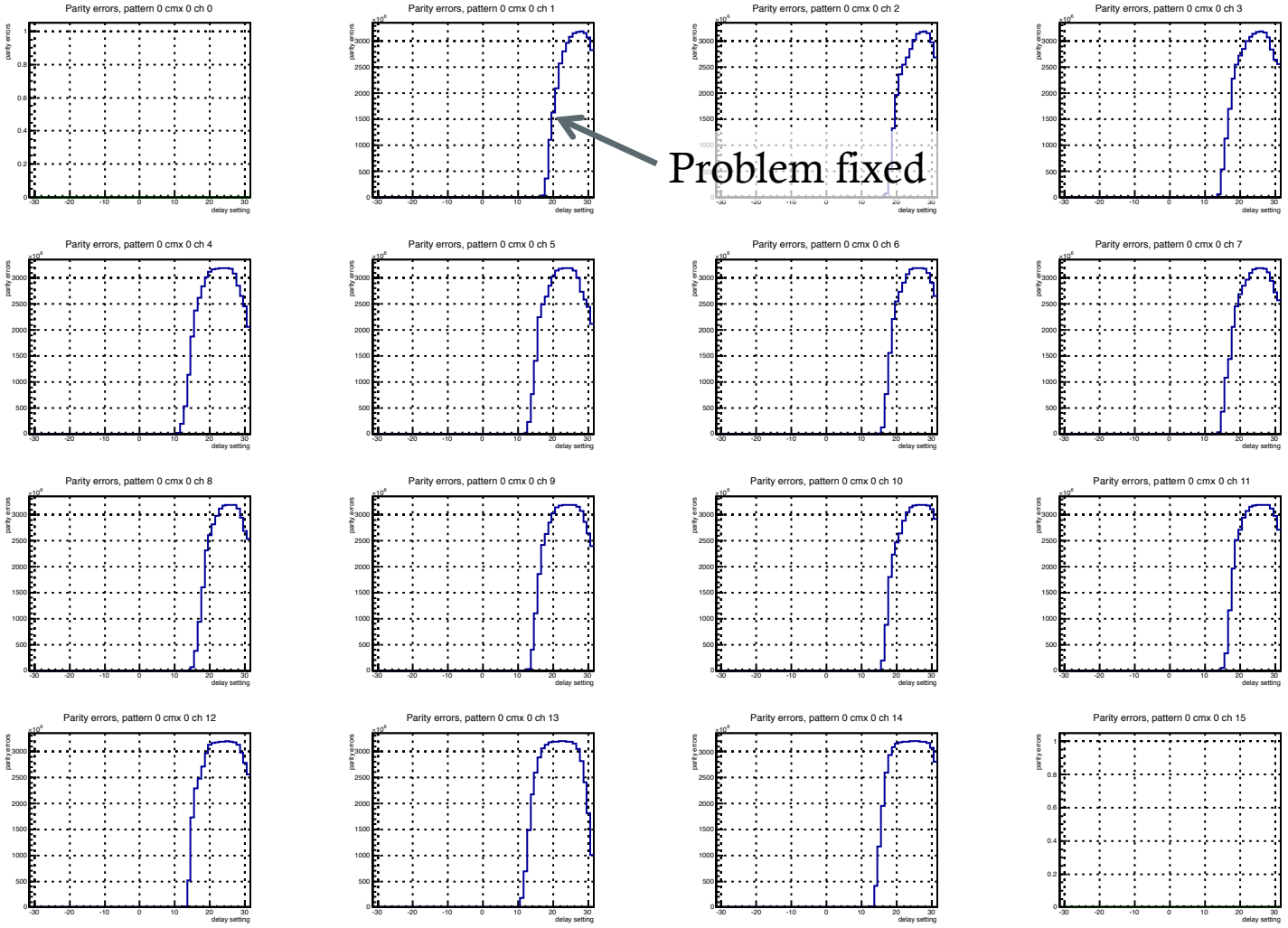
Full crate tests CPMs

- **Full crate tests in CP0 crate with 14 CPMs**

NO	run	CMX	time [s]	cycles	patterns	delay	total time [h]
1	1396388038	0/1	5.0	1	all patterns	scan	4.81
2	1396406084+	0/1	50.0	8	all patterns	-10/-10	6.11
3	1396625660	0/1	0.1	1	all patterns	scan	0.10
4	1396629697	0/1	5.0	1	all patterns	scan	4.81
5	1396650911+	0/1	50.0	23	all patterns	-10/-10	17.57
6	1396647710	0/1	50.0	1	random	scan	0.88
7	1396716630+	0/1	50.0	1265	random	-10/-10	17.57
8	1396949335+	0	85.0	1	random	scan	1.49

- problems with error counting in meta stable timing region fixed
- feature understood: counts are almost 2x event counts, error checking with 80 MHz clock, counting with 40 MHz clock, double counting in meta stable region possible
- no influence on timing window width or position

Post-test timing scan CPMs



Run #8: CMX0, pseudo-random data, 85s dwell time per scan point

Full crate tests CPMs

- **Comfortable window of at least ~3.1ns**
  - More homogenous timing window width and position
  - In all tests the other edge cannot be probed
- **No power or heat issues**
- **Longest runs with -10/-10 delay settings for 23.7h and all patterns**
  - Limit on bit error ratio is 7.3×10^{-14}, would translate into event error rate of 0.03 Hz (assuming one bit in any of the 400 data lines and 6 CMX will trigger an event)

Conclusions

- **Operation of both CMX prototypes in full crates of JEMs/CPMs in USA15**
- **Results indicate good data integrity, wide good timing window for data capture and stable data reception over hours**
  - Limit on event error rate seems to be sufficient for L1 trigger requirement
  - A few not well understood features of the variation in the position and width of the timing window
  - None indicate problems with the CMX backplane itself
  - Timing scan procedure will be develop into a timing calibration procedure

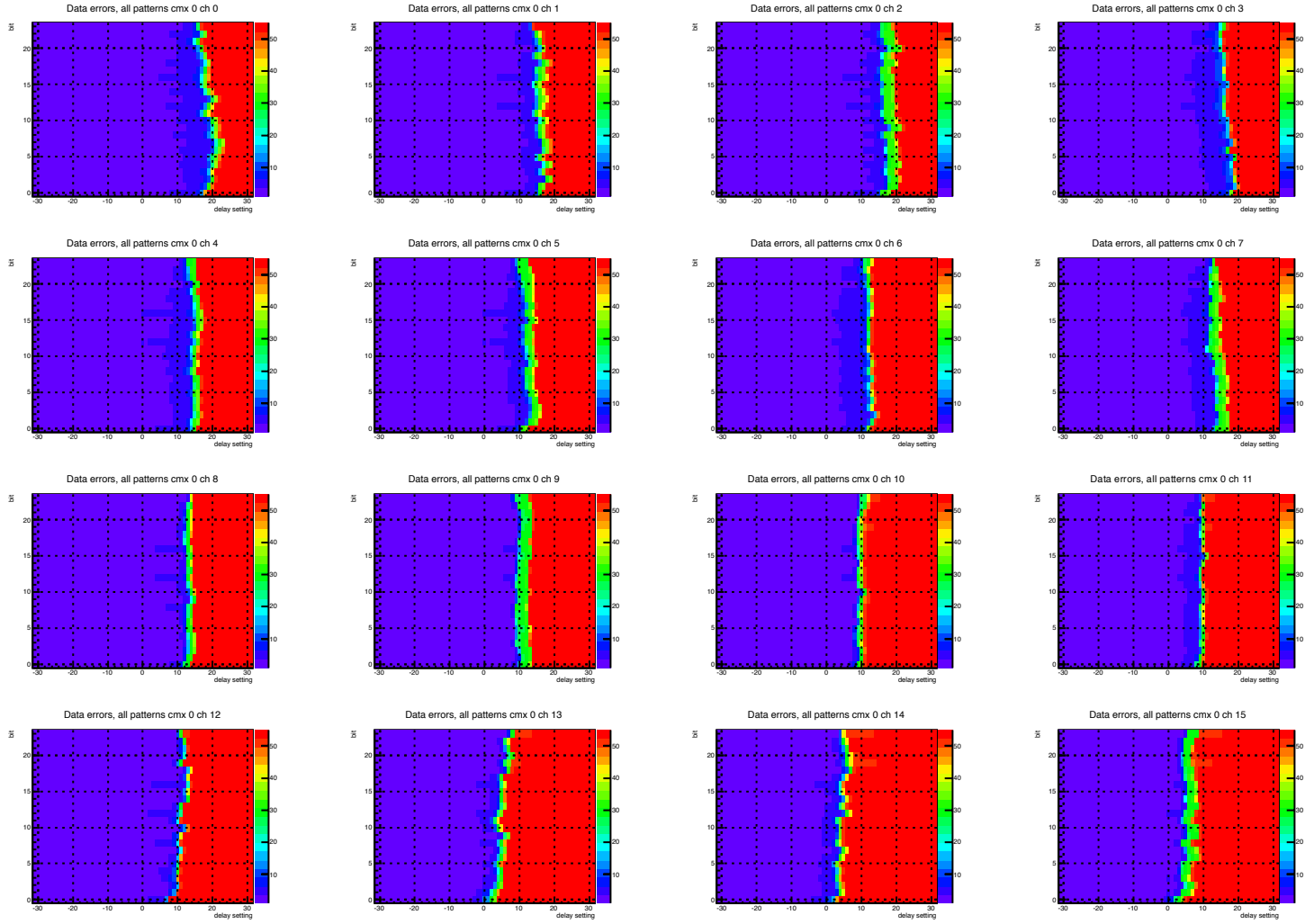
- **Patterns 52-54**

Pattern 52:
0110 1010 1010 1010 1010 ...
0110 1010 1010 1010 1010 ...
0110 1010 1010 1010 1010 ...
up to 24th bit...

Pattern 53:
0110 0110 0110 0110 0110 ...
0110 0110 0110 0110 0110 ...
0110 0110 0110 0110 0110 ...
up to 24th bit...

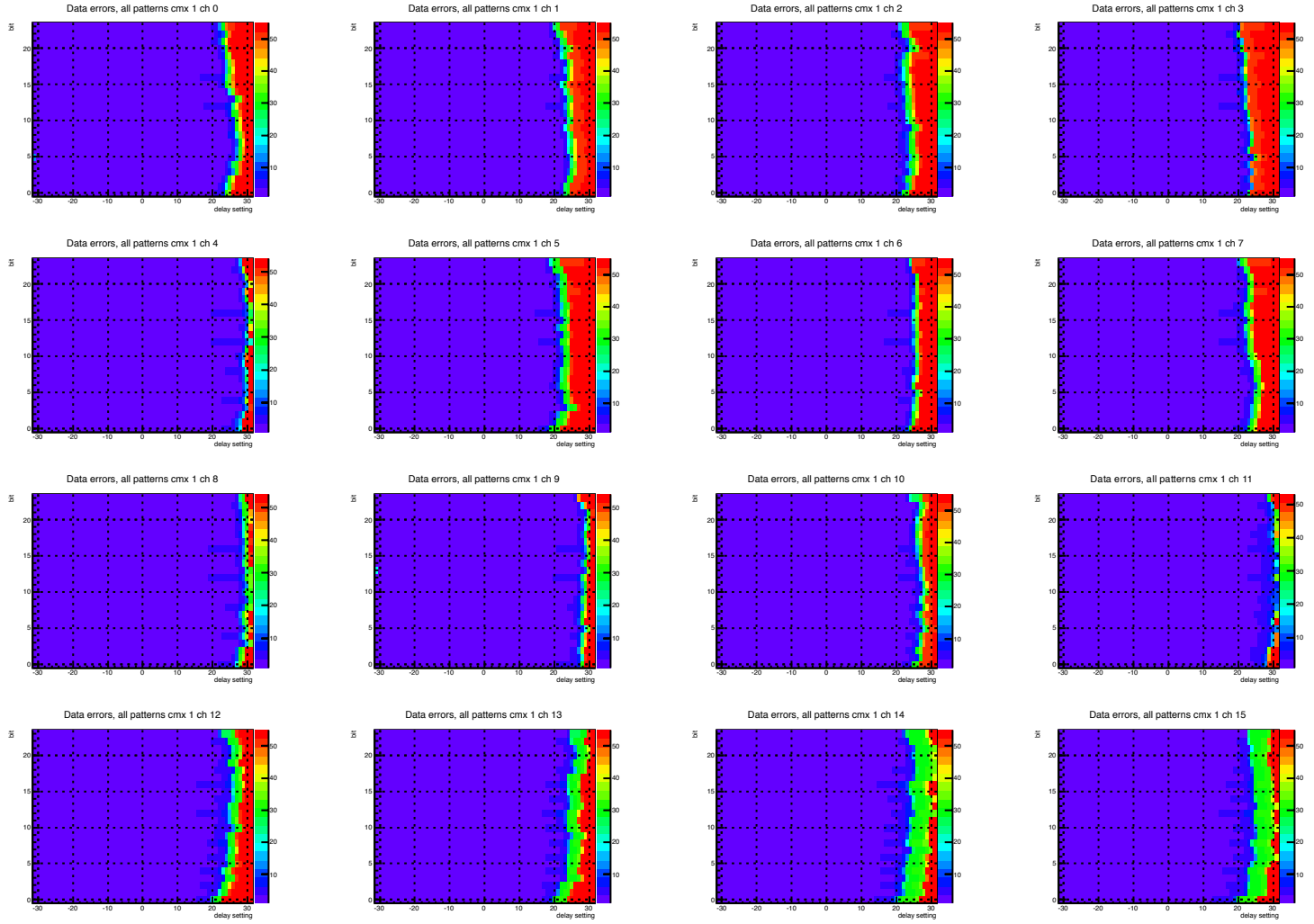
Pattern 54:
1001 0110 0110 0110 0110 ...
1001 0110 0110 0110 0110 ...
1001 0110 0110 0110 0110 ...
up to 24th bit...

Pretests timing scans JEMs



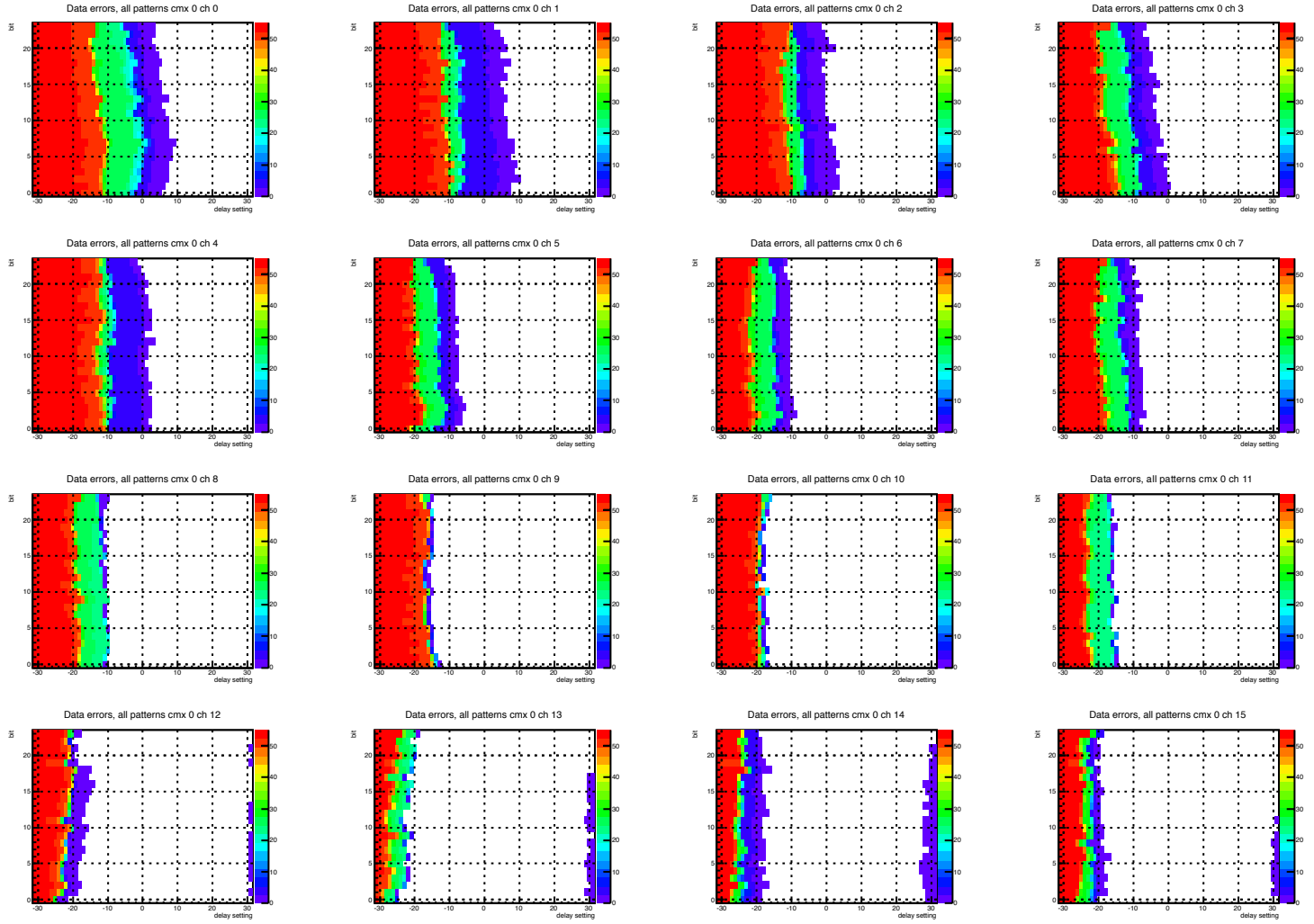
Run #1: CMX0, all patterns, 0.1s dwell time per scan point

Pretests timing scans JEMs



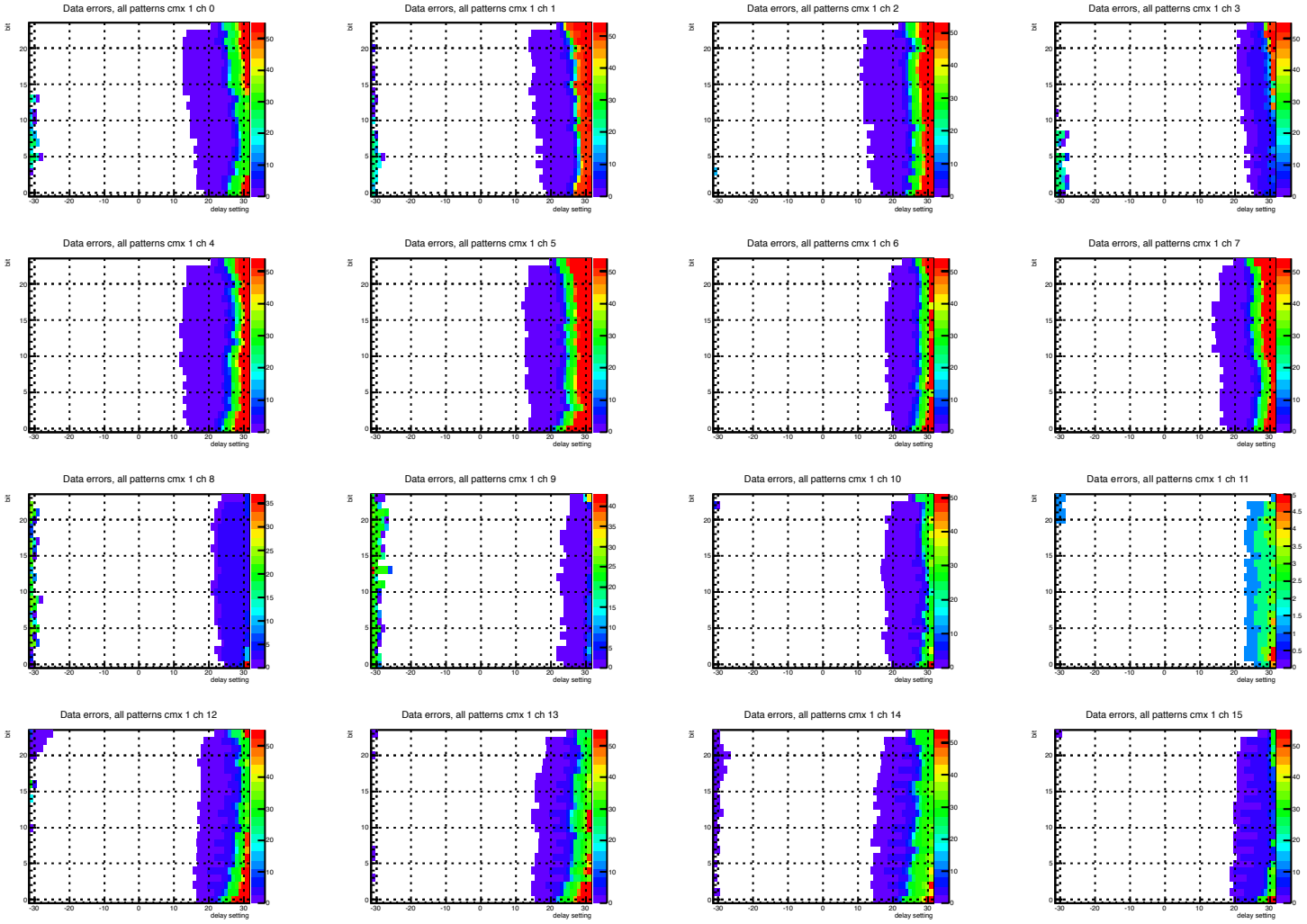
Run #1: CMX1, all patterns, 0.1s dwell time per scan point

Pretests timing scans JEMs



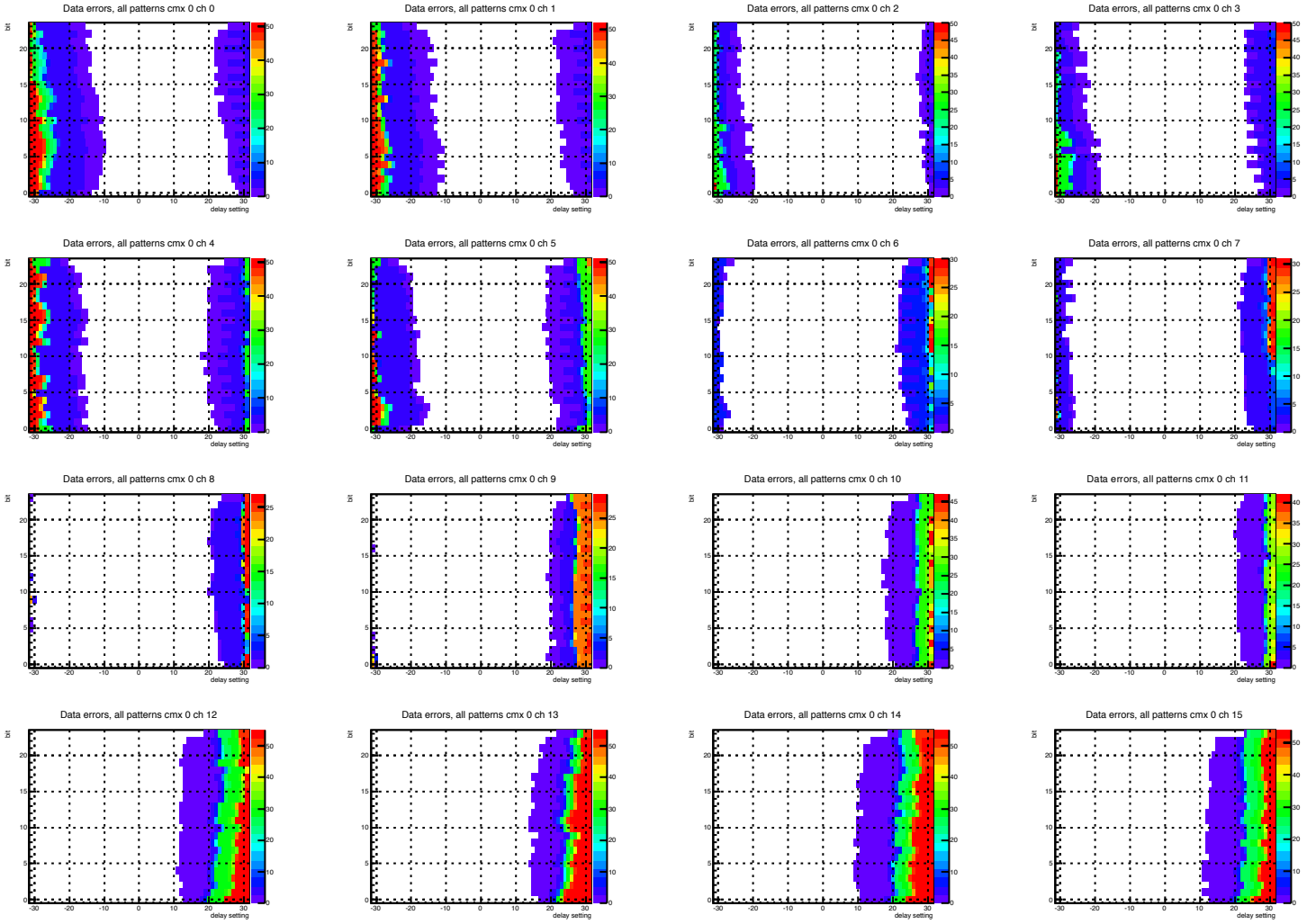
Run #2: CMX0, all patterns, 0.1s dwell time per scan point

Pretests timing scans JEMs



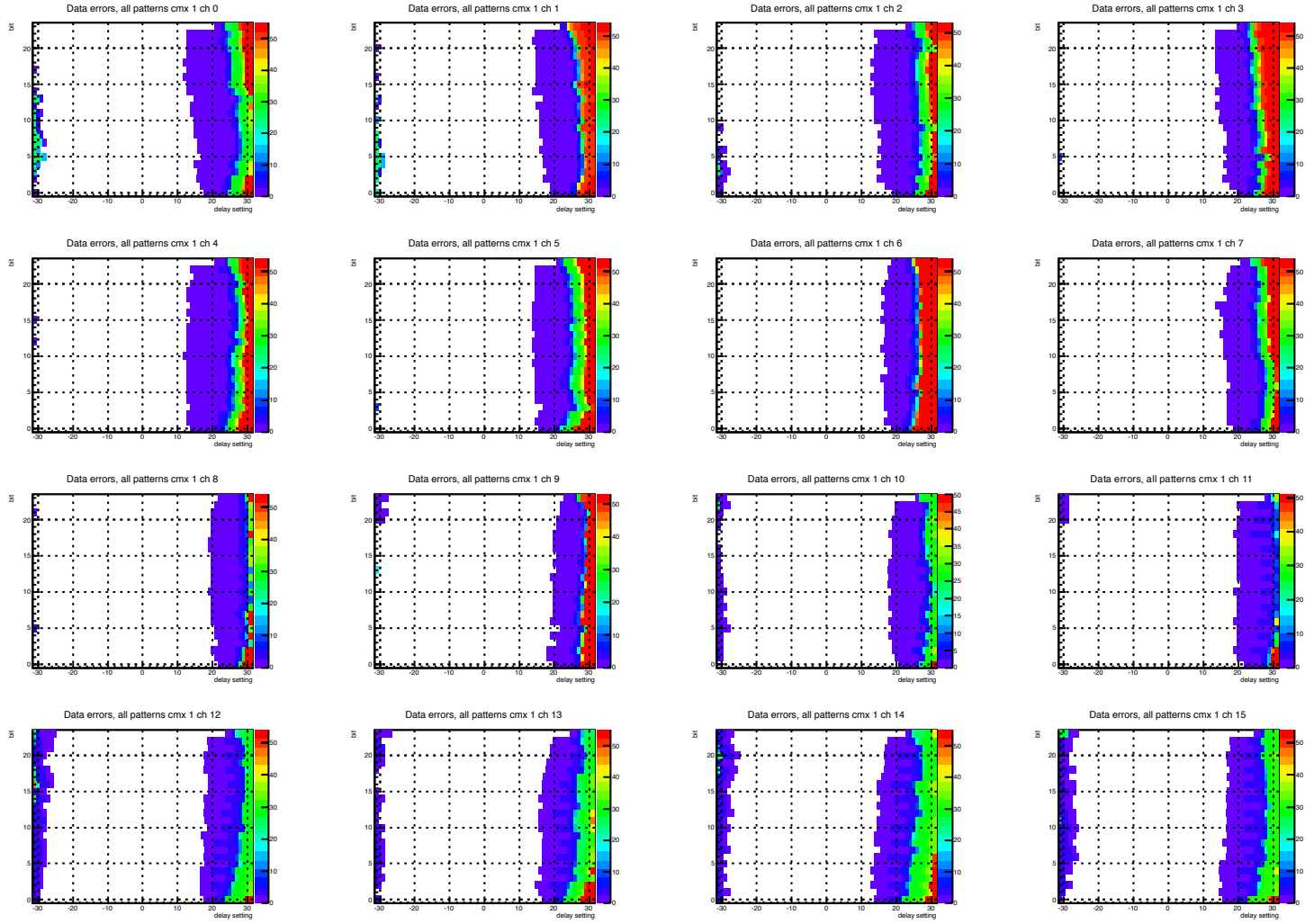
Run #2: CMX1, all patterns, 0.1s dwell time per scan point

Pretests timing scans JEMs



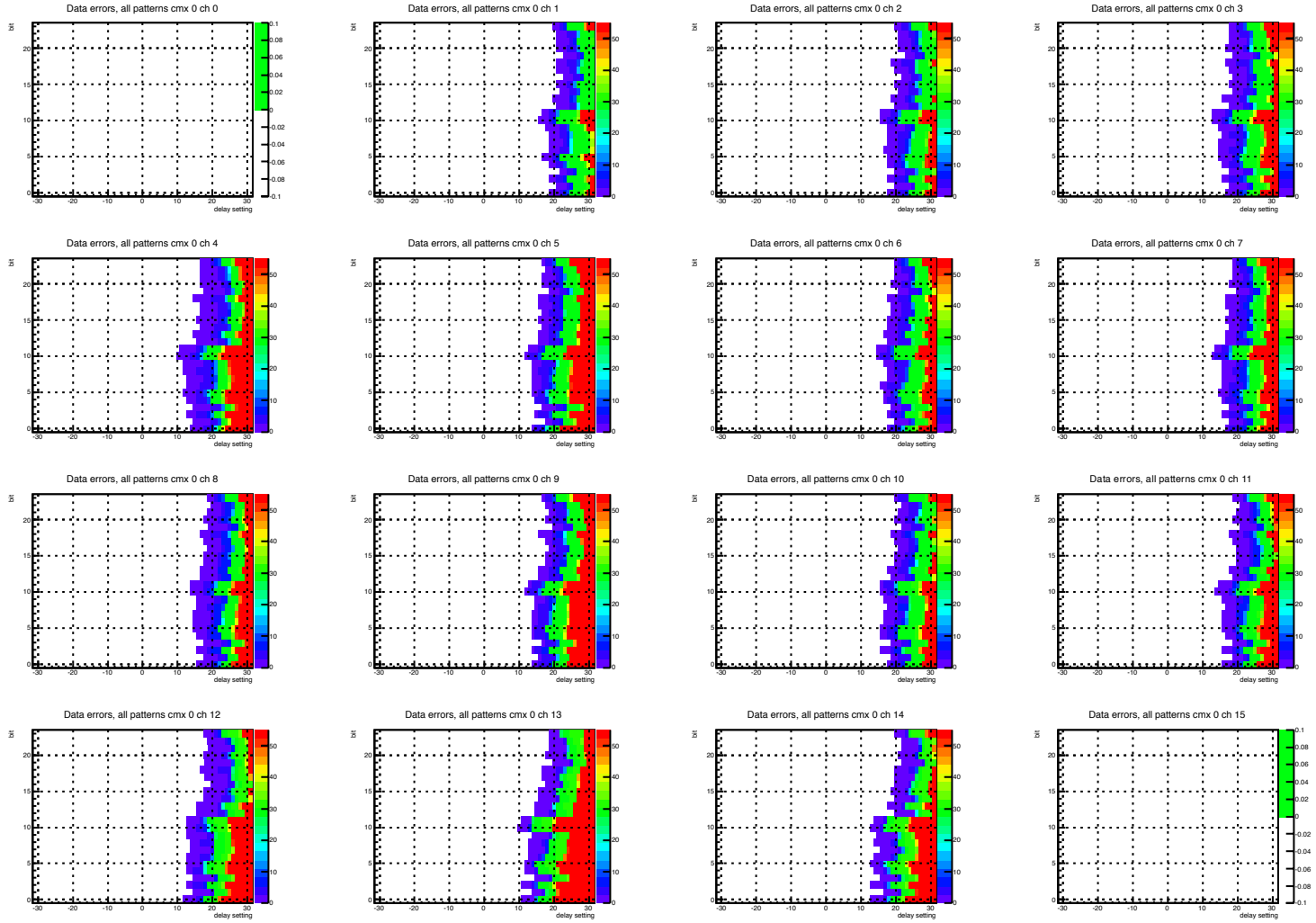
Run #3: CMX0, all patterns, 0.1s dwell time per scan point

Pretests timing scans JEMs



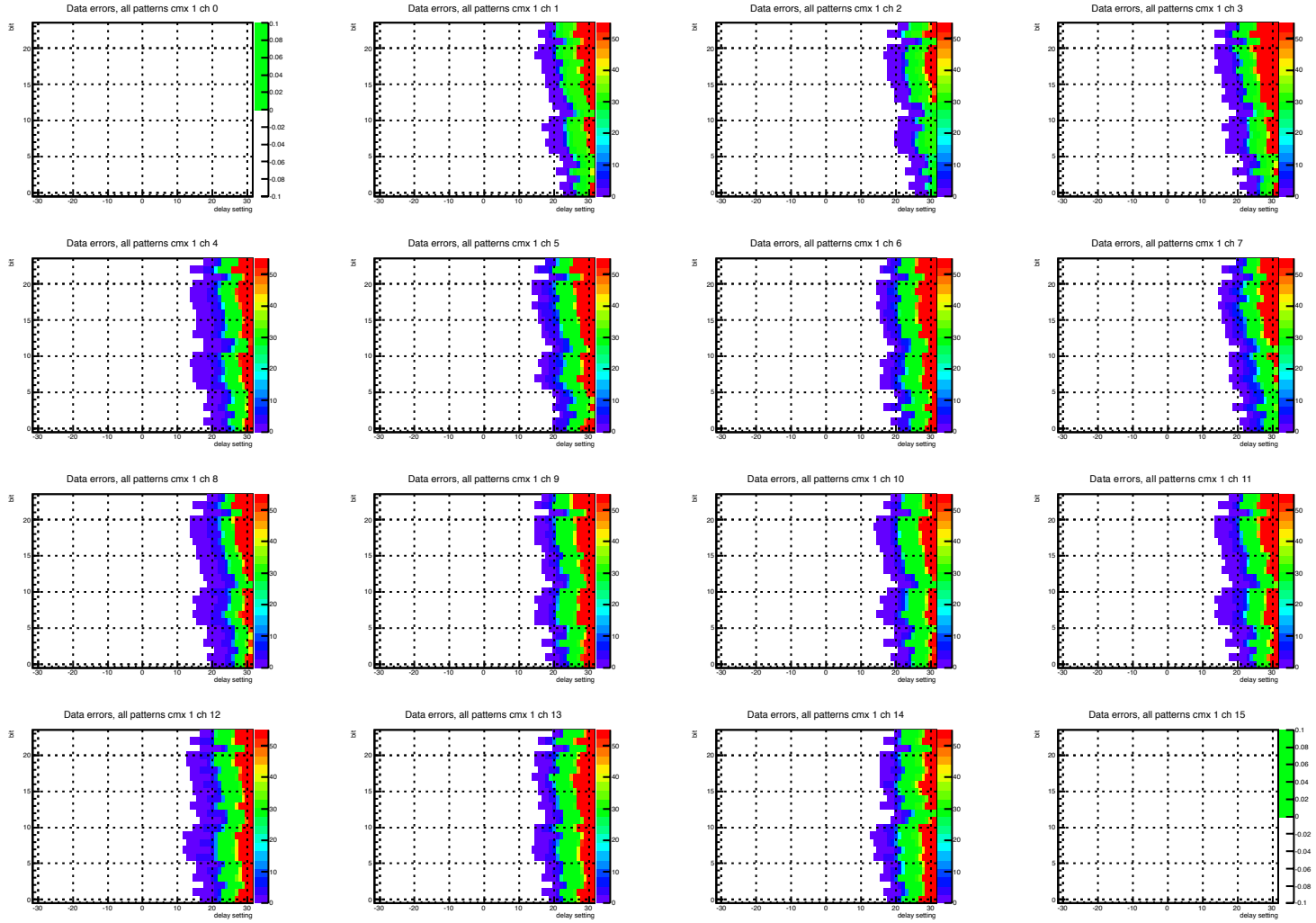
Run #3: CMX1, all patterns, 0.1s dwell time per scan point

Pretests timing scans CPMs



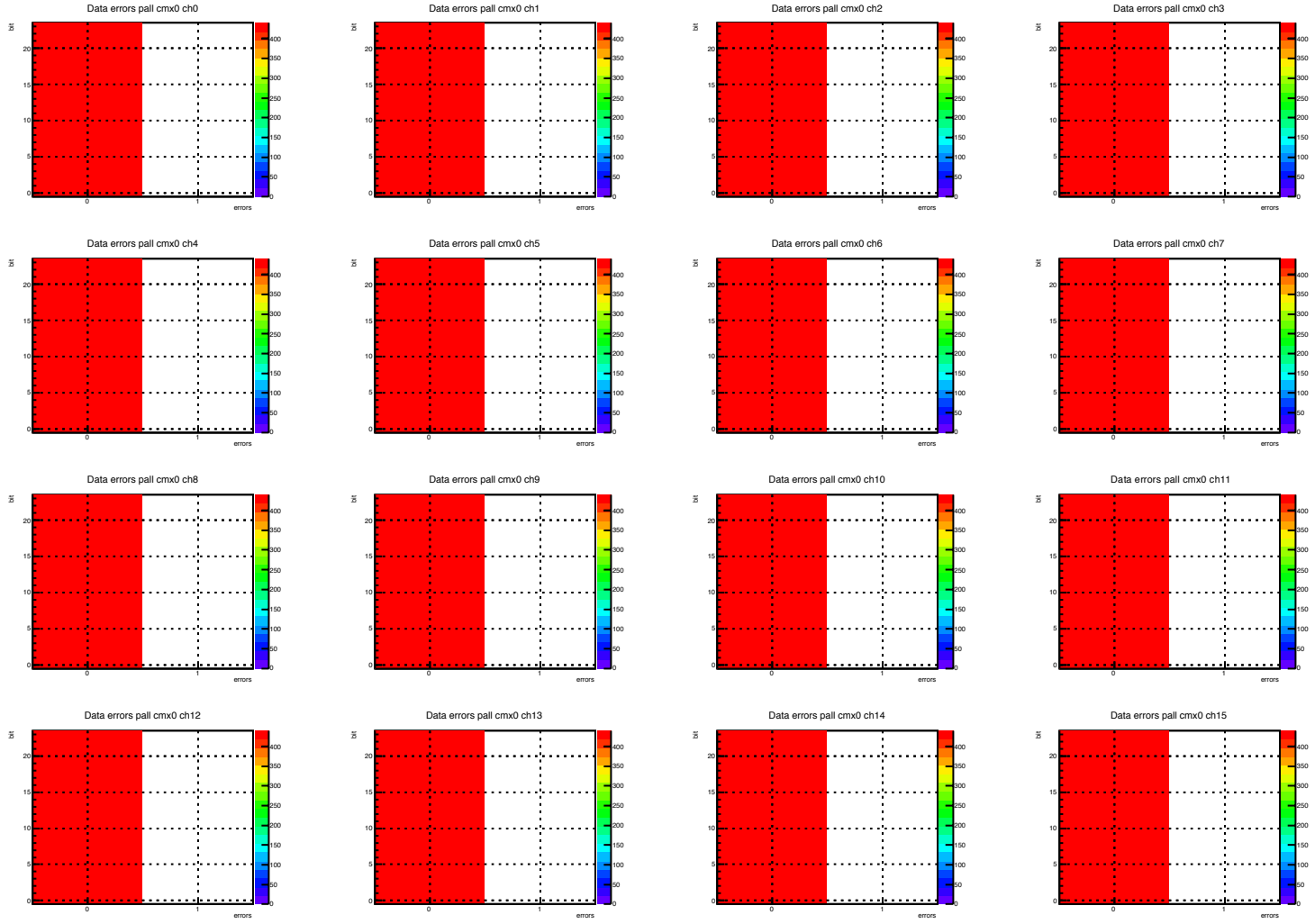
Run #1: CMX0, all patterns, 5s dwell time per scan point

Pretests timing scans CPMs



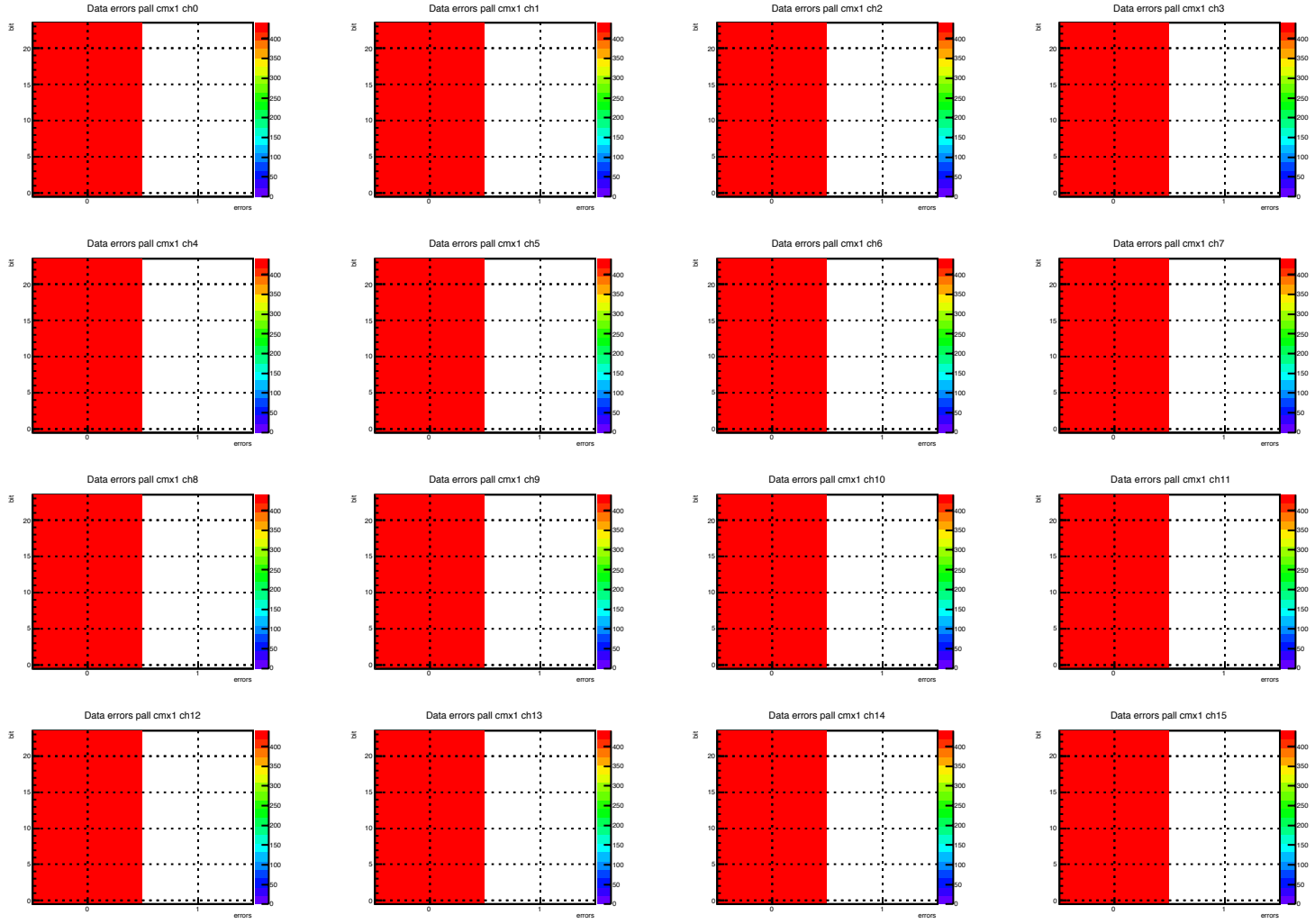
Run #1: CMX1, all patterns, 5s dwell time per scan point

Pretests long term CPMs



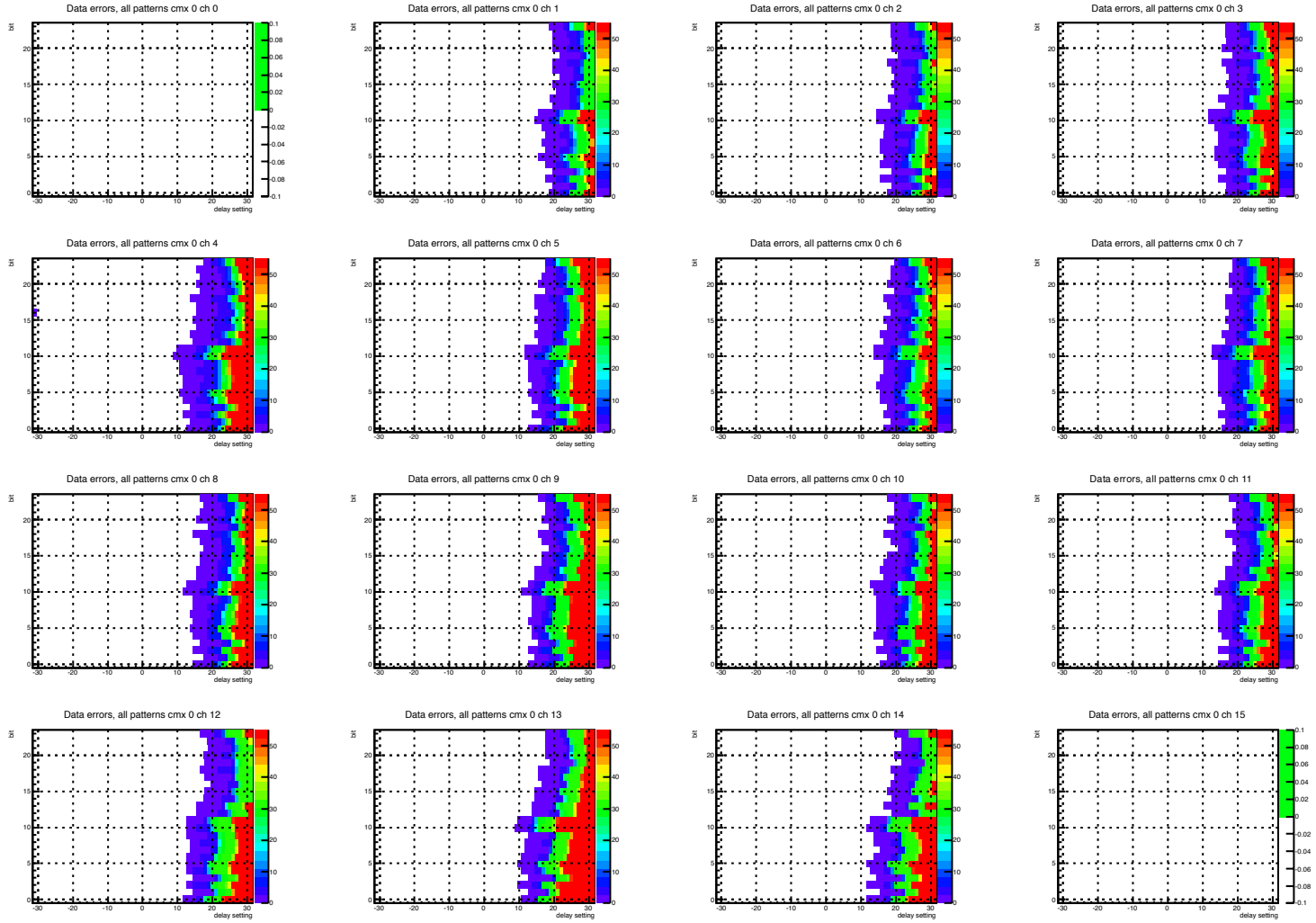
Run #2: CMX0, all patterns, 50s dwell time per scan point

Pretests long term CPMs



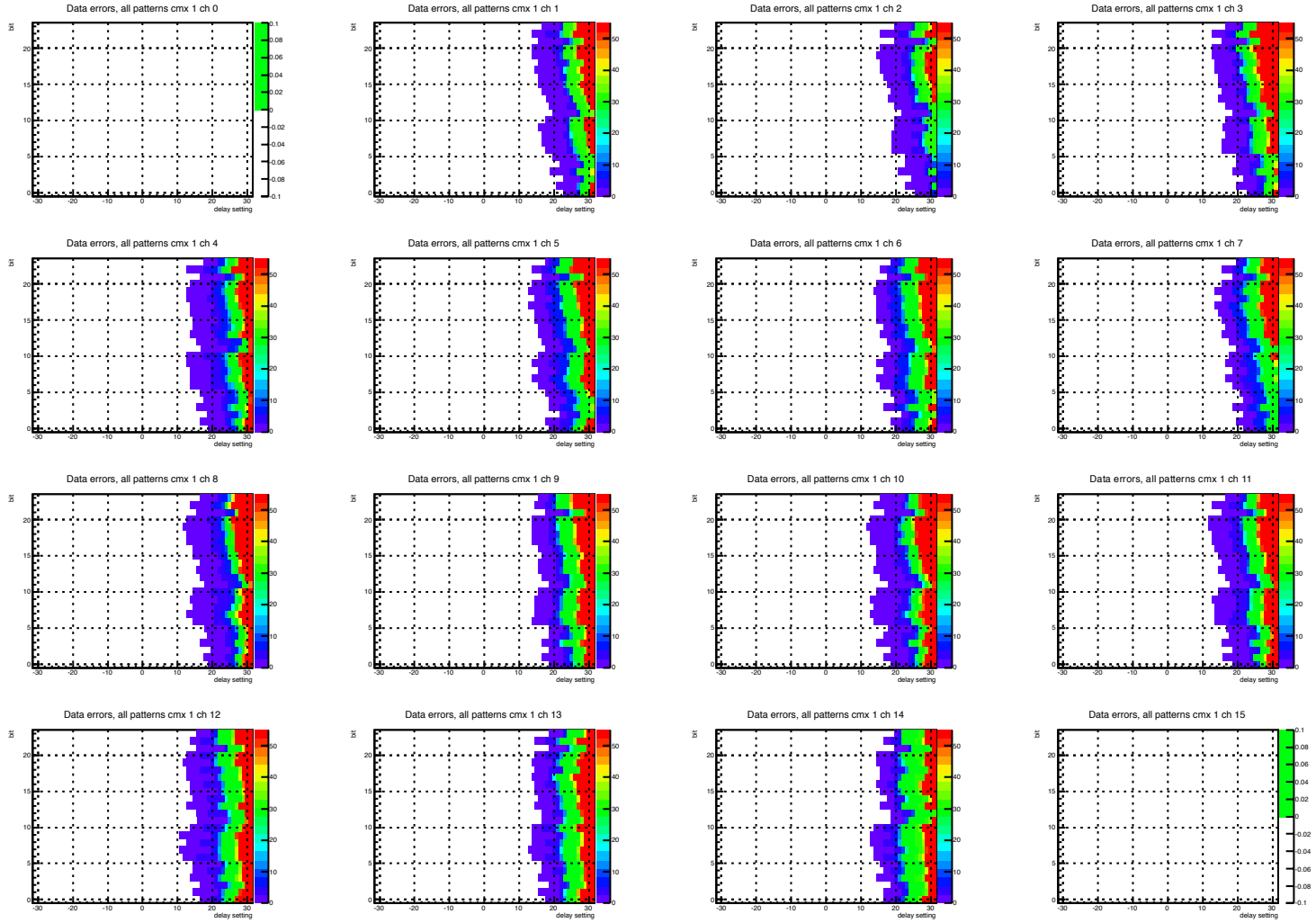
Run #2: CMX1, all patterns, 50s dwell time per scan point

Pretests timing scans CPMs



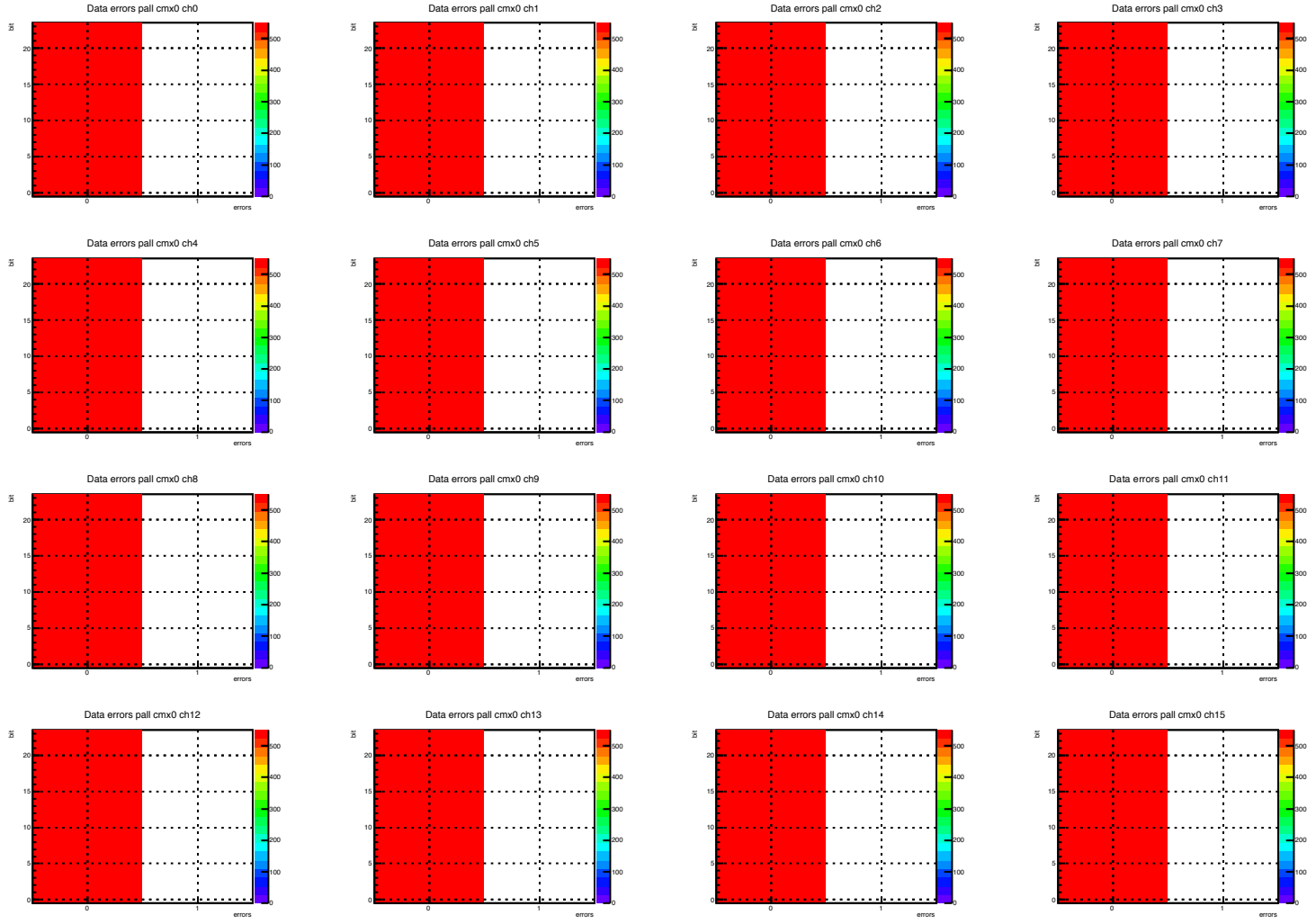
Run #3: CMX0, all patterns, 0.1s dwell time per scan point

Pretests timing scans CPMs



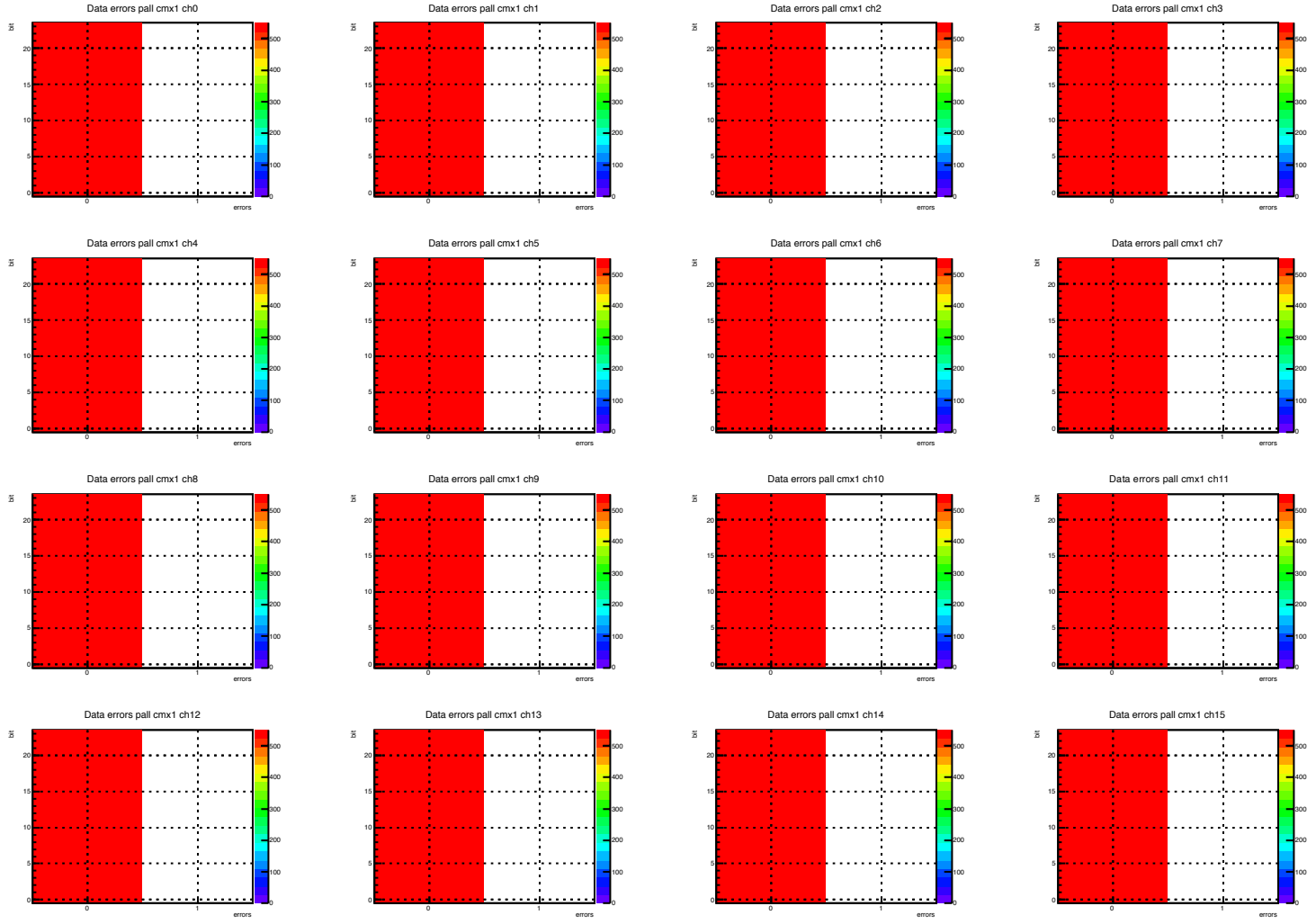
Run #3: CMX1, all patterns, 0.1s dwell time per scan point

Long term run JEMs



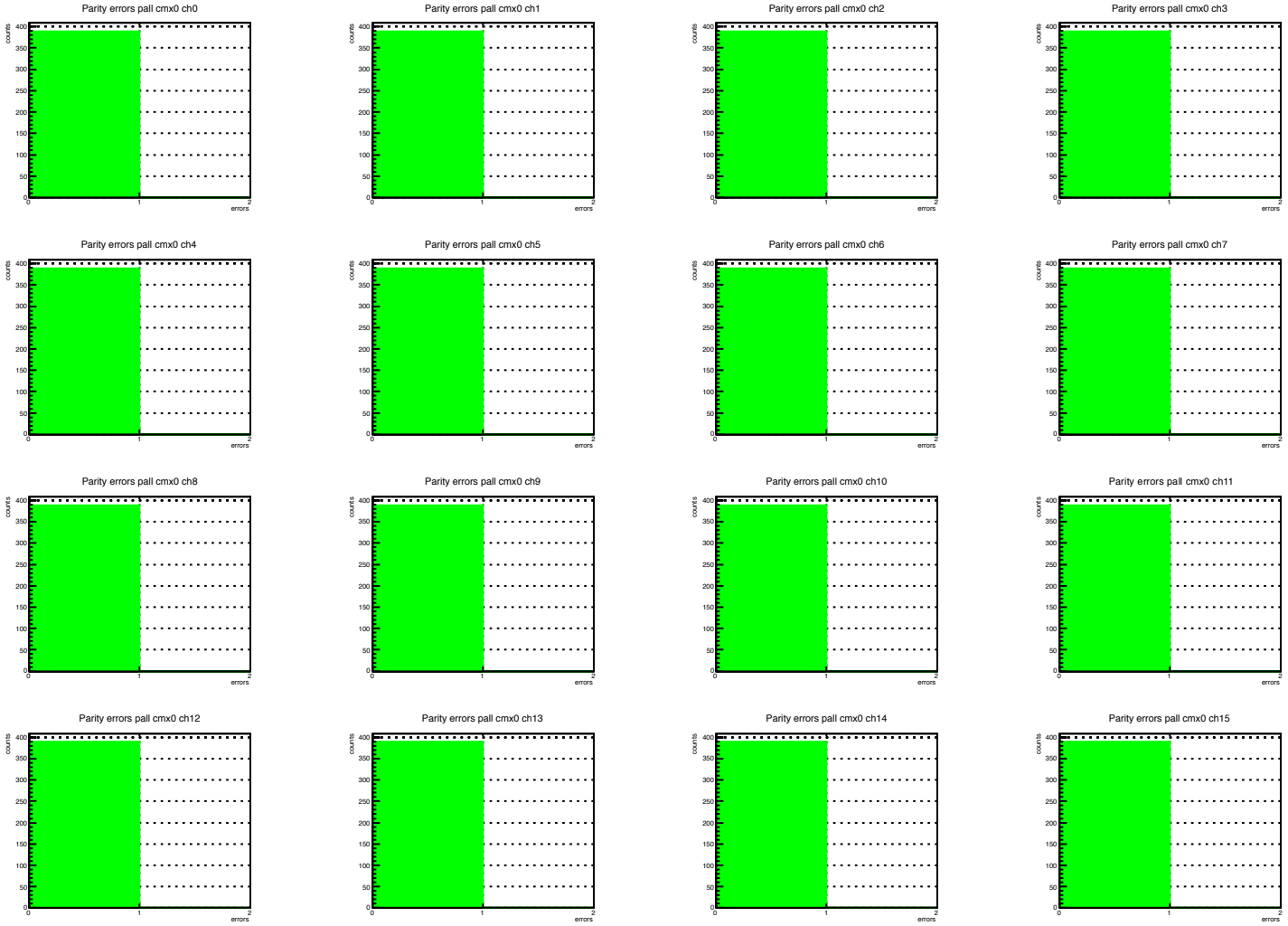
Run #5: CMX0, all patterns, 50s dwell time, 10 cycles at delay 0

Long term run JEMs



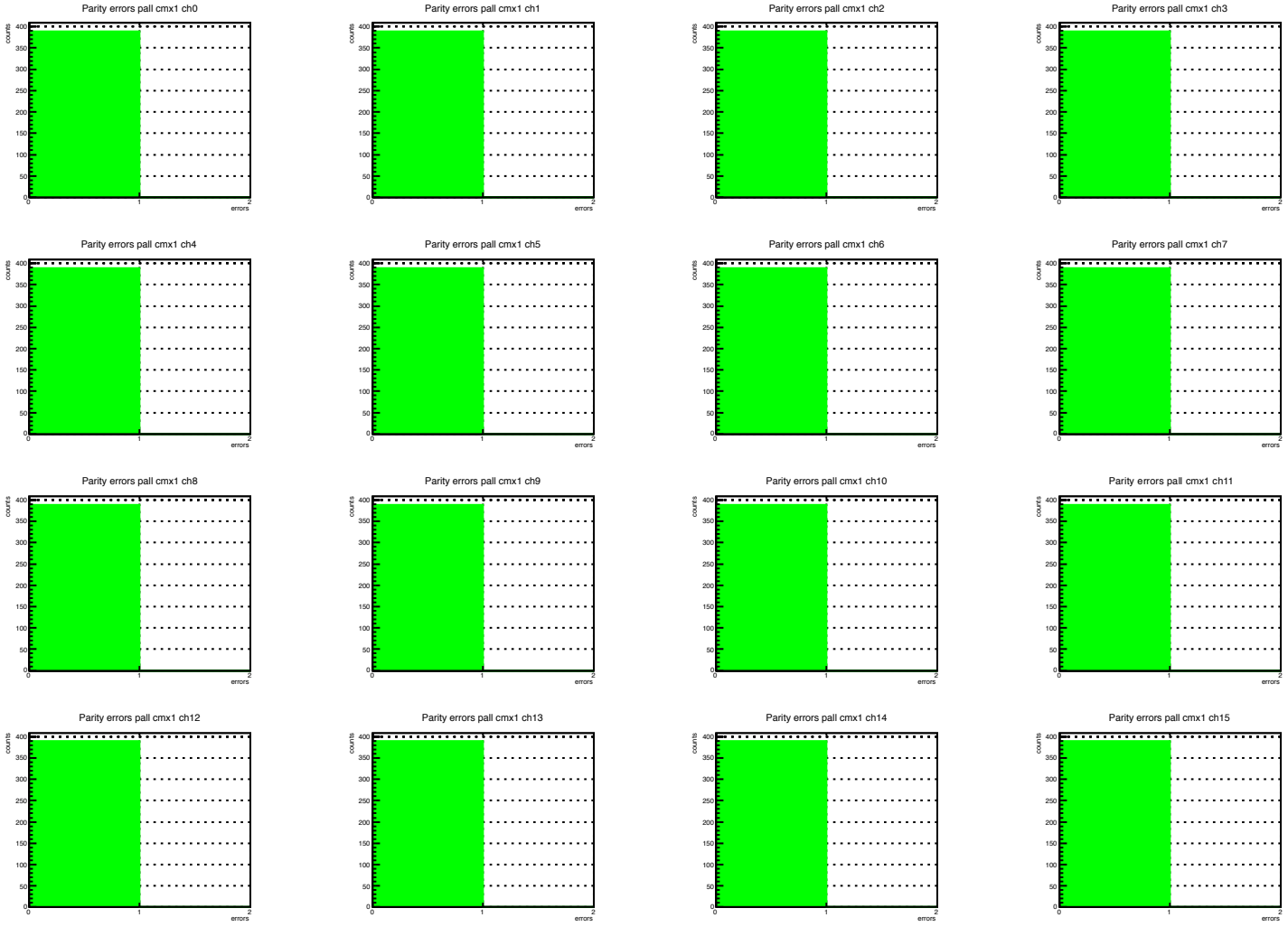
Run #5: CMX1, all patterns, 50s dwell time, 10 cycles at delay 0

Long term run JEMs



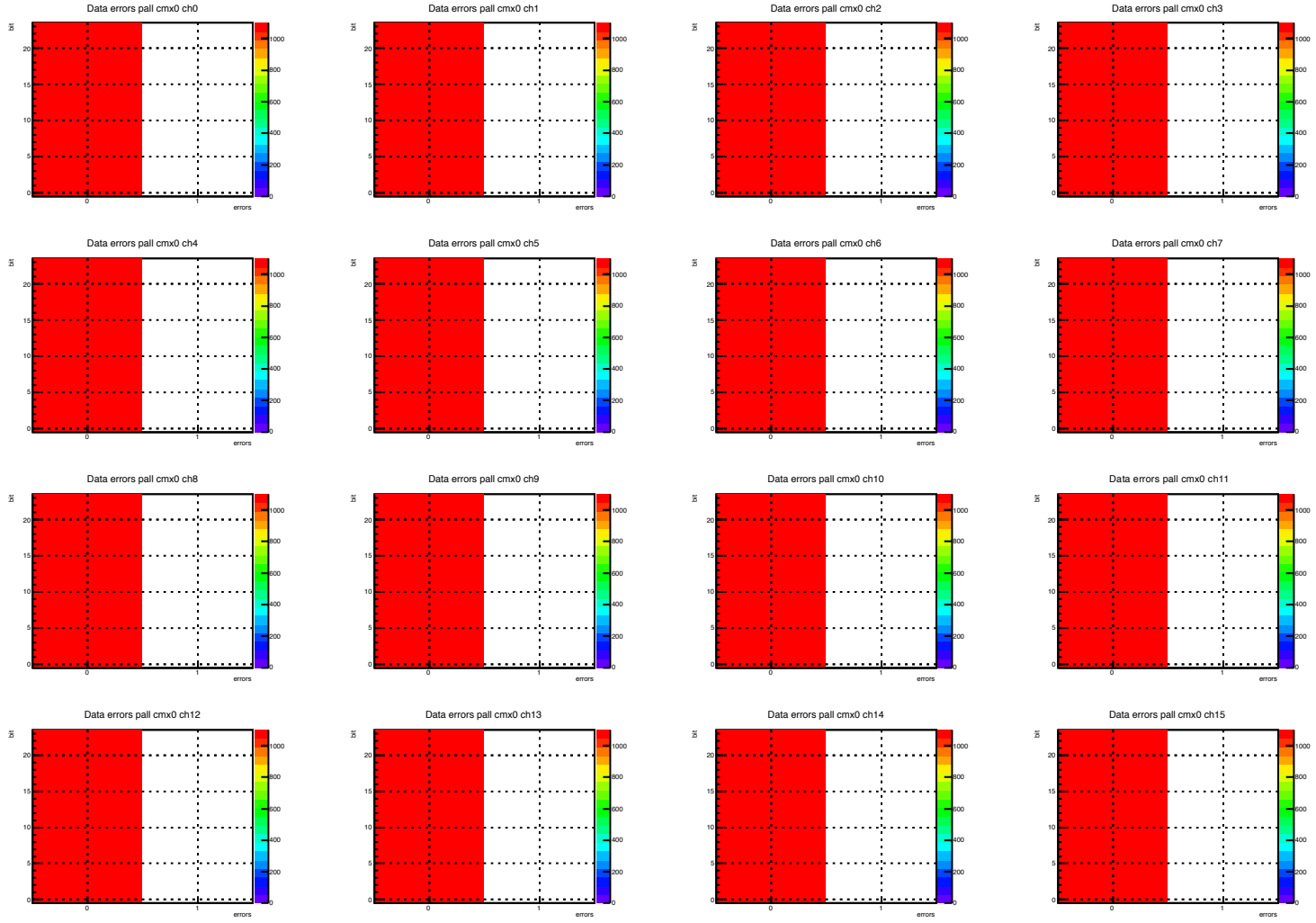
Run 7: CMX0, pseudo-random data, 50s dwell time, 384 cycles at delay 10

Long term run JEMs



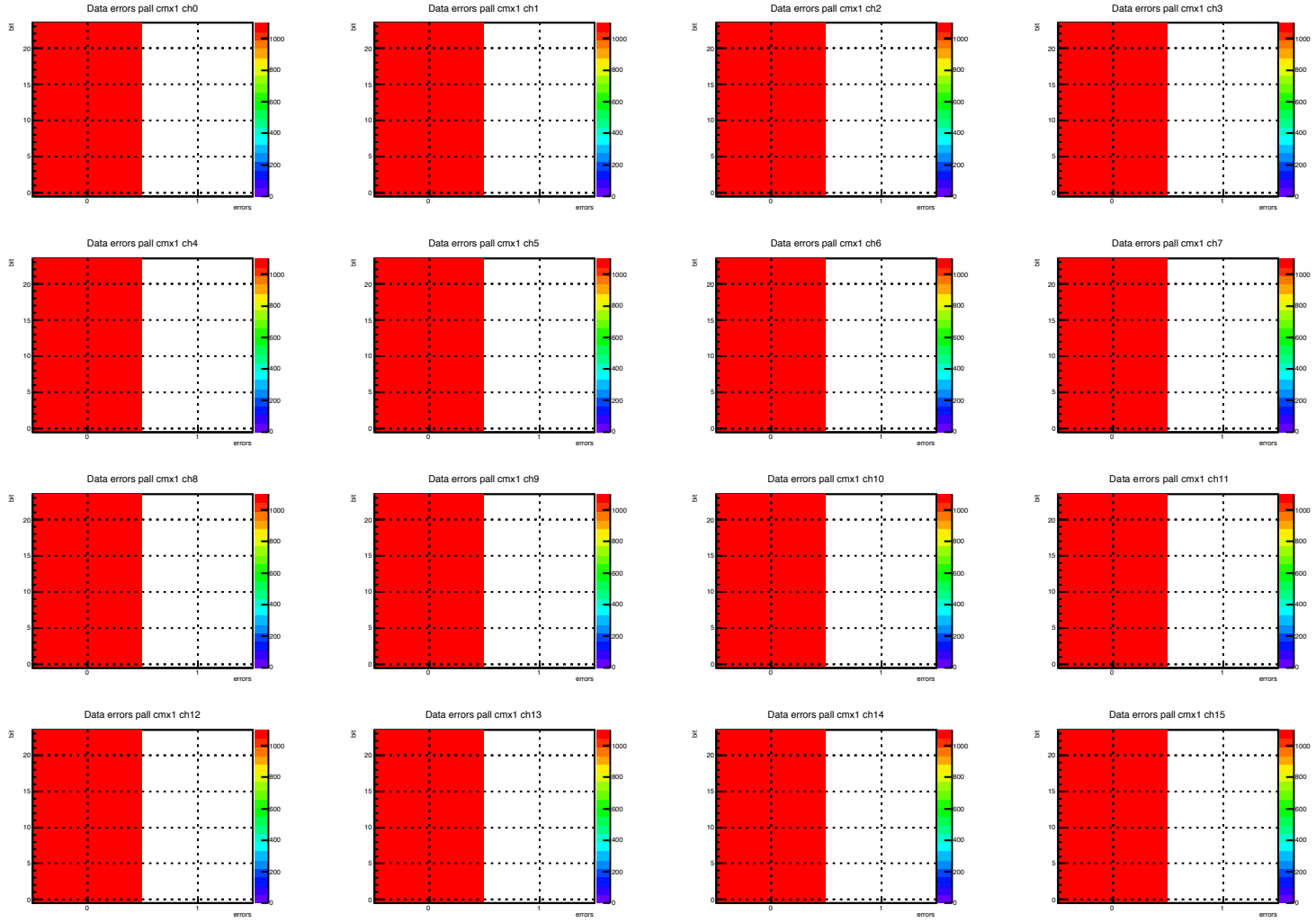
Run 7: CMX1, pseudo-random data, 50s dwell time, 384 cycles at delay 10

Long term run CPMs



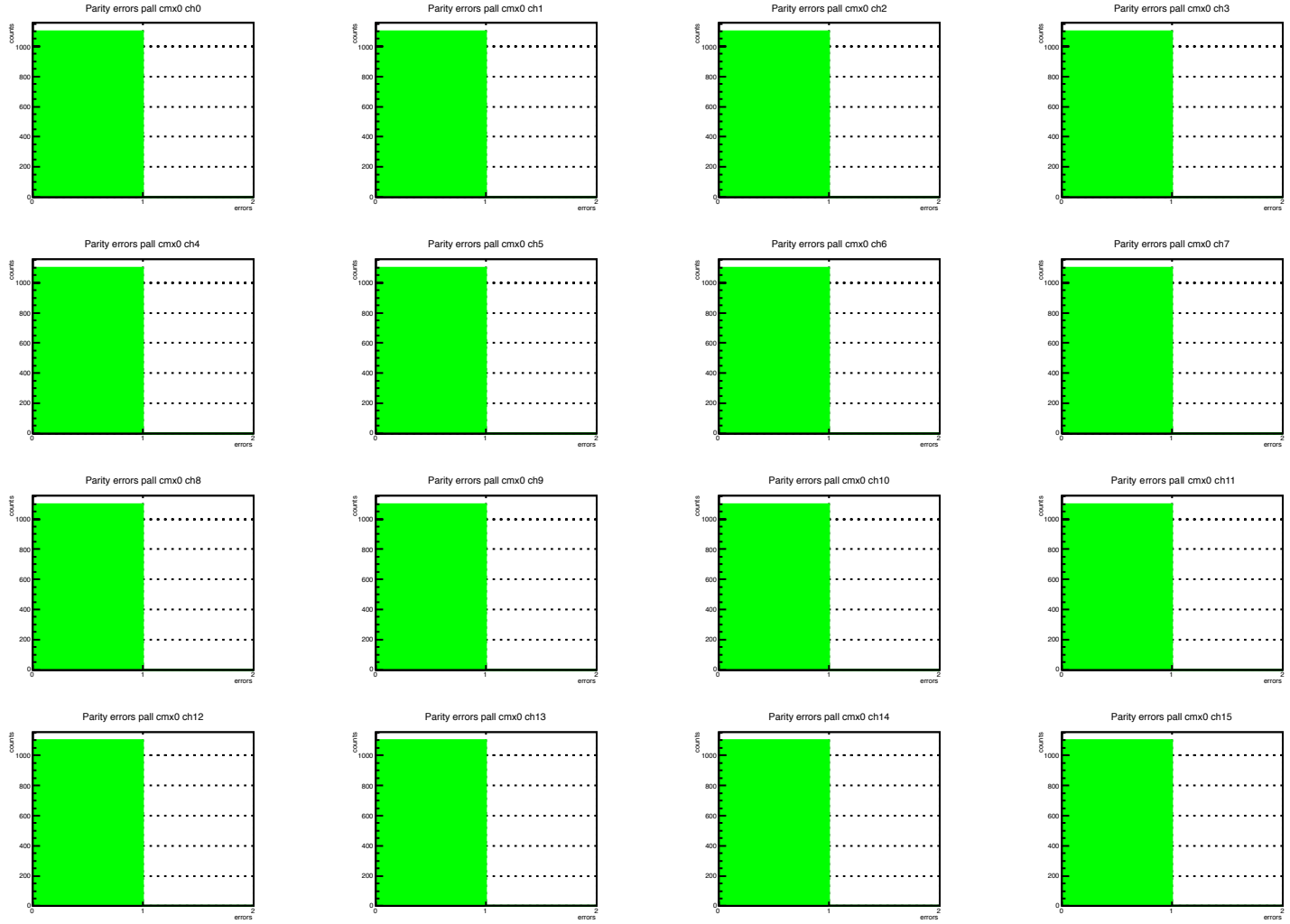
Run #5: CMX0, all patterns, 50s dwell time, 23 cycles at delay -10

Long term run CPMs



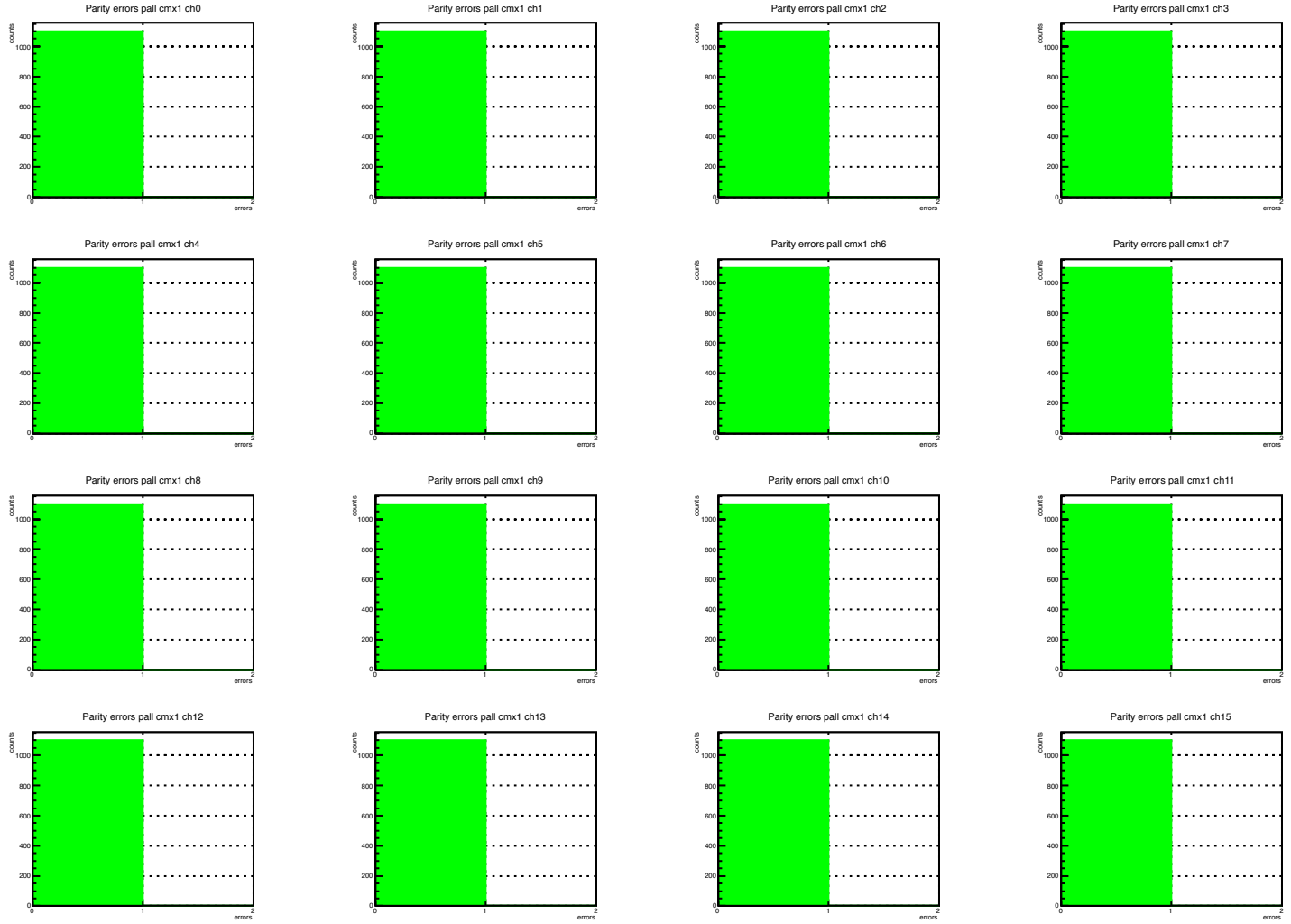
Run #5: CMX1, all patterns, 50s dwell time, 23 cycles at delay -10

Long term run CPMs



Run #7: CMX0, pseudo-random data, 50s dwell time, 1265 cycles at delay -10

Long term run CPMs



Run #7: CMX1, pseudo-random data, 50s dwell time, 1265 cycles at delay -10