



# Low speed optical links and G-Link protocol tests

*CMX project team*

- Background information
- LSO tests procedures and results
- G-Link tests procedures and results
- Conclusions

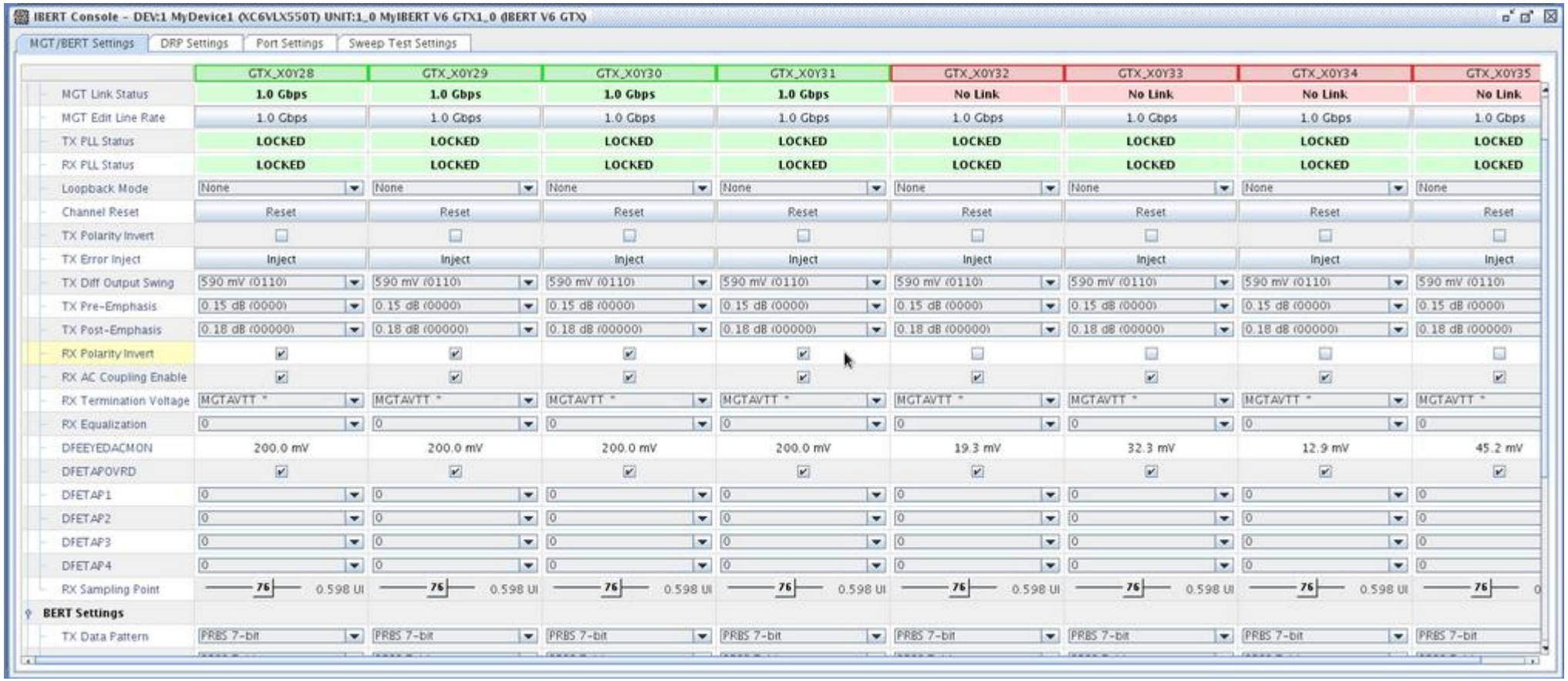
# Background information

- Low Speed Optical components are being used on the CMX to transmit the DAQ and ROI information from BF and TP.
- These components are labeled SFP1 though SFP4.
- CMX card does not use the HP G-Link to encode its ROI and DAQ information
- The required functionality of the HP G-Link is implemented by a combination of Virtex-6 FPGA resources and a GTX transmitter at 960 Mbit/s.

# LSO test procedures

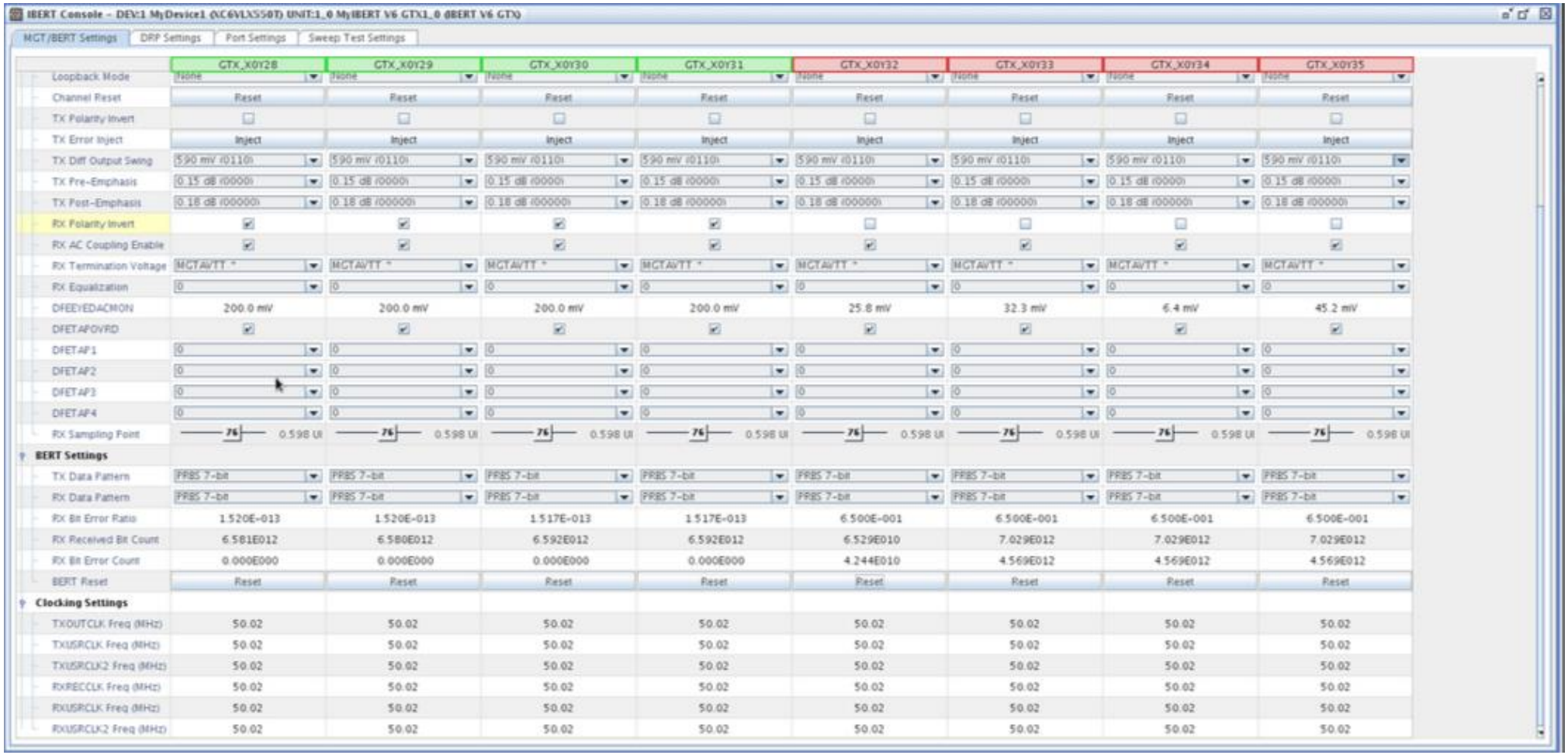
- Initial hardware tests were conducted with an Integrated Bit Error Ratio Tester (IBERT) core and Chipscope Pro Analyzer.
- In the current setup two transmitters connected to the TP FPGA send out the data to the two receivers on the BF while two transmitters connected to the BF send out data to the other two RX's on the BF FPGA.
- For this test the line rate was set to 1 Gbps.
- RX bit error ratio was found to be less than 1.5E-13.

# LSO test results




Screenshot of the Low Speed Optical components tests showing TX and RX PLL status.

# LSO tests results



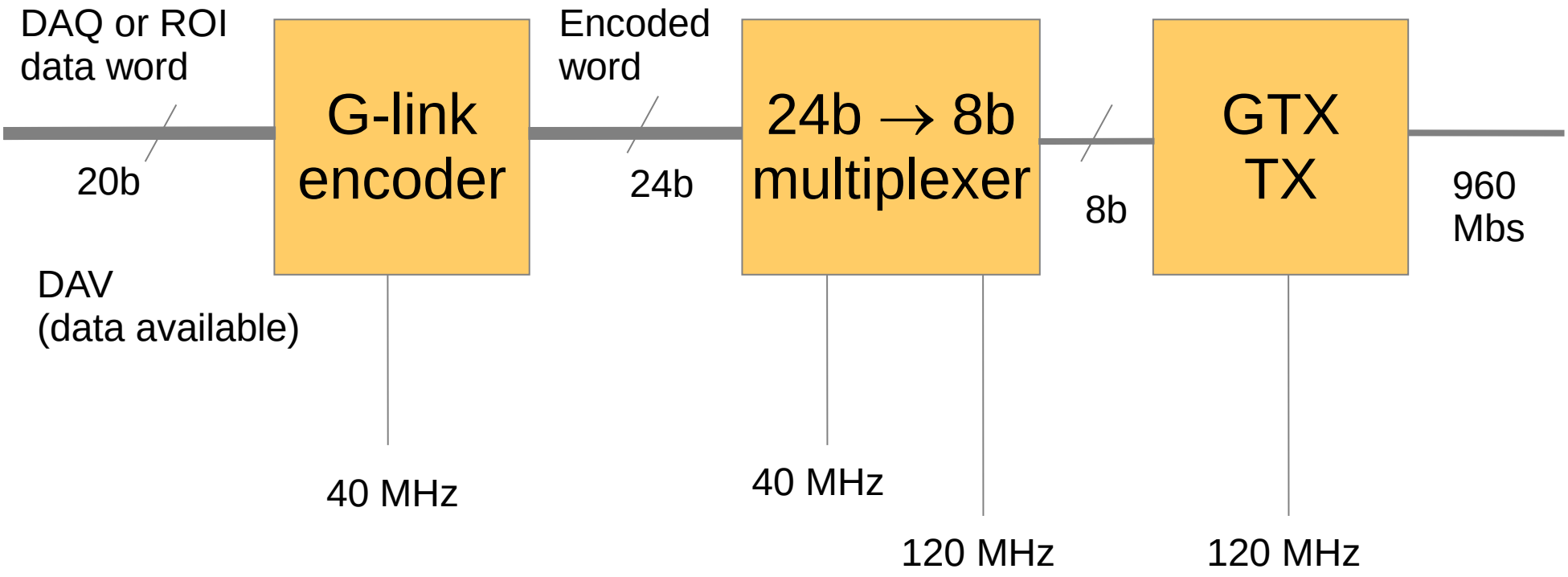

Screenshot of the Low Speed Optical components tests showing the BER information.

# G-Link test procedures

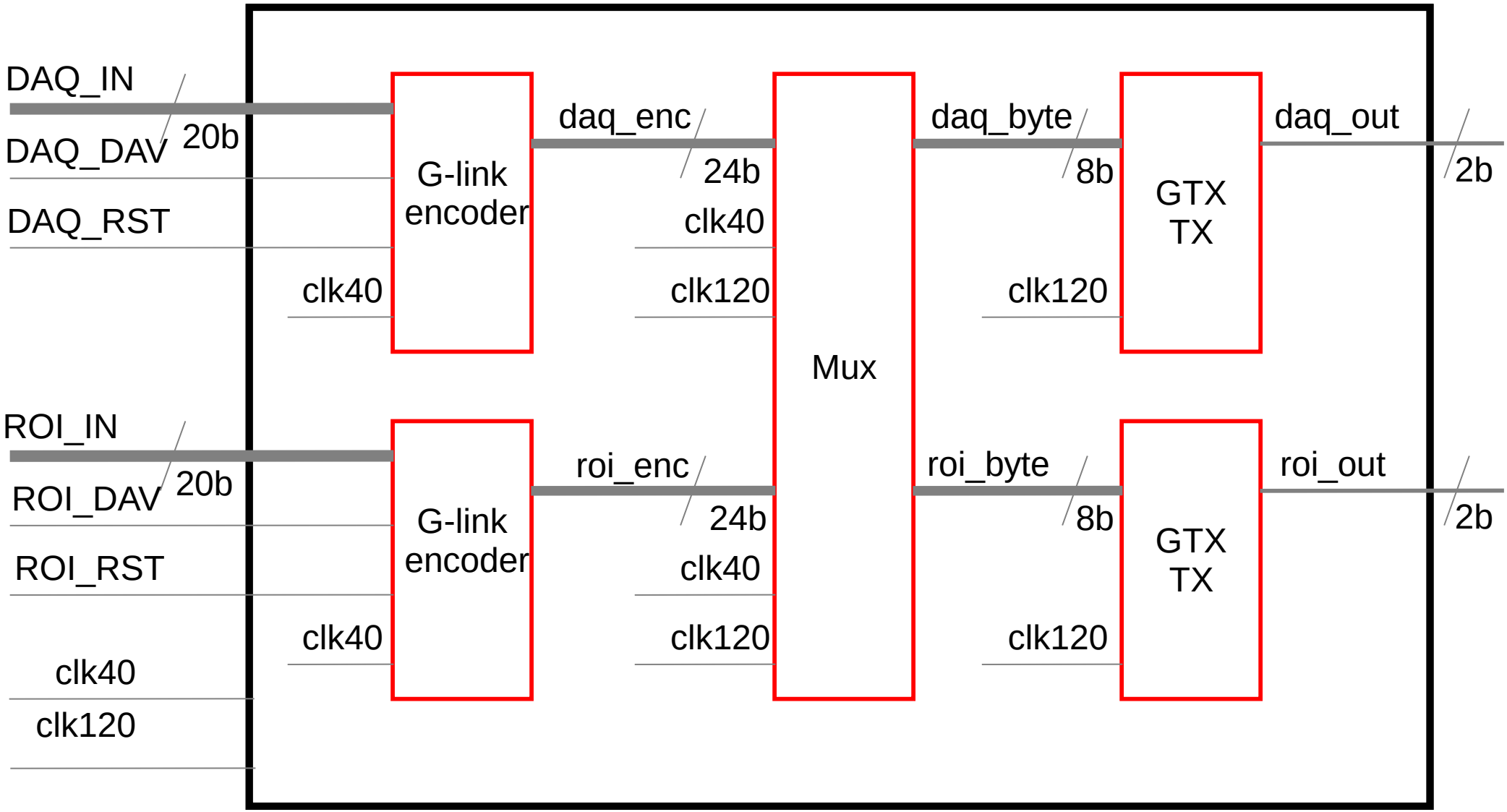
- Next step only concerns the G-Link emulation with the Virtex-6 ML605 evaluation board.

- The scope tests of the optical output (an eye diagram) executed with the evaluation board proved that there is no problem to emulate the G-Link protocol in FPGA.

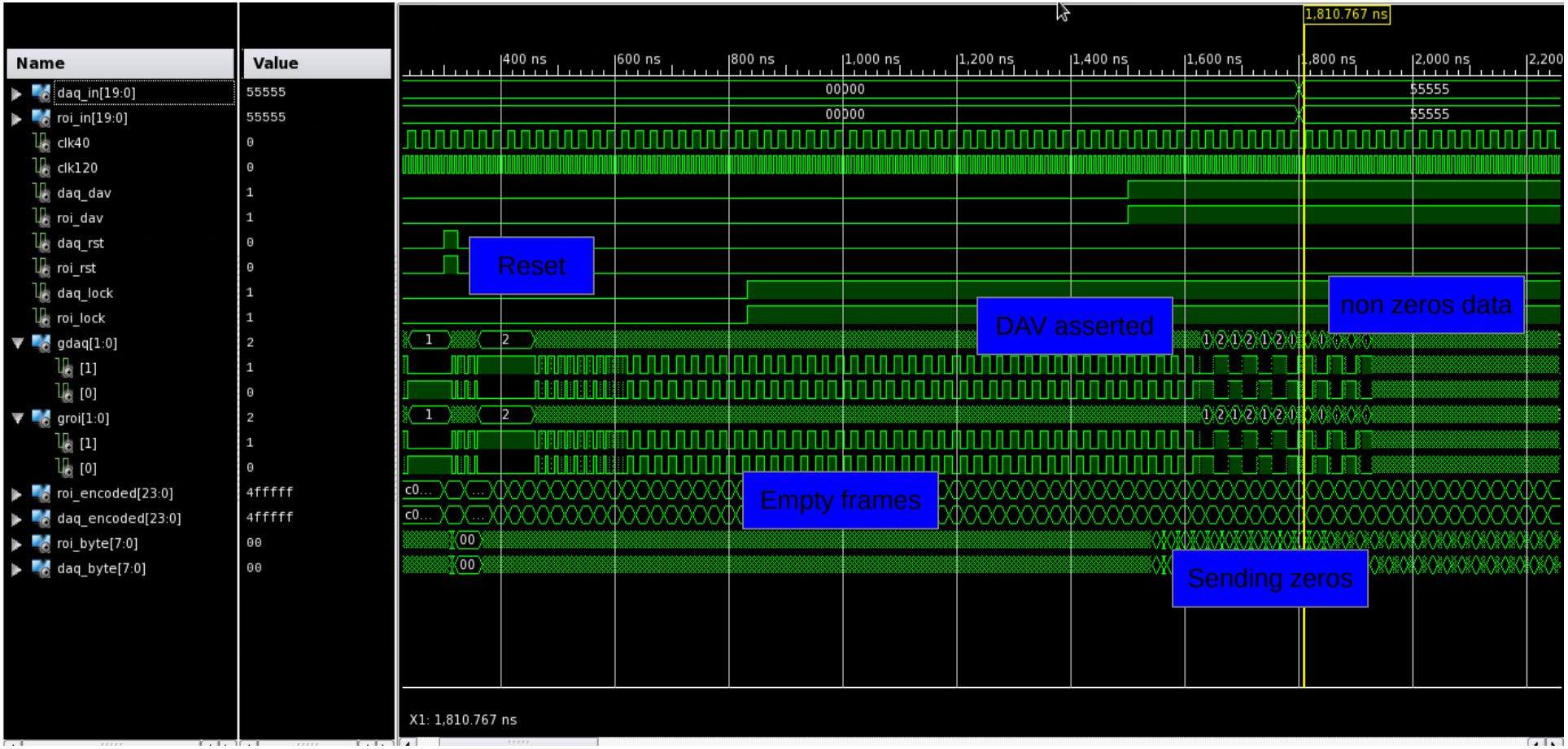
# G-link emulation in Virtex 6



# G-link emulation in Virtex-6
# The readout scheme



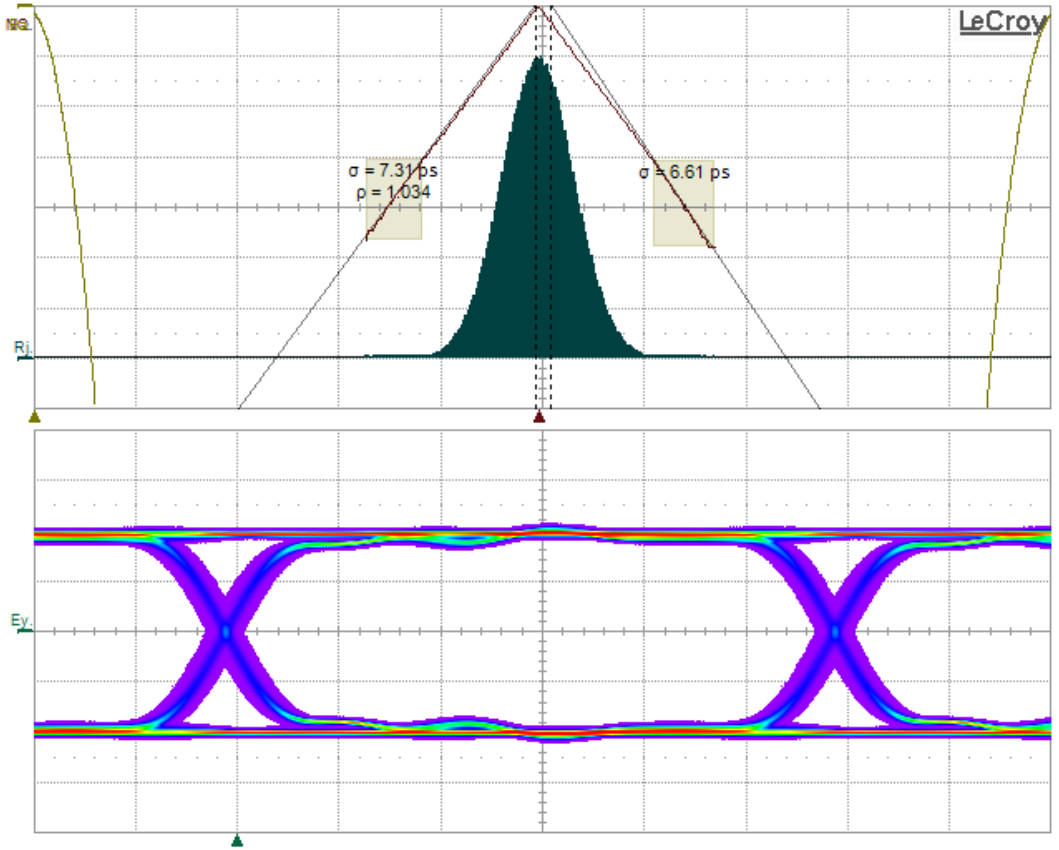
# G-link emulation in Virtex 6




Behavioral simulation results.

# G-link emulation in Virtex-6 “An eye diagram”

Scope tests of the optical output (target ML605):




Good result: Rise and Fall time below 240 psec!

# G-Link test procedures

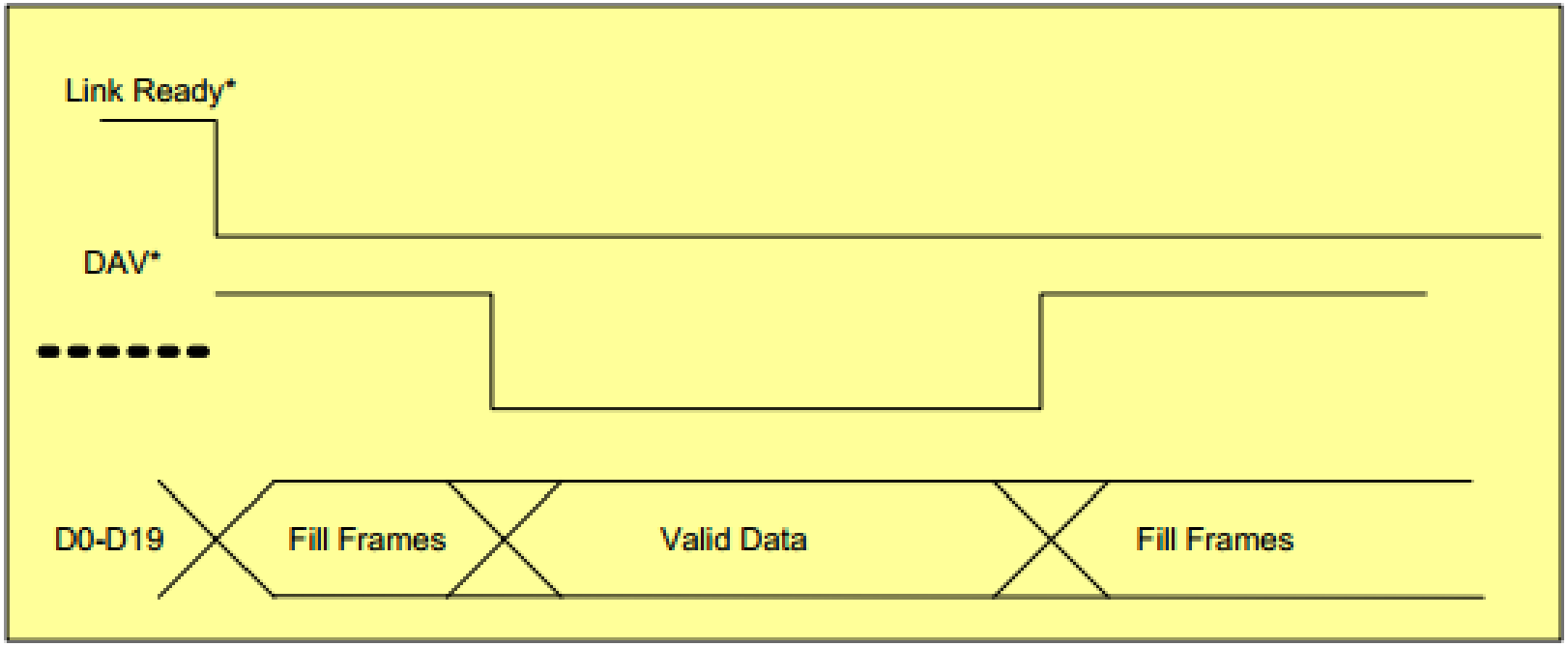
- Final step concerns the CMX G-Link communication tests.
- Hardware setup consists of the CMX and ROD card.
- Two LSO components were used to transmit the DAQ and ROI information to the ROD.
- CMX G-Link protocol, which encodes 20 bit of user data, was emulated in FPGA.
- ROD G-Link receiver recovers the user data from the serial data stream and it also checks the framing bits to verify the link stability.

# G-Link test procedures

- The final idea for the G-Link protocol tests:

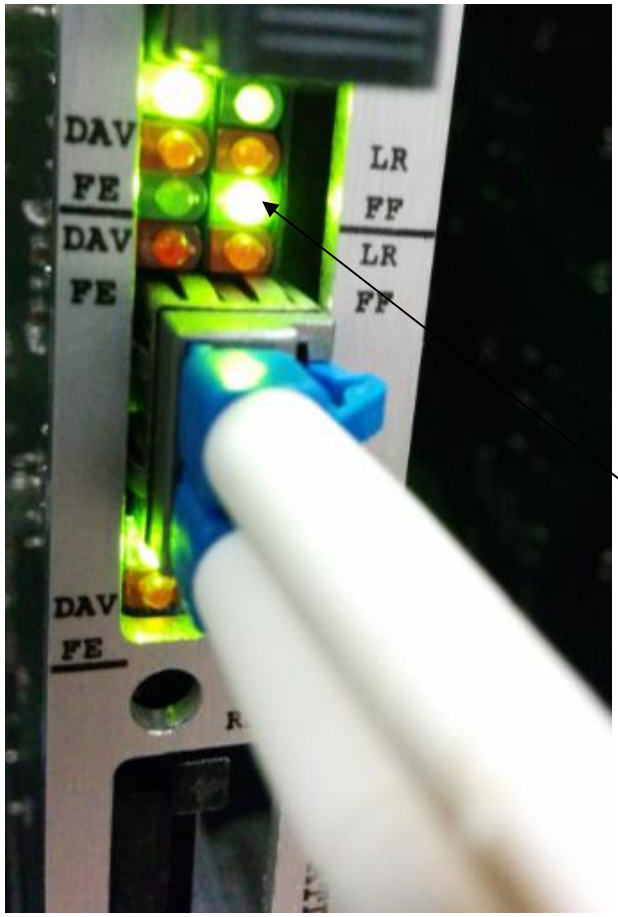
- On receipt of an L1A signal, the G-Link control firmware is obliged to extract data from its diagnostics component.
- The data is connected via a shift register to one of G-Link emulated user data pins.
- The internal logic moves the diagnostic data into the shift register and asserts the Data Available (DAV) signal to the G-Link logic.
- LSO components are being used to transmit the encoded data from G-Link to the RODs.
- An odd parity bit is appended to each G-Link line when the shift register contains have been transmitted.
- The logic de-asserts the DAV signal and the G-Link returns to its quiescent state for at least one clock.
- During the time period when there is no L1A signal, the CMX G-Link protocol transmits so-called fill frames.

# G-Link test procedures




Use of DAV signal to frame valid G-Link data (ROD card)

# G-Link test results




The ROD front panel. In the current test only the fill frames were transferred to the ROD and the lock between the transmitter and receiver was established.

# Conclusions

- The CMX LSO components tests were performed with an IBERT.
- Result is encouraging and indicates that the CMX LSO have capability to be used to transmit the DAQ and ROI information.
- The G-Link emulated protocol was implemented in FPGA.
- The CMX G-Link communication tests with the ROD are in progress. The first results are promising and indicate that the lock between the transmitters and receivers can be established.
- The G-Link protocol tests will be continued.