

MICHIGAN STATE
UNIVERSITY

TileFOX_E Construction

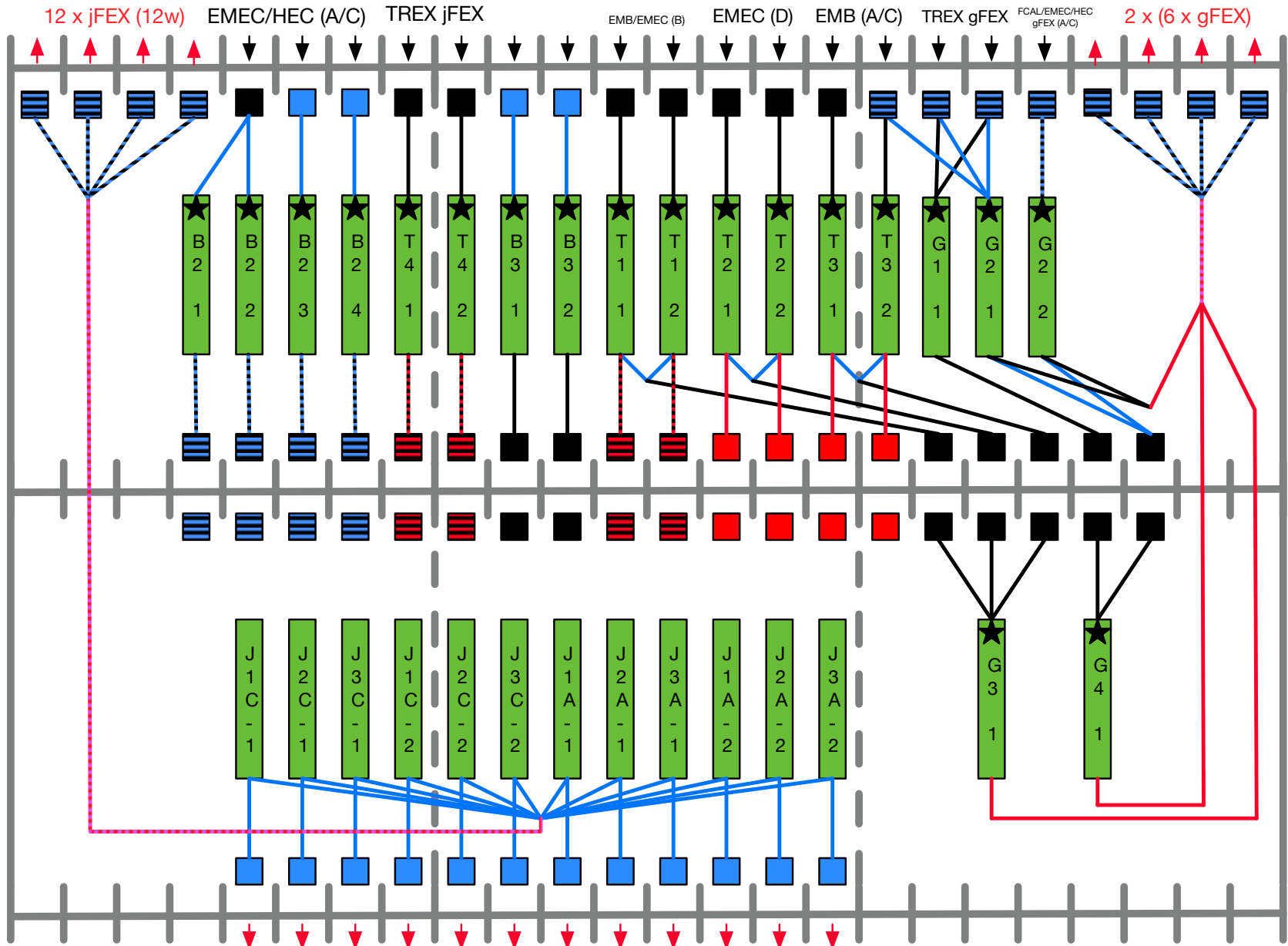
FOX

3rd - 7th July 2019

Daniel Hayden
daniel.hayden@cern.ch



F



TileFOX E

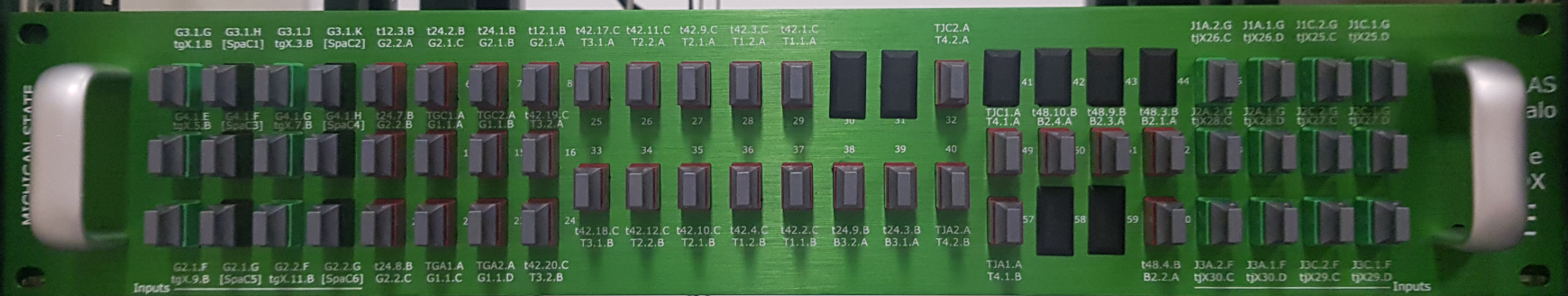
Key

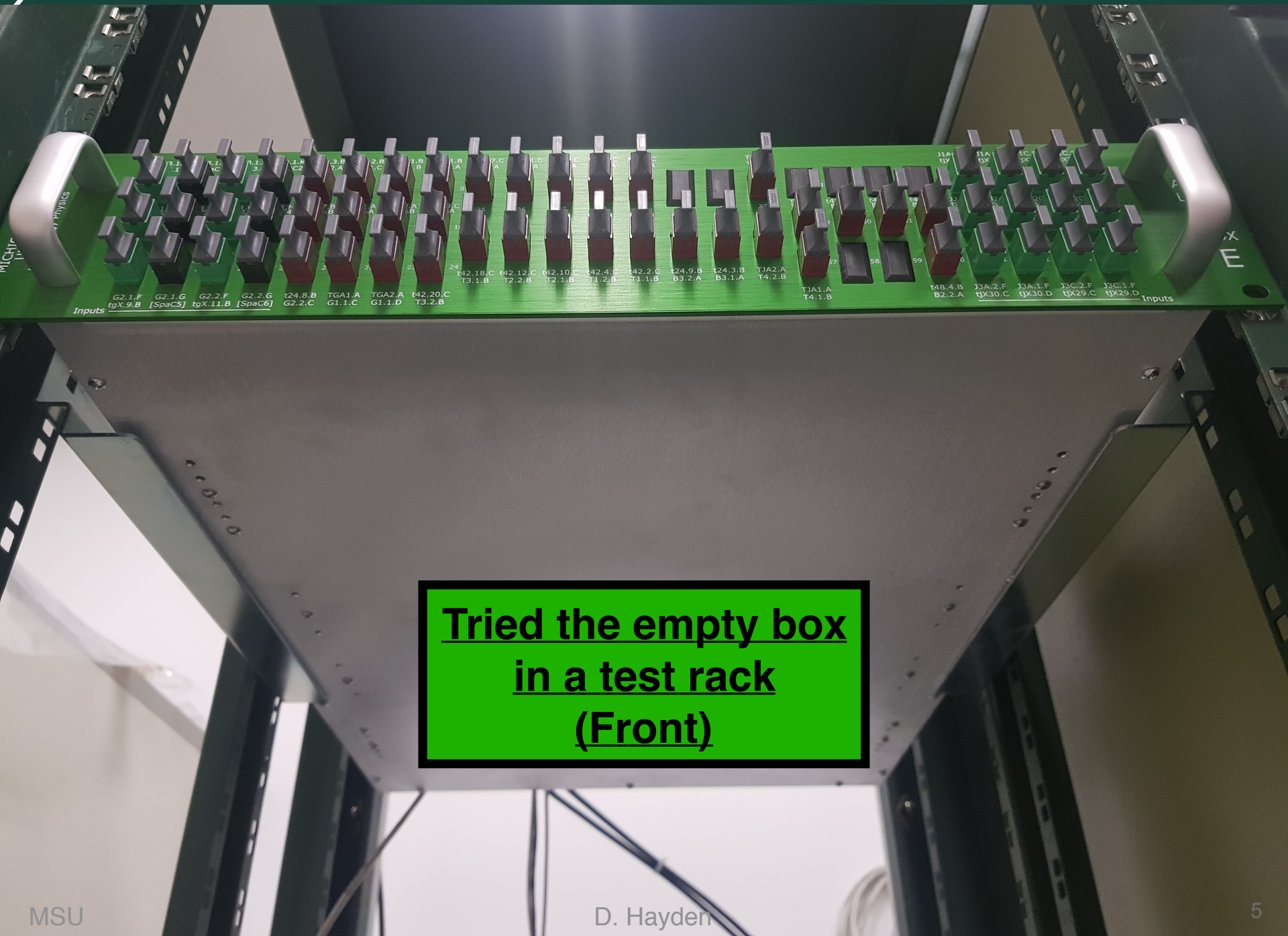
- x1
- x2
- x4
- x8
- x16
- Shuffle Box
- Short Side
- Input/Output

B

12 x jFEX (48w)

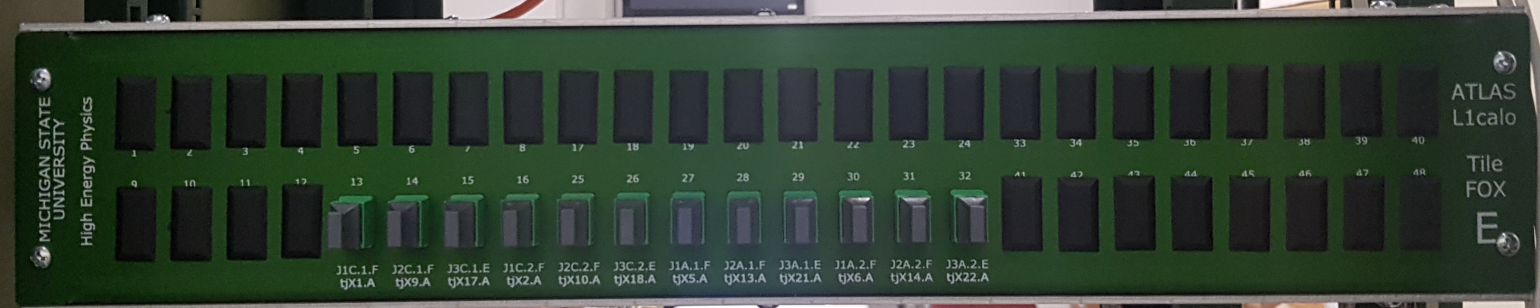
**Tried the empty box
in a test rack
(Front)**





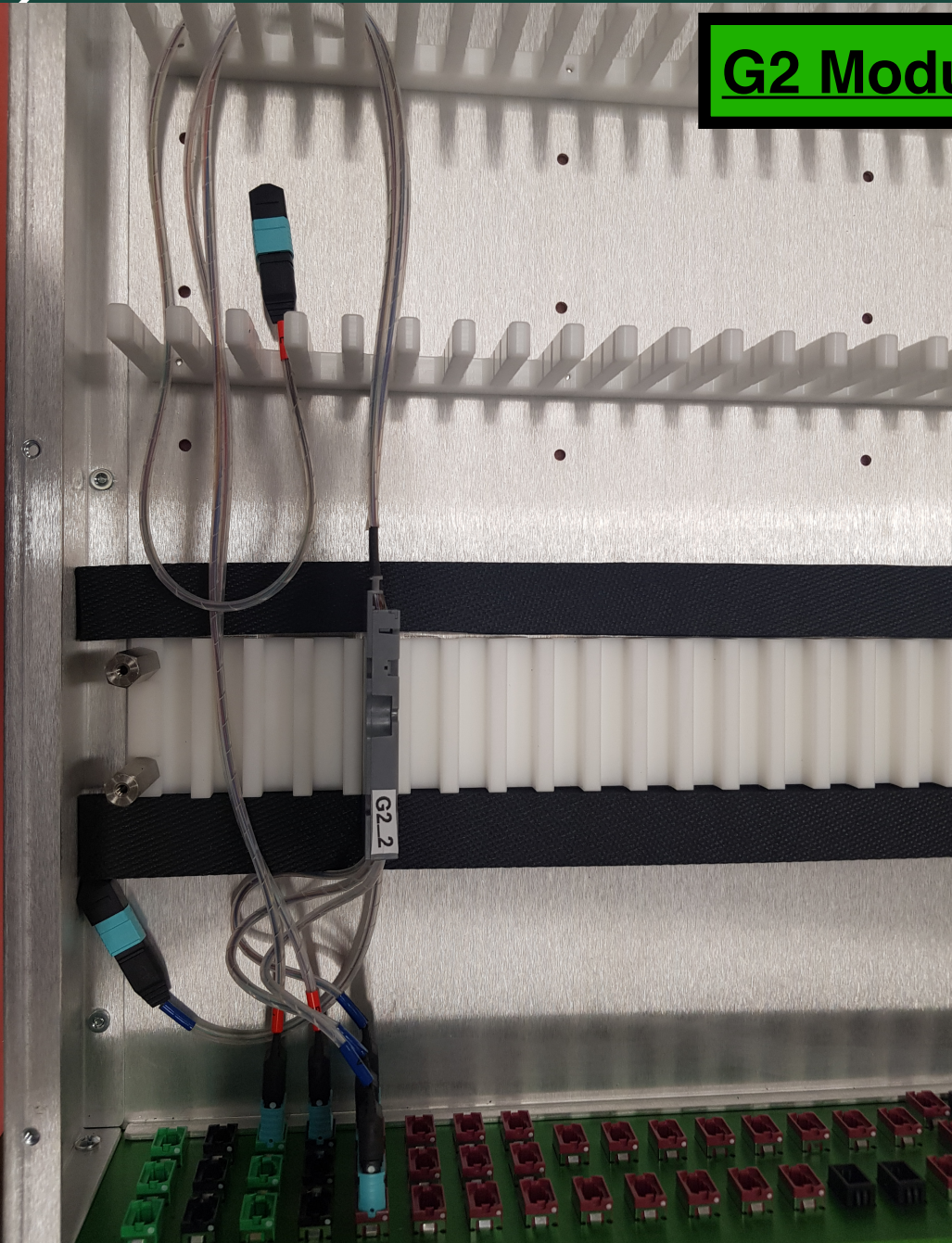
Tried the empty box
in a test rack
(Front)

**Tried the empty box
in a test rack
(Back)**



**Tried the empty box
in a test rack
(Side)**

G2 Modules



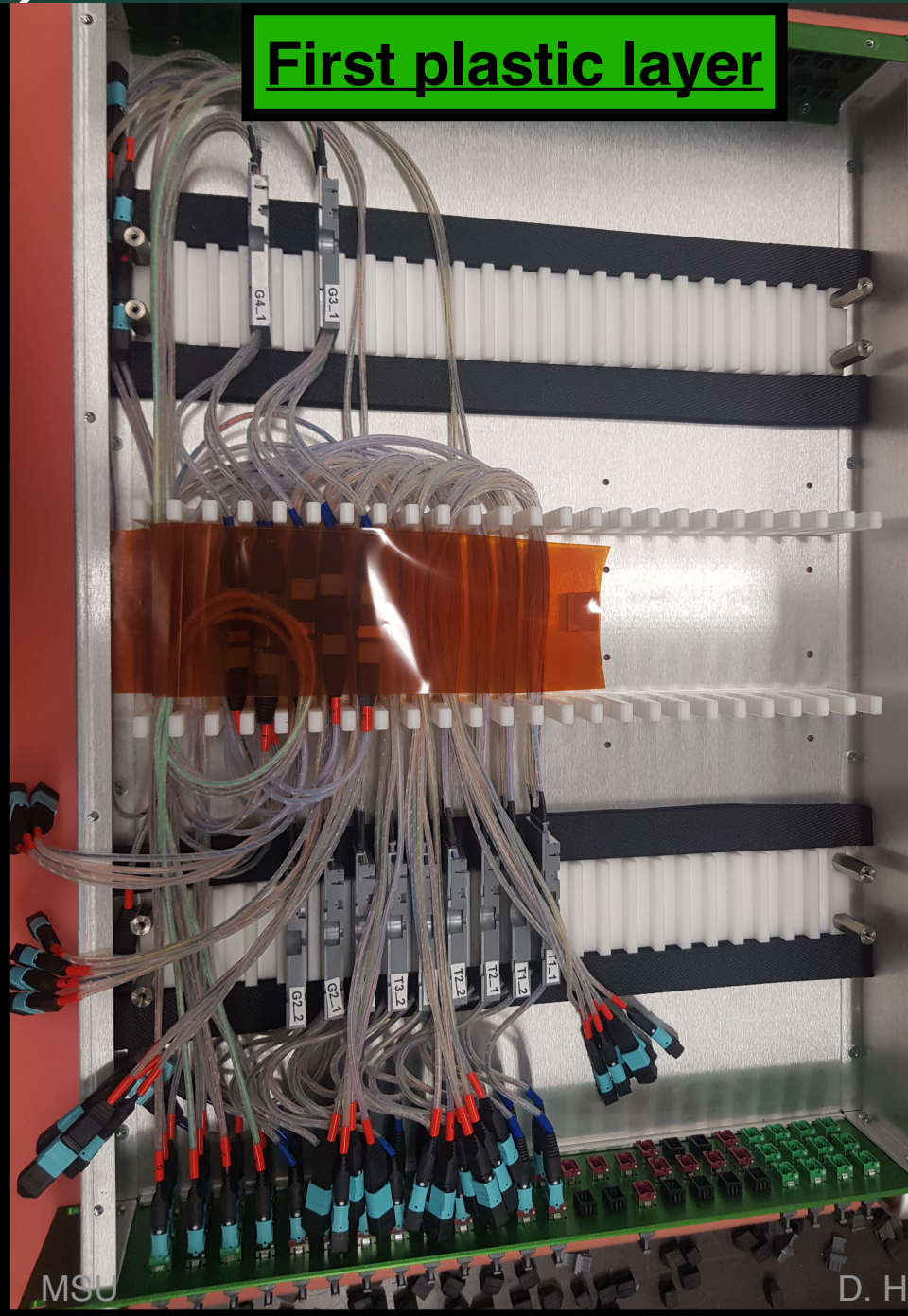
G1 / T1 / T2 / T3 Modules



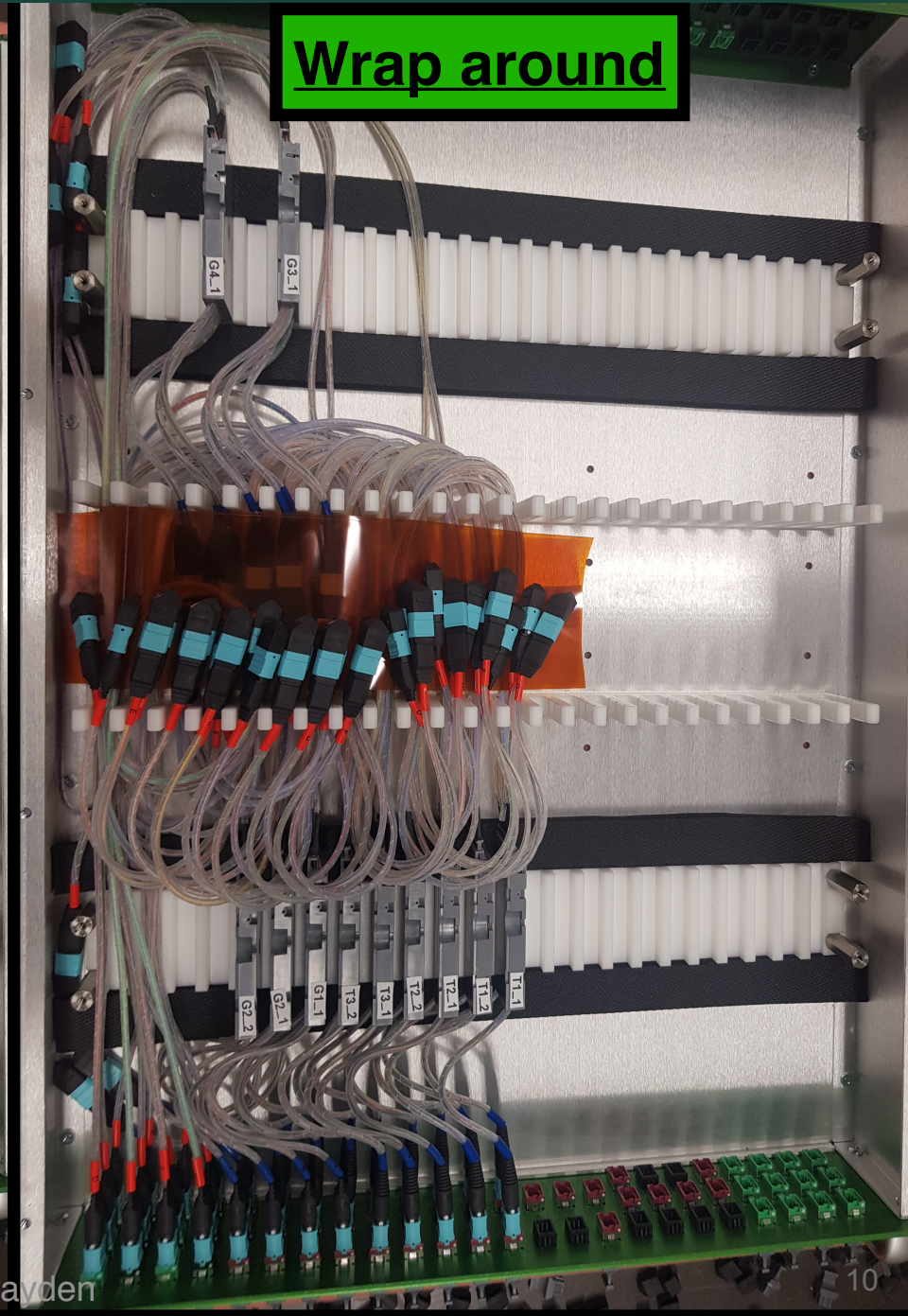
G4 and G3 Modules



First plastic layer



Wrap around



Test gFEX Connections (All Okay)



B3 Modules

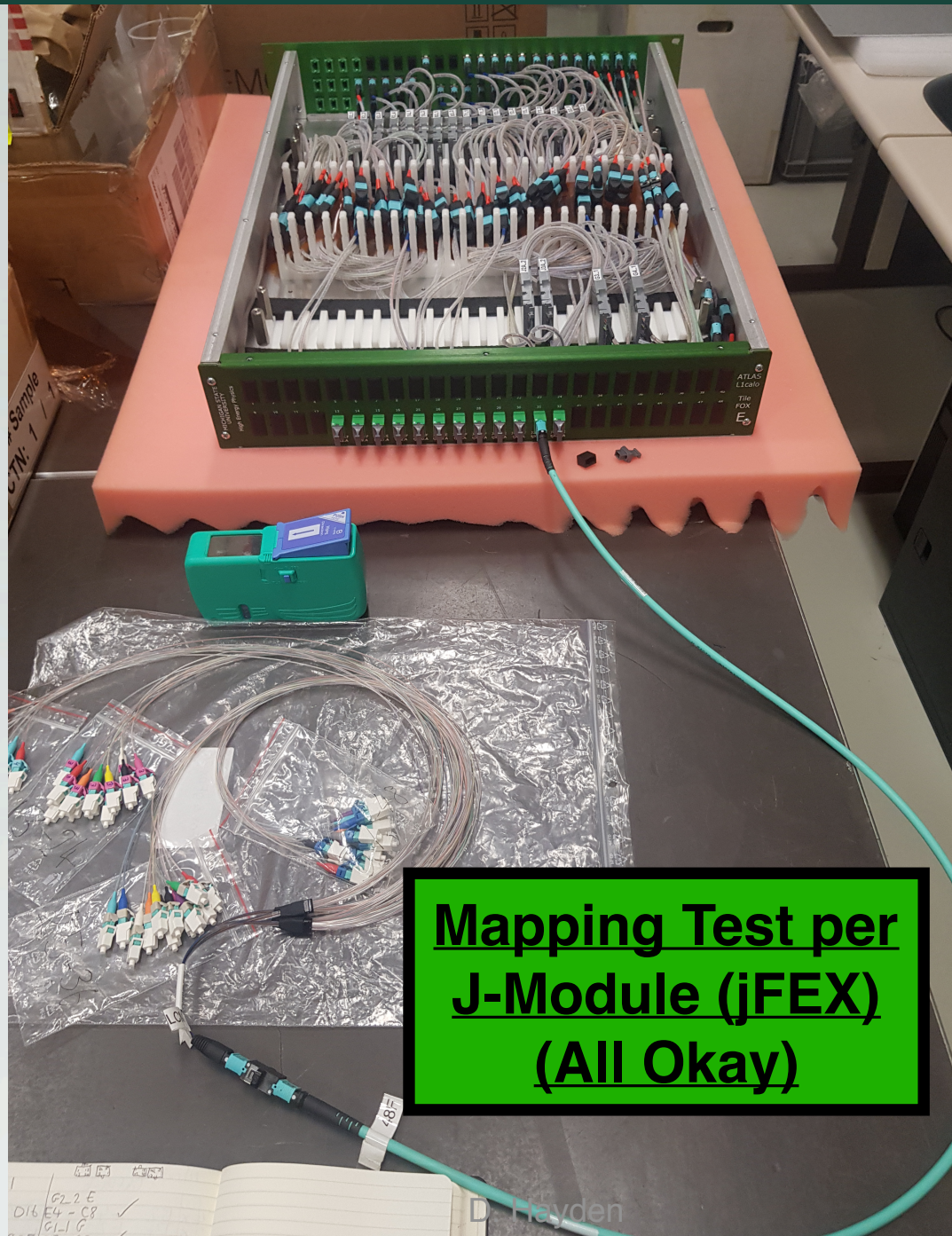


T4 / B2 Modules

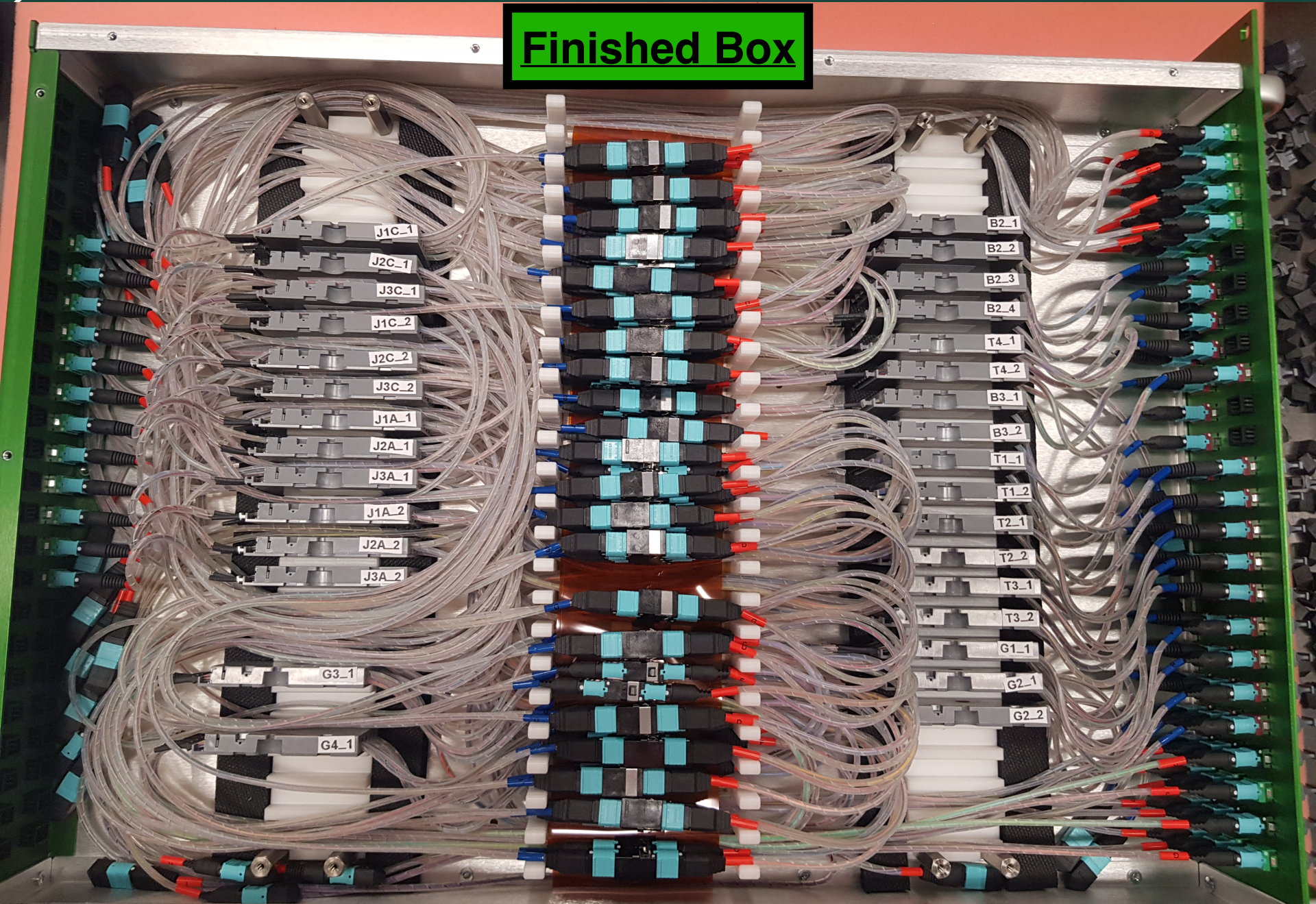


**Plastic Layer
and
Wrap Around**

First J2A Module



Finished Box



Box Locks



Final Plastic Layer

