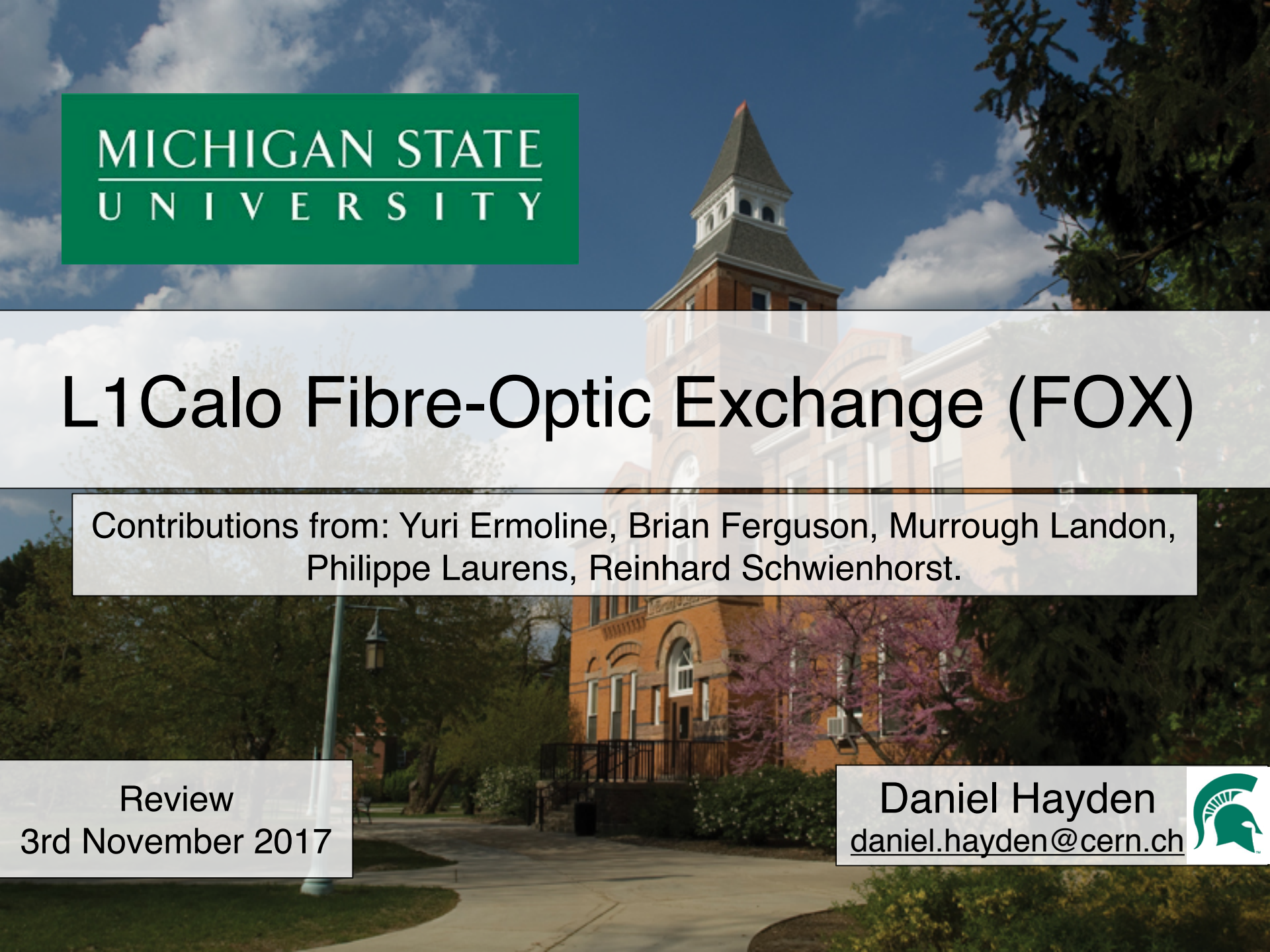

MICHIGAN STATE UNIVERSITY

L1Calo Fibre-Optic Exchange (FOX)

Contributions from: Yuri Ermoline, Brian Ferguson, Murrough Landon, Philippe Laurens, Reinhard Schwienhorst.

Review
3rd November 2017

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LAr Phase-I Upgrade

- The LHC is foreseen to be upgraded during the shut-down period of December 2018 - February 2021.
- Part of this upgrade will improve the selectivity of EM objects, discrimination power against background emerging from pileup, and the trigger readout of LAr.
- The LAr granularity will be increased by 10 times!

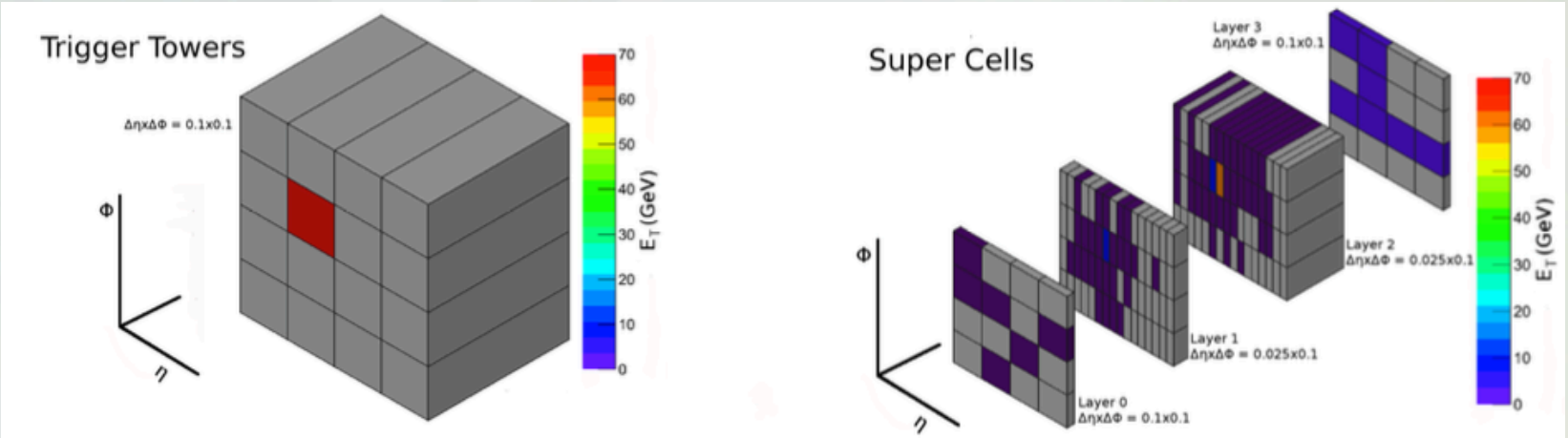
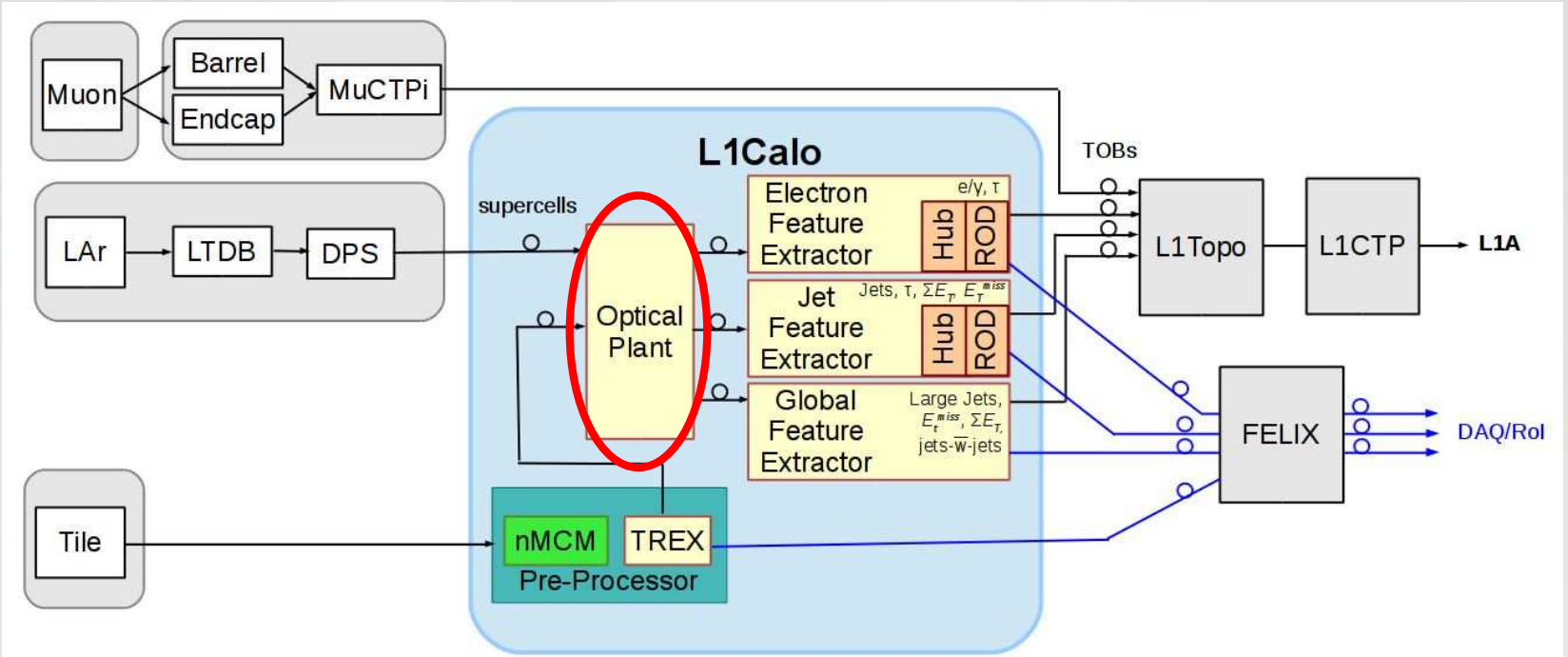


Figure 1: The energy depositions of an electron which carries energy of 70 GeV are illustrated for two cases. (Left) Trigger Tower readout, which sums the energy deposition across the longitudinal layers of the calorimeters in an area of $\Delta\eta \times \Delta\varphi = 0.1 \times 0.1$.
(Right) Super Cell readout, which provides information for each calorimeter layer for the full η range of the calorimeter, and finer segmentation ($\Delta\eta \times \Delta\varphi = 0.025 \times 0.1$) in the front and middle layers.

What is the FOX?

- Need to link the backend of the LAr (LATOMES/DPS) and Tile (TREX), to the feature extractors (FEX).
- Incoming cables contain many fibres that all need to go to specific and different locations (eFEX, jFEX, gFEX).
- The FOX contains this mapping, ideally with a simple and robust scheme, also considering future upgrades.



Hurdles for FOX

- Figure out a mapping scheme that is simple and robust, while also being able to account for specific features.
  - FOX internally divided into LArFOX and TileFOX parts.
  - Incoming cable → FOX → Fibres for specific FEX.
  - Consists of 6 x 2U boxes (4 x LArFOX, 2 x TileFOX).
- The naming scheme will be important, as there are thousands of fibres with unique routes from source to destination: Backend → FOX-In → FOX-Out → FEX.
  - Must also support automatic construction of firmware configuration files.
  - Must be updateable for re-routed links and Phase-II.
- Not possible to fix broken or scratched fibres without intervention. Agreed on 100% spare policy for gFEX.

FEX Details

- Baseline LAr/TREX → FEX link speed is 11.2 Gb/s.
- eFEX:
  - 20 EM supercells equivalent to covering 0.1 x 0.2.
  - 16 HAD towers covering $(0.4)^2$.
- jFEX:
  - 16 towers covering $(0.4)^2$.
  - Larger ϕ segmentation in special EMEC & HEC.
  - All FCAL supercells available.
- gFEX:
  - 8 x $(0.2)^2$ towers covering 0.8×0.4 or 0.4×0.8.
  - FCAL transmitted as 4-5 η rings in 16 ϕ wedges.

How many Fibres per Latome go to each FEX?

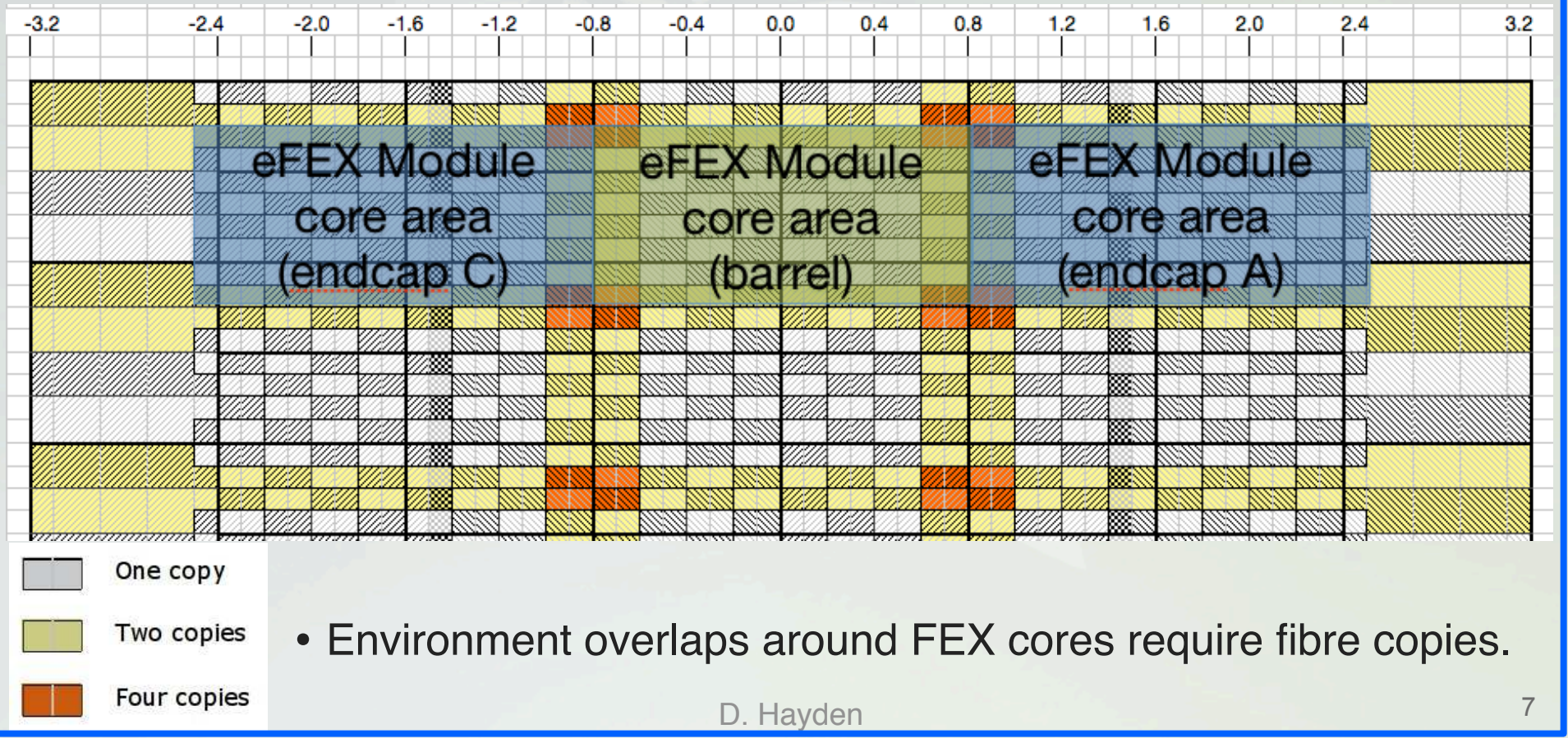
Central Latome Example

Total per Latome:	48
Total available to eFEX:	36
Total available to jFEX:	10
Total available to gFEX:	1 (+1 spare)

We know the total, but need to figure out mapping.

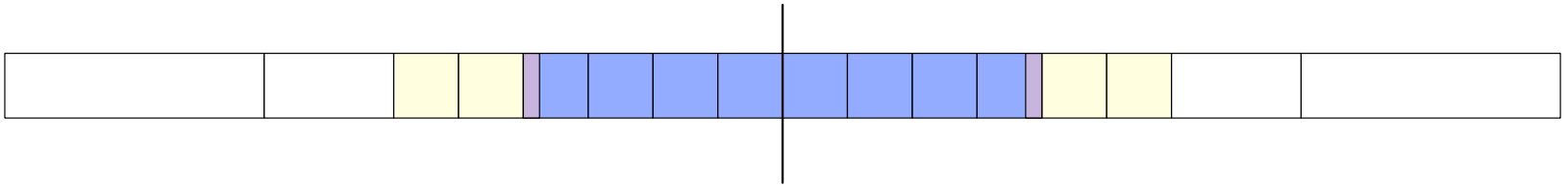
EM to eFEX: Layout

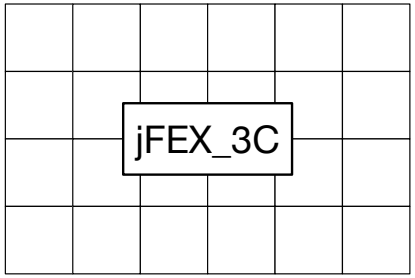
- Cells in Eta are numbered from 1-15 in ~ 0.1 or 0.2 increments in delta(eta), depending on where you are (EMB, EMEC, HEC, FCAL).
- Cells in Phi are lettered from A-P, again in 0.1 or 0.2 increments of delta(phi), depending on where you are in the detector.

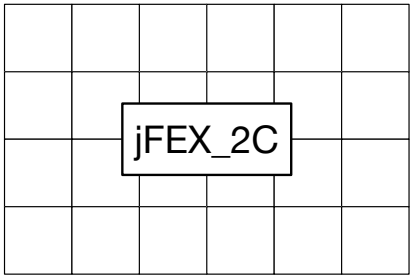


- Environment overlaps around FEX cores require fibre copies.

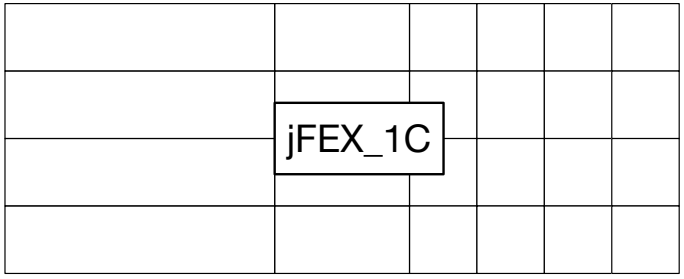
jFEX Coverage



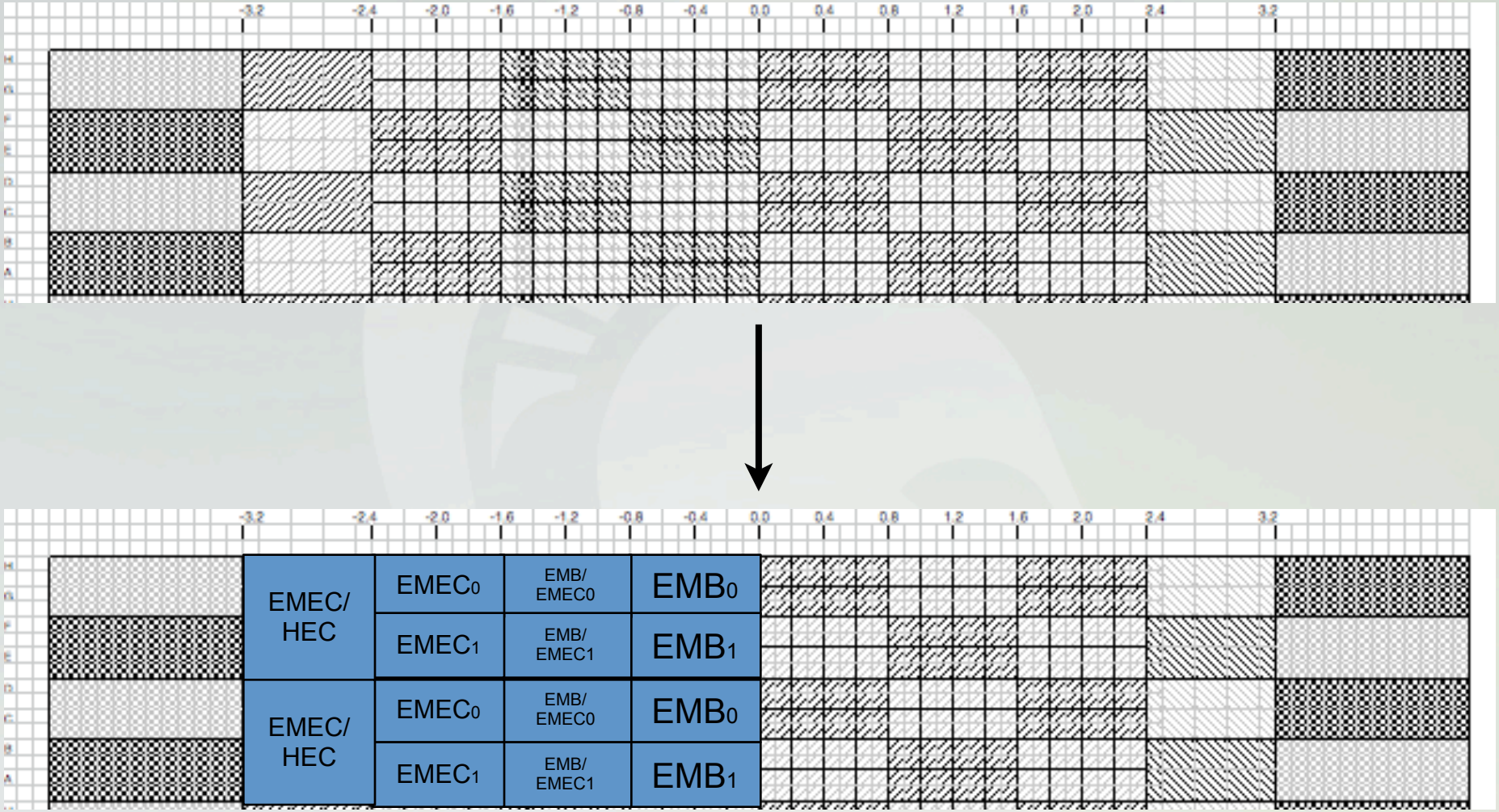




One quadrant shown for each jFEX.
Equivalent to 1/4 Connector.
One jFEX covers all Phi.



EM to gFEX: Layout



- The full calorimeter is covered by one gFEX, so no need for overlaps.
- 1 fibre per Latome in the central region (more in EMEC & FCAL).

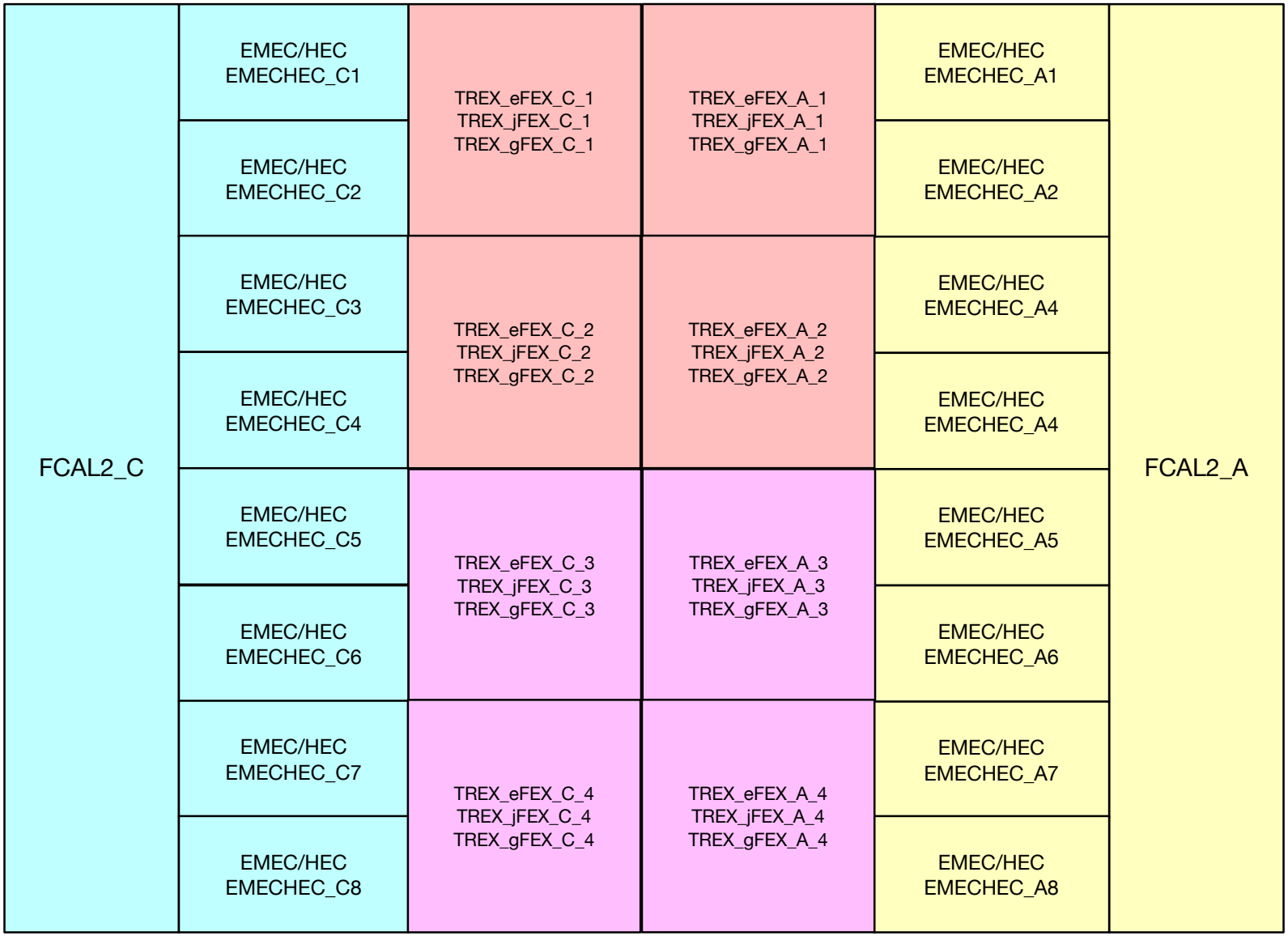
LATOMES - EM

FCAL1_C	EMEC/HEC EMECHEC_C1	EMEC0 EMEC0_C1	EMB/EMEC0 EMBEC0_C1	EMB0 EMB0_C1	EMB0 EMB0_A1	EMB/EMEC0 EMBEC0_A1	EMEC0 EMEC0_A1	EMEC/HEC EMECHEC_A1	FCAL1_A
		EMEC1 EMEC1_C1	EMB/EMEC1 EMBEC1_C1	EMB1 EMB1_C1	EMB1 EMB1_A1	EMB/EMEC1 EMBEC1_A1	EMEC1 EMEC1_A1		
	EMEC/HEC EMECHEC_C2	EMEC0 EMEC0_C2	EMB/EMEC0 EMBEC0_C2	EMB0 EMB0_C2	EMB0 EMB0_A2	EMB/EMEC0 EMBEC0_A2	EMEC0 EMEC0_A2	EMEC/HEC EMECHEC_A2	
		EMEC1 EMEC1_C2	EMB/EMEC1 EMBEC1_C2	EMB1 EMB1_C2	EMB1 EMB1_A2	EMB/EMEC1 EMBEC1_A2	EMEC1 EMEC1_A2		
	EMEC/HEC EMECHEC_C3	EMEC0 EMEC0_C3	EMB/EMEC0 EMBEC0_C3	EMB0 EMB0_C3	EMB0 EMB0_A3	EMB/EMEC0 EMBEC0_A3	EMEC0 EMEC0_A3	EMEC/HEC EMECHEC_A3	
		EMEC1 EMEC1_C3	EMB/EMEC1 EMBEC1_C3	EMB1 EMB1_C3	EMB1 EMB1_A3	EMB/EMEC1 EMBEC1_A3	EMEC1 EMEC1_A3		
	EMEC/HEC EMECHEC_C4	EMEC0 EMEC0_C4	EMB/EMEC0 EMBEC0_C4	EMB0 EMB0_C4	EMB0 EMB0_A4	EMB/EMEC0 EMBEC0_A4	EMEC0 EMEC0_A4	EMEC/HEC EMECHEC_A4	
		EMEC1 EMEC1_C4	EMB/EMEC1 EMBEC1_C4	EMB1 EMB1_C4	EMB1 EMB1_A4	EMB/EMEC1 EMBEC1_A4	EMEC1 EMEC1_A4		
	EMEC/HEC EMECHEC_C5	EMEC0 EMEC0_C5	EMB/EMEC0 EMBEC0_C5	EMB0 EMB0_C5	EMB0 EMB0_A5	EMB/EMEC0 EMBEC0_A5	EMEC0 EMEC0_A5	EMEC/HEC EMECHEC_A5	
		EMEC1 EMEC1_C5	EMB/EMEC1 EMBEC1_C5	EMB1 EMB1_C5	EMB1 EMB1_A5	EMB/EMEC1 EMBEC1_A5	EMEC1 EMEC1_A5		
	EMEC/HEC EMECHEC_C6	EMEC0 EMEC0_C6	EMB/EMEC0 EMBEC0_C6	EMB0 EMB0_C6	EMB0 EMB0_A6	EMB/EMEC0 EMBEC0_A6	EMEC0 EMEC0_A6	EMEC/HEC EMECHEC_A6	
		EMEC1 EMEC1_C6	EMB/EMEC1 EMBEC1_C6	EMB1 EMB1_C6	EMB1 EMB1_A6	EMB/EMEC1 EMBEC1_A6	EMEC1 EMEC1_A6		
	EMEC/HEC EMECHEC_C7	EMEC0 EMEC0_C7	EMB/EMEC0 EMBEC0_C7	EMB0 EMB0_C7	EMB0 EMB0_A7	EMB/EMEC0 EMBEC0_A7	EMEC0 EMEC0_A7	EMEC/HEC EMECHEC_A7	
		EMEC1 EMEC1_C7	EMB/EMEC1 EMBEC1_C7	EMB1 EMB1_C7	EMB1 EMB1_A7	EMB/EMEC1 EMBEC1_A7	EMEC1 EMEC1_A7		
	EMEC/HEC EMECHEC_C8	EMEC0 EMEC0_C8	EMB/EMEC0 EMBEC0_C8	EMB0 EMB0_C8	EMB0 EMB0_A8	EMB/EMEC0 EMBEC0_A8	EMEC0 EMEC0_A8	EMEC/HEC EMECHEC_A8	
		EMEC1 EMEC1_C8	EMB/EMEC1 EMBEC1_C8	EMB1 EMB1_C8	EMB1 EMB1_A8	EMB/EMEC1 EMBEC1_A8	EMEC1 EMEC1_A8		

Key

- LArFOX_B
- LArFOX_D
- LArFOX_A
- LArFOX_C
- TileFOX_E
- TileFOX_F

LATOMES/TREX - Had



Latomes, Fibres, and FEXs

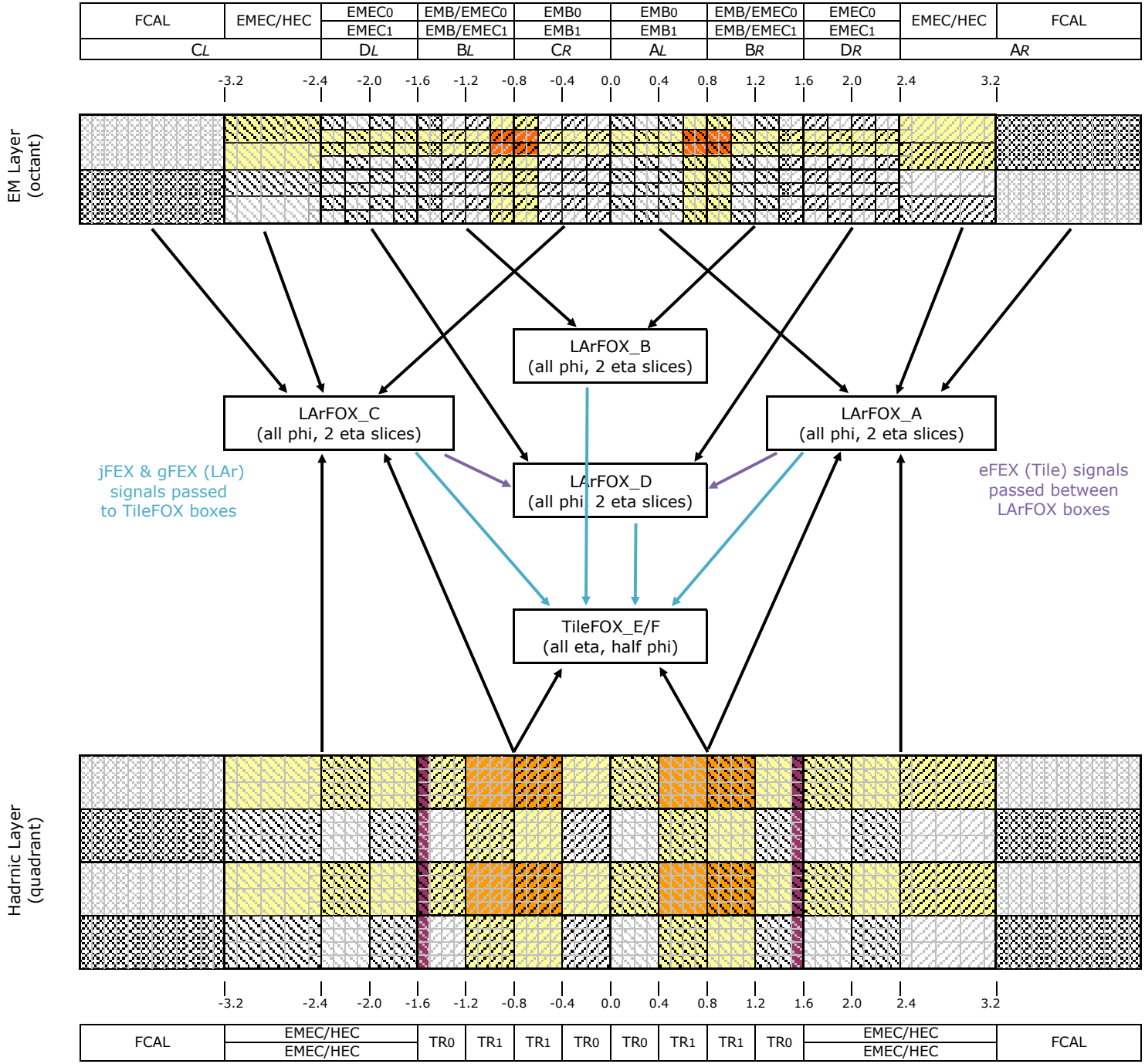
LATOME type	Detector	$\Delta\Phi$	$\lvert\eta\rvert$	# SCS	# LATOME boards
EMB	EMB	0.393	0-0.8	320	32
EMB/EMEC	EMB,EMEC	0.393	0.8-1.6	320	32
EMEC	EMEC	0.393	1.6-2.4	312	32
EMEC/HEC	EMEC HEC	0.785	2.4-3.2 1.5-3.2	80 96	16
FCAL1	FCAL Layer 1	6.280	3.1-4.9	192	2
FCAL2	FCAL Layers 2&3	6.280	3.2-4.9	192	2

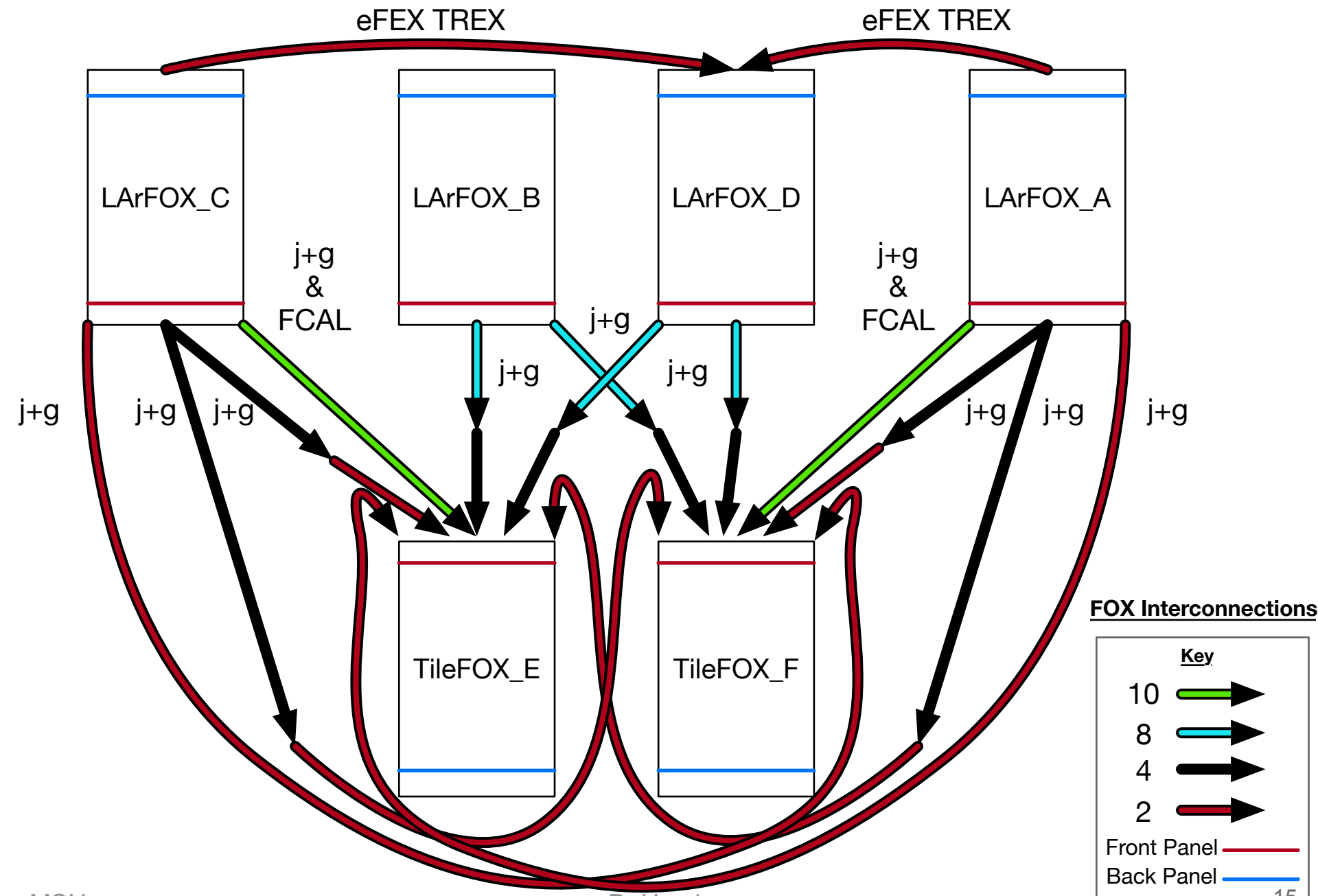
Table 3: Coverage and number of the various LATOME board types.

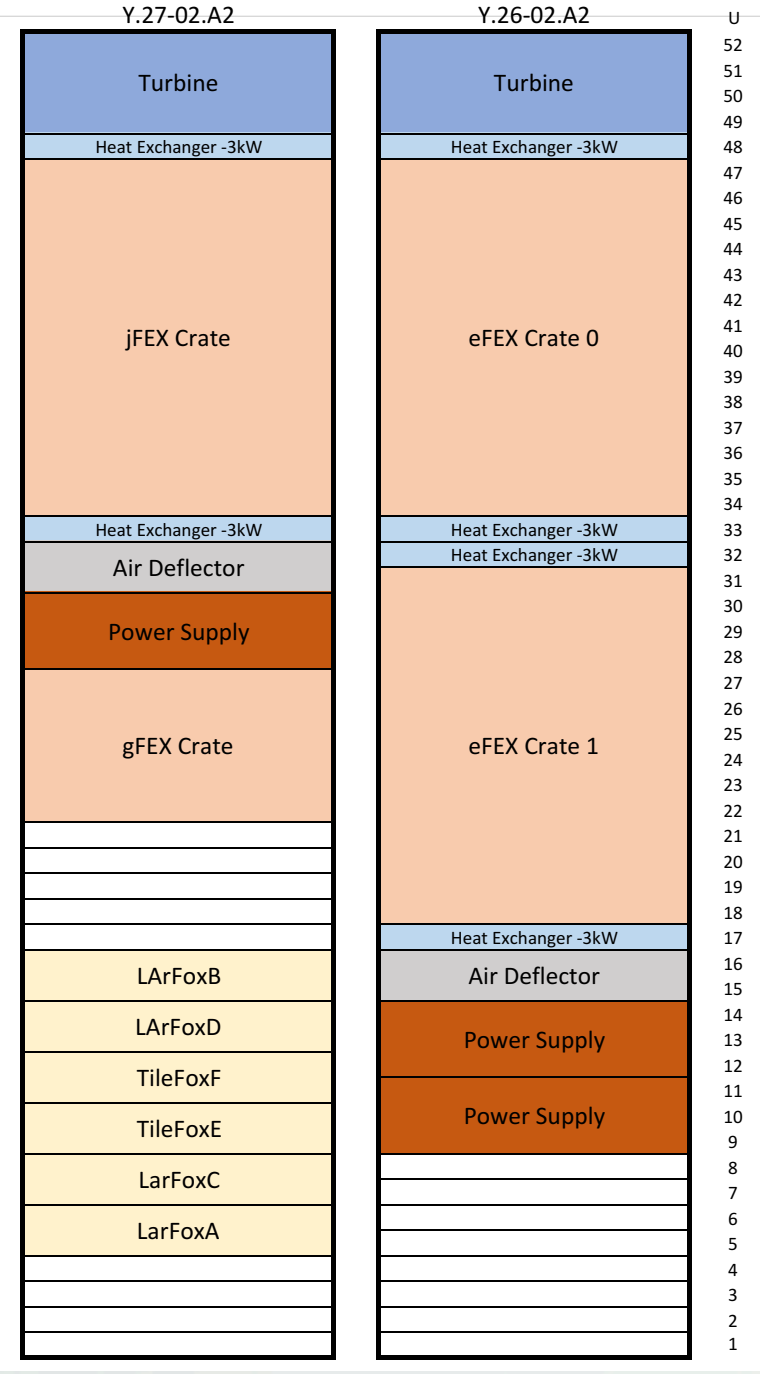
	Number of Fibers (Unique)				Channels per Fiber		
LATOME type	eFEX	jFEX	gFEX	all	eFEX	jFEX	gFEX
EMB_0	30(16)	6(2)	1	37(19)	20	16	8
EMB_1	20(16)	6(2)	1	27(19)	20	16	8
$EMB/EMEC_0$	30(16)	6(2)	1	37(19)	20	16	8
$EMB/EMEC_1$	20(16)	6(2)	1	27(19)	20	16	8
$EMEC_0$	24(16)	5(2)	1	30(19)	18-20	16	8
$EMEC_1$	16(16)	5(2)	1	22(19)	18-20	16	8
EMEC/HEC	15(10)	21(9)	4	40(23)	16-20	8-16	14-16
FCAL1	-	16	5	21	-	12	16
FCAL2	-	16	4	20	-	12	16

Table 4: Output fiber count and content for each of the LATOME types.

FOX Overview

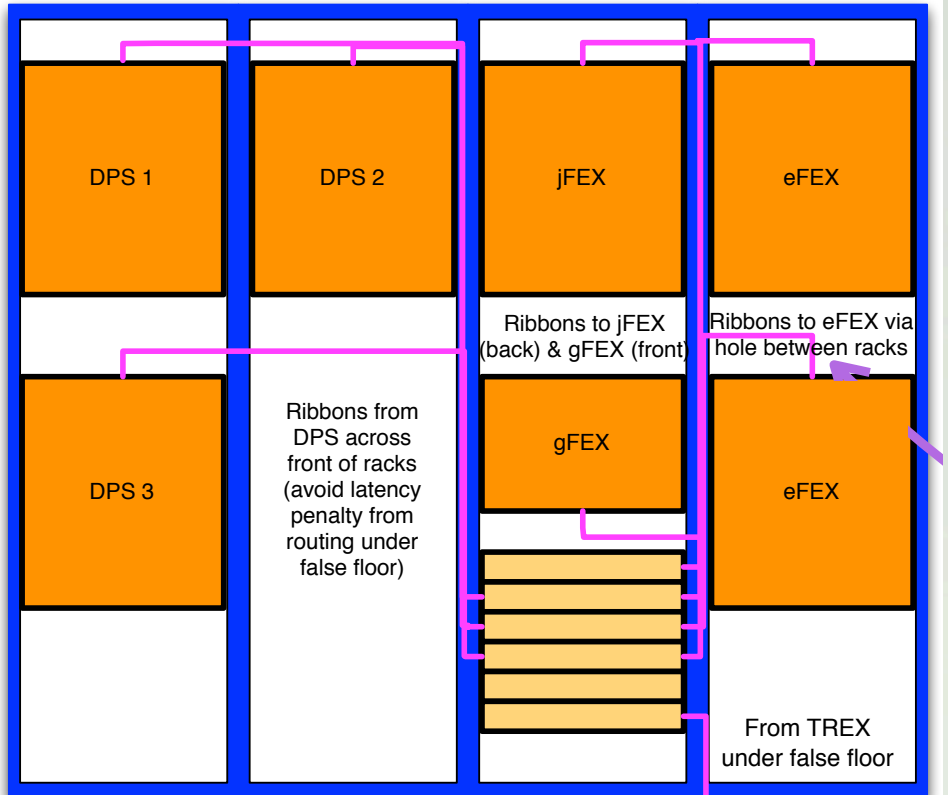

FCAL
EMEC/HEC
EMEC0
EMEC1
EMB/EMEC0
EMB/EMEC1
EMB0
EMB1
EMB0
EMB1
EMB/EMEC0
EMB/EMEC1
EMEC0
EMEC1
EMEC/HEC
FCAL
CL
DL
BL
CR
AL
BR
DR
AR
-3.2 -2.4 -2.0 -1.6 -1.2 -0.8 -0.4 0.0 0.4 0.8 1.2 1.6 2.0 2.4 3.2
EM Layer (octant)
LArFOX_B (all phi, 2 eta slices)
LArFOX_C (all phi, 2 eta slices)
LArFOX_A (all phi, 2 eta slices)
LArFOX_D (all phi, 2 eta slices)
jFEX & gFEX (LAr) signals passed to TileFOX boxes
eFEX (Tile) signals passed between LArFOX boxes
TileFOX_E/F (all eta, half phi)
Hadrnic Layer (quadrant)
-3.2 -2.4 -2.0 -1.6 -1.2 -0.8 -0.4 0.0 0.4 0.8 1.2 1.6 2.0 2.4 3.2
FCAL
EMEC/HEC
EMEC/HEC
TR0
TR1
TR1
TR0
TR0
TR1
TR1
TR0
EMEC/HEC
EMEC/HEC
FCAL

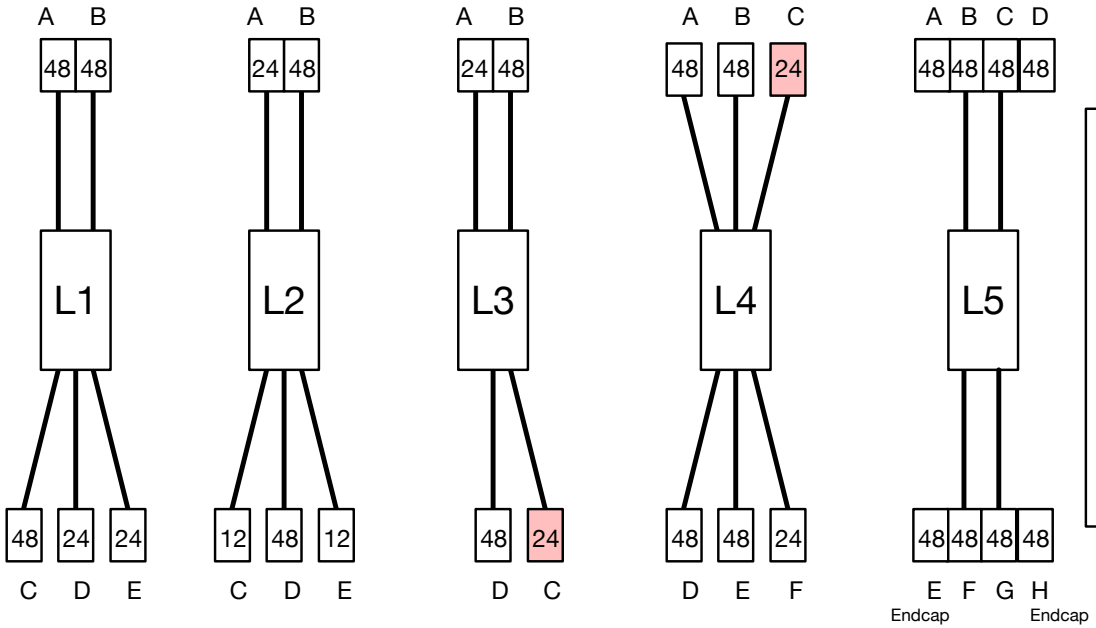

eFEX TREX
eFEX TREX
LArFOX_C
LArFOX_B
LArFOX_D
LArFOX_A
j+g
&
FCAL
j+g
j+g
&
FCAL
j+g
j+g
j+g
j+g
j+g
j+g
j+g
j+g
TileFOX_E
TileFOX_F
FOX Interconnections
Key
10
8
4
2
Front Panel
Back Panel



Preliminary Rack Layout

- Current plan is to use 6 x 2U-high boxes.
- eFEX may need extra crate - gets tight.
- Minimal latency path: across racks from DPS and to gFEX, via back to jFEX, and via hole between racks to back of eFEX.





Key

Upper = Input
Lower = Output

Unused MTP

Naming

Everywhere:

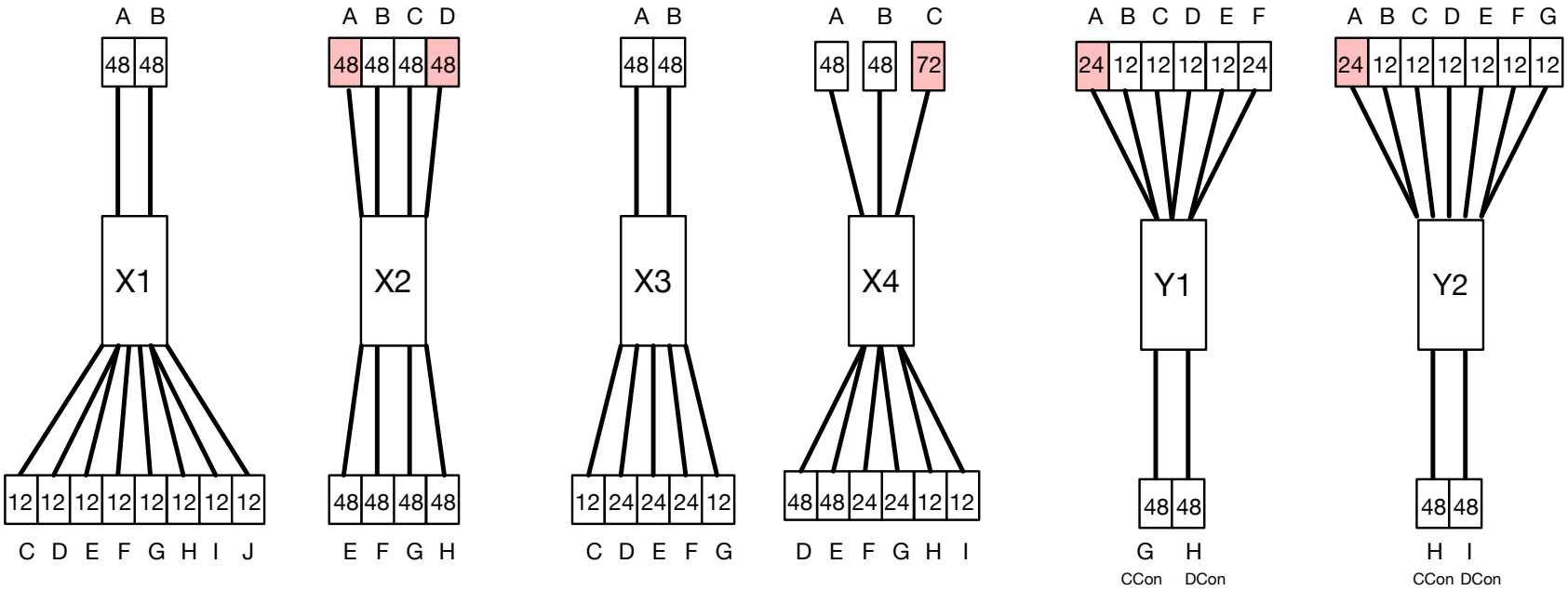
1 = (I)	= B
1 = (O)	= C

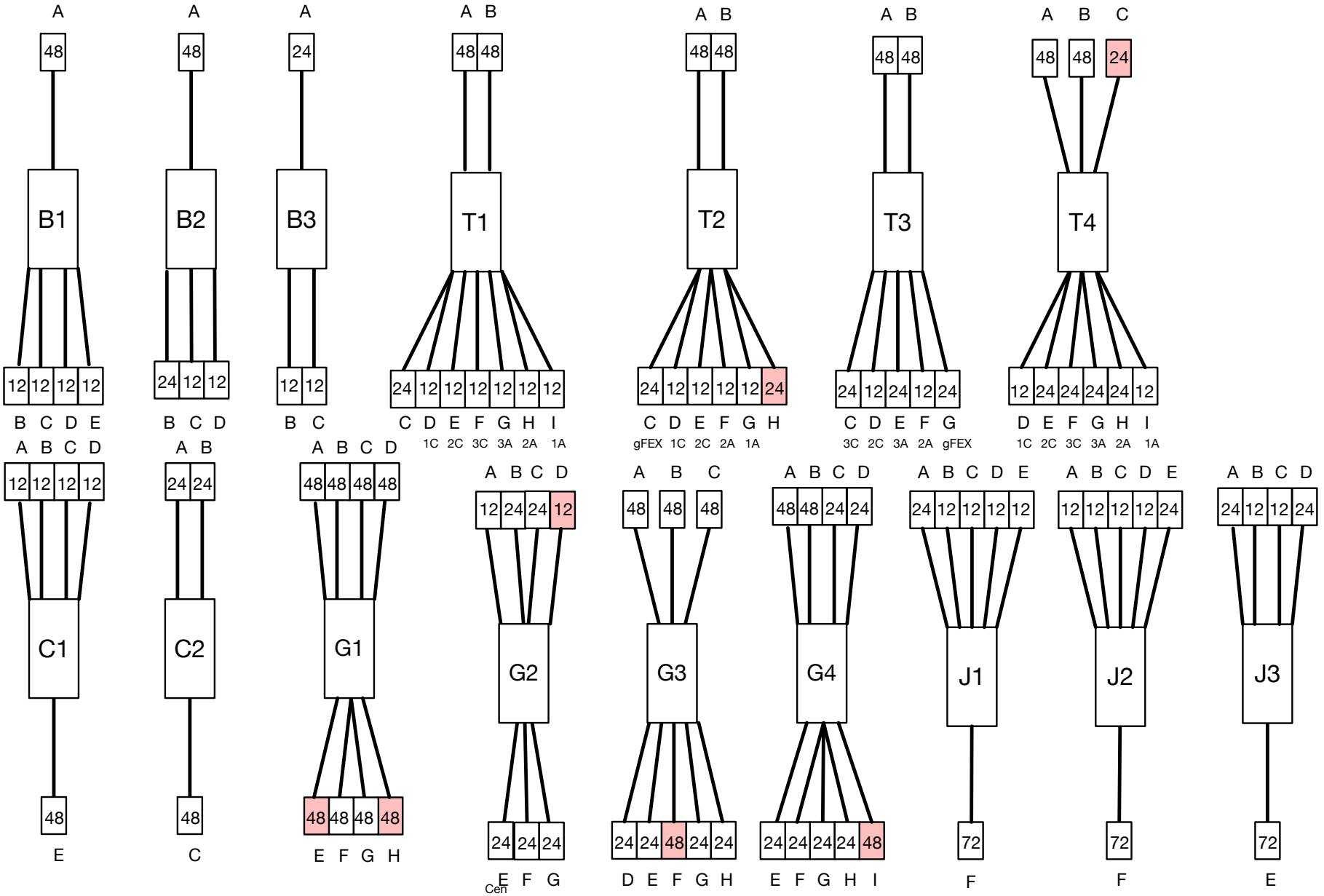
LArFOX Boxes:

1 < (I/O) < 4	= L
>= 4 (O)	= X
>= 4 (I)	= Y

TileFOX Boxes:

jFEX first half	= T
jFEX output	= J
gFEX output	= G



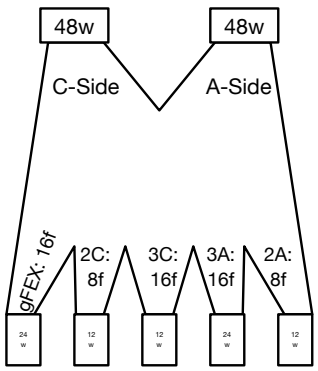

A
48
B1
12 12 12 12
B C D E
A
48
B2
24 12 12
B C D
A
24
B3
12 12
B C
A B
48 48
T1
24 12 12 12 12 12 12
C D E F G H I
1C 2C 3C 3A 2A 1A
A B
48 48
T2
24 12 12 12 12 24
C D E F G H
gFEX 1C 2C 2A 1A
A B
48 48
T3
24 12 24 12 24
C D E F G
3C 2C 3A 2A gFEX
A B C
48 48 24
T4
12 24 24 24 24 12
D E F G H I
1C 2C 3C 3A 2A 1A
A B C D
12 12 12 12
C1
48
E
A B
24 24
C2
48
C
A B C D
48 48 48 48
G1
48 48 48 48
E F G H
A B C D
12 24 24 12
G2
24 24 24
E F G
Cen
A B C
48 48 48
G3
24 24 48 24 24
D E F G H
A B C D
48 48 24 24
G4
24 24 24 24 48
E F G H I
A B C D E
24 12 12 12 12
J1
72
F
A B C D E
12 12 12 12 24
J2
72
F
A B C D
24 12 12 24
J3
72
E

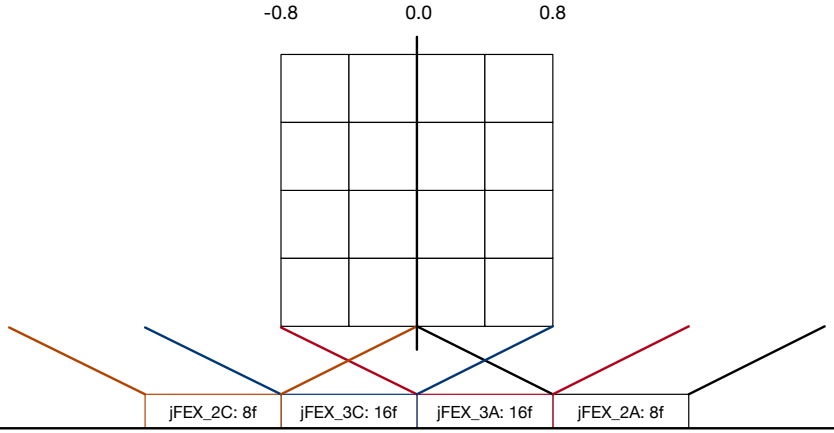
Ribbon Type (27)	LArFOX B	LArFOX D	LArFOX A+C	TileFOX E+F	Total (212)
L1	16	16	16	-	48
L2	16	-	-	-	16
L3	-	16	16	-	32
L4	-	-	8	-	8
L5	-	-	2	-	2
X1	-	-	2	-	2
X2	-	2	-	-	2
X3	-	-	4	-	4
X4	-	-	2	-	2
Y1	-	-	12	-	12
Y2	-	-	4	-	4
B1	-	-	4	-	4
B2	-	-	-	8	8
B3	-	-	-	4	4
C1	8	-	-	-	8
C2	-	-	-	6	6
T1	-	-	-	4	4
T2	-	-	-	4	4
T3	-	-	-	4	4
T4	-	-	-	4	4
G1	-	-	-	2	2
G2	-	-	-	4	4
G3	-	-	-	2	2
G4	-	-	-	2	2
J1	-	-	-	8	8
J2	-	-	-	8	8
J3	-	-	-	8	8

Fibre Mapping

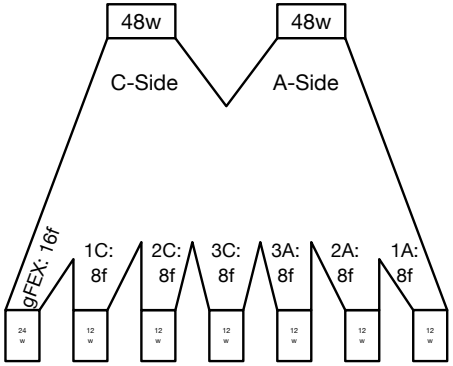
TileFOX Coverage (One quadrant)

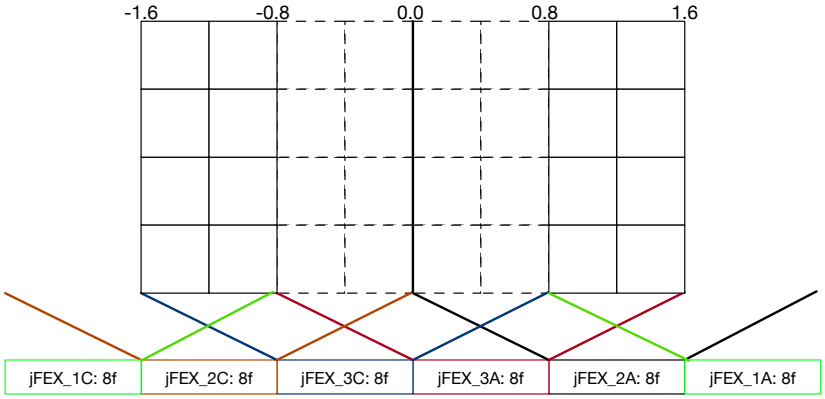
EM Central (A/C)



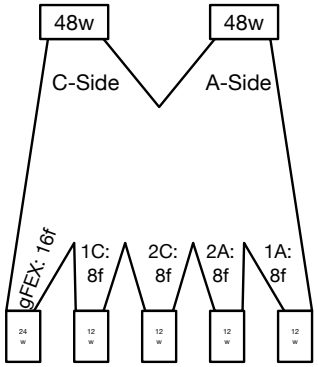


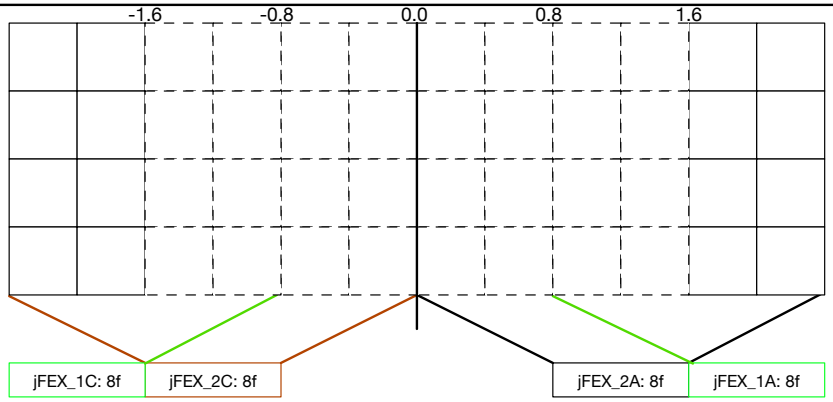
EM Central (B)





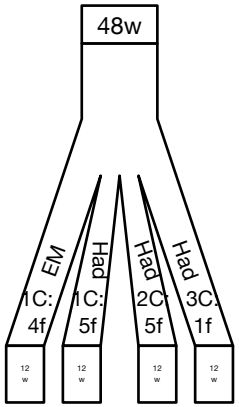
EM Central (D)

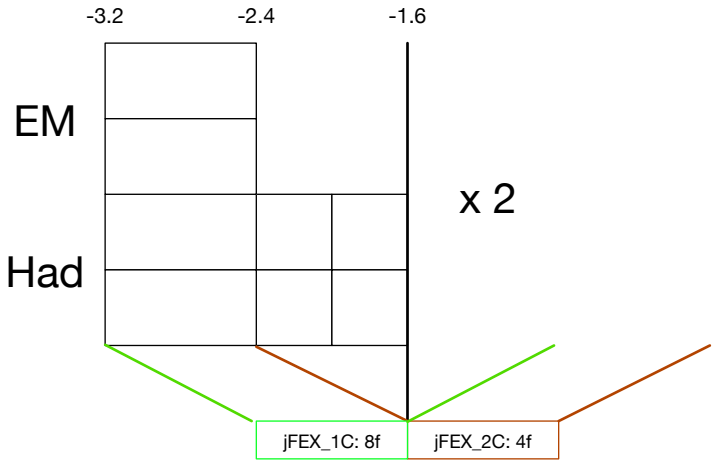




TileFOX Coverage (One quadrant)

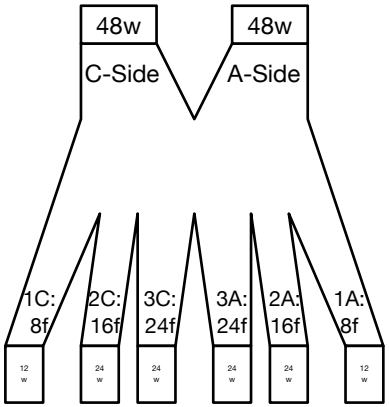
EMEC/HEC

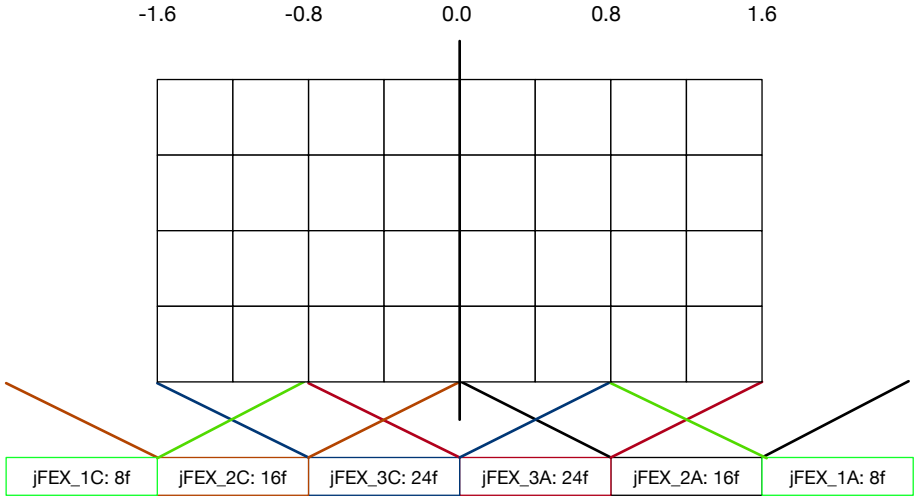




Not including HEC overlap (+1 fibre for each jFEX to include)

TREX Had jFEX





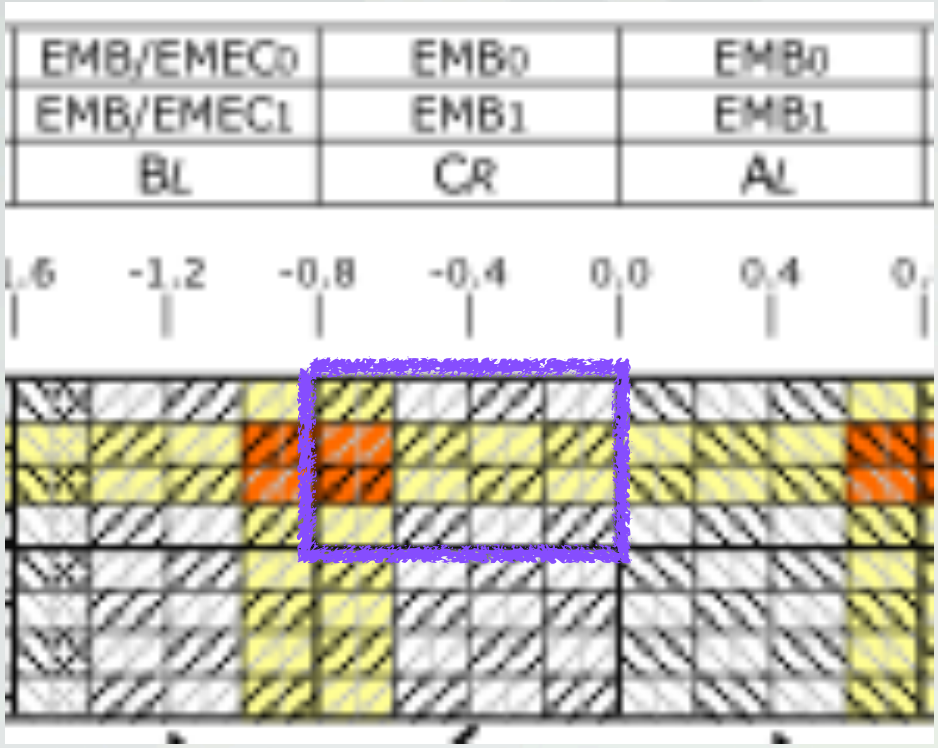
Detector Location Notation

L_ϕ	EMB and EMEC(I_η<12)	EMEC($I_\eta \geq 12$)	HEC(I_η<12)	HEC($I_\eta \geq 12$)	FCAL
A	0.000-0.098	0.000-0.196	0.000-0.098	0.000-0.196	0.000-0.393
B	0.098-0.196	0.196-0.393	0.098-0.196	0.196-0.393	0.393-0.785
C	0.196-0.295	0.393-0.589	0.196-0.295	0.393-0.589	0.785-1.178
D	0.295-0.393	0.589-0.785	0.295-0.393	0.589-0.785	1.178-1.570
E	0.393-0.491	0.785-0.982	0.393-0.491	0.785-0.982	1.570-1.963
F	0.491-0.589	0.982-1.178	0.491-0.589	0.982-1.178	1.963-2.356
G	0.589-0.687	1.178-1.374	0.589-0.687	1.178-1.374	2.356-2.748
H	0.687-0.785	1.374-1.570	0.687-0.785	1.374-1.570	2.748-3.140
I	0.785-0.884	-	0.785-0.884	-	3.140-3.533
J	0.884-0.982	-	0.884-0.982	-	3.533-3.926
K	0.982-1.080	-	0.982-1.080	-	3.926-4.318
L	1.080-1.178	-	1.080-1.178	-	4.318-4.710
M	1.178-1.276	-	1.178-1.276	-	4.710-5.103
N	1.276-1.374	-	1.276-1.374	-	5.103-5.496
O	1.374-1.473	-	1.374-1.473	-	5.496-5.888
P	1.473-1.570	-	1.473-1.570	-	5.888-6.280

I_η	EMB	EMEC	HEC	FCAL
1	0.0-0.1	1.4-1.5	-	3.2-3.6
2	0.1-0.2	1.5-1.6	1.5-1.6	3.6-4.0
3	0.2-0.3	1.6-1.7	1.6-1.7	4.0-4.4
4	0.3-0.4	1.7-1.8	1.7-1.8	4.4-4.9
5	0.4-0.5	1.8-1.9	1.8-1.9	-
6	0.5-0.6	1.9-2.0	1.9-2.0	-
7	0.6-0.7	2.0-2.1	2.0-2.1	-
8	0.7-0.8	2.1-2.2	2.1-2.2	-
9	0.8-0.9	2.2-2.3	2.2-2.3	-
10	0.9-1.0	2.3-2.4	2.3-2.4	-
11	1.0-1.1	2.4-2.5	2.4-2.5	-
12	1.1-1.2	2.5-2.7	2.5-2.7	-
13	1.2-1.3	2.7-2.9	2.7-2.9	-
14	1.3-1.4	2.9-3.1	2.9-3.1	-
15	1.4-1.5	3.1-3.2	3.1-3.2	-

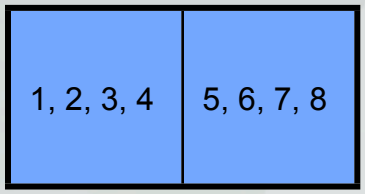
Illustrative (Old) Mapping Example

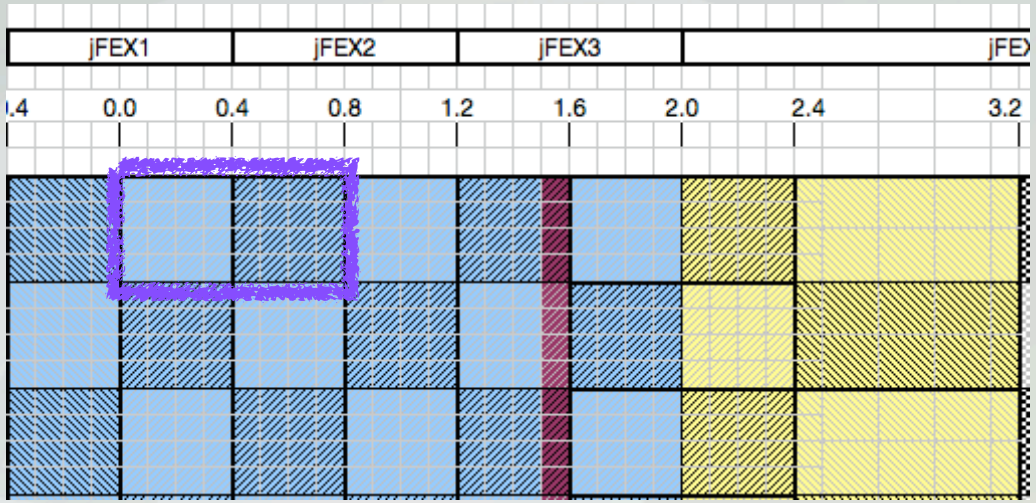
1, 2	3	4	5
7, 8, 13, 14	9, 15	10, 16	11, 17
19, 20, 25, 26	21, 27	22, 28	23, 29
31, 32	33	34	35



Fibre	Type	Location
1	EFEX	8A 7A
2	EFEX	8A 7A
3	EFEX	6A 5A
4	EFEX	4A 3A
5	EFEX	2A 1A
6	EFEX	None
7	EFEX	8B 7B
8	EFEX	8B 7B
9	EFEX	6B 5B
10	EFEX	4B 3B
11	EFEX	2B 1B
12	EFEX	None
13	EFEX	8B 7B
14	EFEX	8B 7B
15	EFEX	6B 5B
16	EFEX	4B 3B
17	EFEX	2B 1B
18	EFEX	None
19	EFEX	8C 7C
20	EFEX	8C 7C
21	EFEX	6C 5C
22	EFEX	4C 3C
23	EFEX	2C 1C
24	EFEX	None
25	EFEX	8C 7C
26	EFEX	8C 7C
27	EFEX	6C 5C
28	EFEX	4C 3C
29	EFEX	2C 1C
30	EFEX	None
31	EFEX	8D 7D
32	EFEX	8D 7D
33	EFEX	6D 5D
34	EFEX	4D 3D
35	EFEX	2D 1D
36	EFEX	None

Illustrative (Old) Mapping Example



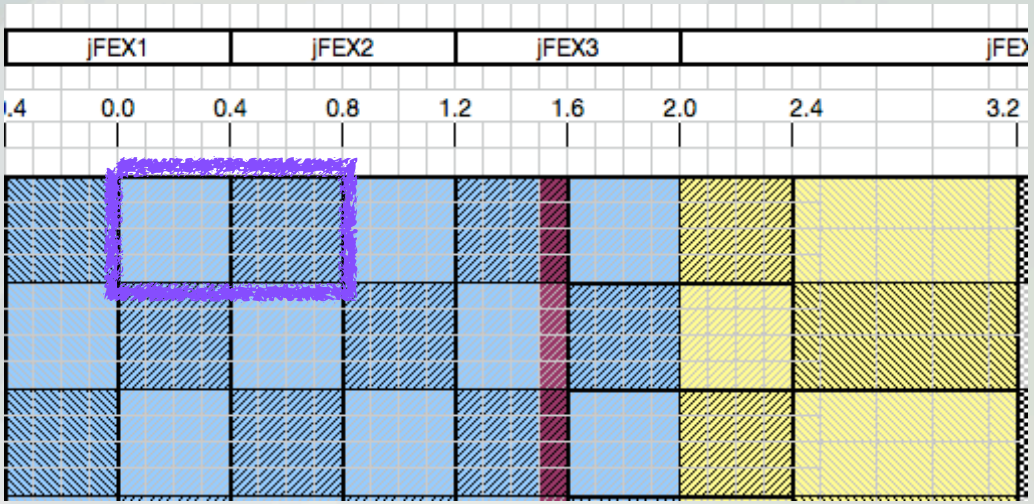


Fibre	Type	Location							
37	JFEX	1A 2A	3A 4A	1B 2B	3B 4B	1C 2C	3C 4C	1D 2D	3D 4D
38	JFEX	1A 2A	3A 4A	1B 2B	3B 4B	1C 2C	3C 4C	1D 2D	3D 4D
39	JFEX	1A 2A	3A 4A	1B 2B	3B 4B	1C 2C	3C 4C	1D 2D	3D 4D
40	JFEX	None None	None None	None None	None None	None None	None None	None None	None None
41	JFEX	5A 6A	7A 8A	5B 6B	7B 8B	5C 6C	7C 8C	5D 6D	7D 8D
42	JFEX	5A 6A	7A 8A	5B 6B	7B 8B	5C 6C	7C 8C	5D 6D	7D 8D
43	JFEX	5A 6A	7A 8A	5B 6B	7B 8B	5C 6C	7C 8C	5D 6D	7D 8D
44	JFEX	None None	None None	None None	None None	None None	None None	None None	None None
45	JFEX	None None	None None	None None	None None	None None	None None	None None	None None
46	JFEX	None None	None None	None None	None None	None None	None None	None None	None None

Last two rows of “none” to fill space.

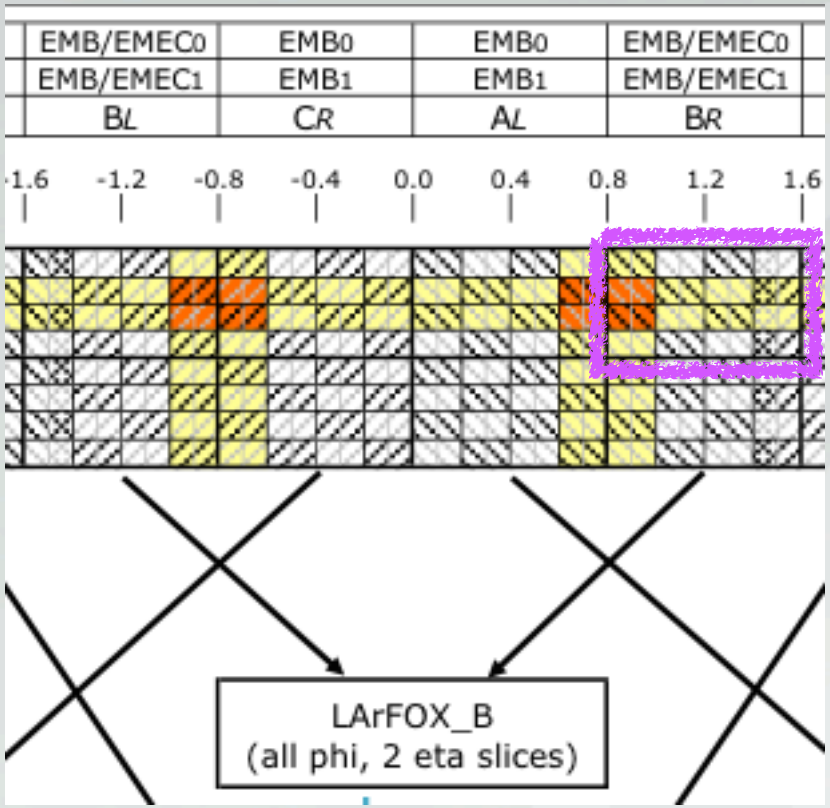
Illustrative (Old) Mapping Example

1, 2



Fibre	Type	Location															
47	GFEX	1A 2A	3A 4A	1B 2B	3B 4B	1C 2C	3C 4C	1D 2D	3D 4D	5A 6A	7A 8A	5B 6B	7B 8B	5C 6C	7C 8C	5D 6D	7D 8D
48	GFEX	1A 2A	3A 4A	1B 2B	3B 4B	1C 2C	3C 4C	1D 2D	3D 4D	5A 6A	7A 8A	5B 6B	7B 8B	5C 6C	7C 8C	5D 6D	7D 8D

Illustrative (Old) Mapping Example



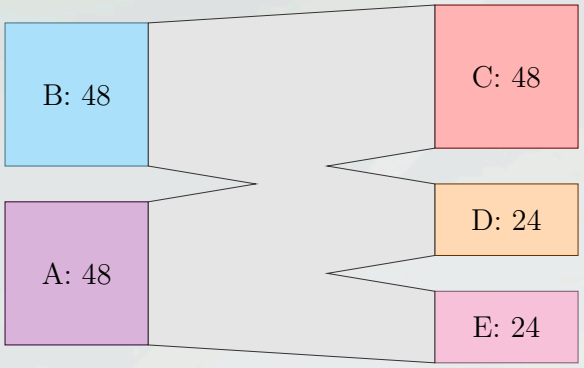
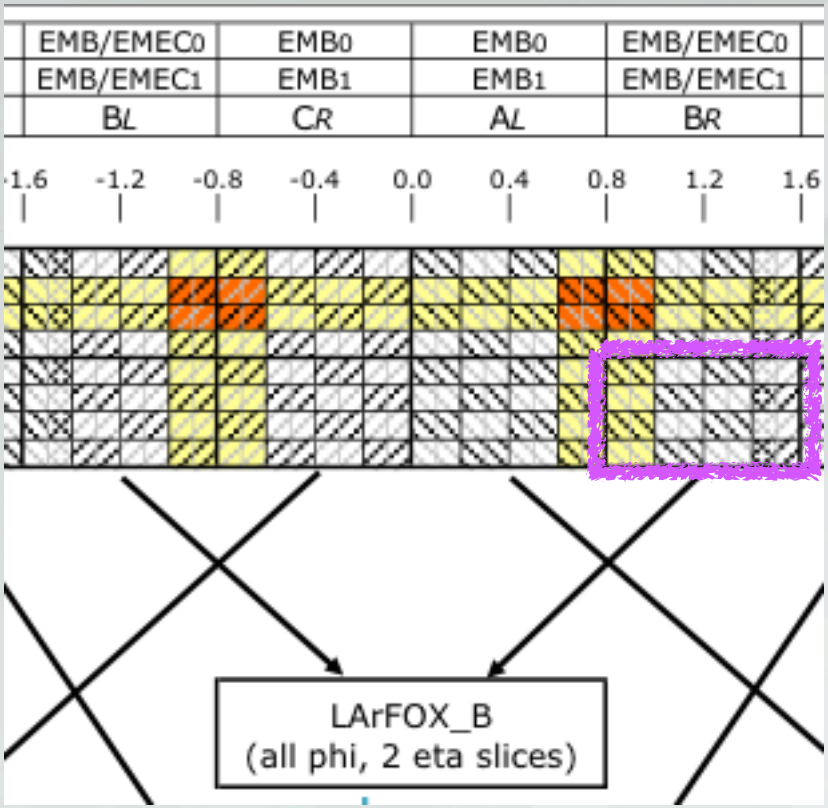


Figure 1: Diagram of ribbon assembly type L1

Fibre	Cell1	Cell2	Type	Side	Octant	L1 In	L1 Out
1	9A	10A	EMBEC0	A	1	A1	D1
2	9A	10A	EMBEC0	A	1	A2	D2
3	11A	12A	EMBEC0	A	1	A3	D3
4	13A	14A	EMBEC0	A	1	A4	D4
5	15A	2A	EMBEC0	A	1	A5	D5
6	None	None	EMBEC0	A	1	A6	D6
7	9B	10B	EMBEC0	A	1	A7	D7
8	9B	10B	EMBEC0	A	1	A8	D8
9	11B	12B	EMBEC0	A	1	A9	D9
10	13B	14B	EMBEC0	A	1	A10	D10
11	15B	2B	EMBEC0	A	1	A11	D11
12	None	None	EMBEC0	A	1	A12	D12
13	9B	10B	EMBEC0	A	1	A13	C1
14	9B	10B	EMBEC0	A	1	A14	C2
15	11B	12B	EMBEC0	A	1	A15	C3
16	13B	14B	EMBEC0	A	1	A16	C4
17	15B	2B	EMBEC0	A	1	A17	C5
18	None	None	EMBEC0	A	1	A18	C6
19	9C	10C	EMBEC0	A	1	A19	D13
20	9C	10C	EMBEC0	A	1	A20	D14
21	11C	12C	EMBEC0	A	1	A21	D15
22	13C	14C	EMBEC0	A	1	A22	D16
23	15C	2C	EMBEC0	A	1	A23	D17
24	None	None	EMBEC0	A	1	A24	D18
25	9C	10C	EMBEC0	A	1	A25	C7
26	9C	10C	EMBEC0	A	1	A26	C8
27	11C	12C	EMBEC0	A	1	A27	C9
28	13C	14C	EMBEC0	A	1	A28	C10
29	15C	2C	EMBEC0	A	1	A29	C11
30	None	None	EMBEC0	A	1	A30	C12
31	9D	10D	EMBEC0	A	1	A31	C13
32	9D	10D	EMBEC0	A	1	A32	C14
33	11D	12D	EMBEC0	A	1	A33	C15
34	13D	14D	EMBEC0	A	1	A34	C16
35	15D	2D	EMBEC0	A	1	A35	C17
36	None	None	EMBEC0	A	1	A36	C18

Illustrative (Old) Mapping Example



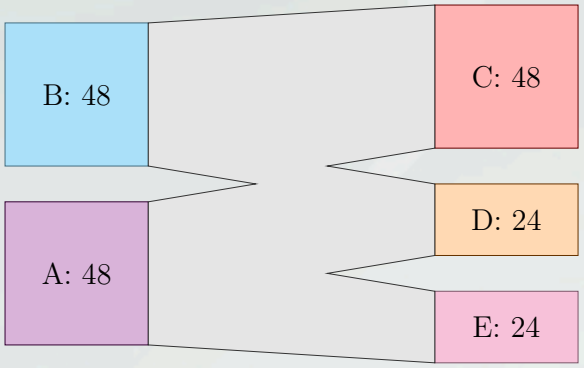


Figure 1: Diagram of ribbon assembly type L1

Fibre	Cell1	Cell2	Type	Side	Octant	L1 In	L1 Out
1	9E	10E	EMBEC1	A	1	B1	C19
2	9E	10E	EMBEC1	A	1	B2	C20
3	11E	12E	EMBEC1	A	1	B3	C21
4	13E	14E	EMBEC1	A	1	B4	C22
5	15E	2E	EMBEC1	A	1	B5	C23
6	None	None	EMBEC1	A	1	B6	C24
7	9F	10F	EMBEC1	A	1	B7	C25
8	9F	10F	EMBEC1	A	1	B8	C26
9	11F	12F	EMBEC1	A	1	B9	C27
10	13F	14F	EMBEC1	A	1	B10	C28
11	15F	2F	EMBEC1	A	1	B11	C29
12	None	None	EMBEC1	A	1	B12	C30
13	None	None	EMBEC1	A	1	B13	C31
14	None	None	EMBEC1	A	1	B14	C32
15	None	None	EMBEC1	A	1	B15	C33
16	None	None	EMBEC1	A	1	B16	C34
17	None	None	EMBEC1	A	1	B17	C35
18	None	None	EMBEC1	A	1	B18	C36
19	9G	10G	EMBEC1	A	1	B19	C37
20	9G	10G	EMBEC1	A	1	B20	C38
21	11G	12G	EMBEC1	A	1	B21	C39
22	13G	14G	EMBEC1	A	1	B22	C40
23	15G	2G	EMBEC1	A	1	B23	C41
24	None	None	EMBEC1	A	1	B24	C42
25	None	None	EMBEC1	A	1	B25	D19
26	None	None	EMBEC1	A	1	B26	D20
27	None	None	EMBEC1	A	1	B27	D21
28	None	None	EMBEC1	A	1	B28	D22
29	None	None	EMBEC1	A	1	B29	D23
30	None	None	EMBEC1	A	1	B30	D24
31	9H	10H	EMBEC1	A	1	B31	C43
32	9H	10H	EMBEC1	A	1	B32	C44
33	11H	12H	EMBEC1	A	1	B33	C45
34	13H	14H	EMBEC1	A	1	B34	C46
35	15H	2H	EMBEC1	A	1	B35	C47
36	None	None	EMBEC1	A	1	B36	C48

The "dead" rows of 6 tacked onto end of C and D connector.

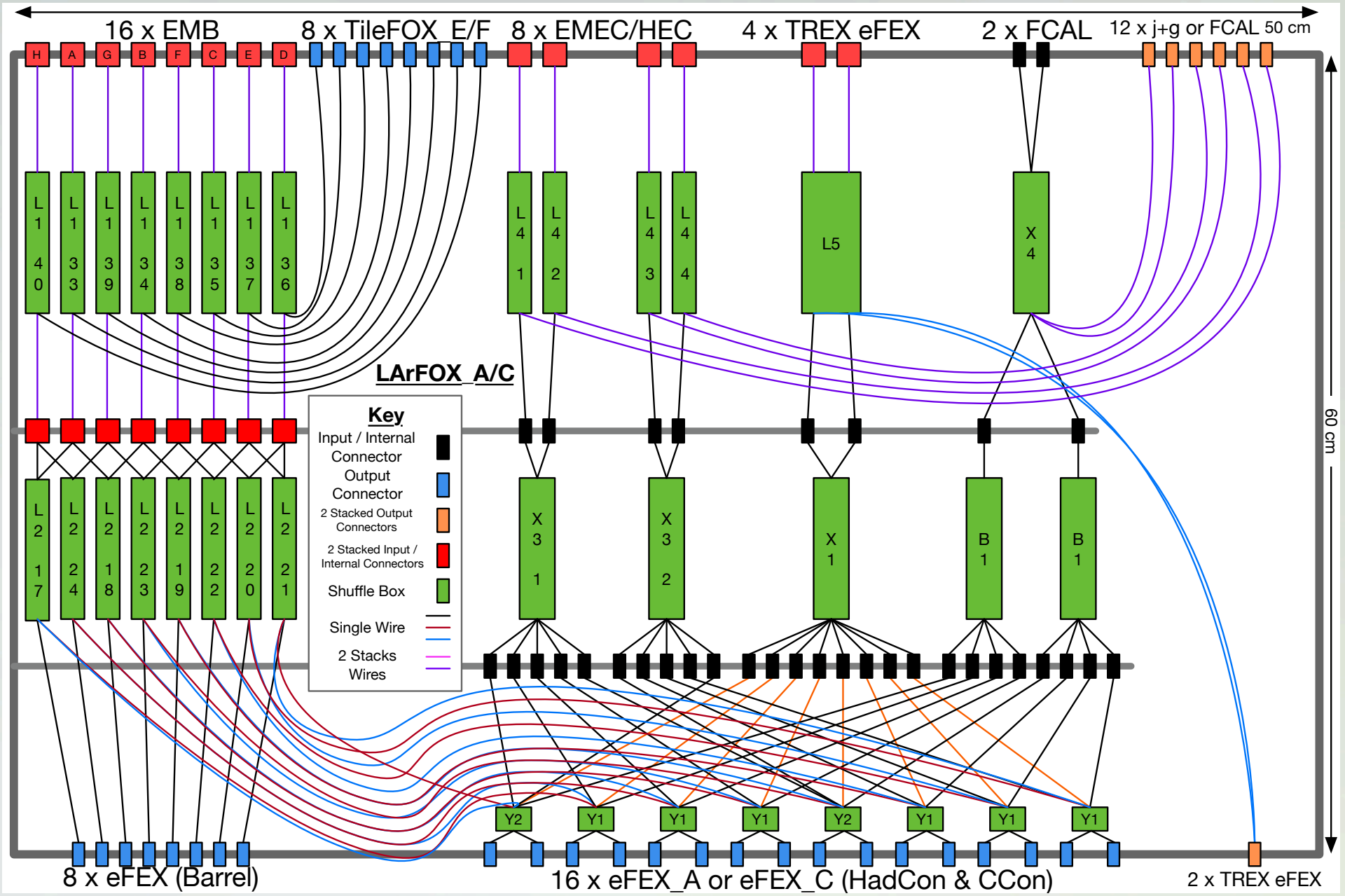
Complete Ribbon Mapping

All 27 Ribbon Types

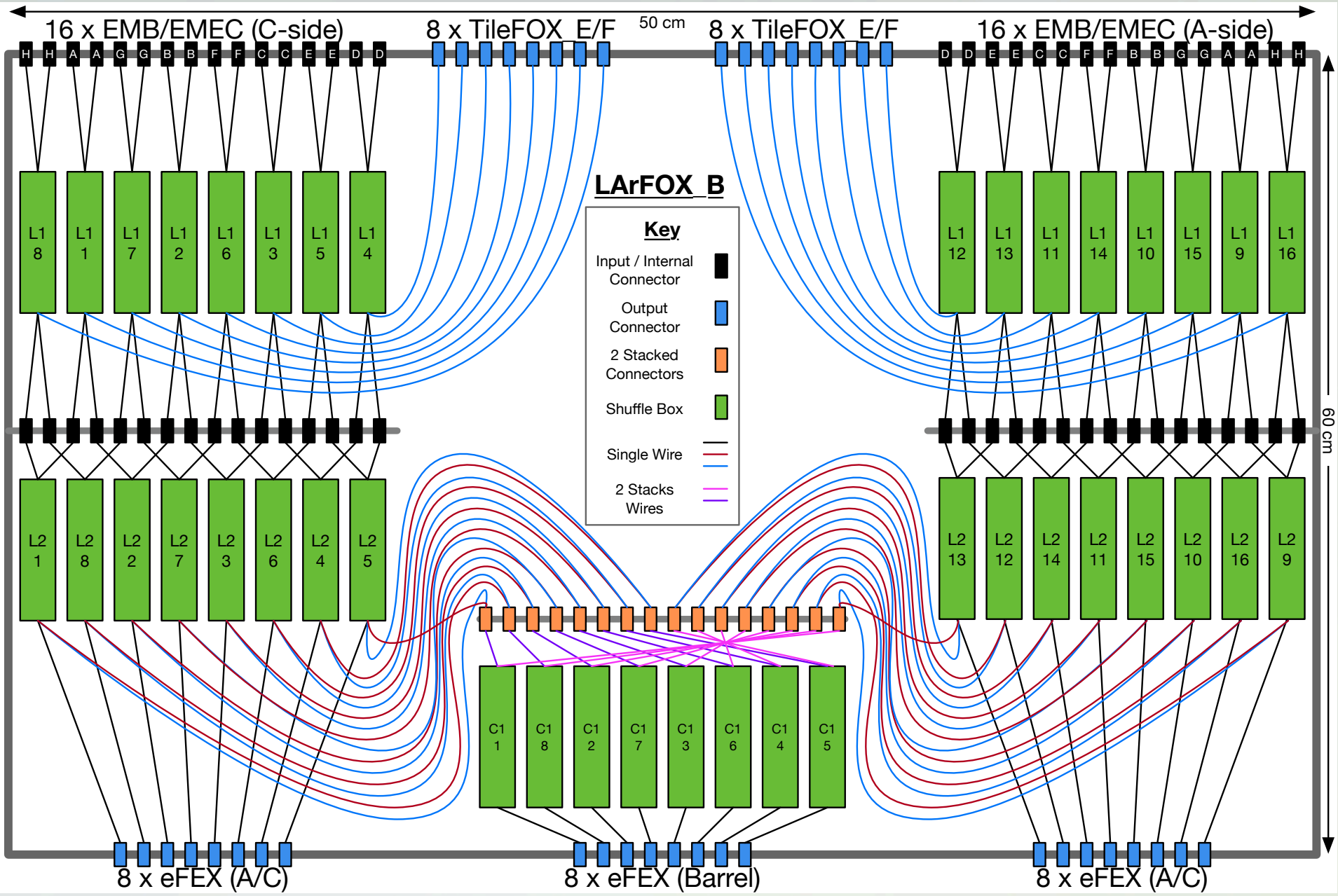
[EDMS Document]

Fibre	FEX	LATOME	Side	Octant	L1 In	L1 Out	Cell1	Cell2	Cell3	Cell4	Cell5	Cell6	Cell7	Cell8	Cell9	Cell10	Cell11	Cell12	Cell13	Cell14	Cell15	Cell16	Cell17	Cell18	Cell19	Cell20	Cell21	Cell22
37	jFEX	EMBEC0	A	1	A37	E1	9A	10A	11A	12A	9B	10B	11B	12B	9C	10C	11C	12C	9D	10D	11D	12D						
38	jFEX	EMBEC0	A	1	A38	E2	9A	10A	11A	12A	9B	10B	11B	12B	9C	10C	11C	12C	9D	10D	11D	12D						
39	jFEX	EMBEC0	A	1	A39	E3	9A	10A	11A	12A	9B	10B	11B	12B	9C	10C	11C	12C	9D	10D	11D	12D						
40	jFEX	EMBEC0	A	1	A40	E4	None	None	None	None	None	None	None	None	None	None	None	None	None	None	None	None						
41	jFEX	EMBEC0	A	1	A41	E5	13A	14A	15A	2A	13B	14B	15B	2B	13C	14C	15C	2C	13D	14D	15D	2D						
42	jFEX	EMBEC0	A	1	A42	E6	13A	14A	15A	2A	13B	14B	15B	2B	13C	14C	15C	2C	13D	14D	15D	2D						
43	jFEX	EMBEC0	A	1	A43	E7	13A	14A	15A	2A	13B	14B	15B	2B	13C	14C	15C	2C	13D	14D	15D	2D						
44	jFEX	EMBEC0	A	1	A44	E8	None	None	None	2A	None	None	None	2B	None	None	None	2C	None	None	None	2D						
45	jFEX	EMBEC0	A	1	A45	E9	None	None	None	None	None	None	None	None	None	None	None	None	None	None	None	None						
46	jFEX	EMBEC0	A	1	A46	E10	None	None	None	None	None	None	None	None	None	None	None	None	None	None	None	None						
47	gFEX	EMBEC0	A	1	A47	E11	9A	10A	11A	12A	9B	10B	11B	12B	9C	10C	11C	12C	9D	10D	11D	gFEX Continuation not shown →						
48	gFEX	EMBEC0	A	1	A48	E12	9A	10A	11A	12A	9B	10B	11B	12B	9C	10C	11C	12C	9D	10D	11D							
37	jFEX	EMBEC1	A	1	B37	E1	9E	10E	11E	12E	9F	10F	11F	12F	9G	10G	11G	12G	9H	10H	11H	12H						
38	jFEX	EMBEC1	A	1	B38	E2	9E	10E	11E	12E	9F	10F	11F	12F	9G	10G	11G	12G	9H	10H	11H	12H						
39	jFEX	EMBEC1	A	1	B39	E3	9E	10E	11E	12E	9F	10F	11F	12F	9G	10G	11G	12G	9H	10H	11H	12H						
40	jFEX	EMBEC1	A	1	B40	E4	None	None	None	None	None	None	None	None	None	None	None	None	None	None	None	None						
41	jFEX	EMBEC1	A	1	B41	E5	13E	14E	15E	2E	13F	14F	15F	2F	13G	14G	15G	2G	13H	14H	15H	2H						
42	jFEX	EMBEC1	A	1	B42	E6	13E	14E	15E	2E	13F	14F	15F	2F	13G	14G	15G	2G	13H	14H	15H	2H						
43	jFEX	EMBEC1	A	1	B43	E7	13E	14E	15E	2E	13F	14F	15F	2F	13G	14G	15G	2G	13H	14H	15H	2H						
44	jFEX	EMBEC1	A	1	B44	E8	None	None	None	2E	None	None	None	2F	None	None	None	2G	None	None	None	2H						
45	jFEX	EMBEC1	A	1	B45	E9	None	None	None	None	None	None	None	None	None	None	None	None	None	None	None	None						
46	jFEX	EMBEC1	A	1	B46	E10	None	None	None	None	None	None	None	None	None	None	None	None	None	None	None	None						
47	gFEX	EMBEC1	A	1	B47	E11	9E	10E	11E	12E	9F	10F	11F	12F	9G	10G	11G	12G	9H	10H	11H	gFEX Continuation not shown →						
48	gFEX	EMBEC1	A	1	B48	E12	9E	10E	11E	12E	9F	10F	11F	12F	9G	10G	11G	12G	9H	10H	11H							

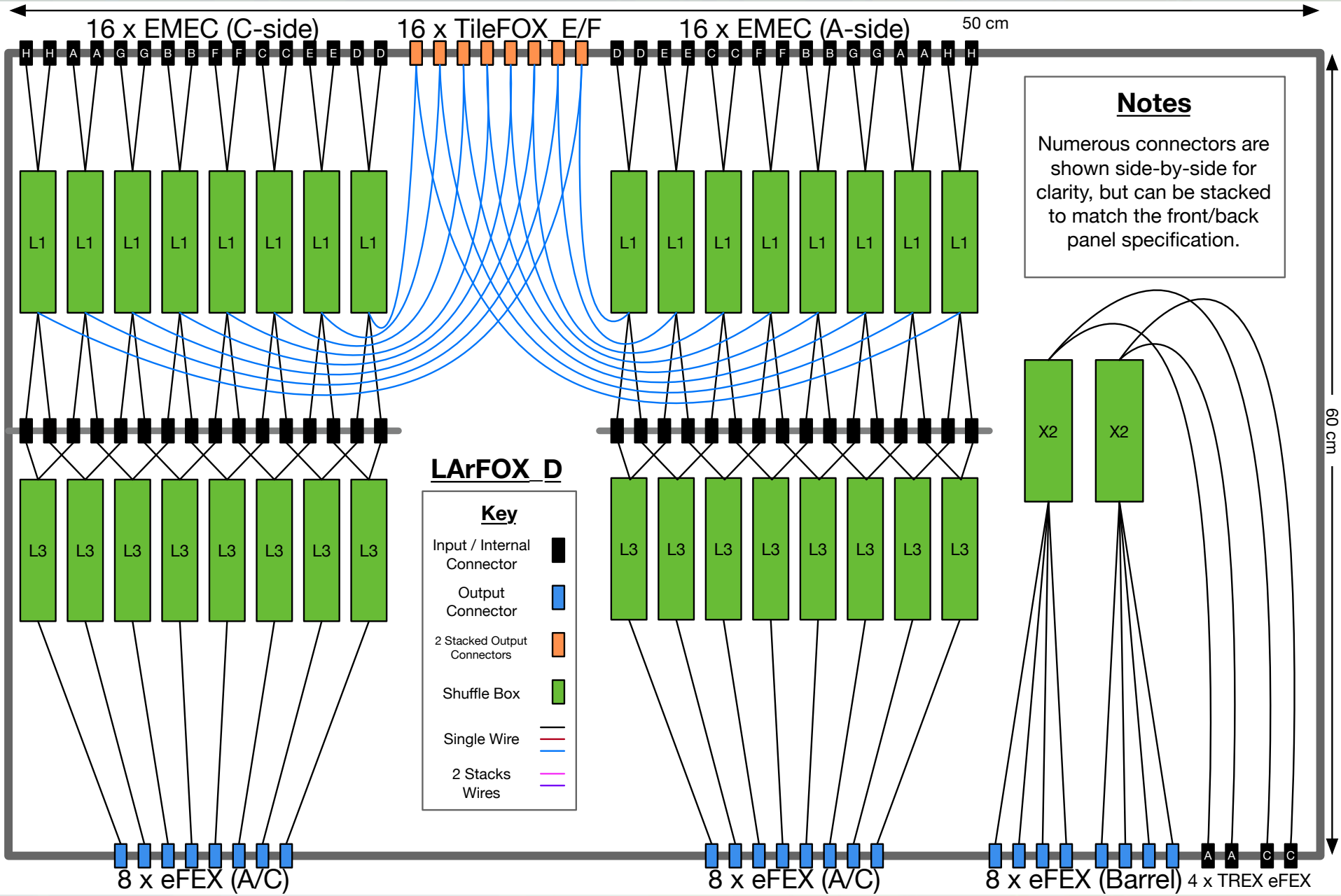
FOX Box Internal Detail


16 x EMB
8 x TileFOX_E/F
8 x EMEC/HEC
4 x TREX eFEX
2 x FCAL
12 x j+g or FCAL 50 cm
H
A
G
B
F
C
E
D
L1 40
L1 33
L1 39
L1 34
L1 38
L1 35
L1 37
L1 36
L41
L42
L43
L44
L5
X4
LArFOX_A/C
Key
Input / Internal Connector
Output Connector
2 Stacked Output Connectors
2 Stacked Input / Internal Connectors
Shuffle Box
Single Wire
2 Stacks Wires
L2 17
L2 24
L2 18
L2 23
L2 19
L2 22
L2 20
L2 21
X31
X32
X1
B1
B1
Y2
Y1
Y1
Y1
Y2
Y1
Y1
Y1
60 cm
8 x eFEX (Barrel)
16 x eFEX_A or eFEX_C (HadCon & CCon)
2 x TREX eFEX

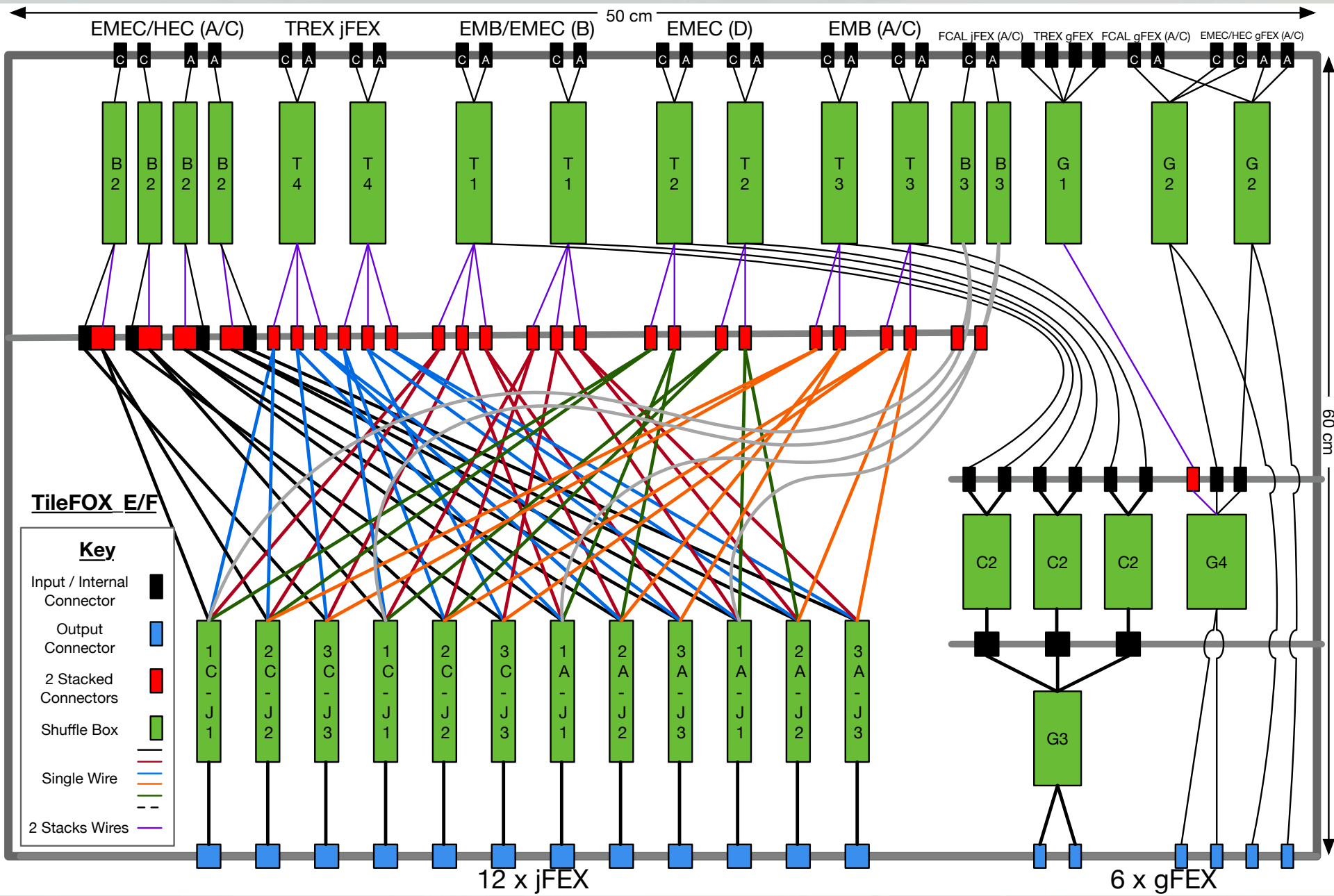
LArFOX_A and LArFOX_C Panel Schematic (Example: C, can be replaced with A)


16 x EMB/EMEC (C-side)
8 x TileFOX_E/F
50 cm
8 x TileFOX_E/F
16 x EMB/EMEC (A-side)
H H A A G G B B F F C C E E D D
D D E E C C F F B B G G A A H H
LAr FOX_B
Key
Input / Internal Connector
Output Connector
2 Stacked Connectors
Shuffle Box
Single Wire
2 Stacks Wires
L1 8
L1 1
L1 7
L1 2
L1 6
L1 3
L1 5
L1 4
L1 12
L1 13
L1 11
L1 14
L1 10
L1 15
L1 9
L1 16
L2 1
L2 8
L2 2
L2 7
L2 3
L2 6
L2 4
L2 5
L2 13
L2 12
L2 14
L2 11
L2 15
L2 10
L2 16
L2 9
C1 1
C1 8
C1 2
C1 7
C1 3
C1 6
C1 4
C1 5
60 cm
8 x eFEX (A/C)
8 x eFEX (Barrel)
8 x eFEX (A/C)

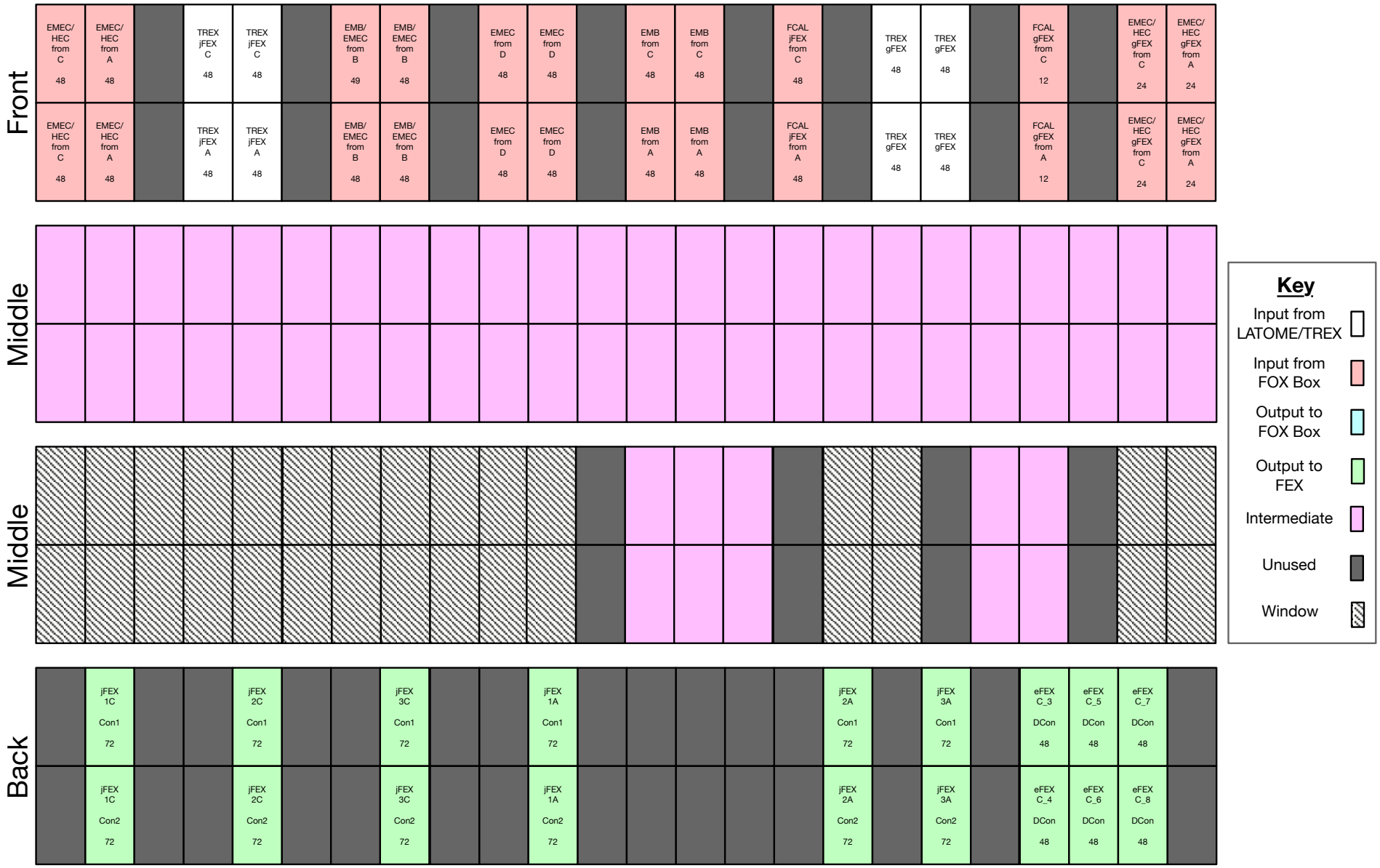
LArFOX_B Panel Schematic


16 x EMEC (C-side)
16 x TileFOX_E/F
16 x EMEC (A-side)
50 cm
60 cm
H H A A G G B B F F C C E E D D
D D E E C C F F B B G G A A H H
L1
L3
X2
LArFOX_D
Key
Input / Internal Connector
Output Connector
2 Stacked Output Connectors
Shuffle Box
Single Wire
2 Stacks Wires
Notes
Numerous connectors are shown side-by-side for clarity, but can be stacked to match the front/back panel specification.
8 x eFEX (A/C)
8 x eFEX (A/C)
8 x eFEX (Barrel)
4 x TREX eFEX
A A C C

LArFOX_D Panel Schematic

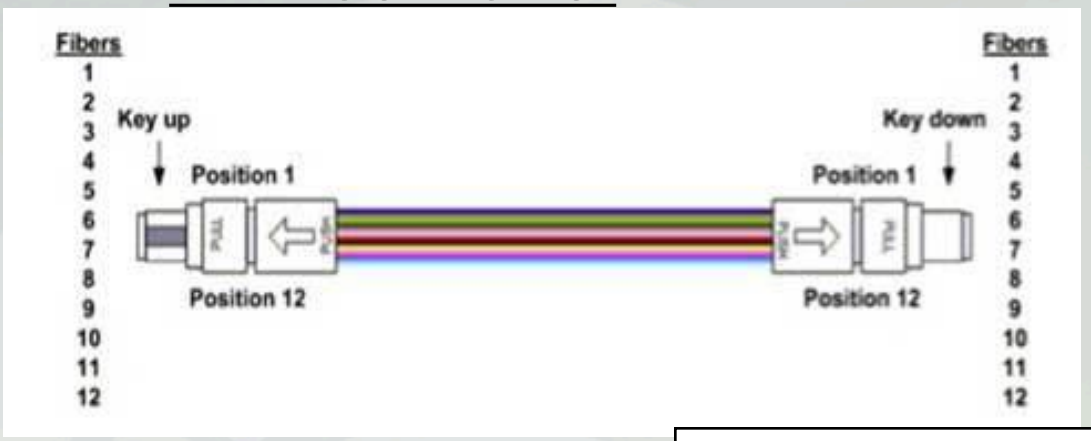

50 cm
EMEC/HEC (A/C)
TREX jFEX
EMB/EMEC (B)
EMEC (D)
EMB (A/C)
FCAL jFEX (A/C)
TREX gFEX
FCAL gFEX (A/C)
EMEC/HEC gFEX (A/C)
60 cm
TileFOX_E/F
Key
Input / Internal Connector
Output Connector
2 Stacked Connectors
Shuffle Box
Single Wire
2 Stacks Wires
12 x jFEX
6 x gFEX

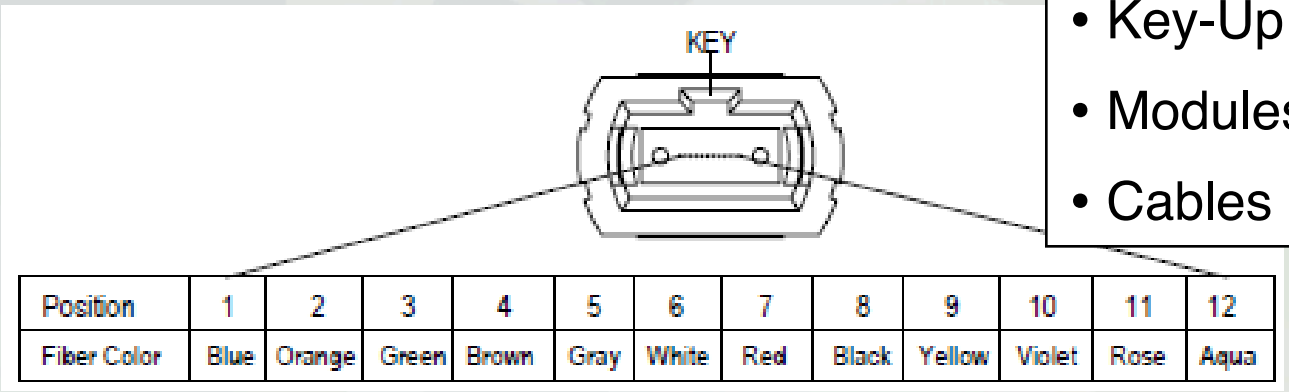
TileFOX_E and TileFOX_F Panel Schematic (Example: E, can be replaced with F)



Output Fibre Order

MTP Connector





Position	1	2	3	4	5	6	7	8	9	10	11	12
Fiber Color	Blue	Orange	Green	Brown	Gray	White	Red	Black	Yellow	Violet	Rose	Aqua

- Key-Up to Key-Down.
- Modules have M-Con.
- Cables have F-Con.

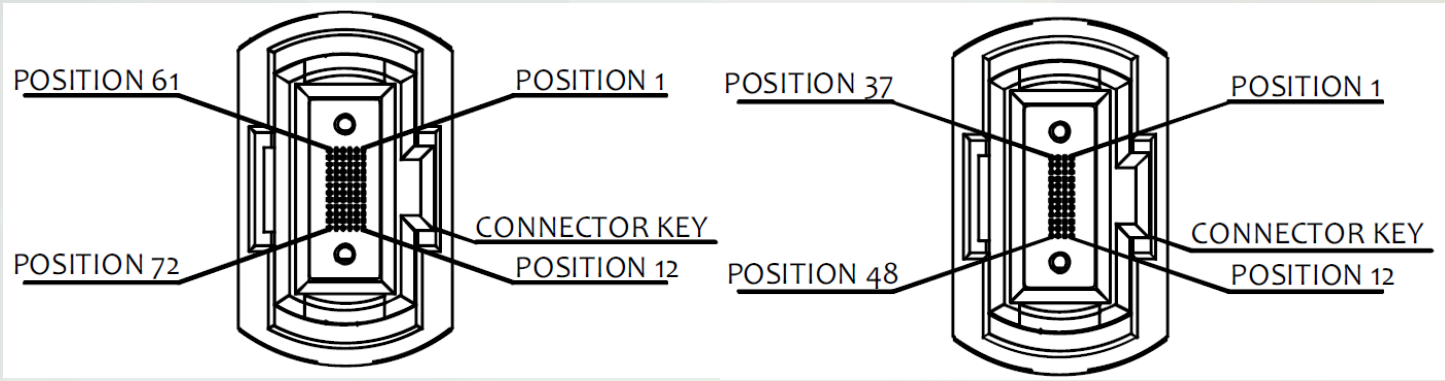


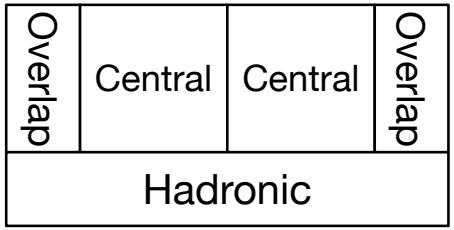
Figure 7: Fiber numbering in 72-fibers female MTP.

Figure 6: Fiber numbering in 48-fibers female MTP.

eFEX Layout, Connectors, and Naming.

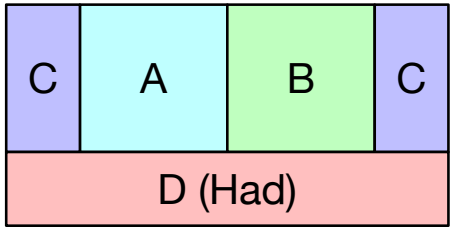
eFEX_C_1	eFEX_B_1	eFEX_A_1
eFEX_C_2	eFEX_B_2	eFEX_A_2
eFEX_C_3	eFEX_B_3	eFEX_A_3
eFEX_C_4	eFEX_B_4	eFEX_A_4
eFEX_C_5	eFEX_B_5	eFEX_A_5
eFEX_C_6	eFEX_B_6	eFEX_A_6
eFEX_C_7	eFEX_B_7	eFEX_A_7
eFEX_C_8	eFEX_B_8	eFEX_A_8

Connector Coverage

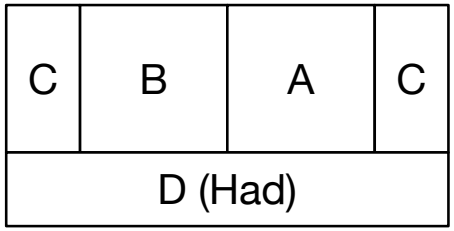


Connector Naming

eFEX_C and eFEX_B



eFEX_A



eFEX C Output Ordering

EM

1	3,7
	4,8
2	5
	6

1	13	25	37
2,4	14,16	26,28	38,40
3,5	15,17	27,29	39,41
6	18	30	42
7	19	31	43
8	20	32	44
9	21	33	45
10	22	34	46

1	13	25	37
2,4	14,16	26,28	38,40
3,5	15,17	27,29	39,41
6	18	30	42
7	19	31	43
8	20	32	44
9	21	33	45
10	22	34	46

37
38,40
39,41
42
43
44
45
46

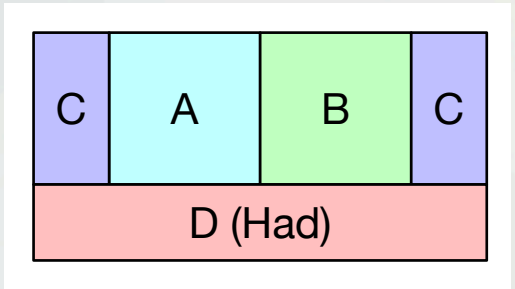
Had

7	1,5	3,6	13,17	1,5	15,18	25,29	27,30
8	2	4	14	2	16	26	28

9-36, 47-48: Spare

9-12, 19-24, 31-48: Spare

Spare = Dark Fibre



eFEX B Output Ordering

EM

1	1	13	25	37	1	13	25	37	37
2,4	2,4	14,16	26,28	38,40	2,4	14,16	26,28	38,40	38,40
3,5	3,5	15,17	27,29	39,41	3,5	15,17	27,29	39,41	39,41
6	6	18	30	42	6	18	30	42	42
7	7	19	31	43	7	19	31	43	43
8	8	20	32	44	8	20	32	44	44
9	9	21	33	45	9	21	33	45	45
10	10	22	34	46	10	22	34	46	46

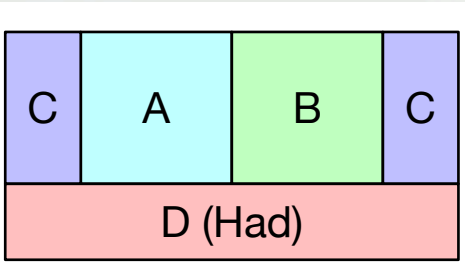
Had

1	4	13	16	25	28
2	5	14	17	26	29
3	6	15	18	27	30

11-36, 47-48: Spare

7-12, 19-24, 31-48: Spare

Spare = Dark Fibre



jFEX Layout, Connectors, and Naming.

jFEX_1C Con1	jFEX_2C Con1	jFEX_3C Con1	jFEX_3A Con1	jFEX_2A Con1	jFEX_1A Con1
jFEX_1C Con2	jFEX_2C Con2	jFEX_3C Con2	jFEX_3A Con2	jFEX_2A Con2	jFEX_1A Con2
jFEX_1C Con3	jFEX_2C Con3	jFEX_3C Con3	jFEX_3A Con3	jFEX_2A Con3	jFEX_1A Con3
jFEX_1C Con4	jFEX_2C Con4	jFEX_3C Con4	jFEX_3A Con4	jFEX_2A Con4	jFEX_1A Con4

EM

1	2	3	4	5	6
7	8	9	10	11	12
13	14	15	16	17	18
19	20	21	22	23	24

J1 (1C/1A) Output Ordering

Had

25	27	29	31	49	33	35
26	28	30	32		34	36
37	39	41	43	50	45	47
38	40	42	44		46	48

51-72 Spare

Spare = Dark Fibre

EM

1	2	3	4	5	6
7	8	9	10	11	12
13	14	15	16	17	18
19	20	21	22	23	24

J2 (2C/2A) Output Ordering

Had

25	27	49	29	31	33	35
26	28		30	32	34	36
37	39	50	41	43	45	47
38	40		42	44	46	48

51-72 Spare

Spare = Dark Fibre

EM

1	2	3	4	5	6
7	8	9	10	11	12
13	14	15	16	17	18
19	20	21	22	23	24

J3 (3C/3A) Output Ordering

Had

49	25	27	29	31	33	35
	26	28	30	32	34	36
50	37	39	41	43	45	47
	38	40	42	44	46	48

51-72 Spare

Spare = Dark Fibre

gFEX Layout, Connectors, and Naming.

EM+Had +FCAL Con gFEX5 $\eta < -2.5$	**EM** Con gFEX1 $-2.4 < \eta < 0.0$ **Had** Con gFEX3 $-2.5 < \eta < 0.0$	**EM** Con gFEX2 $0.0 < \eta < 2.4$ **Had** Con gFEX4 $0.0 < \eta < 2.5$	**EM+Had +FCAL** Con gFEX6 $\eta > 2.5$

Only one gFEX, so name the connectors.

EM

1	9	17
2	10	18
3	11	19
4	12	20
5	13	21
6	14	22
7	15	23
8	16	24
25	33	41
26	34	42
27	35	43
28	36	44
29	37	45
30	38	46
31	39	47
32	40	48

Had

9	1	2	3	4
10				
11				
12				
13	5	6	7	8
14				
15				
16				
33	25	26	27	28
34				
35				
36				
37	29	30	31	32
38				
39				
40				

gFEX_1/2 (EM) G3-Type

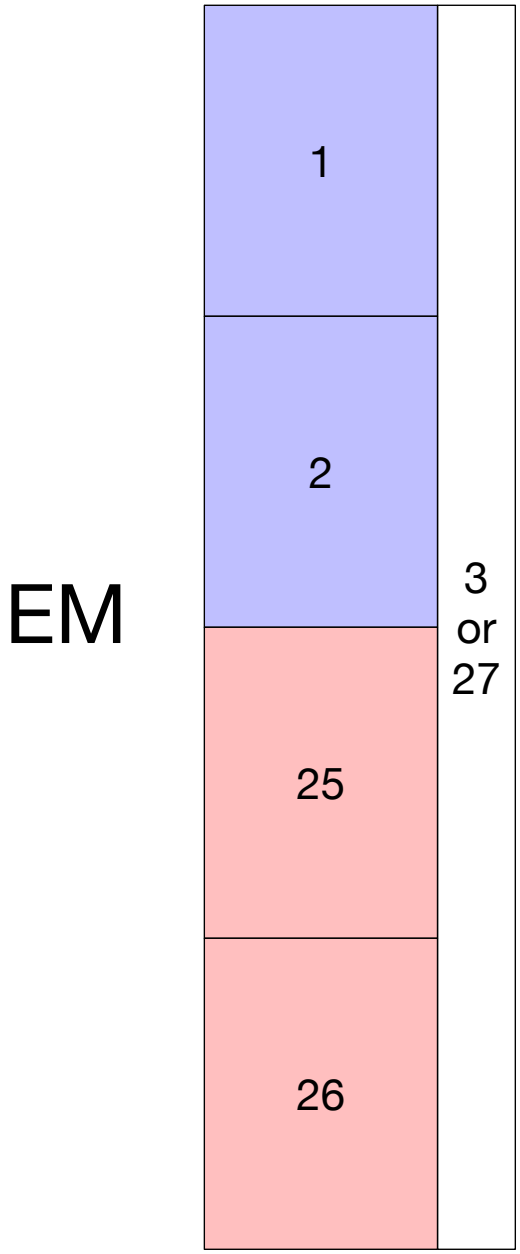
- Part 1 (24w)
- Part 2 (24w)

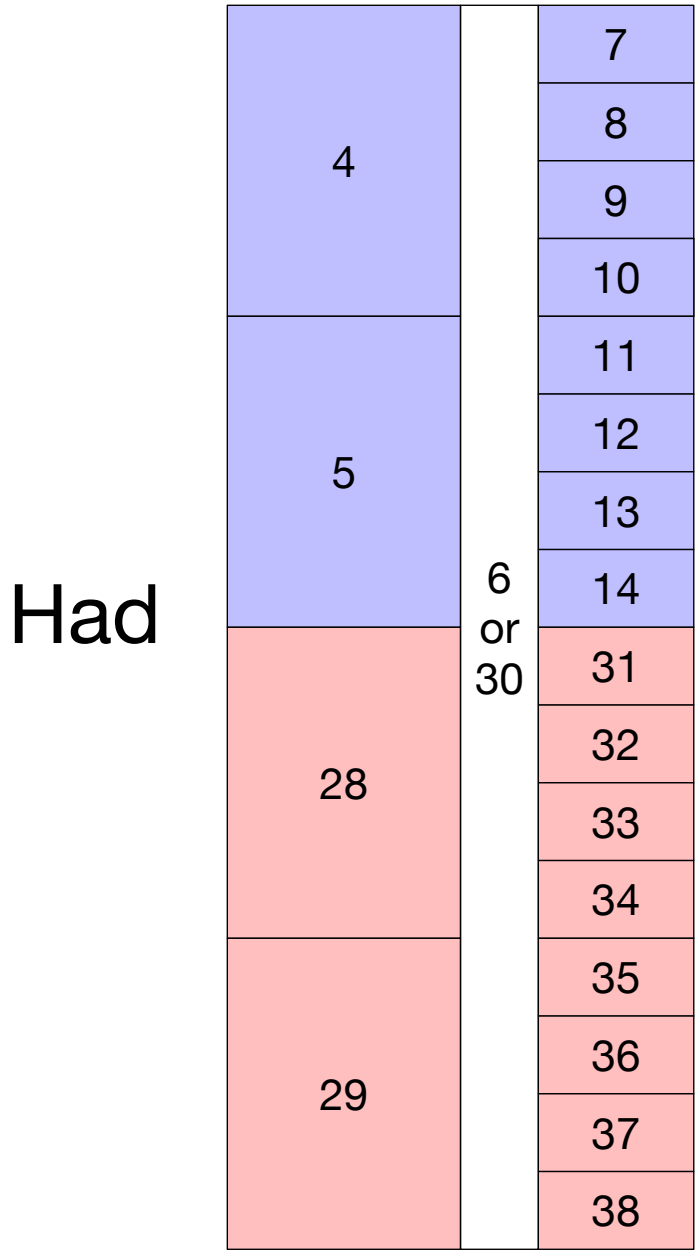
gFEX_3/4 (Had) G4-Type

- Part 1 (24w)
  - 17-24: Spare
- Part 2 (24w)
  - 41-48: Spare

Output Ordering

gFEX_5/6 G2-Type Output Ordering



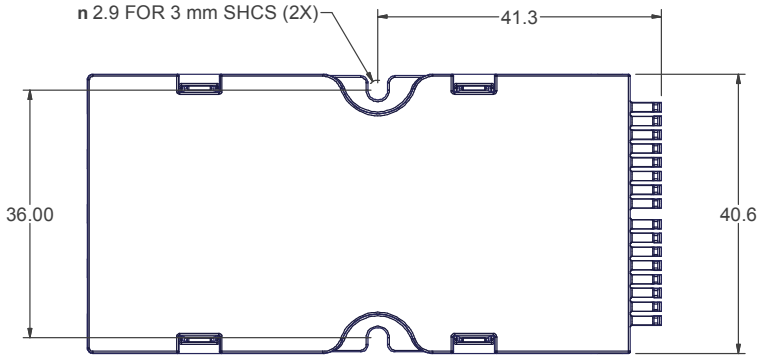


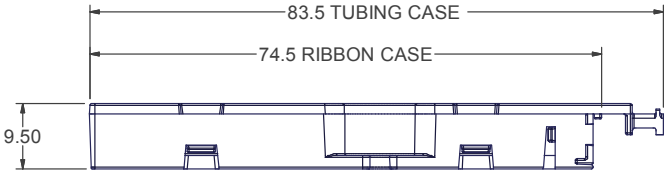
Part 1 (24w)
15-24: Spare

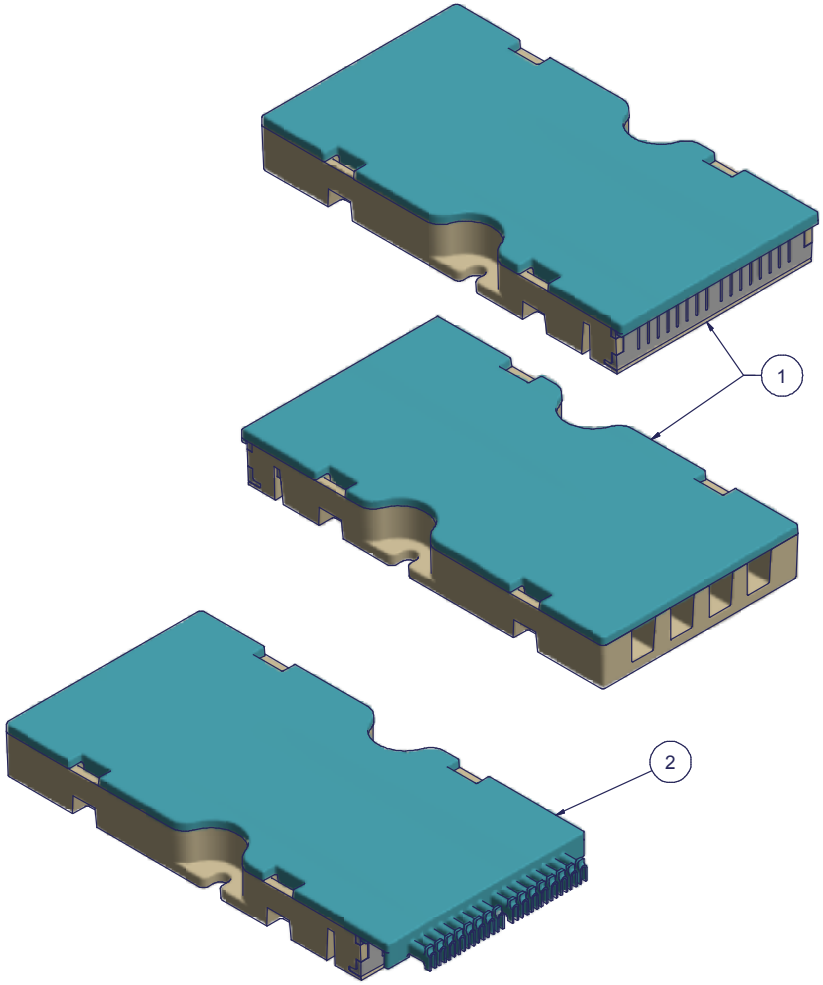
Part 2 (24w)
39-48: Spare

FOX Box and Assembly Mechanical Details

P/N	DESCRIPTION
18872	CASE FOR RIBBON
18913	CASE FOR ROUND TUBING







PRELIMINARY

▲ DENOTES CRITICAL DIMENSION

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Material:

REV	DATE	DESCRIPTION	ECN
X1	X/XX/17	-	XXXX-xx

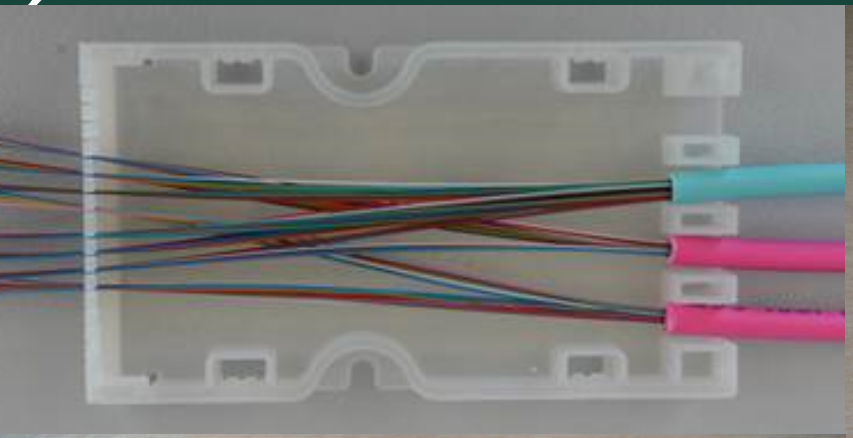
CUSTOMER DRAWING
DIMENSIONS FOR REFERENCE ONLY
THIRD ANGLE PROJECTION
METRIC/mm

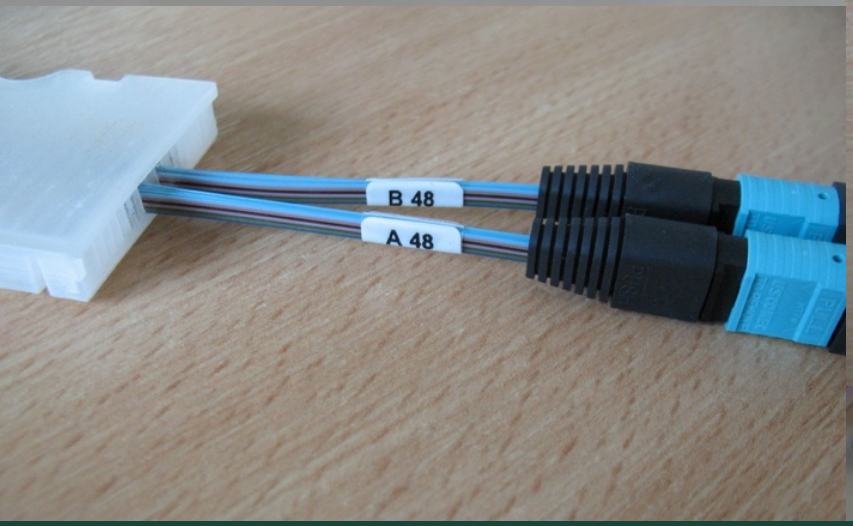
USCONEC
Hickory, NC
800-769-0944
www.usconec.com

TITLE: CASE, SHUFFLE

SIZE	S&M Part No.:	DWG NO	REV
A3	SEE TABLE	C18872	X1

SCALE	Drafter	Date:	SHEET	OF
N.T.S.	craigconrad	4/19/2017	1	1





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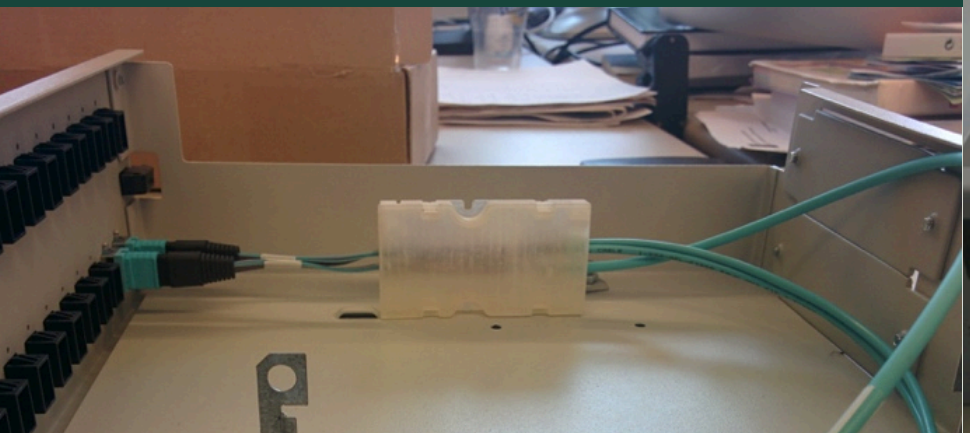


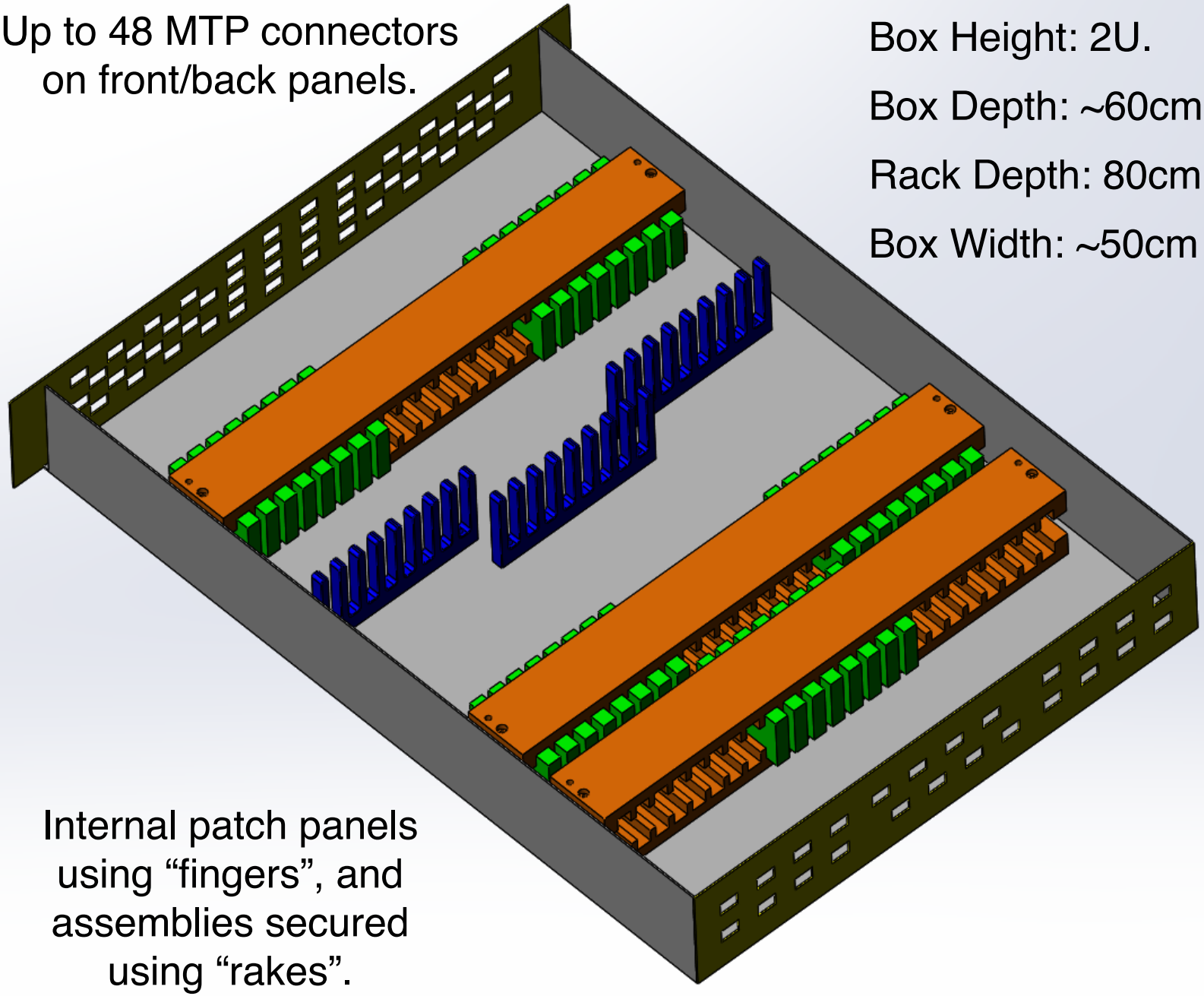
Up to 48 MTP connectors on front/back panels.

Box Height: 2U.

Box Depth: ~60cm

Rack Depth: 80cm

Box Width: ~50cm



Internal patch panels using “fingers”, and assemblies secured using “rakes”.

Testing and Validation

- Assembly/Ribbon Mapping.
  - On Paper: DONE. Checks logical mapping of each ribbon type.
  - Automatic: IN PROGRESS. Test program to build the FOX virtually, test every mapping connection of every ribbon from beginning to end.
  - Physical Subset: NOT STARTED. Order small set of ribbons to have a limited pass-through of the FOX, test mapping and light loss.
  - Final: NOT STARTED. Once full order + spares arrive, test at least one of each ribbon-type, as well as per box / total pass through.
- Light loss, connectivity, etc.
  - Done at Physical Subset, and Final stages.
- Mechanical boxes.
  - Ribbon mock-ups used initially to design box parameters.
  - Physical Subset used to confirm box design.
  - Design/Building at MSU allows for changes to be made as needed.

Timeline

- Mid-October: Initial Cost Estimate for Full system from Sylex.
- Early November: First metal box (LArFOX B) produced at MSU. L1Calo Review, to get approval to order subset of assemblies for physical tests.
- December: All metal boxes produced at MSU (LArFOX A/C, LArFOX D, TileFOX E/F). Narrow pass through for all boxes arrives at MSU, i.e. an adequate subset (and spares) of assemblies to test mapping and light loss tests.
- End of January: Assembly and Tests done at MSU (as described above).
- February: Show results in L1Calo Meeting / PRR, and seek approval to order all remaining components from Sylex.
- March-April: Components arrive at CERN.
- April-May: Assembly and testing at CERN, i.e. octopus cables connected to test all mapping paths, some light loss tests of the whole system, possibly even connection to some real latome and FEXs on the surface for full test. At this point, official task completed.
- Afterwards: Provide "7th" box for Surface Test Facility to use, containing a simple set of ribbons that go from a Latome to a variety of FEXs.
- Fall-Back time allowed in the schedule: 3 months.