Si5338 Reference Manual: Configuring the Si5338 Without ClockBuilder Desktop

This document replaces "AN411: Configuring the Si5338 without ClockBuilder Desktop"

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1. Introduction

The Si5338 is a highly flexible and configurable clock generator/buffer. A block diagram of the Si5338 programmable clock IC is shown in Figure 1.

To support the flexibility, Silicon Labs has created ClockBuilder Desktop to create register maps automatically and easily for a given configuration. Since programming with ClockBuilder Desktop may not always be well suited to every system's requirements, this document presents the procedures and equations for determining a complete register set from a frequency plan.

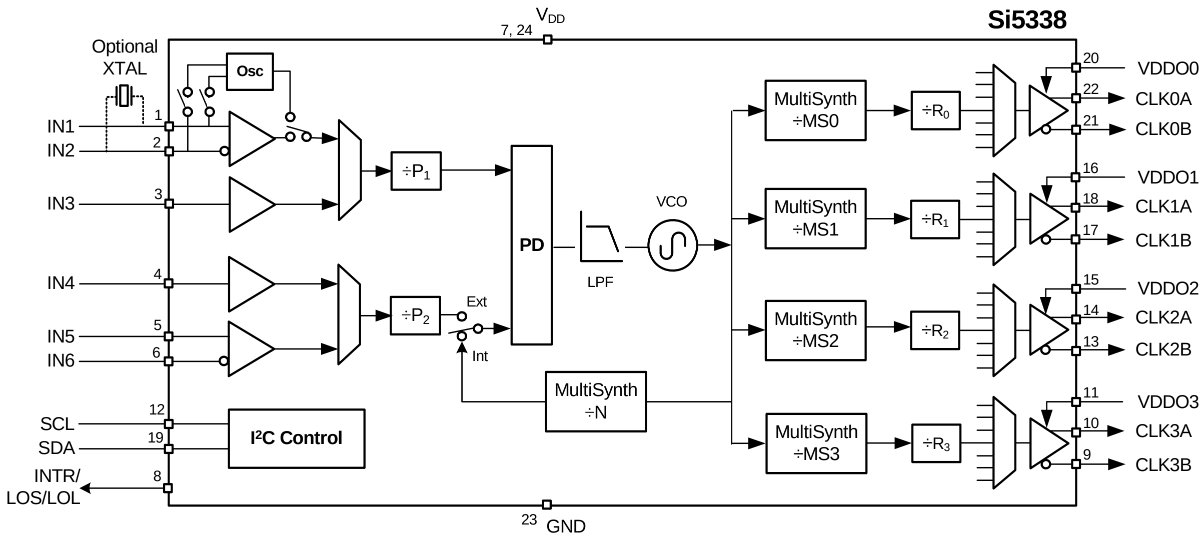


Figure 1. Si5338 Block Diagram

The device may have a factory defined default configuration stored in non-volatile memory (NVM). During powerup, the default configuration is copied into random access memory (RAM). Having its working configuration stored in RAM allows in-system configuration changes through the I^2C port. The memory configuration of the Si5338 is shown in Figure 2.

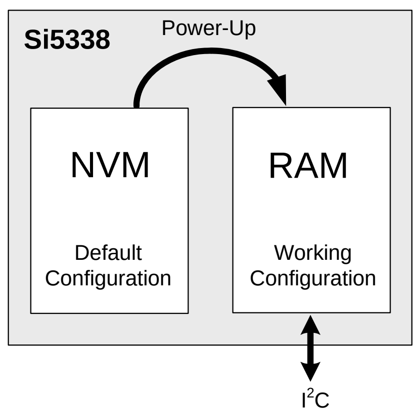


Figure 2. Si5338 Memory Configuration

This application note provides details on configuring the Si5338 by accessing its RAM space through the I^2C bus.

2. Overview of Configuring the Si5338

In order to replicate the functionality of ClockBuilder Desktop, a full register map must be created for all desired features. To create the register map, the programmer must perform the following steps:

1. Configure the clock multiplexors.
   - See "4. Configuring The Input Selection" on page 12.
2. Determine the divider values for the desired input and output frequencies.
   - See "5. Configuring PLL Parameters" on page 15.
3. Configure the frequency and/or phase inc/dec feature (if needed).
   - See "6. Configuring the Frequency Increment/Decrement" on page 16.
   - See "7. Configuring Initial Phase Offset and Phase Step Size" on page 17.
4. Configure spread spectrum (if needed).
   - See "8. Configuring Spread Spectrum" on page 19.
5. Set the output driver format and supply voltage.
   - See "9. Configuring the Output Drivers" on page 22.
6. Assemble the register map.
   - See "10. Si5338 Registers" on page 28.
7. See "10.2. Miscellaneous Register Writes" on page 28 for additional registers that need to be set.

With the assembled register map, follow the procedure in Figure 9 of the Si5338 data sheet.

3. Configuring the Si5338

For the Si5338, the frequency plan is derived from the desired input/output frequencies and desired performance. Once the frequencies are known, one can use the following example method for determining the frequency divider ratios. Once the divider ratios are determined, use the equations to convert the divider ratios into values the device can understand. Silicon Labs strongly suggests that the fully-configured register map be loaded into an Si5338 device and fully tested before ordering pre-programmed devices.

3.1. Example Method for Finding MultiSynth Values for an Si5338 Frequency Plan

The following procedure finds all combinations of MultiSynth values that satisfy the frequency plan.

1. Select a lowest P1 ratio that divides the input frequency (CLKIN) to 40 MHz or less. This is the phase detector input frequency. If the input frequency is from a crystal, the P1 divider is 1.
2. For all the output frequencies, if an output frequency is less than 5 MHz, find the lowest R divider value that increases the output frequency of the MultiSynth to greater than or equal to 5 MHz. Keep these R values. The goal is to get the actual MultiSynth output frequencies and ensure they are in range.
3. Calculate the output frequency of the MultiSynth for the highest performance frequency:
   MultiSynth output frequency = corresponding R value × desired output frequency
   a. The highest performance frequency refers to the clock output where jitter must have the lowest value. The procedure assumes that an integer divider from the VCO will produce the best performance.
4. Collect divider ratios for that yield an integer ratio for the highest performance MultiSynth output. Iterate over all even-numbered divider values between 4 and 568:
   a. Calculate possible f_{vco}:
      f_{vco} = highest performance MultiSynth output frequency × current integer divider
   b. If the f_{vco} value is in range, keep the divider value.
5. Calculate remaining divider ratios for all the solutions found in Step 4.
   a. f_{vco} = Highest-performance MultiSynth output frequency × current divider value
   b. MSn = f_{vco} ÷ phase detector frequency
   c. For all the other MultiSynth output frequencies:
      i. Calculate the corresponding MultiSynth value:
         MultiSynth = f_{vco} ÷ (MultiSynth output frequency × corresponding R divider value)
      ii. If the current MultiSynth value is less than 8 and not 4 or 6, then this plan is invalid. Do not keep. Otherwise, it is a valid plan.

3.1.1. VCO Limitations Impact Achievable Output Frequencies

The range of the f_{vco} is 2.2 to 2.84 GHz. The valid output frequency ranges above f_{vco} divided by 8 are set by the dividers of 4 and 6 and the f_{vco} range such that:

- 2.2 GHz ÷ 6 = 366 2/3 MHz
- 2.84 GHz ÷ 6 = 473 1/3 MHz
- 2.2 GHz ÷ 4 = 550 MHz
- 2.84 GHz ÷ 4 = 710 MHz

There is only one f_{vco} available that can produce the frequencies in the given ranges. For example, to get 600 MHz output use:

f_{vco} = output frequency × MultiSynth divider

f_{vco} = 600 MHz × 4 = 2.4 GHz

If the MultiSynth divider is 6, then the f_{vco} is out of range at 3.6 GHz. So 4 is the only valid divider. The procedure in the previous section comprehends these restrictions.

Note: Spread spectrum clocking and phase and frequency adjustments cannot be used on output frequencies greater than f_{vco} divided by 8.

3.1.2. Sorting the Frequency Plans to Minimize Jitter

The following guidelines help to sort the frequency plans:

1. Use MSn divider values that are integers as much as possible.
2. Look for a MultiSynth value that is an integer on important output channels or frequencies.
3. Pick plans with VCO frequencies (f_{vco}) close to 2.5 GHz.

3.1.3. Using Fractions to Store the MultiSynth Values

One possible problem, when implementing this algorithm, is losing precision or introducing rounding errors in the calculations. To prevent this and to better model the operation of the MultiSynths, use a data structure where the type will have three parts: integer or whole number, numerator and denominator. Using 64-bit unsigned numbers yields high precision in the fraction and more than what the Si5338 supports. Additionally, use this data structure to store the input and output frequencies, MultiSynth values, VCO frequency, and phase detector frequency. Operations like addition, subtraction, division, multiplication, simplifying the fraction, and even comparisons like equal-to, greater-than and less-than are necessary to implement the algorithm.

3.1.4. Truncating MultiSynth Values

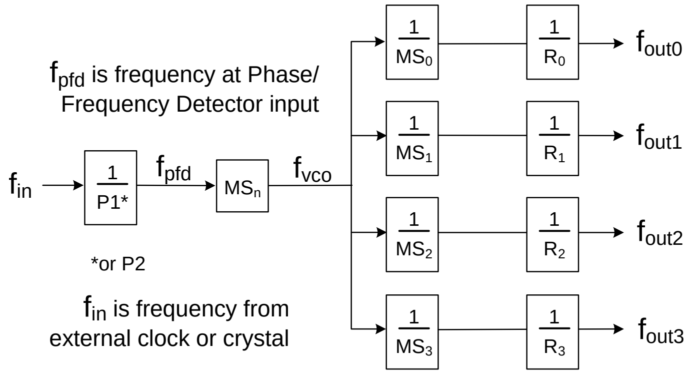
If the MultiSynth reduced fractional values (numerator and denominator) do not fit in the corresponding bit fields in the register map, truncation is necessary. Truncation implies that some of the desired frequencies are not achievable with the specified precision.

First check if the MSn divider needs to be truncated (that is, the numerator or denominator of MSn is greater than $2^{30} – 1$). If it does, truncate the f_{vco} and recalculate the MSn. The f_{vco} should stay within the allowed range.

When the MultiSynth dividers (MSx) are calculated after the f_{vco} is calculated with the above procedure, check if the dividers need to be truncated (the numerator or denominator is greater than $2^{30} – 1$). If so, divide the numerator and denominator of the affected MultiSynth by 2 until both the numerator and denominator fit (this is equivalent to bit-shifting to reduce the length of the variable to 30 bits). The division can be done on the actual MultiSynth values, not the P2 or P3 numbers for the registers. Of course, the denominator should not be zero.

3.2. Calculating MultiSynth Values

Because of its flexibility, the Si5338 uses several parameters to determine the final output frequency. A summary of these parameters is shown in Figure 3.



$$f_{pfd} = \frac{f_{in}}{P_1} \qquad f_{vco} = f_{pfd} \cdot MSn \qquad f_{outx} = \frac{f_{vco}}{MS_x \cdot R_x}$$

$$2.2\text{GHz} <= f_{vco} <= 2.84\text{GHz}$$

$$5\text{MHz} <= f_{pfd} <= 40\text{MHz}$$

Figure 3. Frequency Plan Parameters

When the MS0,1,2,3 output is $f_{vco}/4$ or $f_{vco}/6$ the following functions are not available:

1. Frequency Increment/Decrement
2. Phase Increment/Decrement
3. Spread Spectrum

In order for an output to be at a frequency of fvco/4 or fvco/6, a bit in Register51[7:4] must be set. See the description for these bits in "10. Si5338 Registers" on page 28. In some cases, a very slight improvement in output jitter may be obtained by setting MSn (feedback MultiSynth) to an integer value. All the output jitter specifications in the data sheet were based upon characterization data with a 25 MHz PFD input. In general, the higher the PFD input frequency the lower the jitter on the output clock.

Once MSn and MSx values have been determined, they must be converted to their digital representations and written to the appropriate registers. The conversion for these are shown in Equation 1.

$$\text{Let MSn or MSx} = a + \frac{b}{c} \qquad \text{Where } a = 4, 6, 8, 9 \ldots 567, \quad b = 0 \ldots (2^{30} - 1), \quad c = 1 \ldots (2^{30} - 1)$$

Note: When MSn or MSx is an integer, you must set b = 0 and c = 1

$$MSx\_P1 = \text{Floor}\left(\frac{(a * c + b) * 128}{c} - 512\right)$$

$$MSx\_P2 = \text{Mod}\left(b * 128 , c\right)$$

$$MSx\_P3 = c$$

Note: The Floor function rounds down to the closest integer value.
Mod(b*128,c) returns the remainder of b*128/c

Example:

a + b/c = 99.5328 a = 99, b=333, c=625

MSx_P1 = 12228 (0x02FC4)
MSx_P2 = 124 (0x0000007C)
MSx_P3 = 625 (0x00000271)

Alternately let a = 99, b = 5328, c=10000

MSx_P1 = 12228 (0x02FC4)
MSx_P2 = 1984 (0x0000007C0)
MSx_P3 = 10000 (0x000002710)

Both results can be used to program the Si5338
because in both cases b/c = .5328

Equation 1. Frequency Programming

Register values for MSx_P1, MSx_P2, and MSx_P3 must be written to the appropriate registers as shown in Figure 4 and Figure 5. To ensure that the MultiSynth is properly configured, it is recommended to write all bytes (even ones that are zero) associated with MSx_P1, MSx_P2, and MSx_P3. This will ensure that previous configurations are completely overwritten.

Note: MSx_P1, MSx_P2, and MSx_P3 were named INT, NUM, and DEN in an earlier version of this document. Because the values are not equal to the integer, numerator, and denominator, the names have been changed. The equations are identical.

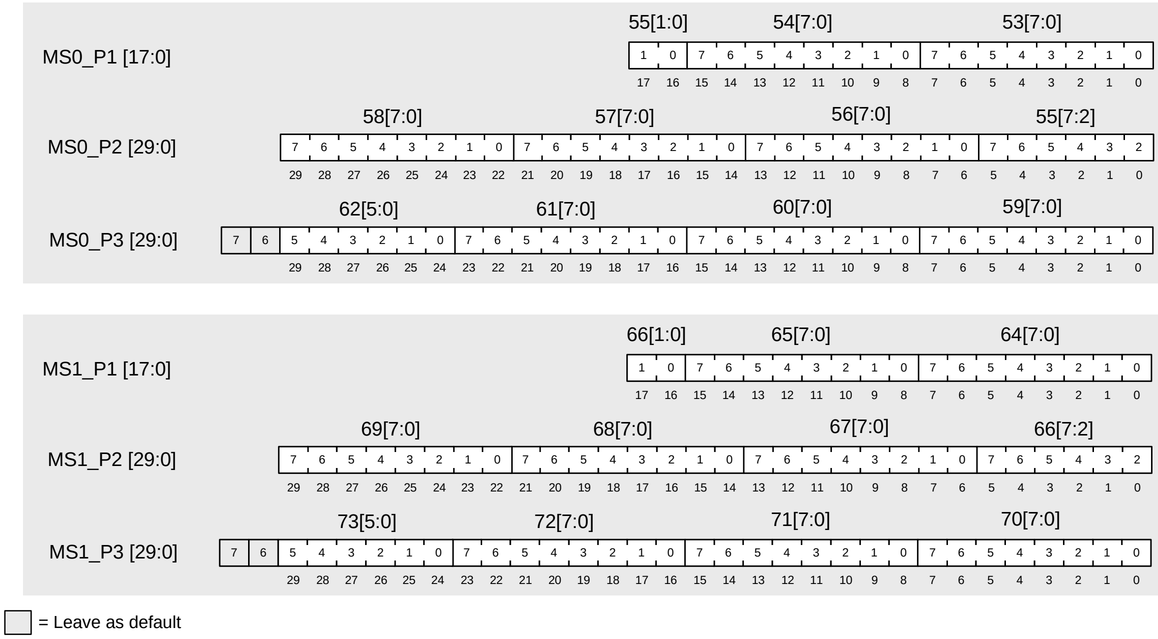


Figure 4. MultiSynth Registers (MS0, MS1)

Figure 5. MultiSynth Registers (MS2, MS3, MSN)

4. Configuring The Input Selection

The Si5338 is capable of locking to a single-ended clock, a differential clock, or an external crystal resonator (XTAL). The XTAL allows the Si5338 to generate its own free-running reference clock. A block diagram of the input configuration of the Si5338 is shown in Figure 6. The Si5338 uses pins IN1/IN2, or IN3 as its main input. Inputs IN5/IN6, and IN4 can serve as an external feedback path for zero delay mode, or as additional clock inputs if the device is operating in internal feedback mode.* The following sections describe how each of the inputs are configured.

***Note:** Only Si5338N/P/Q devices allow IN4 to be used as a single-ended clock input.

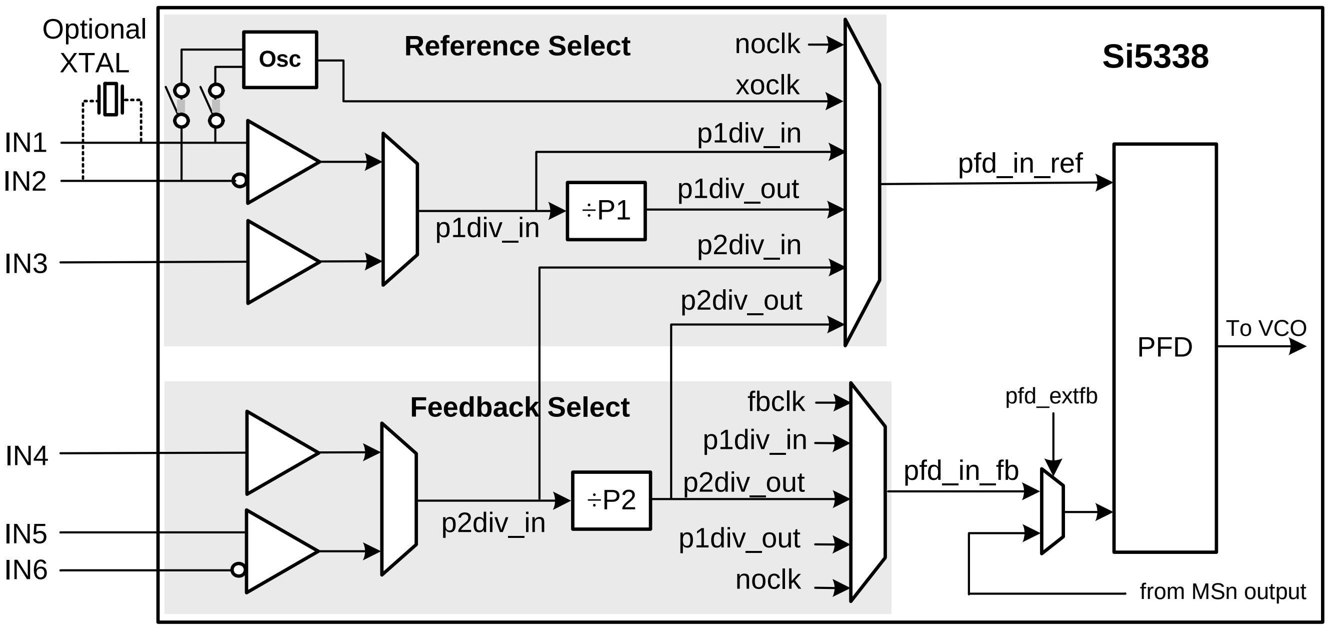


Figure 6. Si5338 Input Selection Block Diagram

4.1. Reference Clock Select

In this section, the configurations for all the muxes within the Reference Select area of Figure 6 are described.

Register	7	6	5	4	3	2	1	0
28[7:0]	1	0		P1DIV_IN[2:0]			XTAL_FREQ[1:0]	
29[7:0]				P1DIV_IN[4:3]				

Crystal Frequency	XTAL_FREQ[1:0]
26 MHz < Fxtal <= 30 MHz	11
19 MHz < Fxtal <= 26 MHz	10
11 MHz < Fxtal <= 19 MHz	01
8 MHz < Fxtal <= 11 MHz	00

Reference Clock	P1DIV_IN[4:3]	P1DIV_IN[2:0]
IN1/IN2 (differential)	00	000
IN1/IN2 (XTAL)*	10	101
IN3 (single-ended)	01	010

* If IN1/IN2 (XTAL) is selected, XTAL_FREQ must be configured. Otherwise XTAL_FREQ is a don't care

Register	7	6	5	4	3	2	1	0
29[7:0]	PFD_IN_REF[2:0]					P1DIV[2:0]		
30[7:0]	PFD_IN_FB[2:0]					P2DIV[2:0]		

Input to PFD Reference Side	PFD_IN_REF[2:0]
p1div_in (refclk)	000
p2div_in (fbclk)	001
p1div_out (divrefclk)	010
p2div_out (divfbclk)	011
xoclk	100
noclk	101

Input to PFD Feedback Side	PFD_IN_FB[2:0]
p2div_in (fbclk)	000
p1div_in (refclk)	001
p2div_out (divfbclk)	010
p1div_out (divrefclk)	011
reserved	100
noclk	101

P1 divider setting	P1DIV[2:0]
/1	000
/2	001
/4	010
/8	011
/16	100
/32	101

P2 divider setting	P2DIV[2:0]
/1	000
/2	001
/4	010
/8	011
/16	100
/32	101

Figure 7. Reference Input Configuration Registers

4.2. Feedback Clock Select

The feedback pins (IN4, IN5/IN6) can be used in external feedback mode (for zero delay applications), or as alternate reference inputs. The IN5/IN6 pins provide a differential input and IN4 accepts a single-ended input. Only the Si5338N/P/Q devices allow IN4 to be used as a single-ended clock input. The registers responsible for selecting/configuring external feedback clock inputs are shown in Figure 8.

30[7:0]	7	6	5	4	3	2	1	0
				P2DIV_IN[2:1]				

28[7:0]	7	6	5	4	3	2	1	0
	1	0	P2DIV _IN[0]					

Feedback Clock	P2DIV_IN[2:1]	P2DIV_IN[0]
IN5/IN6 (differential)	00	0
IN4 (single-ended)	01	1
No clock input to P2	10	0

Figure 8. Feedback Input Configuration Registers

When the Si5338 is used in the zero delay mode, set the PFD_EXTFB bit = 1 (register 48[7] = 1). When the Si5338 is not in the zero delay mode, set the PFD_EXTFB bit = 0 (register 48[7] = 0).

5. Configuring PLL Parameters

Once the MultiSynth registers (MS0,1,2,3, and MSn) have been calculated, the PLL parameters PLL_Kphi, VCO_GAIN, RSEL, BWSEL, MSCAL, and MS_PEC need to be calculated according to the information in the figure below. These PLL parameters depend on the values of f_{vco} and f_{pfd} which were calculated in “5. Configuring PLL Parameters”.

48[7:0]

7	6	5	4	3	2	1	0
	PLL_KPHI[6:0]						

f_{pfd}	K	RSEL[1:0]	BWSEL[1:0]
f_{pfd} >= 15 MHz	925	00	00
8 MHz <= f_{pfd} < 15 MHz	325	01	01
5 MHz <= f_{pfd} < 8 MHz	185	11	10

f_{vco}	Q	VCO_GAIN[2:0]
f_{vco} >= 2.425 GHz	3	000
f_{vco} < 2.425 GHz	4	001

$$\text{PLL\_KPHI[6:0]} = \text{Round}\left(\frac{K}{533 * Q} * \frac{f_{vco\,(MHz)}}{f_{pfd\,(MHz)}} * \left(\frac{2500}{f_{vco\,(MHz)}}\right)^3\right)$$

Notes: 1. PLL_KPHI should always be at least 1 and no more than 127

2. Register 48[7] sets internal or external feedback mode. See note in figure 6 for more details. Also see Section 4.2.

49[7:0]

7	6	5	4	3	2	1	0
0	VCO_GAIN[2:0]			RSEL[1:0]		BWSEL[1:0]	

50[7:0]

7	6	5	4	3	2	1	0
1	1	MSCAL[5:0]					

$$\text{MSCAL[5:0]} = \text{ROUND}\left(-6.67 * \frac{f_{vco\,(MHz)}}{1000} + 20.67\right)$$

51[7:0]

7	6	5	4	3	2	1	0
0	0	0	0	0	MS_PEC[2:0]		

Set MS_PEC[2:0] to 111

Figure 9.

6. Configuring the Frequency Increment/Decrement

The Si5338 has a glitchless frequency increment/decrement (Finc/Fdec) feature that allows each output MultiSynth frequency to be independently stepped up or down in predefined steps. Finc/Fdec is not provided on the feedback MultiSynth. When using the Finc/Fdec feature, care must be taken to ensure that the resulting MultiSynth0,1,2,3 output frequency (Fout) stays in the range of 5 MHz to Fvco/8. The divider values, a, b, and c, in "3.2. Calculating MultiSynth Values" on page 8 are used to calculate the Finc/Fdec parameters. Note that the Fout term in Equations 2 and 3 is a constant as defined by the equations in "3. Configuring the Si5338" on page 6. In other words, if a step size (Fstep) of 10 kHz is programmed, the step size will stay 10 kHz regardless of the number of increments or decrements that have occurred. The control of Finc/Fdec can be via external pins or internal register bits. See Registers 52, 63, 74, and 85 for more information.

6.1. Step Size Resolution of 1 ppm

Under all conditions, a step size resolution as small as 1 ppm can be achieved. The actual step size would then be an integer multiple of 1 ppm. Equation 2 shows how to configure the Si5338 with a 1 ppm step size resolution.

$$\text{MSx\_FIDP1} = 10^6 \times c$$

$$\text{MSx\_FIDP2} = 10^6 \times c \times \left(\frac{F_{step}}{F_{out}}\right)$$

$$\text{MSx\_FIDP3} = 10^6 \times (a \times c + b)$$

Where Fstep/Fout must be an integer multiple of 1 ppm.

Equation 2. Frequency Increment/Decrement for 1 ppm Resolution

6.2. Step Size as Small as .931 ppb

The divider parameter c (= MSx_P3) can be up to 30 bits wide as needed to define the fractional part of the MultiSynth output divider value. When the divider parameter c is limited to < 22 bits the Si5338 can achieve increment/decrement step size as small as .931 ppb (2^{-30}). Limiting the c parameter to < 22 bits has the effect of limiting the precision of the MultiSynth output divider. However in practice it is extremely rare that more than 22 bits are needed for the divider parameter c, hence in most cases this limitation of 22 bits for the c parameter will not be an issue.

The following three conditions must be met for step sizes down to .931 ppb.

1. $c < 2^{22}$; c is from "3.2. Calculating MultiSynth Values" on page 8.
2. Fout/Fstep $\leq 2^{30}$; Fout is the frequency out of the MultiSynth.
3. Fout/Fstep is an integer.

The MSx_FIDPx parameters can be calculated as follows:

$$\text{MSx\_FIDP1} = c \times \left(\frac{F_{out}}{F_{step}}\right)$$

$$\text{MSx\_FIDP2} = c$$

$$\text{MSx\_FIDP3} = (a \times c + b) \times \left(\frac{F_{out}}{F_{step}}\right)$$

Equation 3. Frequency Increment/Decrement for Step Size >0.931 ppb

7. Configuring Initial Phase Offset and Phase Step Size

7.1. Initial Phase Offset

Each output of the Si5338 can be programmed with an independent initial phase offset. The phase offset parameter is represented as a 2s complement integer and is calculated as follows:

$$\text{MSx\_PHOFF} = \text{Round}(\text{Phase Offset in Seconds}) \times 128 \times \text{Fvco}$$

Where: Fvco is in Hz

Equation 4. Phase Offset

Make sure to convert MSx_PHOFF to a 2s complement number if a negative value is required. The initial phase offset adjustment has a range of ±45 ns. For the initial phase offset to work properly, the R divider must be set to 1. A soft reset must be applied for the phase offset value to take effect.

7.2. Phase Step Size

Additionally, each output can have its phase stepped up and down in predefined steps. The phase step size has an inc/dec range of ±45 ns and an accuracy of better than 20 ps. The phase step convention is that a positive value will delay the output in time. A phase step increment or decrement is controlled by the Pinc/Pdec pins or register bits. See bits [1:0] of Registers 52, 63, 74, and 85 for more information. The phase step size register parameter is an unsigned integer calculated as follows:

$$\text{MSx\_PHSTEP} = \text{Round}(\text{Desired Phase Step Size in seconds}) \times 128 \times \text{Fvco}$$

Where: Fvco is in Hz

Equation 5. Phase Inc/Dec

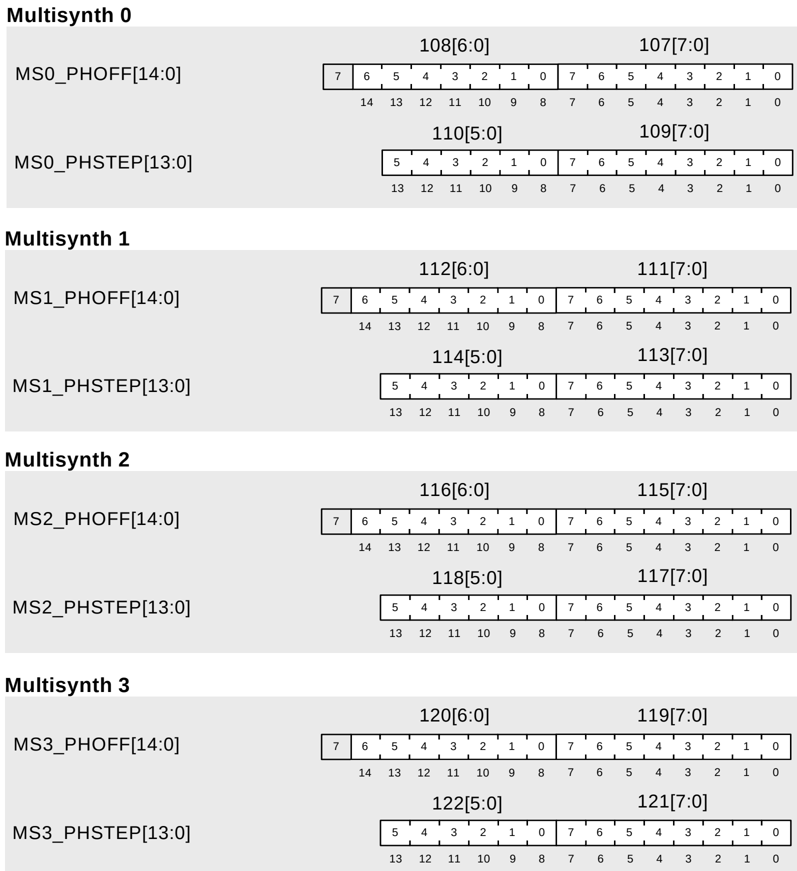


Figure 10. PINC_PDEC Registers

8. Configuring Spread Spectrum

Spread spectrum is available on each of the clock outputs. The device can be set up in down- or center-spread mode. The Si5338 supports spread spectrum under the following conditions:

1. MultiSynth output frequencies $\geq$ 5 MHz and $\leq f_{vco}/8$
2. Spreading rates from 31.5 to 63 kHz
3. Down spread from 0.1 to 5% in 0.01% steps
4. Center spread from ±0.1 to ±2.5% in .01% steps

If your spread spectrum requirements are outside of these parameters, contact Silicon Labs.

8.1. Down Spread

To configure down spread, use the following equations:

Up/Down Parameter:

$$\text{MSx\_SSUDP1} = \text{Floor}\left(\frac{F_{out}}{4 \times \text{sscFreq}}\right)$$

where
Fout = MultiSynthx output frequency in Hz)
sscFreq = spreading frequency in Hz

Down Parameters:

Let x and y be defined as:

$x = \text{Floor}(1e12 \times (64 \times \text{sscAmp} \times (a + b/c)))$

$y = \text{Floor}(1e12 \times (1 – \text{sscAmp}) \times \text{MSx\_SSUDP1})$

where
sscAmp = spread amplitude (e.g, for 1.3 % down spread, sscAmp = .013)
a +b/c is the MultiSynth divider ratio from section 5

$$\text{MSx\_SSDNP1} = \text{Floor}\left(\frac{x}{y}\right)$$

$$\text{MSx\_SSDNP2} = \frac{\text{Mod}(x,y)}{\text{GCD}(x, y)}$$

GCD (x,y) returns the greatest common denominator of x and y
Mod(x,y) returns the remainder of x/y

$$\text{MSx\_SSDNP3} = \frac{y}{\text{GCD}(x, y)}$$

Up Parameters:

MSx_SSUPP1 = 0

MSx_SSUPP2 = 0

MSx_SSUPP3 = 1

Equation 6. SSC Down-Spread Equations

8.2. Center Spread

Rev B devices do not provide native support for center-spread clocking. Center-spread clocks must be implemented as modified down-spread clocks. For example, to implement 100 MHz ±1% on CLKx, you must modify the associated Multisynth and R dividers to output 101 MHz (see "3.2. Calculating MultiSynth Values" on page 8) and configure the device for 2% down-spread according to the equations in “8.1. Down Spread”. Note that ClockBuilder Desktop 6.0 (or later) takes care of configuring the registers properly for center spread operation on rev B devices.

8.2.1. Center Spread Equations for Rev A Devices

The part can be configured for this mode using the following equations. The Spread Spectrum parameters are located within Registers 288–347.

Up/Down Parameter:

$$MSx\_SSUDP1 = \text{Floor}\left(\frac{F_{out}}{4 \times sscFreq}\right)$$

where
Fout = MultiSynthx output frequency in Hz)
sscFreq = spreading frequency in Hz

Down Parameters:

Let x and y_{down} be defined as:

$$x = \text{Floor}(1e12 \times (128 \times sscAmp \times (a + b/c)))$$
$$y_{down} = \text{Floor}(1e12 \times (1 - sscAmp) \times MSx\_SSUDP1)$$

where
sscAmp = spread amplitude (e.g, for +-1.3 % center spread, sscAmp = .013)
a +b/c is the MultiSynth divider ratio from section 5

$$MSx\_SSDNP1 = \text{Floor}\left(\frac{x}{y_{down}}\right)$$

$$MSx\_SSDNP2 = \frac{\text{Mod}(x, y_{down})}{\text{GCD}(x, y_{down})}$$

$$MSx\_SSDNP3 = \frac{y_{down}}{\text{GCD}(x, y_{down})}$$

Up Parameters:

Let y_{up} be defined as:

$$y_{up} = \text{Floor}(1e12 \times (1 + sscAmp) \times MSx\_SSUDP1)$$

$$MSx\_SSUPP1 = \text{Floor}\left(\frac{x}{y_{up}}\right)$$

$$MSx\_SSUPP2 = \frac{\text{Mod}(x, y_{up})}{\text{GCD}(x, y_{up})}$$

$$MSx\_SSUPP3 = \frac{y_{up}}{\text{GCD}(x, y_{up})}$$

Equation 7. SSC Center-Spread Equations

8.3. Spread Spectrum Register Precision

The parameters MSx_SSUPP2, MSx_SSUPP3, MSx_SSDNP2, and MSx_SSDNP3 can each be no more than 15 bits in length. For most combinations of output frequencies and spread profiles, the equations above will yield values greater than (2^{15} – 1). If either MSx_SSUPP2 or MSx_SSUPP3 is greater than (2^{15} – 1), both MSx_SSUPP2 and MSx_SSUPP3 values must be truncated to fit in 15-bits. Similarly, if either MSx_DNPP2 or MSx_DNPP3 is greater than (2^{15} – 1), both must be truncated to fit in 15-bits.

Use the following algorithm to truncate the length of these parameters:

```
while ( MSx_SSUPP2 > (2^15 - 1) || MSx_SSUPP3 > (2^15 – 1)){
        MSx_SSUPP2 = MSx_SSUPP2 >> 2;      // shift right 2 places
        MSx_SSUPP3 = MSx_SSUPP3 >> 2;      // shift right 2 places
}
```

Note: Truncation of the SSC values will not change the reduction in measurable carrier power.

9. Configuring the Output Drivers

The output drivers offer several programmable features which are configured or controlled with register access through the I^2C serial port. The following sections describe each of these features.

9.1. Output Signal Type

Each of the outputs can be configured as CMOS, SSTL, HSTL, LVDS, LVPECL, HSCL. Registers 36-39 define the output type as shown in Figure 11.

Register	7	6	5	4	3	2	1	0
36[7:0]						DRV0_FMT[2:0]		
37[7:0]						DRV1_FMT[2:0]		
38[7:0]						DRV2_FMT[2:0]		
39[7:0]						DRV3_FMT[2:0]		

Output Signal Type	DRVx_FMT x=0,1,2,3
Reserved	000
CMOS/SSTL/HSTL. A enabled, B disabled.	001
CMOS/SSTL/HSTL. A disabled, B enabled.	010
CMOS/SSTL/HSTL. A enabled, B enabled.	011
LVPECL	100
LVDS	110
CML	101
HCSL	111

Figure 11. Setting Output Signal Type

The Si5338 has a CML driver that can be used to replace an LVPECL driver in AC coupled applications and save ~15 mA for each output driver in the process. The output voltage swing of the CML driver is very similar to the LVPECL driver. When using the CML driver, no external bias resistors to ground or Vtt should be connected. The CML driver can be used anytime a large swing AC coupled output is needed. The CML driver is individually available for all 4 differential outputs.

The Si5338 CML output driver can be used as long as the following conditions are met

1. Both pins of the differential output pair are ac coupled to the load
2. The load at the receiver is effectively 100 Ω differential
3. The Si5338 PLL is not bypassed
4. The VDDOx supply voltage is 3.3 V or 2.5 V

The CML driver has the following output swing specifications:

1. Max Vsepp = 1.07 V
2. Min Vsepp = 0.67 V
3. Typ Vsepp = 0.85 V

Figure 11 shows the selection of the CML driver and Figure 13 shows the driver trim settings for the CML driver. The output common mode voltage of the CML driver is not specified.

9.2. Output Voltage

Each of the output drivers can operate from a different VDDO supply. See Register 35 in the Si5338 Data Sheet to know which supply voltage settings can be used with each output driver format. Register 35 is used to configure VDDO as 3.3 V, 2.5 V, 1.8 V, or 1.5 V as shown in Figure 12. The actual VDDOx supply voltage needs to agree to within 10% of the settings in Register 35.

35[7:0]	DRV3_VDDO[1:0]		DRV2_VDDO[1:0]		DRV1_VDDO[1:0]		DRV0_VDDO[1:0]	
	7	6	5	4	3	2	1	0

Supply Voltage	DRVx_VDDO[1:0] x=0,1,2,3
3.3V	00
2.5V	01
1.8V	10
1.5V	11

Figure 12. Supply Voltage Programming

9.3. Output Driver Trim

Once the signal types and VDDO of the output drivers have been configured, the outputs must be trimmed using registers 40-42 as shown in the table in Figure 13.

42[7:0]								41[7:0]								40[7:0]							
0	0	1	DRV3_Trim[4:0]						DRV2_Trim[4:0]					DRV1_Trim[4:0]					DRV0_Trim[4:0]				
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Driver Type	DRVx_Trim[4:0] x=0,1,2,3
3.3V CMOS	10111
2.5V CMOS	10011
1.8V CMOS	10101
1.5V HSTL	11111
3.3V SSTL	00100
2.5V SSTL	01101
1.8V SSTL	10111
3.3V LVPECL	01111
2.5V LVPECL	10000
3.3V LVDS	00011
2.5V or 1.8V LVDS	00100
3.3V HCSL	00111
2.5V HCSL	00111
1.8V HCSL	00111
3.3V CML	01000
2.5V CML	01001

Figure 13. Setting Output Driver Trim

9.4. Output Driver Powerup/Powerdown

The device allows powering down unused output clocks (CLK_n) to save on overall power consumption. Register 31[0] controls this function for CLK0, 32[0] controls CLK1, 33[0] controls CLK2, and 34[0] controls CLK3. Setting the register bit to 0 enables power to the CLK output; setting it to 1 powers it down. The default value is set to 0.

9.5. Output Driver Enable/Disable

Each of the output clocks (CLK_n) can be enabled or disabled once they have been powered up as described in Section 9.4. Register 230 controls this function as shown in Figure 14. Drivers are enabled by default. Register 230[4] disables/enables all outputs simultaneously, and, when disabled, overrides the effect of OEB_0,1,2,3. Set each OEB_x to 0 to enable.

230[7:0]	7	6	5	4	3	2	1	0
	0	0	0	OEB_all	OEB_3	OEB_2	OEB_1	OEB_0

Figure 14. Setting Output Driver Enable/Disable

9.6. Output Drive State When Disabled

When an output is disabled, its state is configurable as Hi-Z, Low, High, or Always On. Any output clock that is fed back to IN4,5,6 (for zero delay mode) must have its output disable state set to always on. Registers 110[7:6], 114[7:6], 118[7:6], and 122[7:6] control this feature as shown in Figure 15.

Driver State When Disabled	CLKx_DISST[1:0] x=0,1,2,3
Hi-Z	00
Disables Low	01
Disables High	10
Always On	11

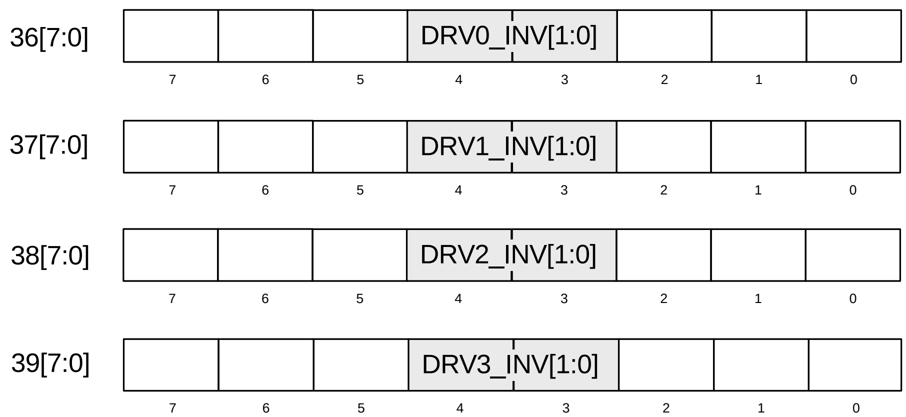
Register	7	6	5	4	3	2	1	0
110[7:0]	CLK0_DISST[1:0]							
114[7:0]	CLK1_DISST[1:0]							
118[7:0]	CLK2_DISST[1:0]							
122[7:0]	CLK3_DISST[1:0]							

Figure 15. Setting Output Drive State

9.7. Output Clock Invert

An output configured as CMOS/SSTL/HSTL will have both of its outputs (A/B) in phase by default, but, by using the invert bits, one or both outputs can be inverted. The invert feature allows a CMOS/SSTL/HSTL output to have complimentary outputs. Differential outputs (LVPECL, LVDS, HCSL, CML) are always complimentary even when inverted.

Upon power up or a soft_reset, the Si5338 synchronizes the output clocks. With normal output polarity (no output clock inversion), the Si5338 synchronizes the output clocks to the falling, not rising, edge. Synchronization at the rising edge can be done by inverting all the clocks that are to be synchronized.

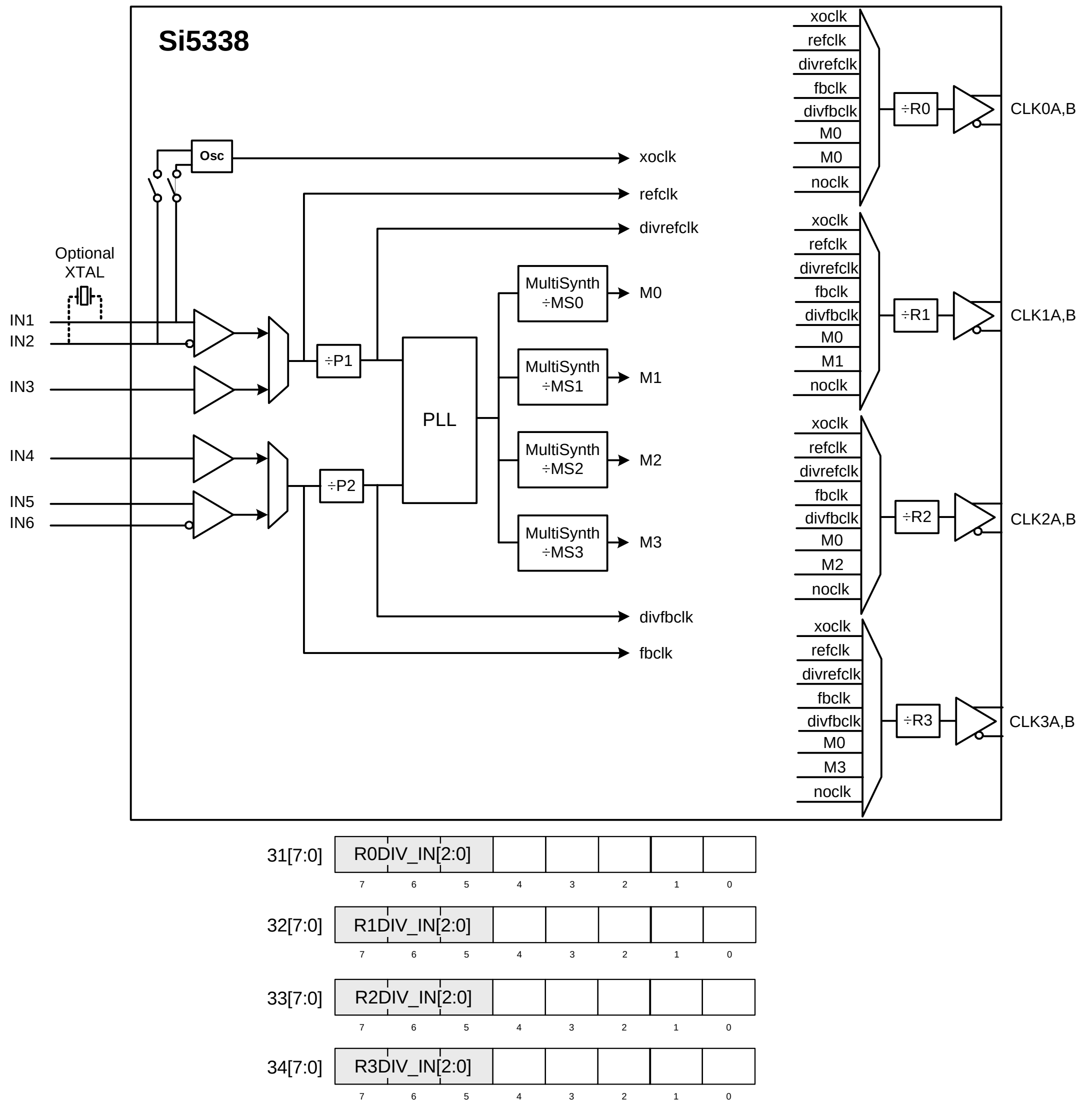


Inversion	DRVx_INV[1:0] x=0,1,2,3
No inversion	00
Invert A side (CMOS/SSTL/HSTL only)	01
Invert B side (CMOS/SSTL/HSTL only)	10
Invert both A and B sides	11

Figure 16. Setting Output Clock Inversion

9.8. Output Clock Select

The source of each of the clock outputs (CLKx) can be selected as shown in Figure 17. This level of flexibility allows the drivers to output any of the synthesized clocks (MSx) or bypass the PLL and output any of the input clocks directly. This allows the Si5338 to operate as a PLL, a clock buffer, or a combination of both. Any active output buffer that does not receive its clock from the PLL should have its disable state (“9.6. Output Drive State When Disabled”) set to “always on”. The register settings are shown in Figure 17.

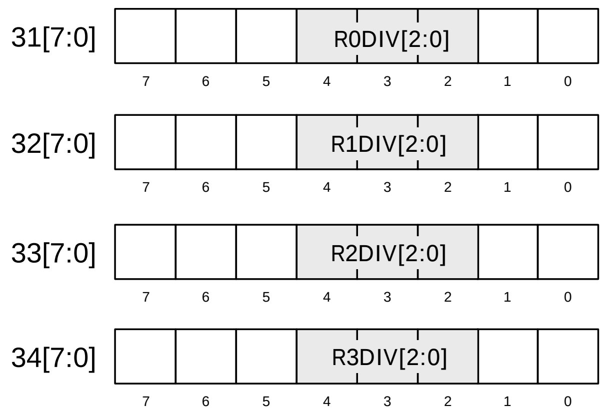


Selected Source	RxDIV_IN[2:0] x=0,1,2,3
fbclk (p2div_in)	000
refclk (p1div_in)	001
divfbclk (p2div_out)	010
divrefclk (p1div_out)	011
xoclk	100
M0	101
Mn	110
No clock	111

Figure 17. Selecting the Output Clock Source

9.9. Output Clock Dividers

The output clock dividers (R_x) allow a final stage of division. The division ratio is configurable using registers 31-34 as shown in Figure 18. These dividers can be useful for generating clocks below the 5 MHz frequency limit of the MultiSynth dividers (M_x). Note that when using a division value other than 1, the outputs may not be in phase. If using the part in zero delay mode then make sure all Rx dividers for all outputs that are to be zero delay, as well as the divider for the feedback output, are set to 1.



Output Divider Value	RxDIV[2:0] x=0,1,2,3
1	000
2	001
4	010
8	011
16	100
32	101
Reserved	110
Reserved	111

Figure 18. Setting Output Clock Dividers

10. Si5338 Registers

This section describes the registers and their usage in detail. These values are easily configured using the ClockBuilder Desktop (see “3.1.1. ClockBuilder™ Desktop Software in the Si5338 data sheet). See AN428 for a working example using Silicon Labs' F301 MCU.

10.1. Assembling the Si5338 Register Map

Once all of the desired features have been configured, the values should be collected into a single list in order to write to the device. Collect register values for the required registers:

1. All MultiSynth, R, and P divider ratios
2. PLL parameters
3. Output driver parameters and multiplexors
4. Input multiplexors
5. Miscellaneous register values

And any additional/optional features:

6. Frequency inc/dec
7. Phase inc/dec
8. Initial phase offset
9. Spread spectrum

10.2. Miscellaneous Register Writes

The following register bits must also be written to ensure proper device functionality.

- Register 47[7:2] = 000101b
- Register 106[7] = 1b
- Register 116[7] = 1b
- Register 42[5] = 1b
- Register 6[7:5] = 000b
- Register 6[1] = 0b
- Register 28[7:6] = 00b

With the register information from 10.1 and 10.2, assemble the register map, and follow the procedure in Figure 9 of the Si5338 data sheet.

10.3. Register Write-Allowed Mask

The masks listed in Table 1 indicate which bits in each register of the Si5338 can be modified and which bits cannot. Therefore, these masks are write-allowed or write-enabled bits. These masks must be used to perform a read-modify-write on each register.

If a mask is 0x00, all bits in the associated register are reserved and must remain unchanged. If the mask is 0xFF, all the bits in the register can be changed. All other registers require a read-modify-write procedure to write to the registers. ClockBuilder Desktop can be used to create ANSI C code (Options → Save C code header file) with the register contents and mask values. AN428 demonstrates the usage of this header file and the read-modify-write procedure.

The following code demonstrates the application of the above write allowed mask.

- Let addr be the address of the register to access.
- Let data be the data or value to write to the register located at addr.
- Let mask be the write-allowed bits defined for the corresponding register.

```
// ignore registers with masks of 0x00
if(mask != 0x00){

        if(mask == 0xFF){
                // do a regular I2C write to the register
                // at addr with the desired data value
                write_Si5338(addr, data);

        } else {
                // do a read-modify-write using I2C and
                // bit-wise operations

                // get the current value from the device at the
                // register located at addr
                curr_val = read_Si5338(addr);

                // clear the bits that are allowed to be
                // accessed in the current value of the register
                clear_curr_val = curr_val AND (NOT mask);

                // clear the bits in the desired data that
                // are not allowed to be accessed
                clear_new_val = data AND mask;

                // combine the cleared values to get the new
                // value to write to the desired register
                combined = clear_curr_val OR clear_new_val;

                write_Si5338(addr, combined);
        }

}
```

Table 1. Register Write-Allowed Masks

Address (Decimal)	Mask (Hex)
0	0x00
1	0x00
2	0x00
3	0x00
4	0x00
5	0x00
6	0x1D
7	0x00
8	0x00
9	0x00
10	0x00
11	0x00
12	0x00
13	0x00
14	0x00
15	0x00
16	0x00
17	0x00
18	0x00
19	0x00
20	0x00
21	0x00
22	0x00
23	0x00
24	0x00
25	0x00
26	0x00
27	0x80
28	0xFF
29	0xFF

***Note:** See Figure 9 in the Si5338 data sheet for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

Table 1. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
30	0xFF
31	0xFF
32	0xFF
33	0xFF
34	0xFF
35	0xFF
36	0x1F
37	0x1F
38	0x1F
39	0x1F
40	0xFF
41	0x7F
42	0x3F
43	0x00
44	0x00
45	0xFF
46	0xFF
47	0xFF
48	0xFF
49	0xFF
50	0xFF
51	0xFF
52	0x7F
53	0xFF
54	0xFF
55	0xFF
56	0xFF
57	0xFF
58	0xFF
59	0xFF
60	0xFF

***Note:** See Figure 9 in the Si5338 data sheet for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

Table 1. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
61	0xFF
62	0x3F
63	0x7F
64	0xFF
65	0xFF
66	0xFF
67	0xFF
68	0xFF
69	0xFF
70	0xFF
71	0xFF
72	0xFF
73	0x3F
74	0x7F
75	0xFF
76	0xFF
77	0xFF
78	0xFF
79	0xFF
80	0xFF
81	0xFF
82	0xFF
83	0xFF
84	0x3F
85	0x7F
86	0xFF
87	0xFF
88	0xFF
89	0xFF
90	0xFF
91	0xFF

***Note:** See Figure 9 in the Si5338 data sheet for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

Table 1. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
92	0xFF
93	0xFF
94	0xFF
95	0x3F
96	0x00
97	0xFF
98	0xFF
99	0xFF
100	0xFF
101	0xFF
102	0xFF
103	0xFF
104	0xFF
105	0xFF
106	0xBF
107	0xFF
108	0x7F
109	0xFF
110	0xFF
111	0xFF
112	0x7F
113	0xFF
114	0xFF
115	0xFF
116	0xFF
117	0xFF
118	0xFF
119	0xFF
120	0xFF
121	0xFF
122	0xFF

***Note:** See Figure 9 in the Si5338 data sheet for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

Table 1. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
123	0xFF
124	0xFF
125	0xFF
126	0xFF
127	0xFF
128	0xFF
129	0x0F
130	0x0F
131	0xFF
132	0xFF
133	0xFF
134	0xFF
135	0xFF
136	0xFF
137	0xFF
138	0xFF
139	0xFF
140	0xFF
141	0xFF
142	0xFF
143	0xFF
144	0xFF
145	0x00
146	0x00
147	0x00
148	0x00
149	0x00
150	0x00
151	0x00
152	0xFF
153	0xFF

***Note:** See Figure 9 in the Si5338 data sheet for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

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Table 1. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
154	0xFF
155	0xFF
156	0xFF
157	0xFF
158	0x0F
159	0x0F
160	0xFF
161	0xFF
162	0xFF
163	0xFF
164	0xFF
165	0xFF
166	0xFF
167	0xFF
168	0xFF
169	0xFF
170	0xFF
171	0xFF
172	0xFF
173	0xFF
174	0xFF
175	0xFF
176	0xFF
177	0xFF
178	0xFF
179	0xFF
180	0xFF
181	0x0F
182	0xFF
183	0xFF
184	0xFF

***Note:** See Figure 9 in the Si5338 data sheet for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

Table 1. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
185	0xFF
186	0xFF
187	0xFF
188	0xFF
189	0xFF
190	0xFF
191	0xFF
192	0xFF
193	0xFF
194	0xFF
195	0xFF
196	0xFF
197	0xFF
198	0xFF
199	0xFF
200	0xFF
201	0xFF
202	0xFF
203	0x0F
204	0xFF
205	0xFF
206	0xFF
207	0xFF
208	0xFF
209	0xFF
210	0xFF
211	0xFF
212	0xFF
213	0xFF
214	0xFF
215	0xFF

***Note:** See Figure 9 in the Si5338 data sheet for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

Table 1. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
216	0xFF
217	0xFF
218	0x00
219	0x00
220	0x00
221	0x00
222	0x00
223	0x00
224	0x00
225	0x00
226	0x04
227	0x00
228	0x00
229	0x00
230*	0xFF
231	0x00
232	0x00
233	0x00
234	0x00
235	0x00
236	0x00
237	0x00
238	0x00
239	0x00
240	0x00
241*	0xFF
242	0x02
243	0x00
244	0x00
245	0x00
246*	0xFF

***Note:** See Figure 9 in the Si5338 data sheet for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

Table 1. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
247	0x00
248	0x00
249	0x00
250	0x00
251	0x00
252	0x00
253	0x00
254	0x00
255	0xFF
256	0x00
257	0x00
258	0x00
259	0x00
260	0x00
261	0x00
262	0x00
263	0x00
264	0x00
265	0x00
266	0x00
267	0x00
268	0x00
269	0x00
270	0x00
271	0x00
272	0x00
273	0x00
274	0x00
275	0x00
276	0x00
277	0x00

***Note:** See Figure 9 in the Si5338 data sheet for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

Table 1. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
278	0x00
279	0x00
280	0x00
281	0x00
282	0x00
283	0x00
284	0x00
285	0x00
286	0x00
287	0xFF
288	0xFF
289	0xFF
290	0xFF
291	0xFF
292	0xFF
293	0xFF
294	0xFF
295	0xFF
296	0xFF
297	0xFF
298	0xFF
299	0x0F
300	0x00
301	0x00
302	0x00
303	0xFF
304	0xFF
305	0xFF
306	0xFF
307	0xFF
308	0xFF

***Note:** See Figure 9 in the Si5338 data sheet for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

Table 1. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
309	0xFF
310	0xFF
311	0xFF
312	0xFF
313	0xFF
314	0xFF
315	0x0F
316	0x00
317	0x00
318	0x00
319	0xFF
320	0xFF
321	0xFF
322	0xFF
323	0xFF
324	0xFF
325	0xFF
326	0xFF
327	0xFF
328	0xFF
329	0xFF
330	0xFF
331	0x0F
332	0x00
333	0x00
334	0x00
335	0xFF
336	0xFF
337	0xFF
338	0xFF
339	0xFF

***Note:** See Figure 9 in the Si5338 data sheet for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

Table 1. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
340	0xFF
341	0xFF
342	0xFF
343	0xFF
344	0xFF
345	0xFF
346	0xFF
347	0x0F
348	0x00
349	0x00
350	0x00

***Note:** See Figure 9 in the Si5338 data sheet for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

10.4. Register Categories

This is a list of registers needed to define the Configuration of a device. Set the PAGEBIT to access registers with addresses greater than 255.

Address (Decimal)	Bits	Function
0	2:0	Rev ID
2	7:0	Device Configuration
3	7:0	
4	7:0	
5	7:0	
6	4:0	Mask bits for LOS_CLKIN,LOS_FB, LOL, SYS_CAL
27	7:6	I^2C Configuration
27	7	
28–30	7:0	Input Mux Configuration
31–39	7:0	Output Configuration
40	7:0	Output Driver Trim Bits
41	6:0	
42	4:0	
47	5:2	Input Configuration
48	7:0	PLL Configuration
49	6:0	
50	7:0	
51	7:4, 2:0	
52	6:0	MultiSynth0 Freq inc/dec, SS, Phase inc/dec Configuration
53–61	7:0	MultiSynth0 frequency Configuration
62	5:0	
63	6:0	MultiSynth1 frequency Configuration
64–72	7:0	
73	5:0	
74	6:0	MultiSynth2 frequency Configuration
75–83	7:0	
84	5:0	
85	6:0	MultiSynth3 frequency Configuration
86–94	7:0	
95	5:0	

Address (Decimal)	Bits	Function
97–105	7:0	MultiSynthN Feedback divider Configuration
106	5:0	
107–110	7:0	MultiSynth0 Phase inc/dec, SS Configuration, drive state
111–114	7:0	MultiSynth1 Phase inc/dec, SS Configuration, drive state
115–118	7:0	MultiSynth2 Phase inc/dec, SS Configuration, drive state
119	7:0	MultiSynth3 Phase inc/dec, SS Configuration, drive state
120	6:0	
121–122	7:0	
123–128	7:0	MultiSynth0 freq inc/dec Configuration, ID config
129	3:0	
130	6:0	
131–144	7:0	
152–173	7:0	MultiSynth1 freq inc/dec Configuration
174–195	7:0	MultiSynth2 freq inc/dec Configuration
196–216	7:0	MultiSynth3 freq inc/dec Configuration
217	6:0	
241	7:0	Reserved - set to 0x65 if not factory-programmed.
287	7:0	MultiSynth0 spread spectrum Configuration
288	6:0	
289	7:0	
290	6:0	
291	7:0	
292	7:0	
293	7:0	
294	7:0	
295	6:0	
296	7:0	
297	6:0	
298	7:0	
299	7:0	

Address (Decimal)	Bits	Function
303	7:0	MultiSynth1 spread spectrum Configuration
304	6:0	
305	7:0	
306	6:0	
307	7:0	
308	7:0	
309	7:0	
310	7:0	
311	6:0	
312	7:0	
313	6:0	
314	7:0	
315	7:0	
319	7:0	MultiSynth2 spread spectrum Configuration
320	6:0	
321	7:0	
322	6:0	
323	7:0	
324	7:0	
325	7:0	
326	7:0	
327	6:0	
328	7:0	
329	6:0	
330	7:0	
331	7:0	

Address (Decimal)	Bits	Function
335	7:0	MultiSynth3 spread spectrum Configuration
336	6:0	
337	7:0	
338	6:0	
339	7:0	
340	7:0	
341	7:0	
342	7:0	
343	6:0	
344	7:0	
345	6:0	
346	7:0	
347	7:0	

10.5. Register Summary

Table 2. Register Summary

<table>
<tr><th>Register</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td></td><td></td><td></td><td></td><td></td><td colspan="3">REVID[2:0]</td></tr>
<tr><td>2</td><td colspan="8">Dev_Config2[7:0]</td></tr>
<tr><td>3</td><td colspan="8">Dev_Config3[7:0]</td></tr>
<tr><td>4</td><td colspan="8">Dev_Config4[7:0]</td></tr>
<tr><td>5</td><td colspan="8">Dev_Config5[7:0]</td></tr>
<tr><td>6</td><td></td><td></td><td></td><td>PLL_LOL_
MASK</td><td>LOS_FDBK_
MASK</td><td>LOS_-
CLKIN_MASK</td><td></td><td>SYS_CAL_
MASK</td></tr>
<tr><td>27</td><td>I2C_1P8_SEL</td><td colspan="7">I2C_ADDR[6:0]</td></tr>
<tr><td>28</td><td></td><td></td><td>P2DIV_IN[0]</td><td colspan="3">P1DIV_IN[2:0]</td><td colspan="2">XTAL_FREQ[1:0]</td></tr>
<tr><td>29</td><td colspan="3">PFD_IN_REF[2:0]</td><td colspan="2">P1DIV_IN[4:3]</td><td colspan="3">P1DIV[2:0]</td></tr>
<tr><td>30</td><td colspan="3">PFD_IN_FB[2:0]</td><td colspan="2">P2DIV_IN[2:1]</td><td colspan="3">P2DIV[2:0]</td></tr>
<tr><td>31</td><td colspan="3">R0DIV_IN[2:0]</td><td colspan="3">R0DIV[2:0]</td><td>MS0_PDN</td><td>DRV0_PDN</td></tr>
<tr><td>32</td><td colspan="3">R1DIV_IN[2:0]</td><td colspan="3">R1DIV[2:0]</td><td>MS1_PDN</td><td>DRV1_PDN</td></tr>
<tr><td>33</td><td colspan="3">R2DIV_IN[2:0]</td><td colspan="3">R2DIV[2:0]</td><td>MS2_PDN</td><td>DRV2_PDN</td></tr>
<tr><td>34</td><td colspan="3">R3DIV_IN[2:0]</td><td colspan="3">R3DIV[2:0]</td><td>MS3_PDN</td><td>DRV3_PDN</td></tr>
<tr><td>35</td><td colspan="2">DRV3_VDDO[1:0]</td><td colspan="2">DRV2_VDDO[1:0]</td><td colspan="2">DRV1_VDDO[1:0]</td><td colspan="2">DRV0_VDDO[1:0]</td></tr>
<tr><td>36</td><td></td><td></td><td></td><td colspan="2">DRV0_INV[1:0]</td><td colspan="3">DRV0_FMT[2:0]</td></tr>
<tr><td>37</td><td></td><td></td><td></td><td colspan="2">DRV1_INV[1:0]</td><td colspan="3">DRV1_FMT[2:0]</td></tr>
<tr><td>38</td><td></td><td></td><td></td><td colspan="2">DRV2_INV[1:0]</td><td colspan="3">DRV2_FMT[2:0]</td></tr>
<tr><td>39</td><td></td><td></td><td></td><td colspan="2">DRV3_INV[1:0]</td><td colspan="3">DRV3_FMT[2:0]</td></tr>
<tr><td>40</td><td colspan="3">DRV1_TRIM[2:0]</td><td colspan="5">DRV0_TRIM[4:0]</td></tr>
<tr><td>41</td><td></td><td colspan="5">DRV2_TRIM[4:0]</td><td colspan="2">DRV1_TRIM[4:3]</td></tr>
<tr><td>42</td><td></td><td></td><td></td><td colspan="5">DRV3_TRIM[4:0]</td></tr>
<tr><td>45</td><td colspan="8">FCAL_OVRD[7:0]</td></tr>
<tr><td>46</td><td colspan="8">FCAL_OVRD[15:8]</td></tr>
<tr><td>47</td><td></td><td></td><td></td><td></td><td></td><td></td><td colspan="2">FCAL_OVRD[17:16]</td></tr>
<tr><td>48</td><td>PFD_EXTFB</td><td colspan="7">PLL_KPHI[6:0]</td></tr>
<tr><td>49</td><td>FCAL_OVRD_EN</td><td colspan="3">VCO_GAIN[2:0]</td><td colspan="2">RSEL[1:0]</td><td colspan="2">BWSEL[1:0]</td></tr>
<tr><td>50</td><td colspan="2">PLL_ENABLE[1:0]</td><td colspan="6">MSCAL[5:0]</td></tr>
<tr><td>51</td><td>MS3_HS</td><td>MS2_HS</td><td>MS1_HS</td><td>MS0_HS</td><td></td><td colspan="3">MS_PEC[2:0]</td></tr>
<tr><td>52</td><td></td><td colspan="2">MS0_FIDCT[1:0]</td><td>MS0_FIDDIS</td><td colspan="2">MS0_SSMODE[1:0]</td><td colspan="2">MS0_PHIDCT[1:0]</td></tr>
<tr><td>53</td><td colspan="8">MS0_P1[7:0]</td></tr>
<tr><td>54</td><td colspan="8">MS0_P1[15:8]</td></tr>
<tr><td>55</td><td colspan="6">MS0_P2[5:0]</td><td colspan="2">MS0_P1[17:16]</td></tr>
<tr><td>56</td><td colspan="8">MS0_P2[13:6]</td></tr>
<tr><td>57</td><td colspan="8">MS0_P2[21:14]</td></tr>
</table>

Table 2. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
58	MS0_P2[29:22]							
59	MS0_P3[7:0]							
60	MS0_P3[15:8]							
61	MS0_P3[23:16]							
62			MS0_P3[29:24]					
63		MS1_FIDCT[1:0]		MS1_FIDDIS	MS1_SSMODE[1:0]		MS1_PHIDCT[1:0]	
64	MS1_P1[7:0]							
65	MS1_P1[15:8]							
66	MS1_P2[5:0]						MS1_P1[17:16]	
67	MS1_P2[13:6]							
68	MS1_P2[21:14]							
69	MS1_P2[29:22]							
70	MS1_P3[7:0]							
71	MS1_P3[15:8]							
72	MS1_P3[23:16]							
73			MS1_P3[29:24]					
74		MS2_FRCTL[1:0]		MS2_FIDDIS	MS2_SSMODE[1:0]		MS2_PHIDCT[1:0]	
75	MS2_P1[7:0]							
76	MS2_P1[15:8]							
77	MS2_P2[5:0]						MS2_P1[17:16]	
78	MS2_P2[13:6]							
79	MS2_P2[21:14]							
80	MS2_P2[29:22]							
81	MS2_P3[7:0]							
82	MS2_P3[15:8]							
83	MS2_P3[23:16]							
84			MS2_P3[29:24]					
85		MS3_FIDCTL[1:0]		MS3_FIDDIS	MS3_SSMODE[1:0]		MS3_PHIDCTL[1:0]	
86	MS3_P1[7:0]							
87	MS3_P1[15:8]							
88	MS3_P2[5:0]						MS3_P1DIV[17:16]	
89	MS3_P2[13:6]							
90	MS3_P2[21:14]							
91	MS3_P2[29:22]							
92	MS3_P3[7:0]							
93	MS3_P3[15:8]							
94	MS3_P3[23:16]							
95			MS3_P3[29:24]					

Table 2. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
97	MSN_P1[7:0]							
98	MSN_P1[15:8]							
99	MSN_P2[5:0]						MSN_P1[17:16]	
100	MSN_P2[13:6]							
101	MSN_P2[21:14]							
102	MSN_P2[29:22]							
103	MSN_P3[7:0]							
104	MSN_P3[15:8]							
105	MSN_P3[23:16]							
106			MSN_P3[29:24]					
107	MS0_PHOFF[7:0]							
108		MS0_PHOFF[14:8]						
109	MS0_PHSTEP[7:0]							
110	CLK0_DISST[1:0]		MS0_PHSTEP[13:8]					
111	MS1_PHOFF[7:0]							
112		MS1_PHOFF[14:8]						
113	MS1_PHSTEP[7:0]							
114	CLK1_DISST[1:0]		MS1_PHSTEP[13:8]					
115	MS2_PHOFF[7:0]							
116		MS2_PHOFF[14:8]						
117	MS2_PHSTEP[7:0]							
118	CLK2_DISST[1:0]		MS2_PHSTEP[13:8]					
119	MS3_PHOFF[7:0]							
120		MS3_PHOFF[14:8]						
121	MS3_PHSTEP[7:0]							
122	CLK3_DISST[1:0]		MS3_PHSTEP[13:8]					
123	MS0_FIDP1[7:0]							
124	MS0_FIDP1[15:8]							
125	MS0_FIDP1[23:16]							
126	MS0_FIDP1[31:24]							
127	MS0_FIDP1[39:32]							
128	MS0_FIDP1[47:40]							
129					MS0_FIDP1[51:48]			
130					MS0_FIDP2[51:48]			
131	MS0_FIDP2[47:40]							
132	MS0_FIDP2[39:32]							
133	MS0_FIDP2[31:24]							
134	MS0_FIDP2[23:16]							

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Table 2. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
135	MS0_FIDP2[15:8]							
136	MS0_FIDP2[7:0]							
137	MS0_FIDP3[7:0]							
138	MS0_FIDP3[15:8]							
139	MS0_FIDP3[23:16]							
140	MS0_FIDP3[31:24]							
141	MS0_FIDP3[39:32]							
142	MS0_FIDP3[47:40]							
143	MS0_FIDP3[55:48]							
144	MS0_ALL	MS0_FIDP3[62:56]						
152	MS1_FIDP1[7:0]							
153	MS1_FIDP1[15:8]							
154	MS1_FIDP1[23:16]							
155	MS1_FIDP1[31:24]							
156	MS1_FIDP1[39:32]							
157	MS1_FIDP1[47:40]							
158					MS1_FIDP1[51:48]			
159					MS1_FIDP2[51:48]			
160	MS1_FIDP2[47:40]							
161	MS1_FIDP2[39:32]							
162	MS1_FIDP2[31:24]							
163	MS1_FIDP2[23:16]							
164	MS1_FIDP2[15:8]							
165	MS1_FIDP2[7:0]							
166	MS1_FIDP3[7:0]							
167	MS1_FIDP3[15:8]							
168	MS1_FIDP3[23:16]							
169	MS1_FIDP3[31:24]							
170	MS1_FIDP3[39:32]							
171	MS1_FIDP3[47:40]							
172	MS1_FIDP3[55:48]							
173		MS1_FIDP3[62:56]						
174	MS2_FIDP1[7:0]							
175	MS2_FIDP1[15:8]							
176	MS2_FIDP1[23:16]							
177	MS2_FIDP1[31:24]							
178	MS2_FIDP1[39:32]							
179	MS2_FIDP1[47:40]							

Table 2. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
180					MS2_FIDP1[51:48]			
181					MS2_FIDP2[51:48]			
182	MS2_FIDP2[47:40]							
183	MS2_FIDP2[39:32]							
184	MS2_FIDP2[31:24]							
185	MS2_FIDP2[23:16]							
186	MS2_FIDP2[15:8]							
187	MS2_FIDP2[7:0]							
188	MS2_FIDP3[7:0]							
189	MS2_FIDP3[15:8]							
190	MS2_FIDP3[23:16]							
191	MS2_FIDP3[31:24]							
192	MS2_FIDP3[39:32]							
193	MS2_FIDP3[47:40]							
194	MS2_FIDP3[55:48]							
195		MS2_FIDP3[62:56]						
196	MS3_FIDP1[7:0]							
197	MS3_FIDP1[15:8]							
198	MS3_FIDP1[23:16]							
199	MS3_FIDP1[31:24]							
200	MS3_FIDP1[39:32]							
201	MS3_FIDP1[47:40]							
202					MS3_FIDP1[51:48]			
203					MS3_FIDP2[51:48]			
204	MS3_FIDP2[47:40]							
205	MS3_FIDP2[39:32]							
206	MS3_FIDP2[31:24]							
207	MS3_FIDP2[23:16]							
208	MS3_FIDP2[15:8]							
209	MS3_FIDP2[7:0]							
210	MS3_FIDP3[7:0]							
211	MS3_FIDP3[15:8]							
212	MS3_FIDP3[23:16]							
213	MS3_FIDP3[31:24]							
214	MS3_FIDP3[39:32]							
215	MS3_FIDP3[47:40]							
216	MS3_FIDP3[55:48]							
217		MS3_FIDP3[62:56]						

Table 2. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
218				PLL_LOL	LOS_FDBK	LOS_CLKIN		SYS_CAL
226						MS_RESET		
230				OEB_ALL	OEB_3	OEB_2	OEB_1	OEB_0
235	FCAL[7:0]							
236	FCAL[15:8]							
237						FCAL[17:16]		
241	DIS_LOL							
242							DCLK_DIS	
246							SOFT_RESET	
247				PLL_LOL_STK	LOS_FDBK_ STK	LOS_- CLKIN_STK		SYS_CAL_STK
255								PAGE_SEL
287	MS0_SSUPP2[7:0]							
288		MS0_SSUPP2[14:8]						
289	MS0_SSUPP3[7:0]							
290		MS0_SSUPP3[14:8]						
291	MS0_SSUPP1[7:0]							
292	MS0_SSUDP1[3:0]				MS0_SSUPP1[11:8]			
293	MS0_SSUDP1[11:4]							
294	MS0_SSDNP2[7:0]							
295		MS0_SSDNP2[14:8]						
296	MS0_SSDNP3[7:0]							
297		MS0_SSDNP3[14:8]						
298	MS0_SSDNP1[7:0]							
299					MS0_SSDNP1[11:8]			
303	MS1_SSUPP2[7:0]							
304		MS1_SSUPP2[14:8]						
305	MS1_SSUPP3[7:0]							
306		MS1_SSUPP3[14:8]						
307	MS1_SSUPP1[7:0]							
308	MS1_SSUDP1[3:0]				MS1_SSUPP1[11:8]			
309	MS1_SSUDP1[11:4]							
310	MS1_SSDNP2[7:0]							
311		MS1_SSDNP2[14:8]						
312	MS1_SSDNP3[7:0]							
313		MS1_SSDNP3[14:8]						
314	MS1_SSDNP1[7:0]							
315					MS1_SSDNP1[11:8]			

Table 2. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
319	MS2_SSUPP2[7:0]							
320		MS2_SSUPP2[14:8]						
321	MS2_SSUPP3[7:0]							
322		MS2_SSUPP3[14:8]						
323	MS2_SSUPP1[7:0]							
324	MS2_SSUDP1[3:0]				MS2_SSUPP1[11:8]			
325	MS2_SSUDP1[11:4]							
326	MS2_SSDNP2[7:0]							
327		MS2_SSDNP2[14:8]						
328	MS2_SSDNP3[7:0]							
329		MS2_SSDNP3[14:8]						
330	MS2_SSDNP1[7:0]							
331					MS2_SSDNP1[11:8]			
335	MS3_SSUPP2[7:0]							
336		MS3_SSUPP2[14:8]						
337	MS3_SSUPP3[7:0]							
338		MS3_SSUPP3[14:8]						
339	MS3_SSUPP1[7:0]							
340	MS3_SSUDP1[3:0]				MS3_SSUPP1[11:8]			
341	MS3_SSUDP1[11:4]							
342	MS3_SSDNP2[7:0]							
343		MS3_SSDNP2[14:8]						
344	MS3_SSDNP3[7:0]							
345		MS3_SSDNP3[14:8]						
346	MS3_SSDNP1[7:0]							
347					MS3_SSDNP1[11:8]			

10.6. Register Descriptions

In many registers, the byte reset value contains one or more “x”s because a factory-programmed device can have multiple values for these bits.

Register 0.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						REVID[2:0]		
Type	R							

Reset value = xxxx xxxx

Bit	Name	Function
7:3	Reserved	
2:0	REVID[2:0]	**Device Revision ID.** Rev A = 000b Rev B = 001b

Register 2.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			Dev_Config2[5:0]					
Type	R							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	
5:0	Dev_Config2[5:0]	Bits 5:0 represent the last two digits of the base part number: "38" for Si5338. See "10.6.1. Example Part Number for Device ID Registers" on page 55 for complete part number example.

Register 3.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Dev_Config3[7:3]							Dev_Config3
Type	R							R

Reset value = xxxx xxxx

Bit	Name	Function
7:3	Dev_Config3[7:3]	Bits 7:3 represent the device grade: 1 through 24 = A thorugh Z. See "10.6.1. Example Part Number for Device ID Registers" on page 55 for complete part number example.
2:1	Reserved	
0	Dev_Config3[0]	Bit 0 represents bit 16 of the NVM code assigned by Silicon Labs: 00000 through 99999. See "10.6.1. Example Part Number for Device ID Registers" on page 55 for complete part number example.

Register 4.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Dev_Config4[7:0]							
Type	R							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	Dev_Config4[7:0]	Bits 7:0 represent bits 15:8 of the NVM code assigned by Silicon Labs: 00000 through 99999. See "10.6.1. Example Part Number for Device ID Registers" on page 55 for complete part number example.

Register 5.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Dev_Config5[7:0]							
Type	R							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	Dev_Config5[7:0]	Bits 7:0 represent bits 7:0 of the NVM code assigned by Silicon Labs: 00000 through 99999. See "10.6.1. Example Part Number for Device ID Registers" on page 55 for complete part number example.

10.6.1. Example Part Number for Device ID Registers

Device ID register contents for an example part number Si5338N-B12345-GM:

Register 0[2:0] = 001

Register 2 = 66h = 0110 0110

Register 3 = 72h = 0111 0010

Register 4 = 30h = 0011 0000

Register 5 = 39h = 0011 1001

REVID = B

Dev_Config2[5:0] = 10 0110 = 38 (base part number).

Dev_Config3[7:3] = 0 1110 = 14 = N (device grade).

Dev_Config3[0], Dev_Config4[7:0], Dev_Config5[7:0] = 0 0011 0000 0011 1001 = 12345 (NVM code number).

Please refer to the Si5338 data sheet's Ordering Guide section for detailed information about ordering part numbers.

Register 6.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				PLL_LOL_MASK	LOS_FDBK_MASK	LOS_CLKIN_MASK		SYS_CAL_MASK
Type				R/W	R/W	R/W		R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	Must only write 000b to these bits.
4	PLL_LOL_MASK	**Mask Bit for PLL_LOL.** When true, the PLL_LOL bit (Register 218) will not cause an interrupt. See also Register 247. 0: PLL Loss of Lock (LOL) triggers active interrupt on INTR output pin. 1: PLL Loss of Lock (LOL) ignored in generating interrupt output.
3	LOS_FDBK_MASK	**Mask Bit for Loss of Signal on IN4 or IN5,6.** When true, the LOS_FDBK bit (Register 218) will not cause an interrupt. See also Register 247. 0: FDBK LOS triggers active interrupt on INTR output pin. 1: FDBK LOS ignored in generating interrupt output.
2	LOS_CLKIN_MASK	**Mask Bit for Loss of Signal on IN1,2 or IN3.** When true, the LOS_CLKIN bit (Register 218) will not cause an interrupt. See also Register 247. 0: CLKIN LOS triggers active interrupt on INTR output pin. 1: CLKIN LOS ignored in generating interrupt output.
1	Reserved	Must only write 0 to this bit.
0	SYS_CAL_MASK	**Chip Calibration Mask Bit.** When true, the SYS_CAL bit (Register 218) will not cause an interrupt. See also Register 247. 0:PLL self-calibration triggers active interrupt on INTR output pin. 1:PLL self-calibration ignored in generating interrupt output.

Register 27.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	I2C_1P8_SEL	I2C_ADDR[6:0]						
Type	R/W	R/W*						

Reset value = xxxx xxxx

Bit	Name	Function
7	I2C_1P8_SEL	**I^2C Reference V_{DD}.** External I2C VDD 0 = 3.3 V/2.5 V, 1 = 1.8 V. 0: 3.3 V/2.5 V (default) 1: 1.8 V
6:0*	I2C_ADDR[6:0]	**7-Bit I^2C Address.** If and only if there is an I2C_LSB pin, the actual I^2C LSB address is the logical “or” of the bit in position 0 with the state of the I2C_LSB pin. Otherwise, the actual I2C_LSB is the LSB of this 7-bit address. Custom 7-bit I^2C addresses may be requested but must be even numbers if pin control of the I^2C address is to be implemented. For example, if the I^2C address = 70h, the I2C_LSB pin can change the LSB from 0 to 1. However, if the I^2C address = 71h, the I2C_LSB pin will have no effect upon the I^2C address.

***Note:** Although these bits are R/W, writing them is not supported. Custom I^2C addresses can be set at the factory. Contact your local sales office for details.

Register 28.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			P2DIV_IN[0]	P1DIV_IN[2:0]			XTAL_FREQ[1:0]	
Type	R/W		R/W	R/W			R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	Must only write a 00 to these bits.
5	P2DIV_IN[0]	This bit and Register 30[4:3] create a 3-bit field that selects the input to the P2 divider [reg30[4:3] reg28[5]] = P2DIV_IN[2:0]. 000b: Clock from IN5,IN6 is input to P2 divider 011b: Clock from IN4 is input to P2 100b: No clock is input to P2 All other bit values are reserved.
4:2	P1DIV_IN[2:0]	These three bits are combined with Register 29[4:3] and create a 5-bit field that selects the input to the P1 divider [reg29[4:3] reg28[4:2]] = P1DIV_IN[4:0]. 00000b: Clock from IN1,IN2 selected 01010b: Clock from IN3 selected 10101b: Crystal oscillator selected All other bit values are reserved and should not be written.
1:0	XTAL_FREQ[1:0]	**Crystal Frequency Range.** Select Xtal Frequency that you are using. For more information on using crystals, see “AN360: Crystal Selection Guide for Si533x/5x Devices”. 00b: 8–11 MHz 01b: 11–19 MHz 10b: 19–26 MHz 3: 26–30 MHz

Register 29.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PFD_IN_REF[2:0]			P1DIV_IN[4:3]		P1DIV[2:0]		
Type	R/W			R/W		R/W		

Reset value = xxxx xxxx

Bit	Name	Function
7:5	PFD_IN_REF[2:0]	Selects the input clock to be provided to the reference input of PLL Phase Frequency Detector (PFD). 000b: P1DIV_IN selected 001b: P2DIV_IN selected 010b: P1DIV_OUT (P1 divider output) selected 011b: P2DIV_OUT (P2 divider output) selected 100b: XOCLK selected 101b: No Clock selected 110b: Reserved 111b: Reserved
4:3	P1DIV_IN[4:3]	These two bits along with reg28[4:2] create a 5-bit field that selects the input to the P1 divider [reg29[4:3] reg28[4:2]] = P1DIV_IN[4:0]. 00000b: Clock from IN,2 selected 01010b: Clock from IN3 selected 10101b: Crystal oscillator selected All other bit values are reserved
2:0	P1DIV[2:0]	Sets the value of the P1 divider. 000b: Divide by 1 001b: Divide by 2 010b: Divide by 4 011b: Divide by 8 100b: Divide by 16 101b: Divide by 32 All other bit values are reserved.

Register 30.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PFD_IN_FB[2:0]			P2DIV_IN[2:1]		P2DIV[2:0]		
Type	R/W			R/W		R/W		

Reset value = xxxx xxxx

Bit	Name	Function
7:5	PFD_IN_FB[2:0]	Selects the external input applied to the PFD feedback input. See also Register 48[7]. 000b: P2DIV_IN (fbclk) 001b: P1DIV_IN (refclk) 010b: P2DIV_OUT (P2 divider output) selected 011b: P1DIV_OUT (P1 divider output) selected 100b: Reserved 101b: No Clock selected 110b: Reserved 111b: Reserved
4:3	P2DIV_IN[2:1]	These two bits and Register 28[5] create a 3-Bit field that selects the input to the P2 divider [reg30[4:3] reg28[5]] = P2DIV_IN[2:0]. 000b: Clock from IN5,IN6 is input to P2 divider 011b: Clock from IN4 is input to P2 100b: No clock is input to P2 All other bit values are reserved.
2:0	P2DIV[2:0]	Sets the value of the P2 the divider. 000b: Divide by 1 001b: Divide by 2 010b: Divide by 4 011b: Divide by 8 100b: Divide by 16 101b: Divide by 32 All other bit values are reserved.

Register 31.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	R0DIV_IN[2:0]			R0DIV[2:0]			MS0_PDN	DRV0_PDN
Type	R/W			R/W			R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	R0DIV_IN[2:0]	Selects the input to the R0 divider. R0 divider output goes to CLK0. 000b: P2DIV_IN (fbclk) selected 001b: P1DIV_IN (refclk) selected 010b: P2DIV_OUT (P2 divider output) selected 011b: P1DIV_OUT (P1 divider output) selected 100b: XOCLK selected 101b: MultiSynth0 output selected 110b: MultiSynth0 output selected 111b: No Clock selected
4:2	R0DIV[2:0]	**CLK0 R0 Output Divider.** 000b: Divide by 1 001b: Divide by 2 010b: Divide by 4 011b: Divide by 8 100b: Divide by 16 101b: Divide by 32 All other bit values are reserved.
1	MS0_PDN	**MultiSynth0 Power Down.** 0: MS0 MultiSynth powered up 1: MS0 MultiSynth powered down
0	DRV0_PDN	**R0 and CLK0 Power Down.** 0: R0 output divider and CLK0 driver powered up 1: R0 output divider and CLK0 driver powered down

Register 32.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	R1DIV_IN[2:0]			R1DIV[2:0]			MS1_PDN	DRV1_PDN
Type	R/W			R/W			R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	R1DIV_IN[2:0]	Selects the input to the R1 divider. R1 divider output goes to CLK1. 000b: P2DIV_IN (fbclk) selected 001b: P1DIV_IN (refclk) selected 010b: P2DIV_OUT (P2 divider output) selected 011b: P1DIV_OUT (P1 divider output) selected 100b: XOCLK selected 101b: MultiSynth0 output selected 110b: MultiSynth1 output selected 111b: No Clock selected
4:2	R1DIV[2:0]	**CLK1 R1 Output Divider.** 000b: Divide by 1 001b: Divide by 2 010b: Divide by 4 011b: Divide by 8 100b: Divide by 16 101b: Divide by 32 All other bit values are reserved.
1	MS1_PDN	**MultiSynth1 Power Down.** 0: MultiSynth1 is powered up 1: MultiSynth1 is powered down
0	DRV1_PDN	**R1 and CLK1 Power Down.** 0: R1 output divider and CLK1 driver powered up 1: R1 output divider and CLK1 driver powered down

Register 33.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	R2DIV_IN[2:0]			R2DIV[2:0]			MS2_PDN	DRV2_PDN
Type	R/W			R/W			R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	R2DIV_IN[2:0]	Selects the input to the R2 divider. R2 divider output goes to CLK2. 000b: P2DIV_IN (fbclk) selected 001b: P1DIV_IN (refclk) selected 010b: P2DIV_OUT (P2 divider output) selected 011b: P1DIV_OUT (P1 divider output) selected 100b: XOCLK selected 101b: MultiSynth0 output selected 110b: MultiSynth2 output selected 111b: No Clock selected
4:2	R2DIV[2:0]	**CLK2 R2 Output Divider.** 000b: Divide by 1 001b: Divide by 2 010b: Divide by 4 011b: Divide by 8 100b: Divide by 16 101b: Divide by 32 All other bit values are reserved.
1	MS2_PDN	**MultiSynth2 Power Down.** 0: MultiSynth2 powered up 1: MultiSynth2 powered down
0	DRV2_PDN	**R2 and CLK2 Power Down.** 0: R2 output divider and CLK2 driver powered up 1: R2 output divider and CLK2 driver powered down

Register 34.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	R3DIV_IN[2:0]			R3DIV[2:0]			MS3_PDN	DRV3_PDN
Type	R/W			R/W			R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	R3DIV_IN[2:0]	Selects the input to the R3 divider. R3 divider output goes to CLK3. 000b: P2DIV_IN (fbclk) selected 001b: P1DIV_IN (refclk) selected 010b: P2DIV_OUT (P2 divider output) selected 011b: P1DIV_OUT (P1 divider output) selected 100b: XOCLK selected 101b: MultiSynth0 output selected 110b: MultiSynth3 output selected 111b: No Clock selected
4:2	R3DIV[2:0]	**CLK3 R3 Output Divider.** 000b: Divide by 1 001b: Divide by 2 010b: Divide by 4 011b: Divide by 8 100b: Divide by 16 101b: Divide by 32 All other bit values are reserved.
1	MS3_PDN	**MultiSynth3 Powerdown.** 0: MultiSynth3 is power up 1: MultiSynth3 powered down
0	DRV3_PDN	**R3 and CLK3 Powerdown.** 0: R3 output divider and CLK3 driver powered up 1: R3 output divider and CLK3 driver powered down

Register 35.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DRV3_VDDO[1:0]		DRV2_VDDO[1:0]		DRV1_VDDO[1:0]		DRV0_VDDO[1:0]	
Type	R/W		R/W		R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:6	DRV3_VDDO[1:0]	**VDDO Setting for CLK3.** 00b: VDDO3 = 3.3 V (not for HSTL) 01b: VDDO3 = 2.5 V (not for HSTL) 10b: VDDO3 = 1.8 V (not for HSTL or LVPECL) 11b: VDDO3 = 1.5 V (HSTL only)
5:4	DRV2_VDDO[1:0]	**VDDO Setting for CLK2.** 00b: VDDO2 = 3.3 V (not for HSTL) 01b: VDDO2 = 2.5 V (not for HSTL) 10b: VDDO2 = 1.8 V (not for HSTL or LVPECL) 11b: VDDO2 = 1.5 V (HSTL only)
3:2	DRV1_VDDO[1:0]	**VDDO Setting for CLK1.** 00b: VDDO1 = 3.3 V (not for HSTL) 01b: VDDO1 = 2.5 V (not for HSTL) 10b: VDDO1 = 1.8 V (not for HSTL or LVPECL) 11b: VDDO1 = 1.5 V (HSTL only)
1:0	DRV0_VDDO[1:0]	**VDDO Setting for CLK0.** 00b: VDDO0 = 3.3 V (not for HSTL) 01b: VDDO0 = 2.5 V (not for HSTL) 10b: VDDO0 = 1.8 V (not for HSTL or LVPECL) 11b: VDDO0 = 1.5 V (HSTL only)
Note: If the VDDOx voltage is more than 15% below the programmed voltage setting in Register 35, the output driver may not turn on.		

Register 36.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DRV0_INV[1:0]		DRV0_FMT[2:0]		
Type				R/W		R/W		

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	
4:3	DRV0_INV[1:0]	**Output Driver Invert for CLK0.** 00b: No inversion from default setting 01b: CLK0A inverted (use only for CMOS/SSTL/HSTL) 10b: CLK0B inverted (use only for CMOS/SSTL/HSTL) 11b: CLK0A,B inverted from default setting
2:0	DRV0_FMT[2:0]	**CLK0 Signal Format.** 000b: Reserved 001b: CLK0A = (CMOS/SSTL/HSTL), CLK0B = off 010b: CLK0B = (CMOS/SSTL/HSTL), CLK0A = off 011b: CLK0A,B = (CMOS/SSTL/HSTL) A,B outputs are in phase by default. 100b: LVPECL 101b: CML 110b: LVDS 111b: HCSL

Register 37.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DRV1_INV[1:0]		DRV1_FMT[2:0]		
Type				R/W		R/W		

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	
4:3	DRV1_INV[1:0]	**Output Driver Invert for CLK1.** 00b: No inversion from default setting 01b: CLK1A inverted (use only for CMOS/SSTL/HSTL) 10b: CLK1B inverted (use only for CMOS/SSTL/HSTL) 11b: CLK1A,B inverted from default setting
2:0	DRV1_FMT[2:0]	**CLK1 Signal Format.** 000b: Reserved 001b: CLK1A = (CMOS/SSTL/HSTL), CLK1B = off 010b: CLK1B = (CMOS/SSTL/HSTL), CLK1A = off 011b: CLK1A,B = (CMOS/SSTL/HSTL) A,B outputs are in phase by default. 100b: LVPECL 101b: CML 110b: LVDS 111b: HCSL

Register 38.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DRV2_INV[1:0]		DRV2_FMT[2:0]		
Type				R/W		R/W		

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	
4:3	DRV2_INV[1:0]	**Output Driver Invert for CLK2.** 00b: No inversion from default setting 01b: CLK2A inverted (use only for CMOS/SSTL/HSTL) 10b: CLK2B inverted (use only for CMOS/SSTL/HSTL) 11b: CLK2A,B inverted from default setting
2:0	DRV2_FMT[2:0]	**CLK2 Signal Format.** 000b: Reserved 001b: CLK2A = (CMOS/SSTL/HSTL), CLK2B = off 010b: CLK2B = (CMOS/SSTL/HSTL), CLK2A = off 011b: CLK2A,B = (CMOS/SSTL/HSTL) A,B outputs are in phase by default. 100b: LVPECL 101b: CML 110b: LVDS 111b: HCSL

Register 39.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DRV3_INV[1:0]		DRV3_FMT[2:0]		
Type				R/W		R/W		

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	
4:3	DRV3_INV[1:0]	**Output Driver Invert for CLK3.** 00b: No inversion from default setting 01b: CLK3A inverted (use only for CMOS/SSTL/HSTL) 10b: CLK3B inverted (use only for CMOS/SSTL/HSTL) 11b: CLK3A,B inverted from default setting
2:0	DRV3_FMT[2:0]	**CLK3 Signal Format.** 000b: Reserved 001b: CLK3A = (CMOS/SSTL/HSTL), CLK3B = off 010b: CLK3B = (CMOS/SSTL/HSTL), CLK3A = off 011b: CLK3A,B = (CMOS/SSTL/HSTL) A,B outputs are in phase by default. 100b: LVPECL 101b: CML 110b: LVDS 111b: HCSL

Register 40.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DRV1_TRIM [2:0]			DRV0_TRIM [4:0]				
Type	R/W			R/W				

Reset value = xxxx xxxx

Bit	Name	Function
7:5	DRV1_TRIM [2:0]	**Trim Bits for CLK1 Driver.** Clockbuilder Desktop sets these values automatically.
4:3	DRV0_TRIM [4:0]	**Trim Bits for CLK0 Driver.** Clockbuilder Desktop sets these values automatically.

Register 41.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		DRV2_TRIM [4:0]					DRV1_TRIM [4:3]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	
6:2	DRV2_TRIM [4:0]	**Trim Bits for CLK2 Driver.** Clockbuilder Desktop sets these values automatically.
1:0	DRV1_TRIM [4:3]	**Trim Bits for CLK1 Driver.** Clockbuilder Desktop sets these values automatically.

Register 42.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DRV3_TRIM [4:0]				
Type	R/W							

Reset value = 00xx xxxx

Bit	Name	Function
7:6	Reserved	Must only write 00b to these bits.
5	Reserved	Must write 1b to this bit.
4:0	DRV3_TRIM [4:0]	**Trim Bits for CLK3.** Clockbuilder Desktop sets these values automatically.

Register 45.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FCAL_OVRD[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	FCAL_OVRD[7:0]	Bits 7:0 of the Override Frequency Calibration for the VCO.

Register 46.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FCAL_OVRD[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	FCAL_OVRD[15:8]	Bits 15:8 of the Override Frequency Calibration for the VCO.

Register 47.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							FCAL_OVRD[17:16]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	Reserved	Must write 000101b to these bits if the device is not factory programmed.
1:0	FCAL_OVRD[17:16]	Bits 17:16 of the Override Frequency Calibration for the VCO.

Register 48.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PFD_EXTFB	PLL_KPHI[6:0]						
Type	R/W	R/W						

Reset value = xxxx xxxx

Bit	Name	Function
7	PFD_EXTFB	Selects PFD feedback input from internal (see Register 30[7:5]) or external source. 0: Internal feedback path 1: External feedback path (zero delay mode)
6:0	PLL_KPHI[6:0]	Sets the charge pump current for the PFD. Clockbuilder Desktop sets these values automatically.

Register 49.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FCAL_OVRD_EN	VCO_GAIN[2:0]			RSEL[1:0]		BWSEL[1:0]	
Type	R/W	R/W			R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	FCAL_OVRD_EN	**FCAL Override Enable.** 0: Do not use FCAL value in registers 45,46,47 1: Use FCAL value in registers 45,46,47 Once a part is programmed and calibrated (FCAL), this bit must be set. See Si5338 data sheet for more information.
6:4	VCO_GAIN[2:0]	**Sets the VCO Gain.** Clockbuilder Desktop sets these values automatically.
3:2	RSEL[1:0]	**Loop Filter Resistor Select.** Clockbuilder Desktop sets these values automatically.
1:0	BWSEL[1:0]	**Select the PLL Loopfilter.** Clockbuilder Desktop sets these values automatically.

Register 50.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLL_ENABLE[1:0]		MSCAL[5:0]					
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	PLL_ENABLE[1:0]	00: Disable PLL. 11: Enable PLL. It is expected that all Si5338 applications will need to have the PLL enabled; however, the PLL may be disabled when the Si5338 is set up in buffer mode.
5:0	MSCAL[5:0]	**MultiSynth Calibration Value for Optimum Performance.** Clockbuilder Desktop sets these values automatically.

Register 51.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_HS	MS2_HS	MS1_HS	MS0_HS		MS_PEC[2:0]		
Type	R/W	R/W	R/W	R/W				

Reset value = xxxx x111

Bit	Name	Function
7	MS3_HS	**MultiSynth3 High Speed Mode.** This bit must be asserted to enable MultiSynth3 to divide by 4 or 6. When this bit is asserted, MultiSynth3 will only accept divide ratios of 4.0 or 6.0. Increment/decrement, SSC, and all phase functions are not available when this bit is set. 0: MultiSynth3 implements fractional divide ratios between 8 and 568 1: MultiSynth3 can only implement 4.0 or 6.0 divide ratio.
6	MS2_HS	**MultiSynth2 High Speed Mode.** This bit must be asserted to enable MultiSynth2 to divide by 4 or 6. When this bit is asserted, MultiSynth2 will only accept divide ratios of 4.0 or 6.0. Increment/decrement, SSC, and all phase functions are not available when this bit is set. 0: MultiSynth2 implements fractional divide ratios between 8 and 568. 1: MultiSynth2 can only implement 4.0 or 6.0 divide ratio.
5	MS1_HS	**MultiSynth1 High Speed Mode.** This bit must be asserted to enable MultiSynth1 to divide by 4 or 6. When this bit is asserted, MultiSynth1 will only accept divide ratios of 4.0 or 6.0. Increment/decrement, SSC, and all phase functions are not available when this bit is set. 0: MultiSynth1 implements fractional divide ratios between 8 and 568. 1: MultiSynth1 can only implement 4.0 or 6.0 divide ratio.
4	MS0_HS	**MultiSynth0 High Speed Mode.** This bit must be asserted to enable MultiSynth0 to divide by 4 or 6. When this bit is asserted, MultiSynth0 will only accept divide ratios of 4.0 or 6.0. Increment/decrement, SSC, and all phase functions are not available when this bit is set. 0: MultiSynth0 implements fractional divide ratios between 8 and 568. 1: MultiSynth0 can only implement 4.0 or 6.0 divide ratio.
3	Unused	
2:0	MS_PEC[2:0]	**MultiSynth Phase Error Correction.** All non-factory programmed devices must have 111b written to these bits.

Register 52.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS0_FIDCT[1:0]		MS0_FIDDIS	MS0_SSMODE[1:0]		MS0_PHIDCT[1:0]	
Type	R/W			R/W	R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	
6:5	MS0_FIDCT[1:0]	**MultiSynth0 Frequency Increment/Decrement Control.** Bit 4 (disable) must be 0 before writing an increment or decrement to these bits. Only MS0 can have pin control of Frequency Increment/Decrement. 00b: No frequency inc/dec on MS0 01b: Enable pin control of frequency inc/dec 10b: Frequency increment on MS0, self-clearing 11b: Frequency decrement on MS0, self-clearing
4	MS0_FIDDIS	**MultiSynth0 Frequency Increment/Decrement Disable (see also Register 242[1]).** 0: Frequency inc/dec enabled on MS0 1: Frequency inc/dec disabled on MS0 Set MS0_FIDDIS = 0 prior to writing a frequency increment/decrement command to register 52[6:5]. Writing MS0_FIDDIS back to a 1 (disabled) will cause the MS0 output frequency to go back to its initial programmed frequency.
3:2	MS0_SSMODE[1:0]	**MultiSynth0 Spread Spectrum Mode Select.** 00b: No SSC on MS0 01b or 10b or 11b: Down spread on MS0
1:0	MS0_PHIDCT[1:0]	**MultiSynth0 Phase Increment/Decrement Control.** 00b: No phase inc/dec on MS0 01b: Enable pin control of phase inc/dec 10b: Phase increment on MS0, self clearing 11b: Phase decrement on MS0, self clearing

Register 53.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P1[7:0]	**MultiSynth0 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multi-Synth0 divider.

Register 54.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
15:8	MS0_P1[15:8]	**MultiSynth0 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multi-Synth0 divider.

Register 55.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P2[5:0]						MS0_P1[17:16]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	MS0_P2[5:0]	**MultiSynth0 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth0 Divider.
1:0	MS0_P1[17:16]	**MultiSynth0 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth0 divider.

Register 56.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P2[13:6]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P2[13:6]	**MultiSynth0 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth0 Divider.

Register 57.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P2[21:14]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P2[21:14]	**MultiSynth0 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth0 Divider.

Register 58.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P2[29:22]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P2[29:22]	**MultiSynth0 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth0 Divider.

Register 59.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P3[7:0]	**MultiSynth0 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth0 divider.

Register 60.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P3[15:8]	**MultiSynth0 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth0 divider.

Register 61.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P3[23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P3[23:16]	**MultiSynth0 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth0 divider.

Register 62.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			MS0_P3[29:24]					
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	
5:0	MS0_P3[29:24]	**MultiSynth0 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth0 divider.

Register 63.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS1_FIDCT[1:0]		MS1_FIDDIS	MS1_SSMODE[1:0]		MS1_PHIDCT[1:0]	
Type	R/W			R/W	R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	
6:5	MS1_FIDCT[1:0]	**MultiSynth1 Frequency Increment/Decrement Control.** Bit 4 (disable) must be 0 before writing an increment or decrement to these bits. 00b: No frequency inc/dec on MS1 01b: Reserved 10b: Frequency increment on MS1, self-clearing 11b: Frequency decrement on MS1, self-clearing
4	MS1_FIDDIS	**MultiSynth1 Frequency Increment/Decrement Disable.** See also Register 242[1]. 0: Frequency inc/dec enabled on MS1 1: Frequency inc/dec disabled on MS1 Set MS1_FIDDIS = 0 prior to writing a frequency increment/decrement command to register 63[6:5]. Writing MS1_FIDDIS back to a 1 (disabled) will cause the MS1 output frequency to go back to its initial programmed frequency.
3:2	MS1_SSMODE[1:0]	**MultiSynth1 Spread Spectrum Mode Select.** 00b: No SSC on MS1 01b or 10b or 11b: Down spread on MS1
1:0	MS1_PHIDCT[1:0]	**MultiSynth1 Phase Increment/Decrement Control.** Writing a 10 or 11 will self clear back to 0. 00b: No phase inc/dec on MS1 01b: Enable pin control of phase inc/dec 10b: Phase increment on MS1, self clearing 11b: Phase decrement on MS1, self clearing

Register 64.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P1[7:0]	**MultiSynth1 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multi-Synth1 divider.

Register 65.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P1[15:8]	**MultiSynth1 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multi-Synth1 divider.

Register 66.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P2[5:0]						MS1_P1[17:16]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	MS1_P2[5:0]	**MultiSynth1 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth1 Divider.
1:0	MS1_P1[17:16]	**MultiSynth1 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth1 divider.

Register 67.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P2[13:6]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P2[13:6]	**MultiSynth1 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth1 Divider.

Register 68.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P2[21:14]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P2[21:14]	**MultiSynth1 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth1 Divider.

Register 69.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P2[29:22]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P2[29:22]	**MultiSynth1 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth1 Divider.

Register 70.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P3[7:0]	**MultiSynth1 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth1 Divider.

Register 71.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P3[15:8]	**MultiSynth1 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth1 Divider.

Register 72.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P3[23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P3[23:16]	**MultiSynth1 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth1 Divider.

Register 73.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			MS1_P3[29:24]					
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	
5:0	MS1_P3[29:24]	**MultiSynth1 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth1 Divider.

Register 74.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS2_FIDCT[1:0]		MS2_FIDDIS	MS2_SSMODE[1:0]		MS2_PHIDCT[1:0]	
Type	R/W			R/W	R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	
6:5	MS2_FIDCT[1:0]	**MultiSynth2 Frequency Increment/Decrement Control.** Bit 4 (disable) must be 0 before writing an increment or decrement to these bits. 00b: No frequency inc/dec on MS2 01b: Reserved 10b: Frequency increment on MS2, self-clearing 11b: Frequency decrement on MS2, self-clearing
4	MS2_FIDDIS	**MultiSynth2 Frequency Increment/Decrement Disable (see also Register 242[1]).** 0: Frequency inc/dec enabled on MS2 1: Frequency inc/dec disabled on MS2 Set MS2_FIDDIS = 0 prior to writing a frequency increment/decrement command to register 74[6:5]. Writing MS2_FIDDIS back to a 1 (disabled) will cause the MS2 output frequency to go back to its initial programmed frequency.
3:2	MS2_SSMODE[1:0]	**MultiSynth2 Spread Spectrum Mode Select.** 00b: No SSC on MS2 01b or 10b or 11b: Down spread on MS2
1:0	MS2_PHIDCT[1:0]	**MultiSynth2 Phase Increment/Decrement Control.** 00b: No phase inc/dec on MS2 01b: Enable pin control of phase inc/dec 10b: Phase increment on MS2, self clearing 11b: Phase decrement on MS2, self clearing

Register 75.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P1[7:0]	**MultiSynth2 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multi-Synth2 divider.

Register 76.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P1[15:8]	**MultiSynth2 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multi-Synth2 divider.

Register 77.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P2[5:0]						MS2_P1[17:16]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	MS2_P2[5:0]	**MultiSynth2 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth2 Divider.
1:0	MS2_P1[17:16]	**MultiSynth2 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth2 divider.

Register 78.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P2[13:6]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P2[13:6]	**MultiSynth2 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth2 Divider.

Register 79.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P2[21:14]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P2[21:14]	**MultiSynth2 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth2 Divider.

Register 80.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P2[29:22]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P2[29:22]	**MultiSynth2 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth2 Divider.

Register 81.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
	MS2_P3[7:0]	**MultiSynth2 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth2 Divider.

Register 82.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P3[15:8]	**MultiSynth2 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth2 Divider.

Register 83.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P3[23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P3[23:16]	**MultiSynth2 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth2 Divider.

Register 84.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			MS2_P3[29:24]					
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	
	MS2_P3[29:24]	**MultiSynth2 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth2 Divider.

Register 85.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS3_FIDCT[1:0]		MS3_FIDDIS	MS3_SSMODE[1:0]		MS3_PHIDCT[1:0]	
Type	R/W			R/W	R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	
6:5	MS3_FIDCT[1:0]	**MultiSynth3 Frequency Increment/Decrement Control.** Bit 4 (disable) must be 3 before writing an increment or decrement to these bits. 00b: No frequency inc/dec on MS3 01b: Reserved 10b: Frequency increment on MS3, self-clearing 11b: Frequency decrement on MS3, self-clearing
4	MS3_FIDDIS	**MultiSynth3 Frequency Increment/Decrement Disable (see also Register 242[1]).** 0: Frequency inc/dec enabled on MS3 1: Frequency inc/dec disabled on MS3 Set MS3_FIDDIS = 0 prior to writing a frequency increment/decrement command to register 85[6:5]. Writing MS3_FIDDIS back to a 1 (disabled) will cause the MS3 output frequency to go back to its initial programmed frequency.
3:2	MS3_SSMODE[1:0]	**MultiSynth3 Spread Spectrum Mode Select.** 00b: No SSC on MS3 01b or 10b or 11b: Down spread on MS3
1:0	MS3_PHIDCT[1:0]	**MultiSynth3 Phase Increment/Decrement Control.** 00b: No phase inc/dec on MS3 01b: Enable pin control of phase inc/dec 10b: Phase increment on MS3 11b: Phase decrement on MS3

Register 86.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P1[7:0]	**MultiSynth3 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multi-Synth3 divider.

Register 87.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P1[15:8]	**MultiSynth3 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multi-Synth3 divider

Register 88.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P2[5:0]						MS3_P1[17:16]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	MS3_P2[5:0]	**MultiSynth3 Parameter 2.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider.
1:0	MS3_P1[17:16]	**MultiSynth3 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multi-Synth3 divider.

Register 89.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P2[13:6]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P2[13:6]	**MultiSynth3 Parameter 2.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider.

Register 90.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P2[21:14]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P2[21:14]	**MultiSynth3 Parameter 2.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider.

Register 91.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P2[29:22]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P2[29:22]	**MultiSynth3 Parameter 2.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider.

Register 92.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P3[7:0]	**MultiSynth3 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider.

Register 93.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P3[15:8]	**MultiSynth3 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider

Register 94.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P3[23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P3[23:16]	**MultiSynth3 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider

Register 95.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			MS3_P3[29:24]					
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	
5:0	MS3_P3[29:24]	**MultiSynth3 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider.

Register 97.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P1[7:0]	**Feedback MultiSynthN Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth Feedback divider.

Register 98.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P1[15:8]	**Feedback MultiSynthN Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth Feedback divider.

Register 99.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P2[5:0]						MSN_P1[17:16]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	MSN_P2[5:0]	**Feedback MultiSynthN Parameter 2.** This 18-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth Feedback divider.
1:0	MSN_P1[17:16]	**Feedback MultiSynthN Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth Feedback divider.

Register 100.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P2[13:6]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P2[13:6]	**Feedback MultiSynthN Parameter 2.** This 18-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth Feedback divider.

Register 101.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P2[21:14]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P2[21:14]	**Feedback MultiSynthN Parameter 2.** This 18-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth Feedback divider.

Register 102.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P2[29:22]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P2[29:22]	**Feedback MultiSynthN Parameter 2.** This 18-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth Feedback divider.

Register 103.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P3[7:0]	**Feedback MultiSynthN Parameter 3.** This 18-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth Feedback divider.

Register 104.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P3[15:8]	**Feedback MultiSynthN Parameter 3.** This 18-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth Feedback divider

Register 105.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P3[23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P3[23:16]	**Feedback MultiSynthN Parameter 3.** This 18-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth Feedback divider.

Register 106.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			MSN_P3[29:24]					
Type	R/W		R/W					

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	Must write 1b to this bit.
6	Reserved	
5:0	MSN_P3[29:24]	**Feedback MultiSynthN Parameter 3.** This 18-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth Feedback divider.

Register 107.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_PHOFF[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_PHOFF[7:0]	**MultiSynth0 Initial Phase Offset.** MS0_PHOFF[14:0] is a 2s complement number. See Register 108 for the upper byte. The initial phase offset in seconds is MS0_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO in seconds.

Register 108.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS0_PHOFF[14:8]						
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	
6:0	MS0_PHOFF[14:8]	**MultiSynth0 Initial Phase Offset.** MS0_PHOFF[14:0] is a 2s complement number. See Register 107 for the lower byte. The initial phase offset in seconds is MS0_PHOFF[14:0]*Tvco/128 where Tvco is the period of the VCO in seconds.

Register 109.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_PHSTEP[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_PHSTEP[7:0]	**MultiSynth0 Phase Step Size.** The phase step size is MS0_PHSTEP[13:0]*Tvco/128 where Tvco is the period of the VCO in seconds. See Register 110 for the upper bits. Either the phase inc/dec pins (if available) or register 52[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 110.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK0_DISST[1:0]		MS0_PHSTEP[13:8]					
Type	R/W		R/W					

Reset value = xxxx xxxx

Bit	Name	Function
7:6	CLK0_DISST[1:0]	**CLK0 Output Driver State When Disabled.** 00: High impedance 01: Logic low 10: Logic high 11: Always on even if disabled
5:0	MS0_PHSTEP[13:8]	**MS0 Phase Step Size.** The phase step size is MS0_PHSTEP[13:0]*Tvco/128 where Tvco is the period of the VCO in seconds. See Register 109 for the lower byte. Either the phase inc/dec pins (if available) or register 52[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 111.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_PHOFF[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_PHOFF[7:0]	**MultiSynth1 Initial Phase Offset.** MS1_PHOFF[14:0] is a 2s complement number. See Register 112 for the upper byte. The initial phase offset in seconds is MS1_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO in seconds.

Register 112.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS1_PHOFF[14:8]						
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	
6:0	MS1_PHOFF[14:8]	**MultiSynth1 Initial Phase Offset.** MS1_PHOFF[14:0] is a 2s complement number. See Register 111 for the lower byte. The initial phase offset in seconds is MS1_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO in seconds.

Register 113.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_PHSTEP[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_PHSTEP[7:0]	**MultiSynth1 Phase Step Size.** The phase step size in seconds is MS1_PHSTEP[13:0] x Tvco/128 where Tvco is the period of the VCO in seconds. See Register 114 for the upper bits. Either the phase inc/dec pins (if available) or register 63[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 114.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK1_DISST[1:0]		MS1_PHSTEP[13:8]					
Type	R/W		R/W					

Reset value = xxxx xxxx

Bit	Name	Function
7:6	CLK1_DISST[1:0]	**MultiSynth1 Output Driver State When Disabled.** 00: High impedance 01: Logic low 10: Logic high 11: Always on even if disabled
5:0	MS1_PHSTEP[13:8]	**MultiSynth1 Phase Step Size.** The phase step size in seconds is MS1_PHSTEP[13:0]*Tvco/128 where Tvco is the period of the VCO in seconds. See Register 113 for the lower byte. Either the phase inc/dec pins (if available) or register 63[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 115.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_PHOFF[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_PHOFF[7:0]	**MultiSynth2 Initial Phase Offset.** MS2_PHOFF[14:0] is a 2s complement number. See Register 116 for the upper byte. The initial phase offset in seconds is MS2_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO in seconds.

Register 116.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS2_PHOFF[14:8]						
Type	R/W	R/W						

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	Must write 1b to this bit.
6:0	MS2_PHOFF[14:8]	**MultiSynth2 Initial Phase Offset.** MS2_PHOFF[14:0] is a 2s complement number. See Register 115 for the lower byte. The initial phase offset is MS2_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO in seconds.

Register 117.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_PHSTEP[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_PHSTEP[7:0]	**MultiSynth2 Phase Step Size.** The phase step size in seconds is MS2_PHSTEP[13:0] x Tvco/128 where Tvco is the period of the VCO in seconds. See Register 118 for the upper bits. Either the phase inc/dec pins (if available) or register 74[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 118.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK2_DISST[1:0]		MS2_PHSTEP[13:8]					
Type	R/W		R/W					

Reset value = xxxx xxxx

Bit	Name	Function
7:6	CLK2_DISST[1:0]	**MultiSynth2 Output Driver State When Disabled.** 00: High impedance 01: Logic low 10: Logic high 11: Always on even if disabled
5:0	MS2_PHSTEP[13:8]	**MultiSynth2 Phase Step Size.** The phase step size in seconds is MS2_PHSTEP[13:0]*Tvco/128 where Tvco is the period of the VCO in seconds. See Register 117 for the lower byte. Either the phase inc/dec pins (if available) or register 74[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 119.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_PHOFF[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_PHOFF[7:0]	**MultiSynth3 Initial Phase Offset.** MS3_PHOFF[14:0] is a 2s complement number. The initial phase offset in seconds is MS3_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO in seconds.

Register 120.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS3_PHOFF[14:8]						
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7	Unused	
6:0	MS3_PHOFF[14:8]	**MultiSynth3 Initial Phase Offset.** MS3_PHOFF[14:0] is a 2s complement number. The initial phase offset in seconds is MS3_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO in seconds.

Register 121.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_PHSTEP[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_PHSTEP[7:0]	**MultiSynth3 Phase Step Size.** The phase step size in seconds is MS3_PHSTEP[13:0] x Tvco/128 where Tvco is the period of the VCO in seconds. See Register 122 for the upper bits. Either the phase inc/dec pins (if available) or register 85[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 122.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK3_DISST[1:0]		MS3_PHSTEP[13:8]					
Type	R/W		R/W					

Reset value = xxxx xxxx

Bit	Name	Function
7:6	CLK3_DISST[1:0]	**MultiSynth3 Output Driver State When Disabled.** 00: High impedance 01: Logic low 10: Logic high 11: Always on even if disabled
5:0	MS3_PHSTEP[13:8]	**MultiSynth3 Phase Step Size.** The phase step size in seconds is MS3_PHSTEP[13:0] x Tvco/128 where Tvco is the period of the VCO in seconds. See Register 121 for the lower byte. Either the phase inc/dec pins (if available) or register 85[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 123.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP1[7:0]	**MultiSynth0 Frequency Increment/Decrement Parameter 1.**

Register 124.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP1 [15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP1 [15:8]	**MultiSynth0 Frequency Increment/Decrement Parameter 1.**

Register 125.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP1 [23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP1 [23:16]	**MultiSynth0 Frequency Increment/Decrement Parameter 1.**

Register 126.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP1 [31:24]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP1 [31:24]	**MultiSynth0 Frequency Increment/Decrement Parameter 1.**

Register 127.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP1 [39:32]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP1 [39:32]	**MultiSynth0 Frequency Increment/Decrement Parameter 1.**

Register 128.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP1 [47:40]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP1 [47:40]	**MultiSynth0 Frequency Increment/Decrement Parameter 1.**

Register 129.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS0_FIDP1 [51:48]			
Type					R/W			

Reset value = 001x xxxx

Bit	Name	Function
7:4	Reserved	
3:0	MS0_FIDP1[51:48]	**MultiSynth0 Frequency Increment/Decrement Parameter 1.**

Register 130.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS0_FIDP2 [51:48]			
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:4	Reserved	
3:0	MS0_FIDP2[51:48]	**MultiSynth0 Frequency Increment/Decrement Parameter 2.**

Register 131.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP2 [47:40]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP2 [47:40]	**MultiSynth0 Frequency Increment/Decrement Parameter 2.**

Register 132.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP2 [39:32]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP2 [39:32]	**MultiSynth0 Frequency Increment/Decrement Parameter 2.**

Register 133.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP2 [31:24]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP2 [31:24]	**MultiSynth0 Frequency Increment/Decrement Parameter 2.**

Register 134.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP2 [23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP2 [23:16]	**MultiSynth0 Frequency Increment/Decrement Parameter 2.**

Register 135.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP2 [15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP2 [15:8]	**MultiSynth0 Frequency Increment/Decrement Parameter 2.**

Register 136.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP2 [7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP2 [7:0]	**MultiSynth0 Frequency Increment/Decrement Parameter 2.**

Register 137.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP3 [7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP3 [7:0]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 138.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP3 [15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP3 [15:8]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 139.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP3 [23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP3 [23:16]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 140.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP3 [31:24]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP3 [31:24]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 141.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP3 [39:32]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP3 [39:32]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 142.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP3 [47:40]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP3 [47:40]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 143.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP3 [55:48]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP3 [55:48]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 144.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_ALL	MS0_FIDP3[62:56]						
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7	MS0_ALL	**Use MultiSynth0 for All Outputs.** If set, the MultiSynth0 output is routed to the mux at the input of each R divider. Unused MultiSynths should be powered down to save power.
6:0	MS0_FIDP3[62:56]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 152.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP1[7:0]	**MultiSynth1 Frequency Increment/Decrement Parameter 1.**

Register 153.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP1[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP1[15:8]	**MultiSynth1 Frequency Increment/Decrement Parameter 1.**

Register 154.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP1[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP1[23:16]	**MultiSynth1 Frequency Increment/Decrement Parameter 1.**

Register 155.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP1[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP1[31:24]	**MultiSynth1 Frequency Increment/Decrement Parameter 1.**

Register 156.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP1[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP1[39:32]	**MultiSynth1 Frequency Increment/Decrement Parameter 1.**

Register 157.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP1[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP1[47:40]	**MultiSynth1 Frequency Increment/Decrement Parameter 1.**

Register 158.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS1_FIDP1[51:48]			
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	MS1_FIDP1[51:48]	**MultiSynth1 Frequency Increment/Decrement Parameter 1.**

Register 159.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS1_FIDP2[51:48]			
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	MS1_FIDP2[51:48]	**MultiSynth1 Frequency Increment/Decrement Parameter 2.**

Register 160.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP2[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP2[47:40]	**MultiSynth1 Frequency Increment/Decrement Parameter 2.**

Register 161.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP2[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP2[39:32]	**MultiSynth1 Frequency Increment/Decrement Parameter 2.**

Register 162.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP2[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP2[31:24]	**MultiSynth1 Frequency Increment/Decrement Parameter 2.**

Register 163.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP2[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP2[23:16]	**MultiSynth1 Frequency Increment/Decrement Parameter 2.**

Register 164.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP2[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP2[15:8]	**MultiSynth1 Frequency Increment/Decrement Parameter 2.**

Register 165.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP2[7:0]	**MultiSynth1 Frequency Increment/Decrement Parameter 2.**

Register 166.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP3[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP3[7:0]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 167.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP3[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP3[15:8]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 168.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP3[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP3[23:16]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 169.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP3[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP3[31:24]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 170.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP3[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP3[39:32]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 171.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP3[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP3[47:40]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 172.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP3[55:48]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP3[55:48]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 173.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS1_FIDP3[62:56]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS1_FIDP3[62:56]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 174.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP1[7:0]	**MultiSynth2 Frequency Increment/Decrement Parameter 1.**

Register 175.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP1[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP1[15:8]	**MultiSynth2 Frequency Increment/Decrement Parameter 1.**

Register 176.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP1[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP1[23:16]	**MultiSynth2 Frequency Increment/Decrement Parameter 1.**

Register 177.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP1[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP1[31:24]	**MultiSynth2 Frequency Increment/Decrement Parameter 1.**

Register 178.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP1[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP1[39:32]	**MultiSynth2 Frequency Increment/Decrement Parameter 1.**

Register 179.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP1[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP1[47:40]	**MultiSynth2 Frequency Increment/Decrement Parameter 1.**

Register 180.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS2_FIDP1[51:48]			
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:4	Unused	
3:0	MS2_FIDP1[51:48]	**MultiSynth2 Frequency Increment/Decrement Parameter 1.**

Register 181.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS2_FIDP2[51:48]			
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	MS2_FIDP2[51:48]	**MultiSynth2 Frequency Increment/Decrement Parameter 2.**

Register 182.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP2[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP2[47:40]	**MultiSynth2 Frequency Increment/Decrement Parameter 2.**

Register 183.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP2[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP2[39:32]	**MultiSynth2 Frequency Increment/Decrement Parameter 2.**

Register 184.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP2[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP2[31:24]	**MultiSynth2 Frequency Increment/Decrement Parameter 2.**

Register 185.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP2[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP2[23:16]	**MultiSynth2 Frequency Increment/Decrement Parameter 2.**

Register 186.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP2[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP2[15:8]	**MultiSynth2 Frequency Increment/Decrement Parameter 2.**

Register 187.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP2[7:0]	**MultiSynth2 Frequency Increment/Decrement Parameter 2.**

Register 188.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP3[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP3[7:0]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 189.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP3[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP3[15:8]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 190.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP3[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP3[23:16]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 191.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP3[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP3[31:24]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 192.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP3[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP3[39:32]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 193.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP3[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP3[47:40]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 194.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP3[55:48]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP3[55:48]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 195.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS2_FIDP3[62:56]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS2_FIDP3[62:56]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 196.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP1[7:0]	**MultiSynth3 Frequency Increment/Decrement Parameter 1.**

Register 197.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP1[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP1[15:8]	**MultiSynth3 Frequency Increment/Decrement Parameter 1.**

Register 198.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP1[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP1[23:16]	**MultiSynth3 Frequency Increment/Decrement Parameter 1.**

Register 199.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP1[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP1[31:24]	**MultiSynth3 Frequency Increment/Decrement Parameter 1.**

Register 200.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP1[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP1[39:32]	**MultiSynth3 Frequency Increment/Decrement Parameter 1.**

Register 201.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP1[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP1[47:40]	**MultiSynth3 Frequency Increment/Decrement Parameter 1.**

Register 202.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS3_FIDP1 [51:48]			
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:4	Unused	
3:0	MS3_FIDP1 [51:48]	**MultiSynth3 Frequency Increment/Decrement Parameter 1.**

Register 203.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS3_FIDP2[51:48]			
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	MS3_FIDP2[51:48]	**MultiSynth3 Frequency Increment/Decrement Parameter 2.**

Register 204.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP2[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP2[47:40]	**MultiSynth3 Frequency Increment/Decrement Parameter 2.**

Register 205.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP2[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP2[39:32]	**MultiSynth3 Frequency Increment/Decrement Parameter 2.**

Register 206.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP2[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP2[31:24]	**MultiSynth3 Frequency Increment/Decrement Parameter 2.**

Register 207.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP2[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP2[23:16]	**MultiSynth3 Frequency Increment/Decrement Parameter 2.**

Register 208.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP2[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP2[15:8]	**MultiSynth3 Frequency Increment/Decrement Parameter 2.**

Register 209.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP2[7:0]	**MultiSynth3 Frequency Increment/Decrement Parameter 2.**

Register 210.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP3[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP3[7:0]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 211.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP3[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP3[15:8]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 212.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP3[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP3[23:16]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 213.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP3[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP3[31:24]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 214.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP3[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP3[39:32]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 215.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP3[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP3[47:40]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 216.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP3[55:48]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP3[55:48]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 217.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS3_FIDP3[62:56]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS3_FIDP3[62:56]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 218.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				PLL_LOL	LOS_FDBK	LOS_CLKIN		SYS_CAL
Type				R	R	R		R

Reset value = 0000 0000

Bit	Name	Function
7:5	Reserved	
4	PLL_LOL	**PLL Loss of Lock (LOL).** Asserts when the two PFD inputs have a frequency difference > 1000 ppm. This bit is held high during a POR_reset until the PLL has locked. This bit will not chatter while the PLL is locking. PLL_LOL does not assert when the external input reference clock is lost. When PLL_LOL asserts, the part will automatically try to re-acquire to the input clock. See Register 241[7].
3	LOS_FDBK	**Loss of Signal on Feedback Clock from IN5,6 or IN4.**
2	LOS_CLKIN	**Loss of Signal on Input Clock from IN1,2 or IN3.**
1	Reserved	
0	SYS_CAL	**Device Calibration in Process.**

Register 226.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						MS_RESET		
Type						R		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	
2	MS_RESET	**Multisynth Master Reset.** This reset will disable all clock outputs, reset all Multisynth blocks, and then enable all the clock outputs. Retains device configuration stored in RAM. Do not use read-modify-write procedure to perform soft reset. Instead, write reg242 = 0x04 or 0x00. All Multisynth blocks will remain in reset until a 0 is written to this bit.
1:0	Reserved	

Register 230.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				OEB_ALL	OEB_3	OEB_2	OEB_1	OEB_0
Type				R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7:5	Unused	
4	OEB_ALL	**Output Enable Low for All Clock Outputs** 0: All output clocks are enabled, OEB_3,2,1,0 can still disable each clock. 1: All output clocks are disabled regardless of the state of OEB_3,2,1,0.
3	OEB_3	**Output Enable Low for CLK3** 0: CLK3 output is enabled 1: CLK3 output is disabled
2	OEB_2	**Output Enable Low for CLK2** 0: CLK2 output is enabled 1: CLK2 output is disabled
1	OEB_1	**Output Enable Low for CLK1** 0: CLK1 output is enabled 1: CLK1 output is disabled
0	OEB_0	**Output Enable Low for CLK0** 0: CLK0 output is enabled 1: CLK0 output is disabled

Register 235.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FCAL[7:0]							
Type	R							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	FCAL[7:0]	**Bits 7:0 of the Frequency Calibration for the VCO.**

Register 236.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FCAL[15:8]							
Type	R							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	FCAL[15:8]	**Bits 15:8 of the Frequency Calibration for the VCO.**

Register 237.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						FCAL[17:16]	
Type	R						R	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	Reserved	
1:0	FCAL[17:16]	**Bits 17:16 of the Frequency Calibration for the VCO.**

Register 241.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIS_LOL	Reserved. Write to 0x65.						
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7	DIS_LOL	When asserted, the PLL_LOL status in register 218 is prevented from asserting.
6:0	Reserved	On a non-factory-programmed device this register must be set to 0x65. On a factory programmed device, this register must stay 0x65. See the I^2C Programming Procedure in the Si5338 data sheet for when to write this register.

Register 242.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							DCLK_DIS	
Type							R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	Reserved	
1	DCLK_DIS	**Disable Clock to INC/DEC State Machine.** When true, the frequency inc/dec logic is disabled, which saves about 2 mA of current. See also Registers 52[4], 63[4], 74[4], 85[4].
0	Reserved	

Register 246.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							SOFT_RESET	
Type							R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:2	Reserved	
1	SOFT_RESET	**Soft Reset.** This reset will disable all clock outputs, then re-acquire the PLL to the input clock and then enable all the clock outputs. Retains device configuration stored in RAM. Do not use read-modify-write procedure to perform soft reset. Instead, write reg246=0x02, regardless of the current value of this bit. Reading this bit after a soft reset will return a 1.
0	Reserved	

Register 247.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				PLL_LOL_STK	LOS_FDBK_STK	LOS_CLKIN_STK		SYS_CAL_STK
Type				R/W	R/W	R/W		R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	
4	PLL_LOL_STK	**PLL Loss of Lock Sticky Bit.** Sticky version of PLL_LOL. See also Registers 6 and 218. Only a soft or POR reset or writing a “0” to this bit will clear it.
3	LOS_FDBK_STK	**Feedback Clock Loss of Signal Sticky Bit.** Sticky version of LOS_FDBK. See also Registers 6 and 218. Only a soft or POR reset or writing a “0” to this bit will clear it.
2	LOS_CLKIN_STK	**Input Clock Loss of Signal Sticky Bit.** Sticky version of LOS_CLKIN_STK. See also Registers 6 and 218. Only a soft or POR reset or writing a “0” to this bit will clear it.
1	Reserved	
0	SYS_CAL_STK	**System Calibration in Process Sticky Bit.** Sticky version of SYS_CAL. See also Registers 6 and 218. Only a soft or POR reset or writing a “0” to this bit will clear it.

Register 255.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								PAGE_SEL
Type								R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:1	Unused	
0	PAGE_SEL	Set to 0 to access registers 0–254, set to 1 to access register 256 to 347.

Register 287.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSUPP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS0_SSUPP2[7:0]	**MultiSynth0 Spread Spectrum Up Parameter 2.**

Register 288.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS0_SSUPP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS0_SSUPP2[14:8]	**MultiSynth0 Spread Spectrum Up Parameter 2.**

Register 289.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSUPP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MS0_SSUPP3[7:0]	**MultiSynth0 Spread Spectrum Up Parameter 3.**

Register 290.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS0_SSUPP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS0_SSUPP3[14:8]	**MultiSynth0 Spread Spectrum Up Parameter 3.**

Register 291.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSUPP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS0_SSUPP1[7:0]	**MultiSynth0 Spread Spectrum Up Parameter 1.**

Register 292.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSUDP1[3:0]				MS0_SSUPP1[11:8]			
Type	R/W				R/W			

Reset value = 1001 0000

Bit	Name	Function
7:4	MS0_SSUDP1[3:0]	**MultiSynth0 Spread Spectrum Up/Down Parameter 1.**
3:0	MS0_SSUPP1[11:8]	**MultiSynth0 Spread Spectrum Up Parameter 1.**

Register 293.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSUDP1[11:4]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	MS0_SSUDP1[11:4]	**MultiSynth0 Spread Spectrum Up/Down Parameter 1.**

Register 294.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSDNP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS0_SSDNP2[7:0]	**MultiSynth0 Spread Spectrum Down Parameter 2.**

Register 295.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS0_SSDNP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS0_SSDNP2[14:8]	**MultiSynth0 Spread Spectrum Down Parameter 2.**

Register 296.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSDNP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MS0_SSDNP3[7:0]	**MultiSynth0 Spread Spectrum Down Parameter 3.**

Register 297.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS0_SSDNP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS0_SSDNP3[14:8]	**MultiSynth0 Spread Spectrum Down Parameter 3.**

Register 298.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSDNP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS0_SSDNP1[7:0]	**MultiSynth0 Spread Spectrum Down Parameter 1.**

Register 299.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS0_SSDNP1[11:8]			
Type	R/W				R/W			

Reset value = 0011 0001

Bit	Name	Function
7:4	Reserved	
3:0	MS0_SSDNP1[11:8]	**MultiSynth0 Spread Spectrum Down Parameter 1.**

Register 303.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSUPP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_SSUPP2[7:0]	**MultiSynth1 Spread Spectrum Up Parameter 2.**

Register 304.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS1_SSUPP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS1_SSUPP2[14:8]	**MultiSynth1 Spread Spectrum Up Parameter 2.**

Register 305.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSUPP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MS1_SSUPP3[7:0]	**MultiSynth1 Spread Spectrum Up Parameter 3.**

Register 306.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS1_SSUPP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS1_SSUPP3[14:8]	**MultiSynth1 Spread Spectrum Up Parameter 3.**

Register 307.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSUPP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_SSUPP1[7:0]	**MultiSynth1 Spread Spectrum Up Parameter 1.**

Register 308.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSUDP1[3:0]				MS1_SSUPP1[11:8]			
Type	R/W				R/W			

Reset value = 1001 0000

Bit	Name	Function
7:4	MS1_SSUDP1[3:0]	**MultiSynth1 Spread Spectrum Up/Down Parameter 1.**
3:0	MS1_SSUPP1[11:8]	**MultiSynth1 Spread Spectrum Up Parameter 1.**

Register 309.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSUDP1[11:4]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	MS1_SSUDP1[11:4]	**MultiSynth1 Spread Spectrum Up/Down Parameter 1.**

Register 310.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSDNP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_SSDNP2[7:0]	**MultiSynth1 Spread Spectrum Down Parameter 2.**

Register 311.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS1_SSDNP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS1_SSDNP2[14:8]	**MultiSynth1 Spread Spectrum Down Parameter 2.**

Register 312.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSDNP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MS1_SSDNP3[7:0]	**MultiSynth1 Spread Spectrum Down Parameter 3.**

Register 313.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS1_SSDNP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS1_SSDNP3[14:8]	**MultiSynth1 Spread Spectrum Down Parameter 3.**

Register 314.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSDNP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_SSDNP1[7:0]	**MultiSynth1 Spread Spectrum Down Parameter 1.**

Register 315.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS1_SSDNP1[11:8]			
Type	R/W				R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	MS1_SSDNP1[11:8]	**MultiSynth1 Spread Spectrum Down Parameter 1.**

Register 319.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSUPP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_SSUPP2[7:0]	**MultiSynth2 Spread Spectrum Up Parameter 2.**

Register 320.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS2_SSUPP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS2_SSUPP2[14:8]	**MultiSynth2 Spread Spectrum Up Parameter 2.**

Register 321.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSUPP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MS2_SSUPP3[7:0]	**MultiSynth2 Spread Spectrum Up Parameter 3.**

Register 322.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS2_SSUPP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS2_SSUPP3[14:8]	**MultiSynth2 Spread Spectrum Up Parameter 3.**

Register 323.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSUPP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_SSUPP1[7:0]	**MultiSynth2 Spread Spectrum Up Parameter 1.**

Register 324.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSUDP1[3:0]				MS2_SSUPP1[11:8]			
Type	R/W				R/W			

Reset value = 1001 0000

Bit	Name	Function
7:4	MS2_SSUDP1[3:0]	**MultiSynth2 Spread Spectrum Up/Down Parameter 1.**
3:0	MS2_SSUPP1[11:8]	**MultiSynth2 Spread Spectrum Up Parameter 1.**

Register 325.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSUDP1[11:4]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	MS2_SSUDP1[11:4]	**MultiSynth2 Spread Spectrum Up/Down Parameter 1.**

Register 326.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSDNP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_SSDNP2[7:0]	**MultiSynth2 Spread Spectrum Down Parameter 2.**

Register 327.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS2_SSDNP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS2_SSDNP2[14:8]	**MultiSynth2 Spread Spectrum Down Parameter 2.**

Register 328.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSDNP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MS2_SSDNP3[7:0]	**MultiSynth2 Spread Spectrum Down Parameter 3.**

Register 329.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS2_SSDNP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS2_SSDNP3[14:8]	**MultiSynth2 Spread Spectrum Down Parameter 3.**

Register 330.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSDNP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_SSDNP1[7:0]	**MultiSynth2 Spread Spectrum Down Parameter 1.**

Register 331.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS2_SSDNP1[11:8]			
Type	R/W				R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	MS2_SSDNP1[11:8]	**MultiSynth2 Spread Spectrum Down Parameter 1.**

Register 335.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSUPP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_SSUPP2[7:0]	**MultiSynth3 Spread Spectrum Up Parameter 2.**

Register 336.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS3_SSUPP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS3_SSUPP2[14:8]	**MultiSynth3 Spread Spectrum Up Parameter 2.**

Register 337.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSUPP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MS3_SSUPP3[7:0]	**MultiSynth3 Spread Spectrum Up Parameter 3.**

Register 338.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS3_SSUPP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS3_SSUPP3[14:8]	**MultiSynth3 Spread Spectrum Up Parameter 3.**

Register 339.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSUPP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_SSUPP1[7:0]	**MultiSynth3 Spread Spectrum Up Parameter 1.**

Register 340.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSUDP1[3:0]				MS3_SSUPP1[11:8]			
Type	R/W				R/W			

Reset value = 1001 0000

Bit	Name	Function
7:4	MS3_SSUDP1[3:0]	**MultiSynth3 Spread Spectrum Up/Down Parameter 1.**
3:0	MS3_SSUPP1[11:8]	**MultiSynth3 Spread Spectrum Up Parameter 1.**

Register 341.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSUDP1[11:4]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	MS3_SSUDP1[11:4]	**MultiSynth3 Spread Spectrum Up/Down Parameter 2.**

Register 342.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSDNP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_SSDNP2[7:0]	**MultiSynth3 Spread Spectrum Down Parameter 2.**

Register 343.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS3_SSDNP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS3_SSDNP2[14:8]	**MultiSynth3 Spread Spectrum Down Parameter 2.**

Register 344.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSDNP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MS3_SSDNP3[7:0]	**MultiSynth3 Spread Spectrum Down Parameter 3.**

Register 345.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS3_SSDNP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	
6:0	MS3_SSDNP3[14:8]	**MultiSynth3 Spread Spectrum Down Parameter 3.**

Register 346.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSDNP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_SSDNP1[7:0]	**MultiSynth3 Spread Spectrum Down Parameter 1.**

Register 347.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS3_SSDNP1[11:8]			
Type	R/W				R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	
3:0	MS3_SSDNP1[11:8]	**MultiSynth3 Spread Spectrum Down Parameter 1.**

DOCUMENT CHANGE LIST

Revision 0.3 to Revision 0.4

- Updated "1. Introduction" on page 4.
  - Replaced summary register map with detailed register map.
- Updated "3. Configuring the Si5338" on page 6 for clarity.
- Updated Figure 7 for clarity and correctness.
- Updated Figure 3 to agree with register field names.
- Moved Section 4.3 to 4.1.
- Updated "5. Configuring PLL Parameters" on page 15.
  - Added text for clarity.
- Updated Equation 1 for clarity.
- Consolidated Sections 6.1, 6.2, 6.3, and 6.4 into Section 6.0.
- Updated "5. Configuring PLL Parameters" on page 15 for clarity.
- Added "6. Configuring the Frequency Increment/ Decrement" on page 16.
- Added "7. Configuring Initial Phase Offset and Phase Step Size" on page 17.
- Added "8. Configuring Spread Spectrum" on page 19.
- Removed Section 8.
- Added "10. Si5338 Registers" on page 28, which includes all the registers.
- Added " Table of Contents" on page 3.
- Removed “12. Read Modify Write Requirement” section.
- Removed “13. VCO Calibration and Soft Reset” section.

Revision 0.4 to Revision 0.5

- Added CML driver to 9.2 and 9.3.
- Updated Figure 3 and Equation 1.
- Updated Figure 7 on page 13.
  - Changed the default value of register 28[7] from 0 to 1.
- Updated Figure 8 on page 14.
  - Changed the default value of register 28[7] from 0 to 1 and removed the default values from register 30[7:5].
- Updated "5. Configuring PLL Parameters" on page 15.
  - Added figure number.
  - Added “round()” to the first equation in this section.

Revision 0.5 to Revision 0.6

- Updated "3.2. Calculating MultiSynth Values" on page 8.
  - Added information about Register 51[7:4].
- Updated Equation 1 on page 9.
  - “Note:...to 1” was changed to be a more accurate statement.
- Updated Figure 9 on page 15.
  - Reg50[7:6] changed from 0 to 1.
- Updated "6. Configuring the Frequency Increment/ Decrement" on page 16.
  - Added reference to register locations of Finc/Fdec.
- Updated "7.2. Phase Step Size" on page 17.
  - Added reference to registers for Pinc/Pdec.
- Updated "9.3. Output Driver Trim" on page 23.
  - Specified register42[7:5] = 001b.
  - Added 1.8 V LVDS to Driver type and trim table.
- Updated "10.2. Miscellaneous Register Writes" on page 28.
  - Changed register 47[5:2] = 0101b to Register 47[7:2] = 000101b.
  - Removed Register 241 = 0x65 as this is already detailed in the 5338 data sheet Figure 9.
  - Changed Register 28[7:6] = 10b to 00b.
- Updated Register 42.
  - Changed reset value of bits 7:6 to 00.
- Updated Register 51.
  - Clarified that bits 7:4 must be set to achiev /4 or /6 from the respective MultiSynth.

Revision 0.6 to Revision 1.0

- Changed document type from application note (AN411) to reference manual (Si5338-RM Reference Manual).
- Added information on registers 2–5.
- Corrected register 47 read-modify-write mask to allow writes to bits 7:6.
- Corrected reset value of register 289 from 0x00 to 0x01.
- Corrected reset value of register 292 from 0x30 to 0x90.

Revision 1.0 to Revision 1.1

- Updated "10. Si5338 Registers" on page 28.
  - Added information on Multisynth Reset (MS_RESET) register bit.

Revision 1.1 to Revision 1.2

- Updated "8.2. Center Spread" on page 20 and added “8.2.1. Center Spread Equations for Rev A Devices”.
- Updated descriptions on Registers 0, 52, 63, 74, and 85.
- Updated section 10.6.1. Example Part Number for Device ID Registers to include Rev B information.

Revision 1.2 to Revision 1.3

- Fixed typos in Up Parameters in "8.1. Down Spread" on page 19.

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