Pin Definitions

Table 1-5 lists the pin definitions used in Zynq-7000 AP SoC packages.

Note: There are dedicated general purpose user I/O pins listed separately in Table 1-5. There are also multi-function pins where the pin names start with either IO_LXXY_ZZZ_# or IO_XX_ZZZ_#, where ZZZ represents one or more functions in addition to being general purpose user I/O. If not used for their special function, these pins can be user I/O.

Table 1-5: **Zynq-7000 AP SoC Pin Definitions**

Pin Name	Type	Direction	Description
User I/O Pins			
IO_LXXY_# IO_XX_#	Dedicated	Input/ Output	Most user I/O pins are capable of differential signaling and can be implemented as pairs. The top and bottom I/O pins are always single ended. Each user I/O is labeled IO_LXXY_#, where: • IO indicates a user I/O pin. • L indicates a differential pair, with XX a unique pair in the bank and Y = [P|N] for the positive/negative sides of the differential pair. • # indicates a bank number.
Configuration Pins			
For more information about these pins, see the *Configuration Pin Definitions* table in UG470, *7 Series FPGAs Configuration User Guide*. See also the *Boot and Configuration* chapter in UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual*.			
DONE_0	Dedicated(1)	Bidirectional	Active High, DONE indicates successful completion of configuration.
INIT_B_0	Dedicated(1)	Bidirectional (open-drain)	Active Low, indicates initialization of configuration memory.
PROGRAM_B_0	Dedicated(1)	Input	Active Low, asynchronous reset to configuration logic.
TCK_0	Dedicated(1)	Input	JTAG clock.
TDI_0	Dedicated(1)	Input	JTAG data input.
TDO_0	Dedicated(1)	Output	JTAG data output.
TMS_0	Dedicated(1)	Input	JTAG mode select.
CFGBVS_0	Dedicated(1)	Input	This pin selects the preconfiguration I/O standard type for the dedicated configuration bank 0. If the V_{CCO} for bank 0 is 2.5V or 3.3V, then this pin must be connected to V_{CCO_0}. If the V_{CCO} for bank 0 is less than or equal to 1.8V, then this pin should be connected to GND. ***Note:*** To avoid device damage, this pin must be connected correctly. See the *Configuration Bank Voltage Select* section in UG470, *7 Series FPGAs Configuration User Guide* for more information.

Table 1-5: **Zynq-7000 AP SoC Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
PUDC_B	Multi-function	Input	Pull-Up During Configuration (bar) Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration. ◦ When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin. ◦ When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin. PUDC_B must be tied either directly (or through a 1KΩ or less resistor) to VCCO_34 or GND. **CAUTION!** *Do not allow this pin to float before and during configuration.*
Power/Ground Pins			
GND	Dedicated	N/A	Ground, tied common.
VCCPINT	Dedicated	N/A	1.0V logic supply for PS. Independent from PL V_{CCINT} supply.
VCCPAUX	Dedicated	N/A	1.8V auxiliary power supply for PS. Independent from PL V_{CCAUX} supply.
VCCO_MIO0	Dedicated	N/A	1.8V–3.3V PS I/O supply for MIO bank 500.
VCCO_MIO1	Dedicated	N/A	1.8V–3.3V PS I/O supply for MIO bank 501.
VCCO_DDR	Dedicated	N/A	1.2V–1.8V DDR I/O supply.
VCCPLL(2)	Dedicated	N/A	1.8V PLL supply for PS. A 0.47 µF to 4.7 µF 0402 capacitor must be placed near the V_{CCPLL} BGA via. In addition, when powered by V_{CCPAUX}, the V_{CCPLL} must be filtered through a 120Ω at 100 MHz (size 0603) ferrite bead and a 10 µF (size 0603) decoupling capacitor to minimize PLL jitter.
VCCAUX	Dedicated	N/A	1.8V power-supply pins for auxiliary circuits.
VCCAUX_IO_G#(3)	Dedicated	N/A	1.8V/2.0V power-supply pins for auxiliary I/O circuits.
VCCINT	Dedicated	N/A	1.0V power-supply pins for the internal core logic.
VCCO_#(4)	Dedicated	N/A	Power-supply pins for the output drivers (per bank).
VCCBRAM	Dedicated	N/A	1.0V power-supply pins for the PL block RAM.
VCCBATT_0	Dedicated	N/A	Decryptor key memory backup supply; this pin should be tied to the appropriate V_{CC} or GND when not used.(5)
VREF	Multi-function	N/A	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
RSVDVCC[3:1]	Dedicated	N/A	Reserved pins—must be tied to V_{CCO_0}.
RSVDGND	Dedicated	N/A	Reserved pins—must be tied to GND.

Table 1-5: **Zynq-7000 AP SoC Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
PS MIO Pins			
PS_POR_B	Dedicated	Input	Power on reset. The PS_POR_B must be asserted to GND during the power-on sequence until V_{CCPINT}, V_{CCPAUX}, and V_{CCO_MIO0} have reached the minimum operating levels and the PS_CLK reference is within specification. When deasserted, the PS begins the boot process. Before V_{CCPINT} reaches 0.80V, at least one of these four conditions is required during the power-off stage: ◦ The PS_POR_B input is asserted to GND. ◦ The reference clock to the PS_CLK input is disabled. ◦ V_{CCPAUX} is lower than 0.70V. ◦ V_{CCO_MIO0} is lower than 0.90V. To ensure PS eFUSE integrity, the applicable condition must be held until V_{CCPINT} reaches 0.40V. See the *Zynq-7000 All Programmable SoC (Z-7010, Z-7015, and Z-7020) Data Sheet: DC and AC Switching Characteristics* (DS187) [Ref 4] and *Zynq-7000 All Programmable SoC (Z-7030, Z-7035, Z-7045, and Z-7100) Data Sheet: DC and AC Switching Characteristics* (DS191) [Ref 5] for more information on the power-on sequence.
PS_CLK	Dedicated	Input	System reference clock. PS_CLK must be between 30 MHz and 60 MHz.
PS_SRST_B	Dedicated	Input	System reset. For use with debuggers. When 0, forces the PS to enter the system reset sequence.
PS_MIO_VREF	Dedicated	Voltage Reference	The PS_MIO_VREF provides a reference voltage for the RGMII input receivers. If an RGMII interface is not being used, the PS_MIO_VREF pin can be left to float. If an RGMII interface is being used, tie this pin to a voltage equal to ½ V_{CCO_MIO1}. Example: When using a HSTL18 RGMII interface the V_{CCO_MIO1} is set to 1.8V. The PS_MIO_VREF must be set to 0.9V. A resistor divider can be used to generate the PS_MIO_VREF. See UG933, *Zynq-7000 All Programmable SoC PCB Design Guide* for decoupling recommendations.
PS_MIO[53:0]	Multi-function	Input/Output	Multiuse I/O. Multiuse I/O can be configured to support multiple I/O interfaces. These interfaces include SPI and Quad-SPI flash, NAND, USB, Ethernet, SDIO, UART, SPI, and GPIO interfaces.

Table 1-5: **Zynq-7000 AP SoC Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
PS DDR Pins			
PS_DDR_CKP	Dedicated	Output	DDR differential clock positive.
PS_DDR_CKN	Dedicated	Output	DDR differential clock negative.
PS_DDR_CKE	Dedicated	Output	DDR clock enable.
PS_DDR_CS_B	Dedicated	Output	DDR chip select.
PS_DDR_RAS_B	Dedicated	Output	DDR RAS control signal.
PS_DDR_CAS_B	Dedicated	Output	DDR CAS control signal.
PS_DDR_WE_B	Dedicated	Output	DDR write enable signal.
PS_DDR_BA[2:0]	Dedicated	Output	DDR bank address.
PS_DDR_A[14:0]	Dedicated	Output	DDR row and column address.
PS_DDR_ODT	Dedicated	Output	DDR termination control.
PS_DDR_DRST_B	Dedicated	Output	DDR reset signal for DDR3 devices.
PS_DDR_DQ[31:0]	Dedicated	Input/Output	DDR data.
PS_DDR_DM[3:0]	Dedicated	Output	DDR data mask.
PS_DDR_DQS_P[3:0]	Dedicated	Input/Output	DDR differential data strobe positive.
PS_DDR_DQS_N[3:0]	Dedicated	Input/Output	DDR differential data strobe negative.
PS_DDR_VRP	Dedicated	Output	DDR DCI voltage reference positive. Used to calibrate DDR I/O drive strength. Connect to a resistor to GND. The value of the resistor should be twice the DDR termination and trace impedance.
PS_DDR_VRN	Dedicated	Output	DDR DCI voltage reference negative. Used to calibrate DDR I/O drive strength. Connect to a resistor to V_{CCO_DDR}. The value of the resistor should be twice the DDR termination and trace impedance.
PS_DDR_VREF[1:0]	Dedicated	Voltage Reference	Voltage reference for the DDR interface.
Analog to Digital Converter (XADC) Pins			
For more information, see the *XADC Package Pins* table in UG480, *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide*.			
VCCADC_0(6)	Dedicated	N/A	XADC analog positive supply voltage.
GNDADC_0(6)	Dedicated	N/A	XADC analog ground reference.
VP_0(6)	Dedicated	Input	XADC dedicated differential analog input (positive side).
VN_0(6)	Dedicated	Input	XADC dedicated differential analog input (negative side).
VREFP_0(6)	Dedicated	N/A	1.25V reference input.
VREFN_ 0(6)	Dedicated	N/A	1.25V reference GND reference.
AD0P through AD15P AD0N through AD15N	Multi-function	Input	XADC (analog-to-digital converter) differential auxiliary analog inputs 0–15.

Table 1-5: **Zynq-7000 AP SoC Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
Multi-gigabit Serial Transceiver Pins (GTXE2 and GTPE2)			
For more information on the GTXE2 pins see the *Pin Description and Design Guidelines* section in UG476, *7 Series FPGAs GTX/GTH Transceivers User Guide*. The GTPE2 pins are described in the *Pin Description and Design Guidelines* section of UG482, *7 Series FPGAs GTP Transceivers User Guide*.			
MGTXRXP[0:3] or MGTPRXP[0:3]	Dedicated	Input	Positive differential receive port.
MGTXRXN[0:3] or MGTPRXN[0:3]	Dedicated	Input	Negative differential receive port.
MGTXTXP[0:3] or MGTPTXP[0:3]	Dedicated	Output	Positive differential transmit port.
MGTXTXN[0:3] or MGTPTXN[0:3]	Dedicated	Output	Negative differential transmit port.
MGTAVCC_G#(7)	Dedicated	Input	1.0V analog power-supply pin for the receiver and transmitter internal circuits.
MGTAVTT_G#(7)	Dedicated	Input	1.2V analog power-supply pin for the transmit driver.
MGTVCCAUX_G#(7)	Dedicated	Input	1.8V auxiliary analog Quad PLL (QPLL) voltage supply for the GTXE2 transceivers only.
MGTREFCLK0/1P	Dedicated	Input	Positive differential reference clock for the transceivers.
MGTREFCLK0/1N	Dedicated	Input	Negative differential reference clock for the transceivers.
MGTAVTTRCAL	Dedicated	N/A	Precision reference resistor pin for internal calibration termination. Not used for the XC7Z010, XC7Z015, or XC7Z020 devices.
MGTRREF	Dedicated	Input	Precision reference resistor pin for internal calibration termination.
Other Pins			
MRCC	Multi-function	Input	These are the clock capable I/Os driving BUFRs, BUFIOs, BUFGs, and MMCMs/PLLs. In addition, these pins can drive the BUFMR for multi-region BUFIO and BUFR support. These pins become regular user I/Os when not needed as a clock. When connecting a single-ended clock to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. The MRCC (multi-region) pins, when used as single-region resource, can drive four BUFIOs and four BUFRs in a single bank.
SRCC	Multi-function	Input	These are the clock capable I/Os driving BUFRs, BUFIOs, BUFGs, and MMCMs/PLLs. These pins become regular user I/Os when not needed for clocks. When connecting a single-ended clock to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. The SRCC (single-region) pins can drive four BUFIOs and four BUFRs in a single bank.

Table 1-5: **Zynq-7000 AP SoC Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
VRN[8]	Multi-function	N/A	This pin is for the DCI voltage reference resistor of N transistor (per bank, to be pulled High with reference resistor).
VRP[8]	Multi-function	N/A	This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with reference resistor).
DXP_0, DXN_0[9]	Dedicated	Input	Temperature-sensing diode pins (Anode: DXP; Cathode: DXN). The thermal diode is accessed by using the DXP and DXN pins in bank 0. When not used, tie to GND. To use the thermal diode an appropriate external thermal monitoring IC must be added. The recommended temperature monitoring solution for Zynq-7000 AP SoC devices uses the temperature sensor in the XADC block.
T0, T1, T2, or T3	Multi-function	Input	This pin belongs to the memory byte group 0-3.
T0_DQS, T1_DQS, T2_DQS, or T3_DQS	Multi-function	Input	The DDR DQS strobe pin that belongs to the memory byte group T0–T3.

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CCO_0}.
2. See the *V_{CCPLL}—PS PLL Supply* section in the *Processing System Power and Signaling* chapter in UG933, *Zynq-7000 All Programmable SoC PCB Design Guide*.
3. For devices that do not include $V_{CCAUX_IO_G\#}$ pins, auxiliary I/O circuits are powered by V_{CCAUX} pins.
4. V_{CCO} pins in unbonded banks must be connected to the V_{CCO} for that bank for package migration. Do NOT connect unbonded V_{CCO} pins to different supplies. Without a package migration requirement, V_{CCO} pins in unbonded banks can be tied to a common supply (V_{CCO} or ground).
5. Refer to the data sheet for V_{CCBATT_0} specifications.
6. See UG480, *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* for the default connections required to support on-chip monitoring.
7. In packages with only one MGT power group, the MGTAVCC_G#, MGTAVTT_G#, and MGTVCCAUX_G# pins are labeled without the _G#. These pins also appear without a number in the power and GND placement diagrams in Chapter 3, Device Diagrams.
8. The DCI guidelines in the Zynq-7000 AP SoC devices are different from previous Virtex device DCI guidelines. See the DCI sections in UG471: *7 Series FPGAs SelectIO Resources User Guide* for more information on the VRN/VRP pins.
9. The DXN_0 pin is not accessible in the XC7Z010/XA7Z010 devices in the CL225/CLG225 package. For designs connecting the thermal diode in this package to a thermal monitoring IC, use GNDADC_0 in place of DXN_0.