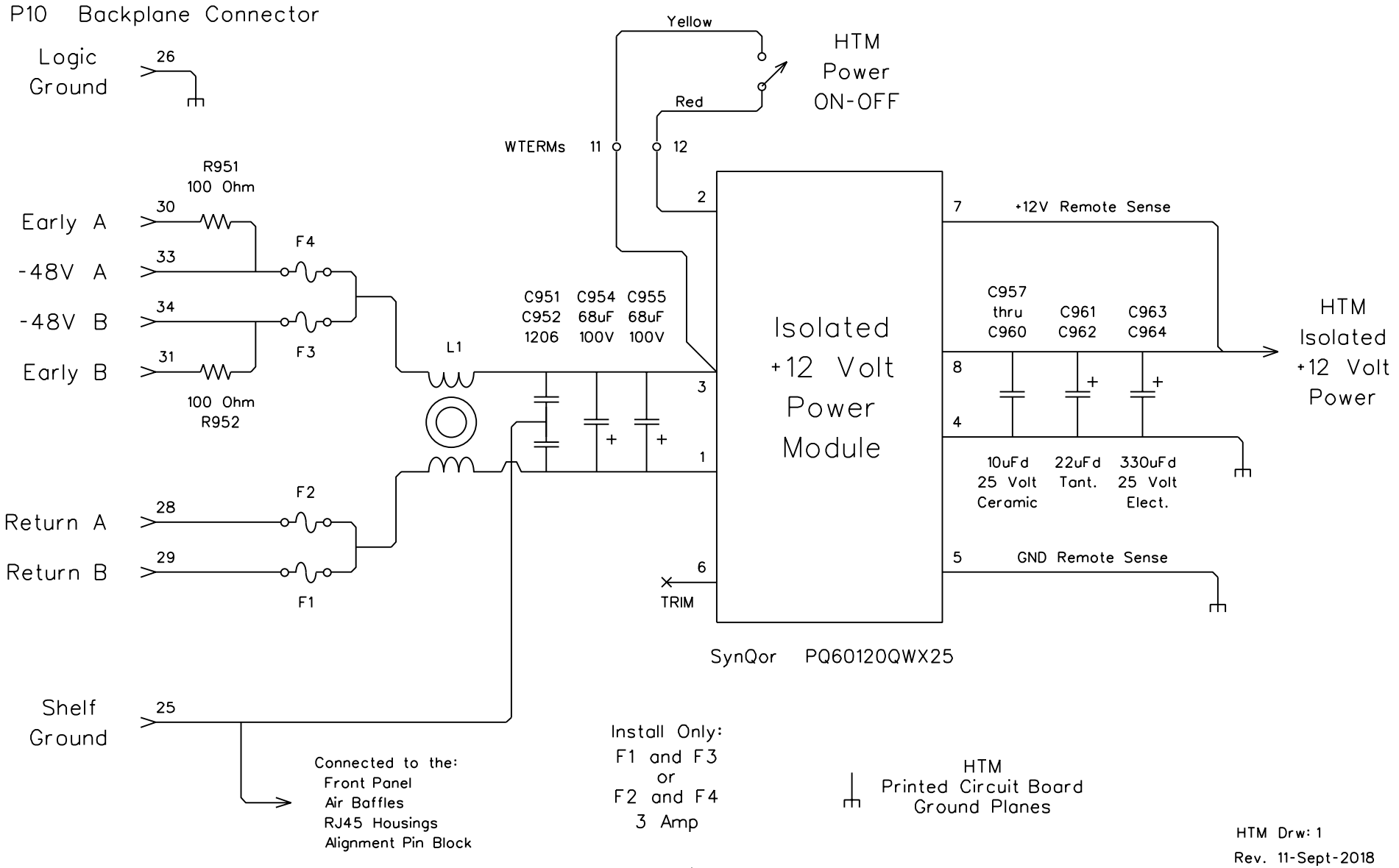
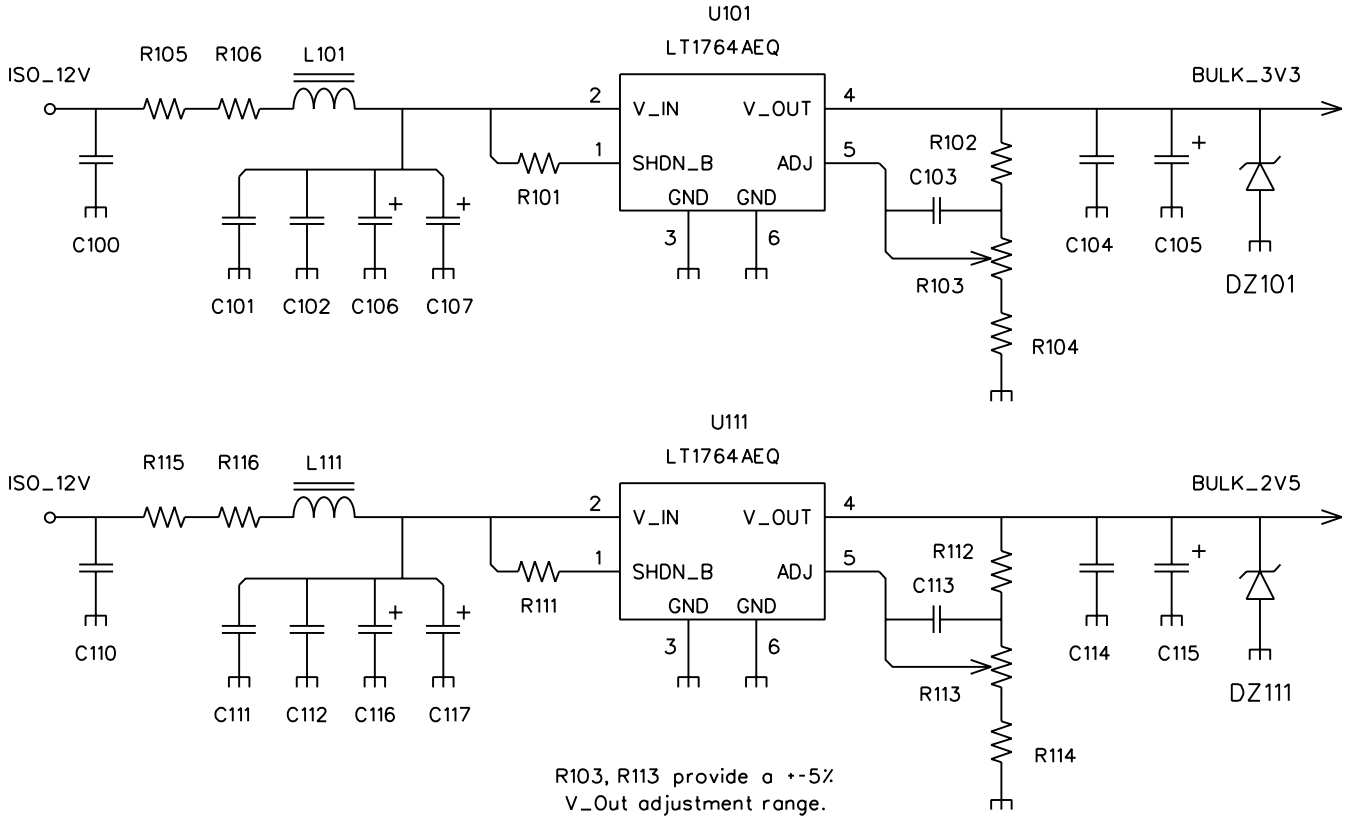
HTM Card Isolated 12 Volt Power



HTM Drw: 1

Rev. 11-Sept-2018

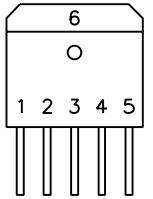
HTM Card Linear Regulators



R103, R113 provide a +-5% V_Out adjustment range.

LT1764AEQ*PBF
LT1764AEQ*TRPBF

Top View DD Package



1 Shut_Down_B
2 V_IN
3 Ground
4 V_OUT
5 Sense/Adjust
6 Ground

Internal reference 1.210 Volt
Expected Voltage Drop about 9 Volts

Expexted Loads

BULK_3V3
3.300 Volt

MiniPOD Trans + Rec
150 mA typ.
275 mA max.

Clock System
175 mA typ.

All Other 3V3 Loads
100 mA typ.

BULK_2V5
2.500 Volt

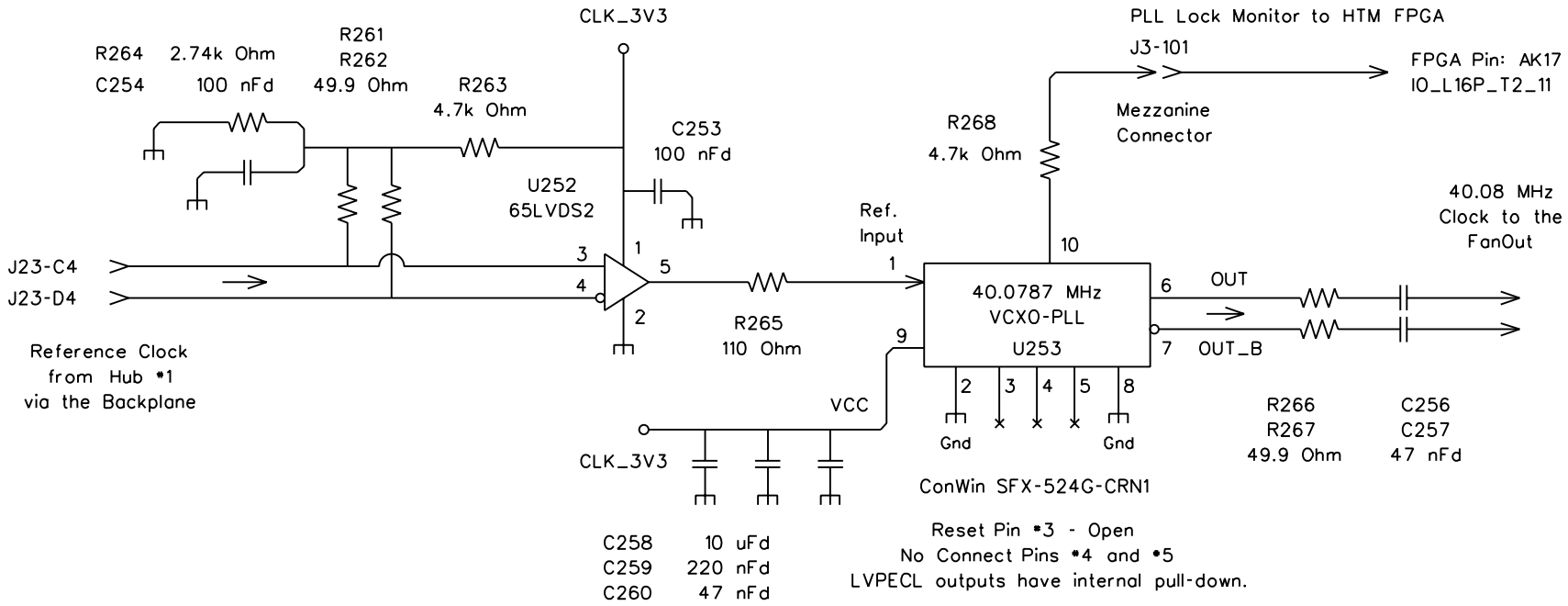
MiniPOD Trans + Rec
630 mA typ.
890 mA max.

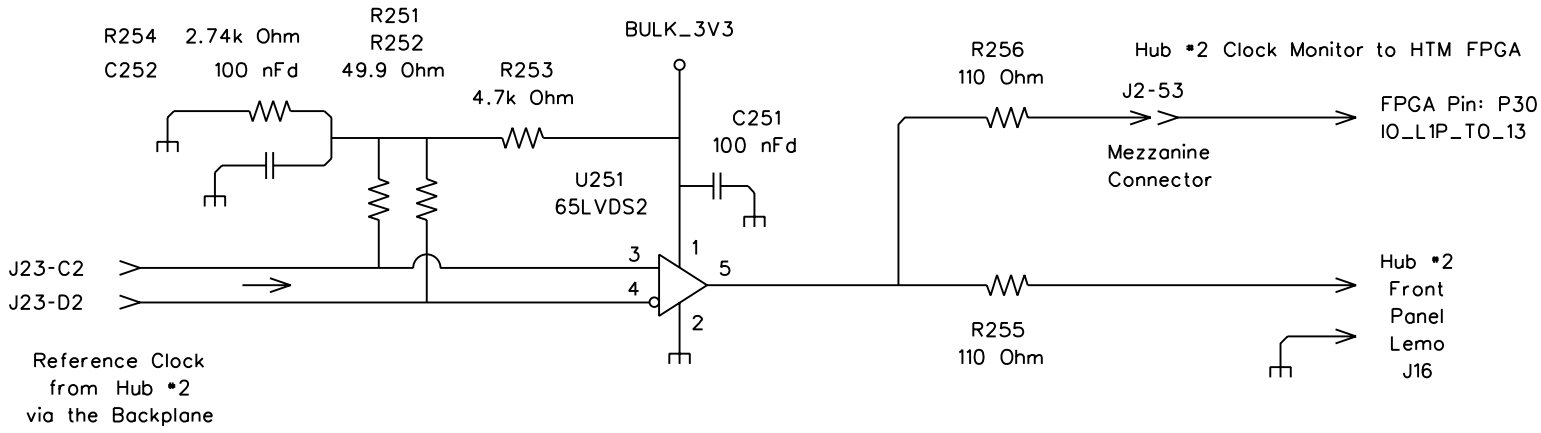
Clock System
60 mA max.

Component Values

C100, C110	Cap_220_nFd_0603	R101, R111	Res_Zero_Ohm_0603	L101	Wurth 744311470
C101, C111	Cap_220_nFd_0603	R102	Res_1780_Ohm_0603_TC	L111	4.7 uH, 6 Amp
C102, C112	Cap_10_uFd_25_V_1206	R112	Res_1070_Ohm_0603_TC		
C103, C113	Cap_220_nFd_0603	R103, R113	Res_100_Ohm_3_Turn_Var	DZ101	MMSZ4686T1G
C104, C114	Cap_10_uFd_25_V_1206	R104, R114	Res_1k_Ohm_0603_TC	DZ111	or
C105, C115	Cap_330_uFd_Tant_V				CMHZ5228B
C106, C116	Cap_22_uFd_Tant_V				
C107, C117	Cap_330_uFd_25V				

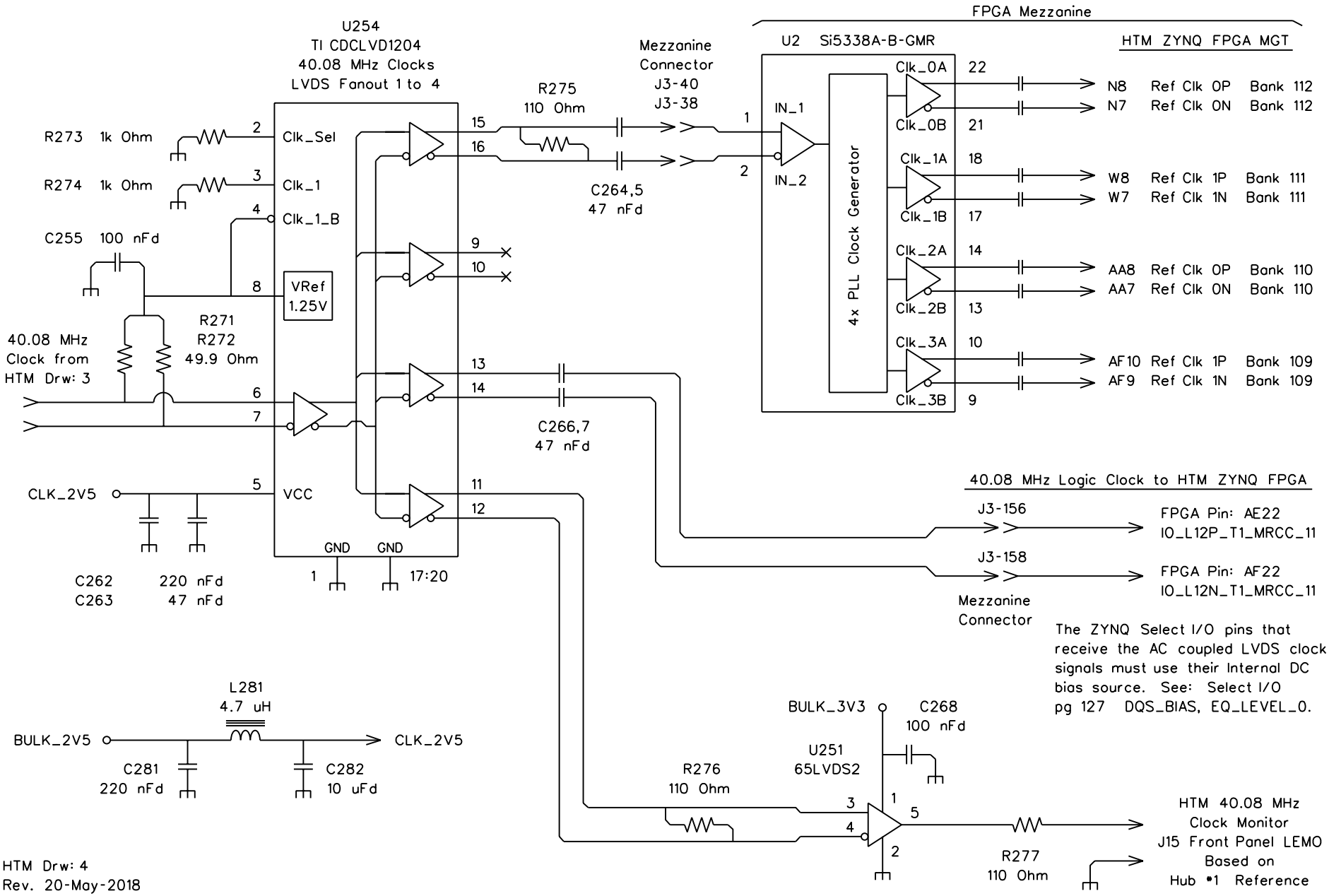
HTM Card - Clock Generation - Hub Input



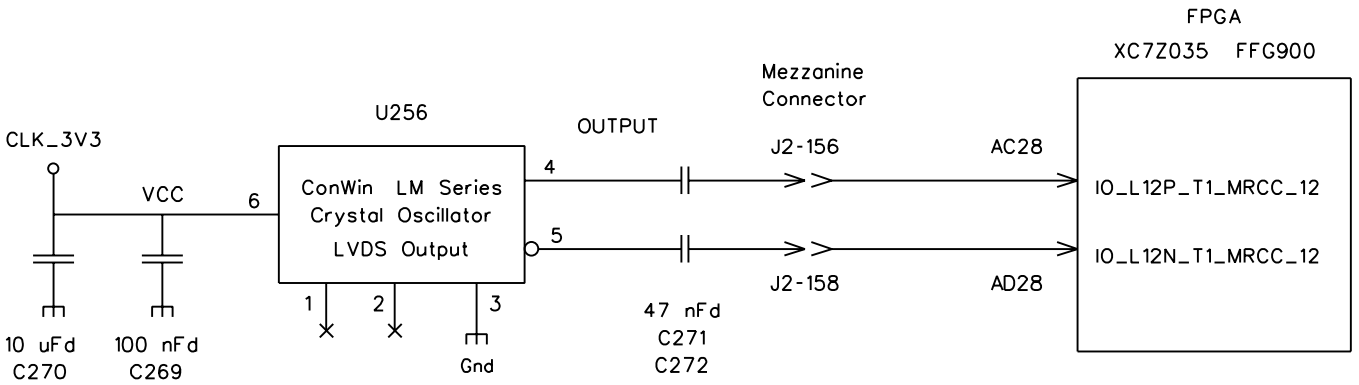


HTM Drw: 3
Rev. 17-May-2018

HTM Card - 40.08 MHz Clock Distribution

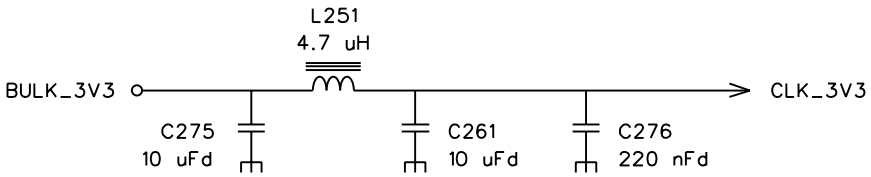


HTM Card - Spare Clock Oscillator



ConWin LM Series Oscillator
+- 25 ppm LVDS Output
Hi / Open Enable on pin #1
2 msec Startup

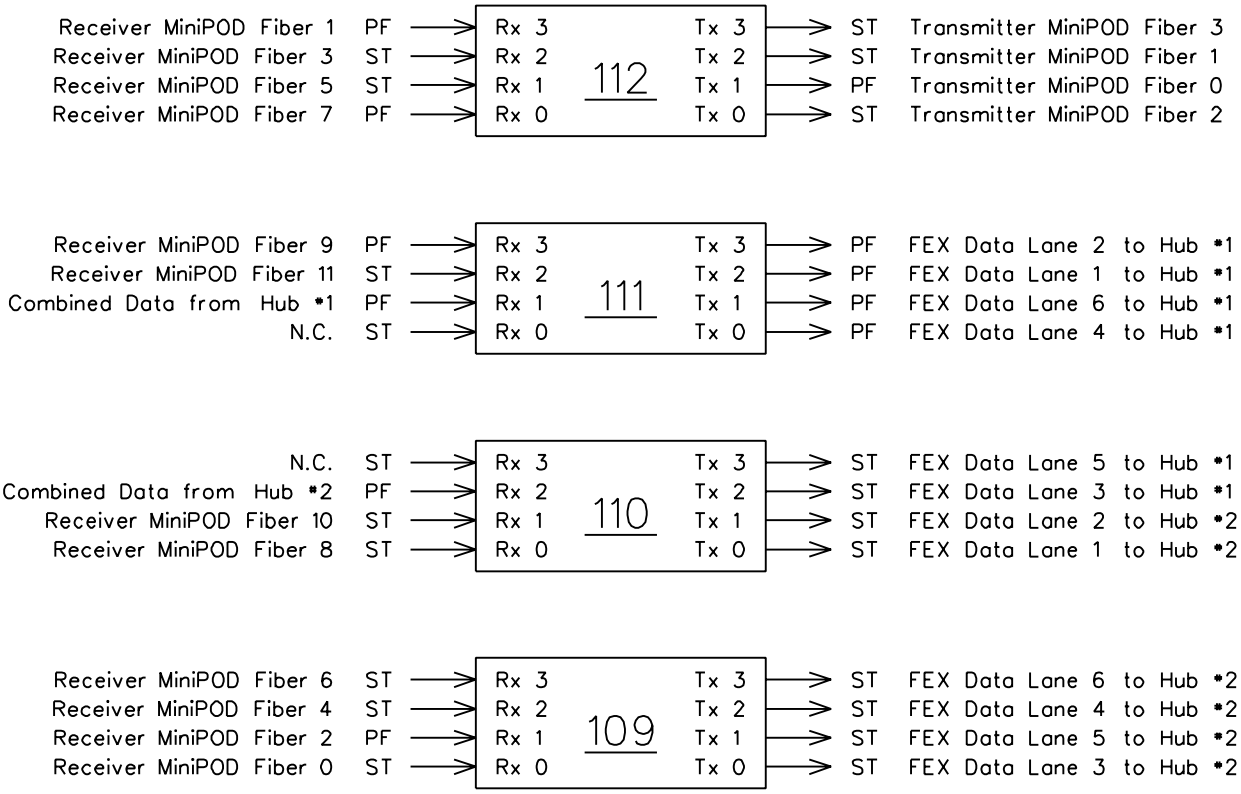
The ZYNQ Select I/O pins that receive the AC coupled LVDS Clock signals must use their Internal DC Bais source. See: Select I/O pg 127, DQS_BIAS, EQ_LEVEL_0.



HTM Drw: 5
Rev. 17-May-2018

HTM Card - GTX Transceivers - QUADs 109:112

MGT Quads



MGT Reference Clocks from the Si5338A

Si5338A Output	MGT Reference Clock Input
CLK_0	MGT Quad 112 Ref Clk 0
CLK_1	MGT Quad 111 Ref Clk 1
CLK_2	MGT Quad 110 Ref Clk 0
CLK_3	MGT Quad 109 Ref Clk 1

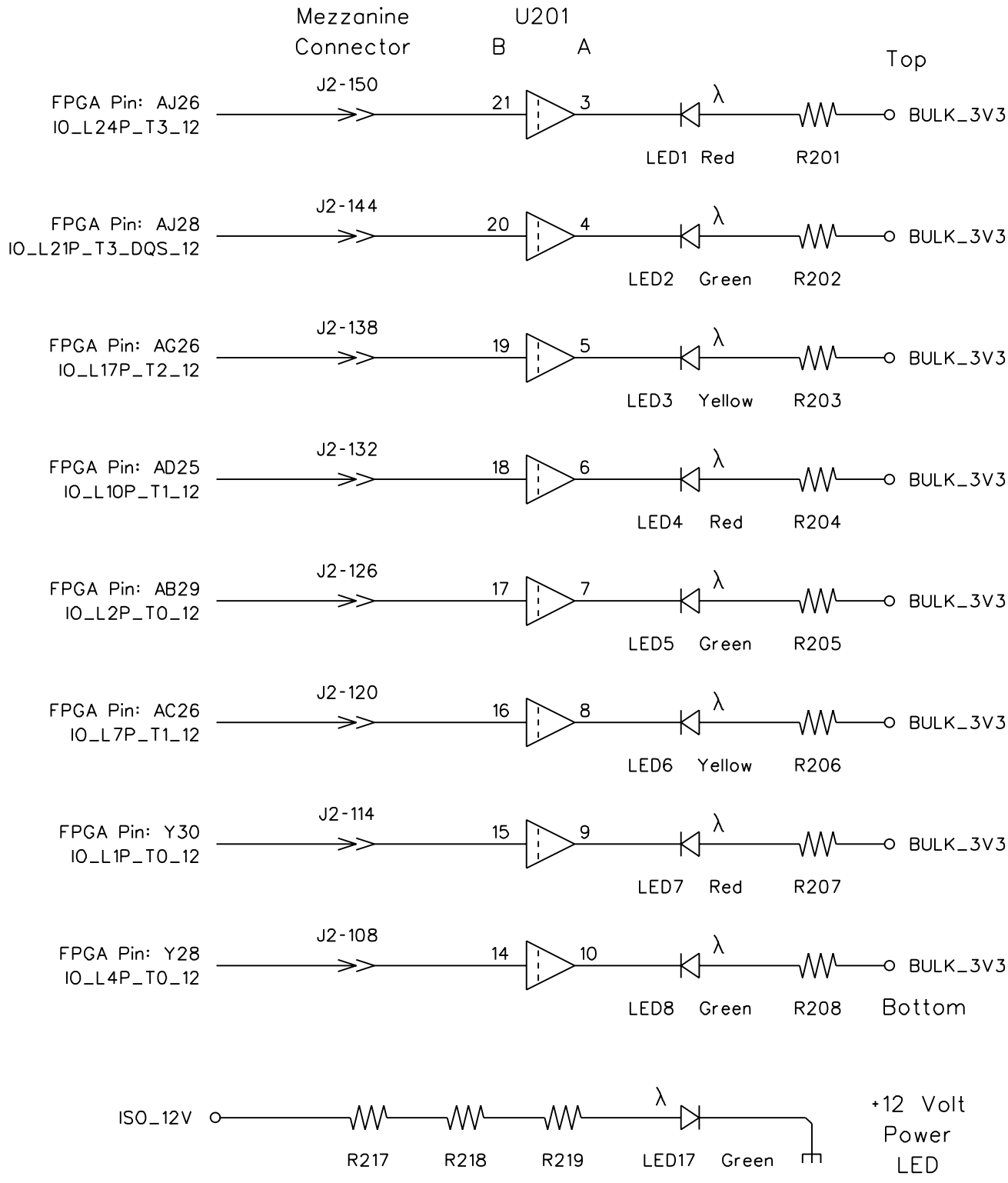
ST → Straight Through N.C. → No Connection

PF → Polarity Flip

HTM Drw: 6

Rev. 21-May-2018

HTM Card - Front Panel 9x LEDs



R201 : R208 240 Ohm

R217 : R219 1k Ohm

U201 74AVCH8T245

VCCA: 1 = 3V3

VCCB: 23, 24 = 3V3

DIR: 2 = GND --> B to A

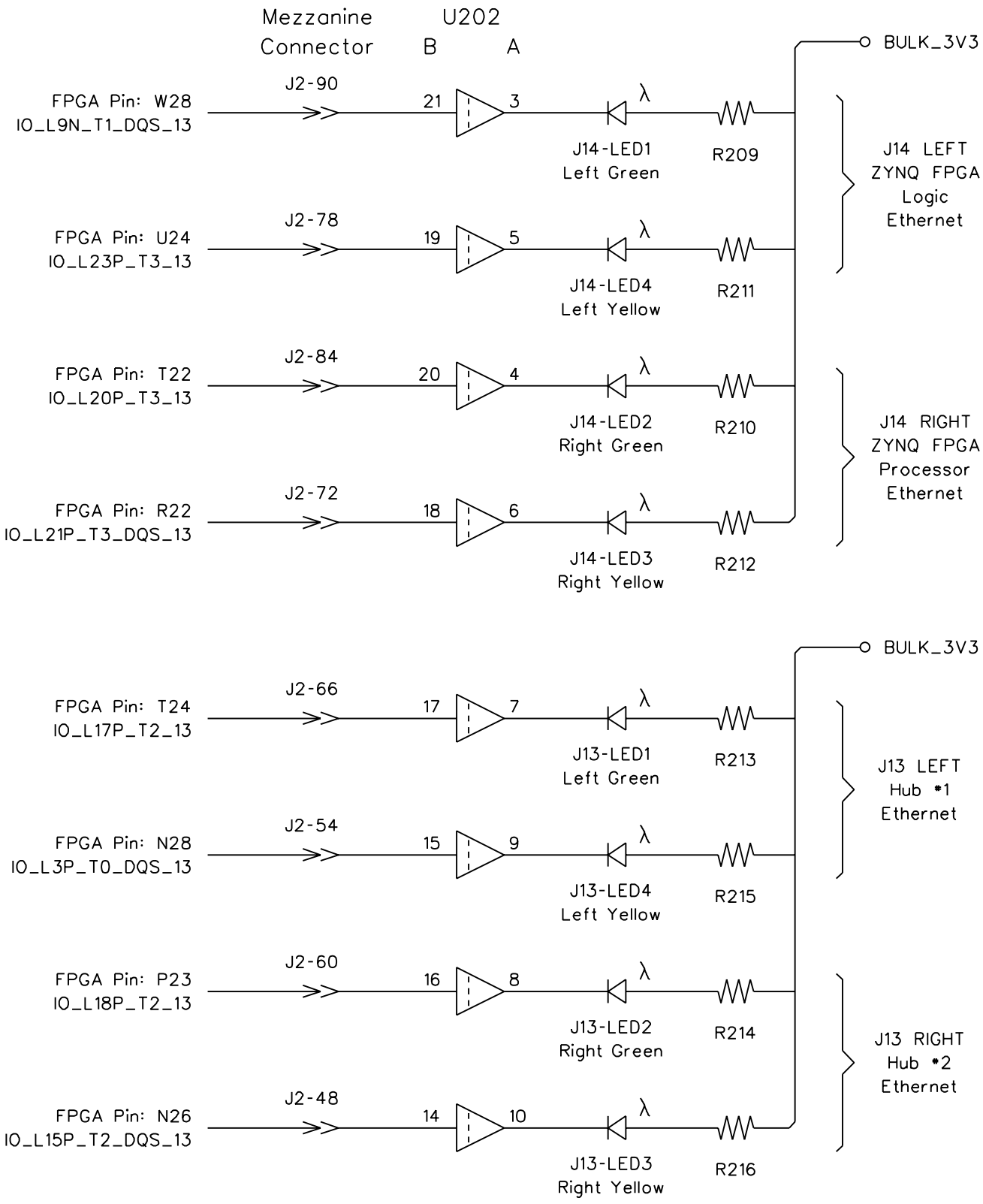
OE_B: 22 = GND --> Outputs Enabled

GNDs: 11, 12, 13 = GND

HTM Drw. 7

Rev. 22-May-2018

HTM Card - Front Panel RJ45 LEDs



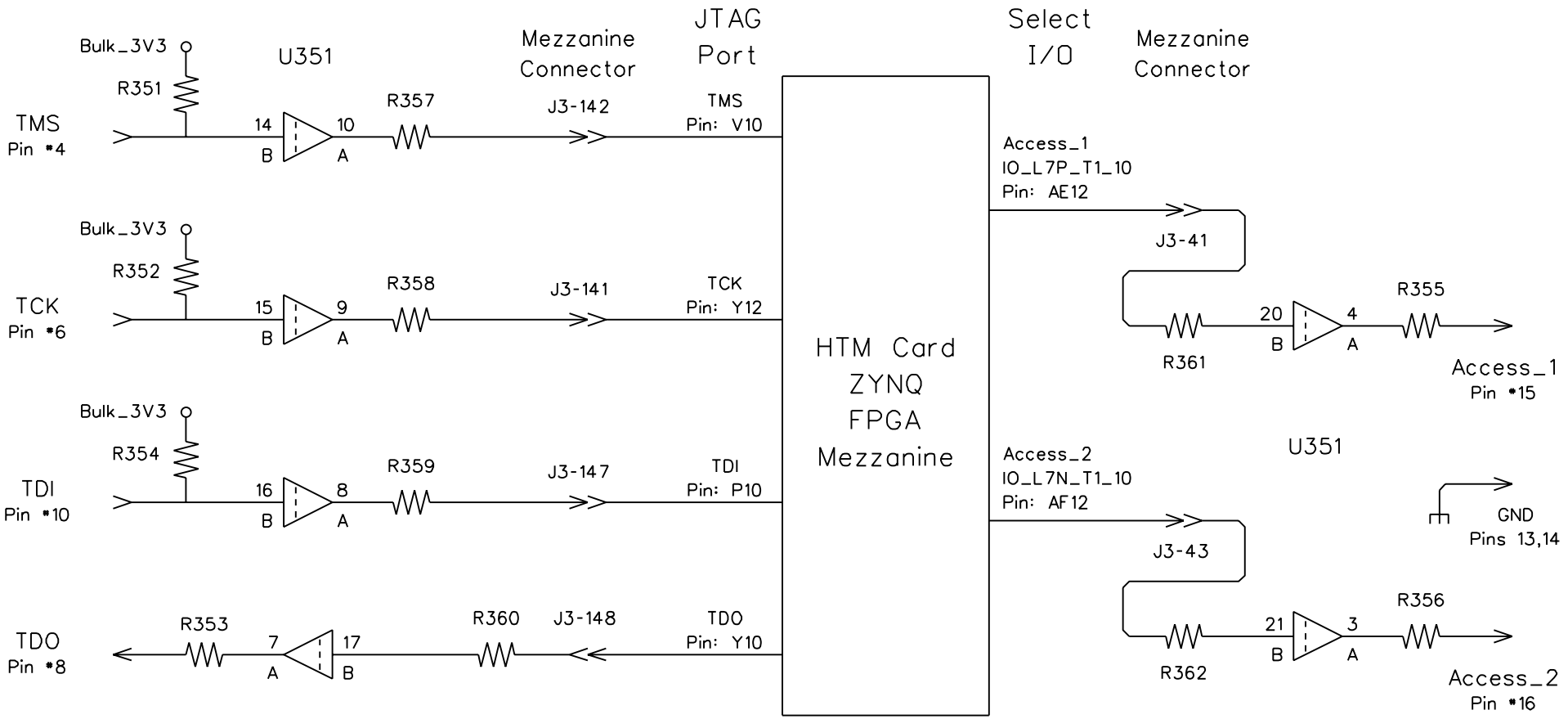
R209 : R216 240 Ohm

HTM Drw. 8
Rev. 22-May-2018

U202 74AVCH8T245
VCCA: 1 = 3V3
VCCB: 23, 24 = 3V3

DIR: 2 = GND --> B to A
OE_B: 22 = GND --> Outputs Enabled
GNDs: 11, 12, 13 = GND

HTM Card - JTAG & Access Signals Connector J12



JTAG Power Pin *2 — F5 — Bulk_3V3

GND Pins 1:9 Odd

Front Panel Connector J12

R351, R352, R354
4.7k Ohm
Pull-Up Resistors

R353, R357:R360
33 Ohm
Series Termination

J12 Connector
No Connect
Pins: 11, 12

ByPass Capacitors
C351 : C354
go with this page.

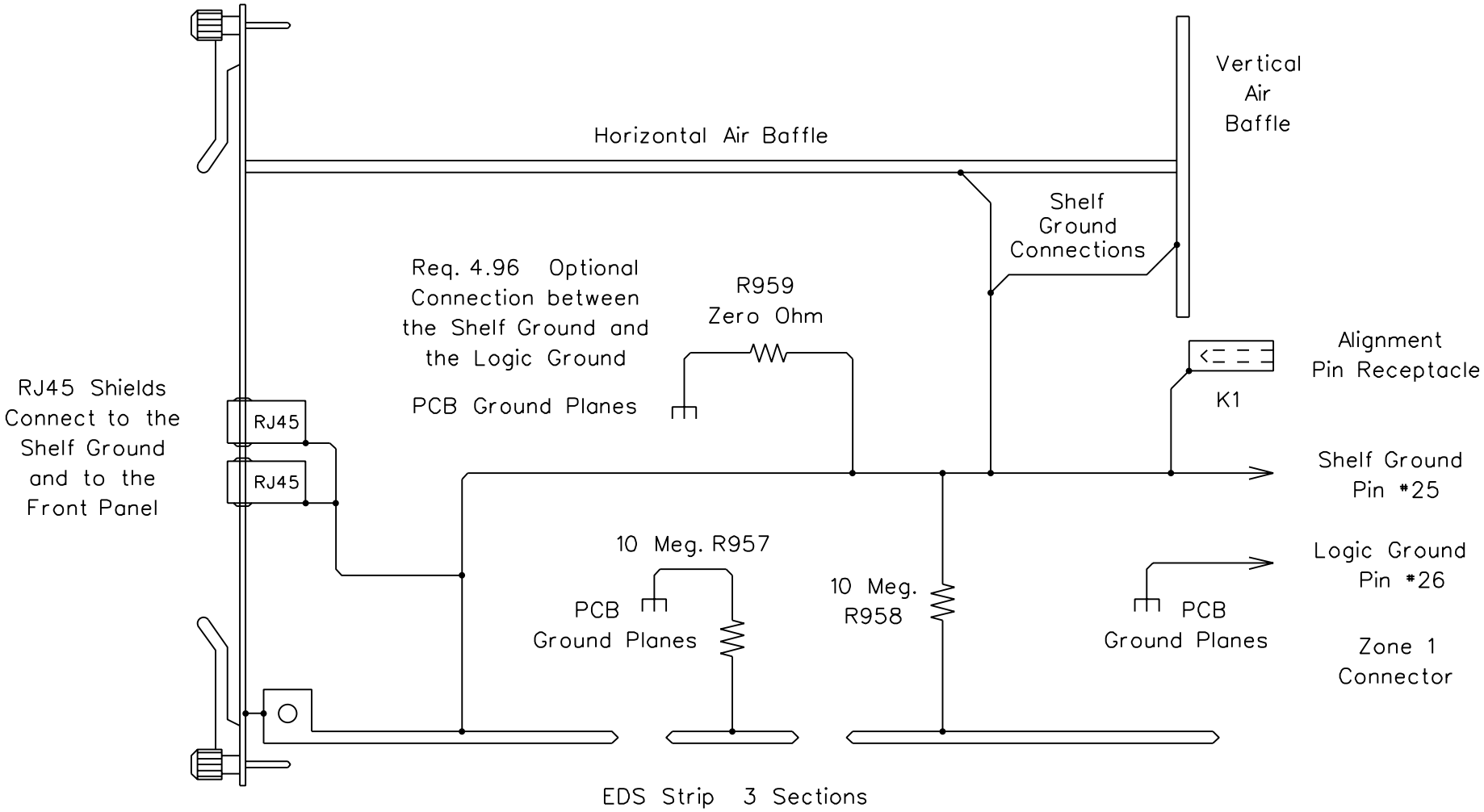
R355, R356
R361, R362
33 Ohm
Series Termination

U351
74AVCH8T245
DIR Low B->A

Spares:
19 → × × ← 5
18 → × × ← 6

HTM Drw. 9
Revision:
23-May-2018

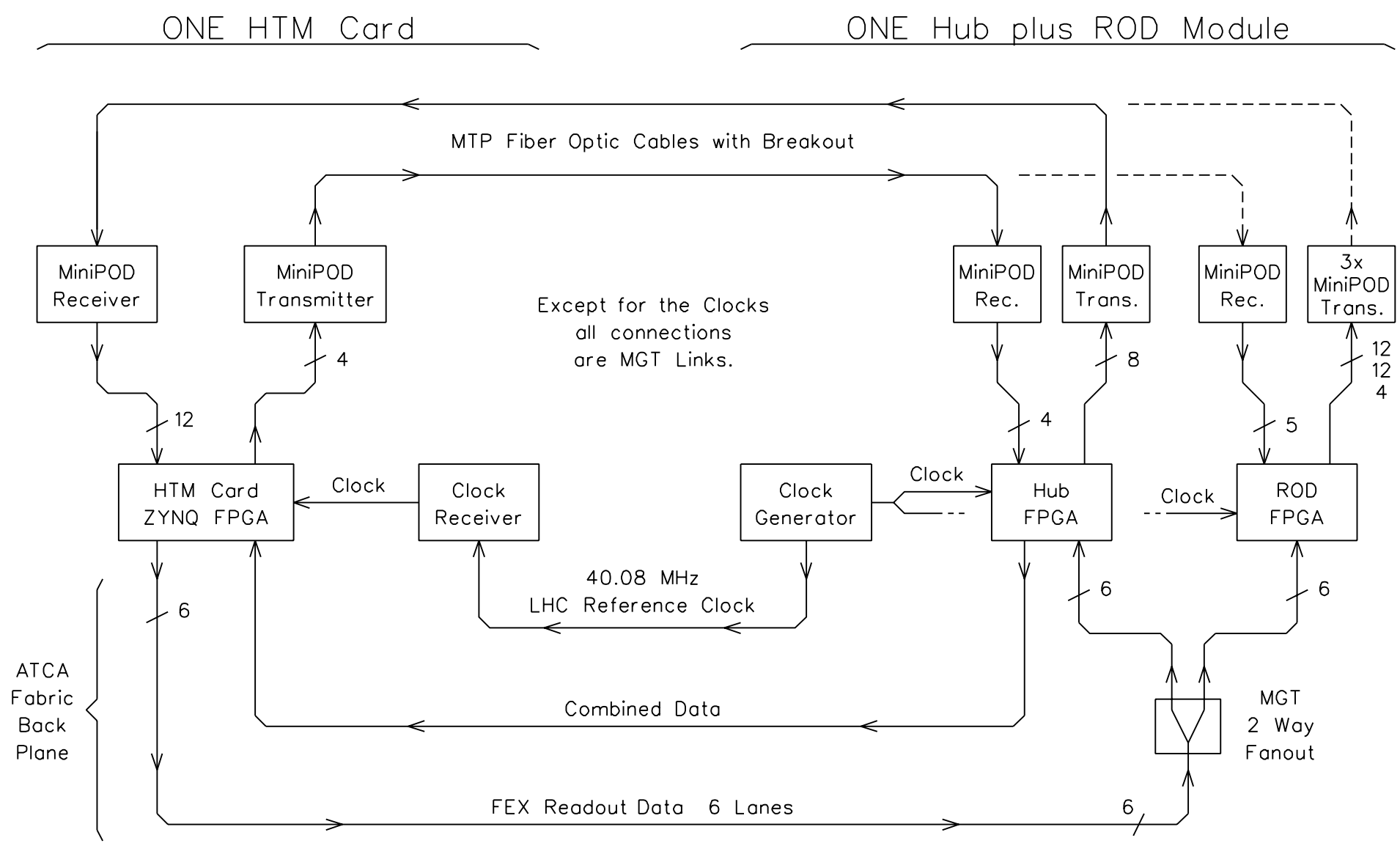
HTM Card - Logic & Shelf Ground Connections



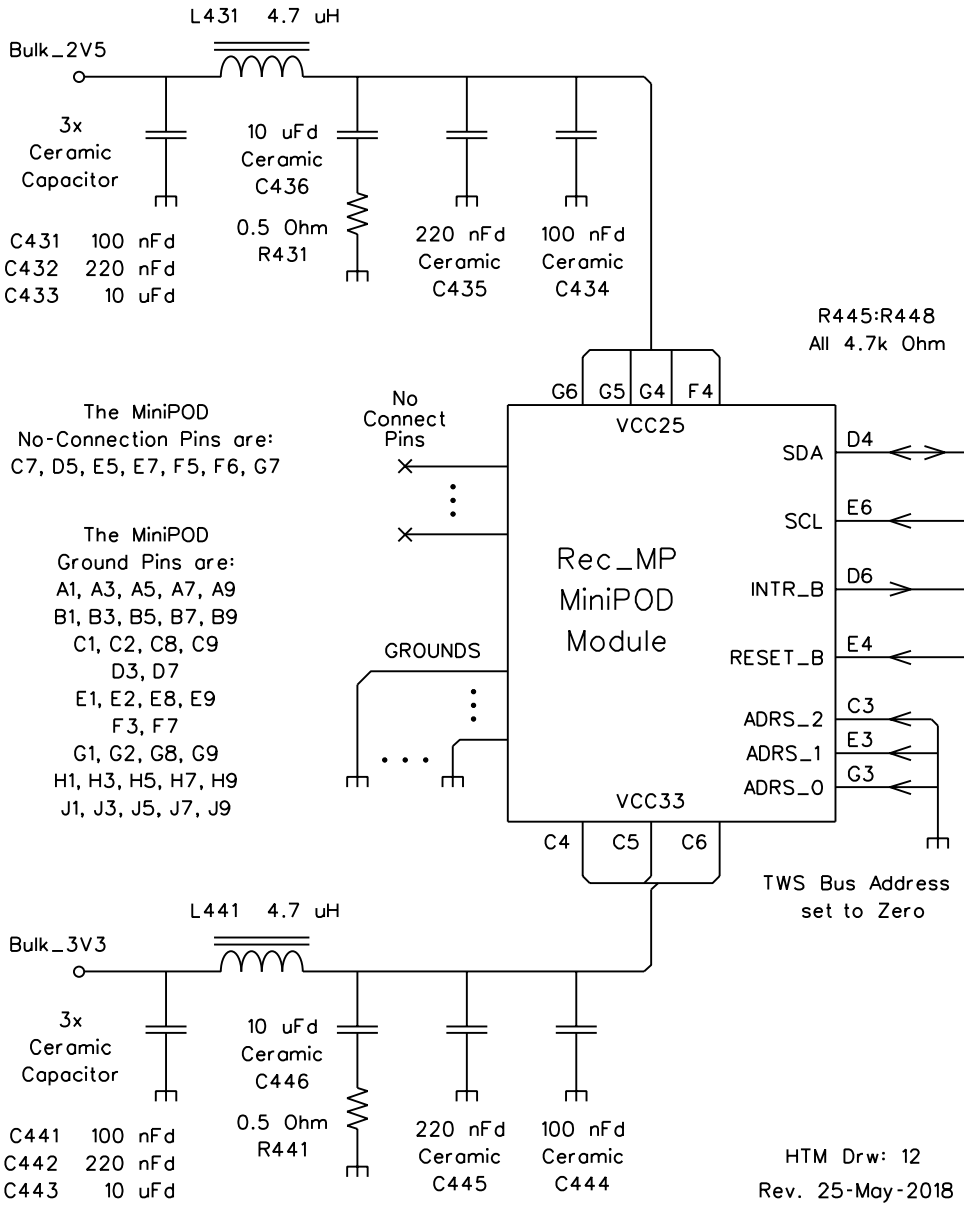
The Front Panel Connects to the
Front Section of the EDS Strip
and thus to the Shelf Ground

HTM Dwg: 10
Rev. 24-May-2018

ONE HTM Card Connection to ONE Hub Module



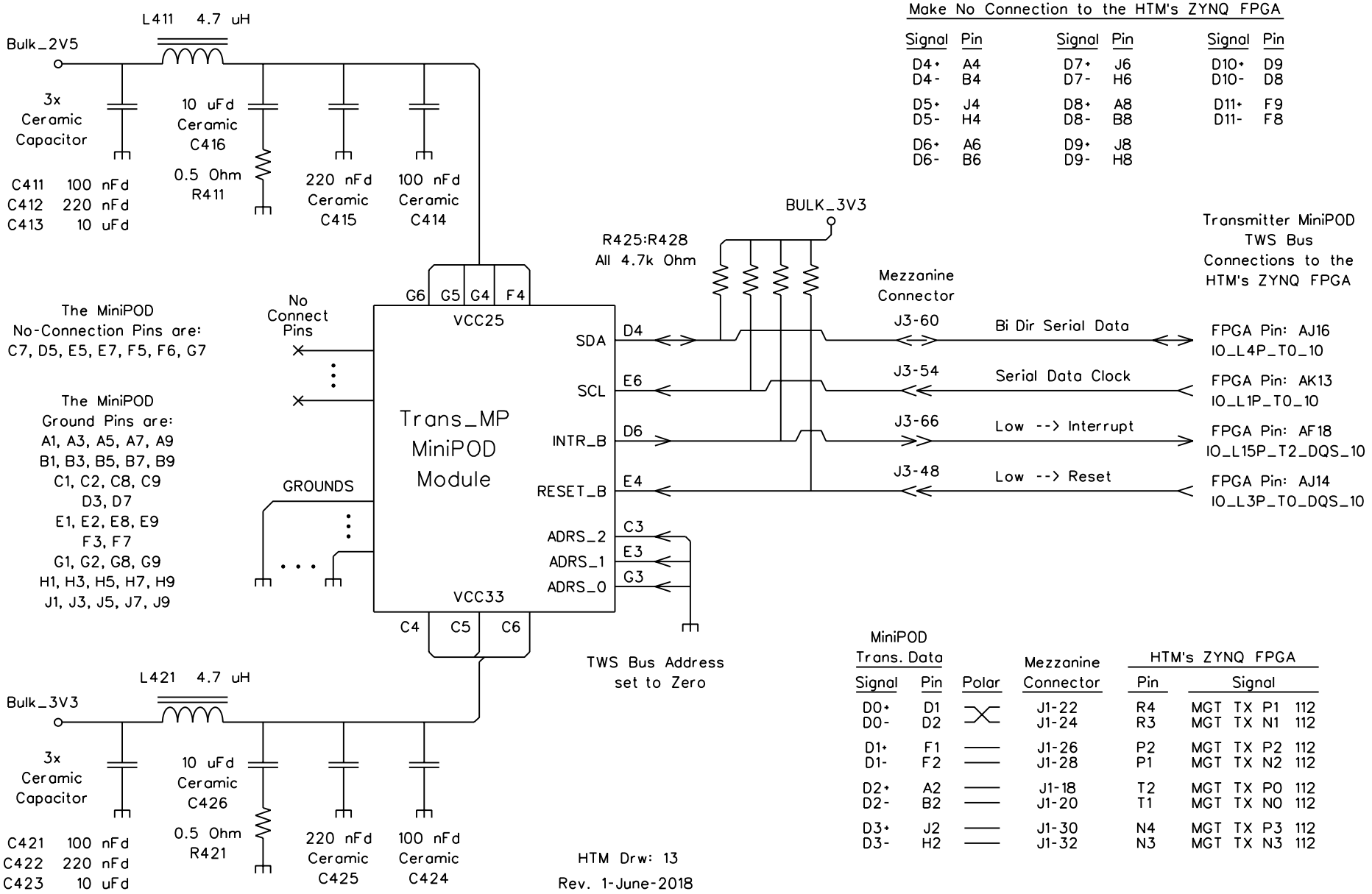
HTM Receiver MiniPOD



MiniPOD Rec. Data Signal	Pin	Coupling Capacitor	Polar	Mezzanine Connector	HTM's ZYNQ FPGA Pin	Signal
D0+	D1	C25	—	J3-32	AH10	MGT RX P0 109
D0-	D2	C26	—	J3-30	AH9	MGT RX N0 109
D1+	F1	C27	X	J1-29	P6	MGT RX P3 112
D1-	F2	C28	X	J1-31	P5	MGT RX N3 112
D2+	A2	C29	X	J3-28	AJ8	MGT RX P1 109
D2-	B2	C30	X	J3-26	AJ7	MGT RX N1 109
D3+	J2	C31	—	J1-25	T6	MGT RX P2 112
D3-	H2	C32	—	J1-27	T5	MGT RX N2 112
D4+	A4	C33	—	J3-24	AG8	MGT RX P2 109
D4-	B4	C34	—	J3-22	AG7	MGT RX N2 109

MiniPOD Rec. Data Signal	Pin	Coupling Capacitor	Polar	Mezzanine Connector	HTM's ZYNQ FPGA Pin	Signal
D5+	J4	C35	—	J1-21	U4	MGT RX P1 112
D5-	H4	C36	—	J1-23	U3	MGT RX N1 112
D6+	A6	C37	—	J3-20	AE8	MGT RX P3 109
D6-	B6	C38	—	J3-18	AE7	MGT RX N3 109
D7+	J6	C39	X	J1-17	V6	MGT RX P0 112
D7-	H6	C40	X	J1-19	V5	MGT RX N0 112
D8+	A8	C41	—	J3-16	AH6	MGT RX P0 110
D8-	B8	C42	—	J3-14	AH5	MGT RX N0 110
D9+	J8	C43	X	J1-13	AA4	MGT RX P3 111
D9-	H8	C44	X	J1-15	AA3	MGT RX N3 111
D10+	D9	C45	—	J3-12	AG4	MGT RX P1 110
D10-	D8	C46	—	J3-10	AG3	MGT RX N1 110
D11+	F9	C47	—	J1-9	Y6	MGT RX P2 111
D11-	F8	C48	—	J1-11	Y5	MGT RX N2 111

HTM Transmitter MiniPOD



The Following 8 Transmitter MiniPOD Fibers Make No Connection to the HTM's ZYNQ FPGA

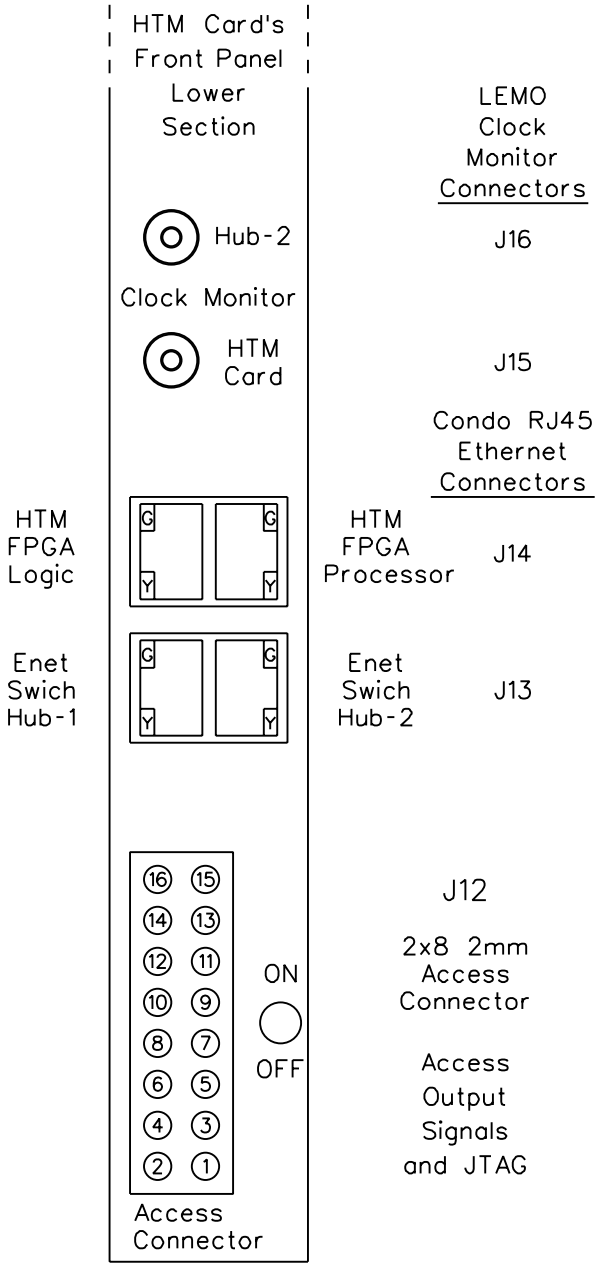
Signal	Pin	Signal	Pin	Signal	Pin
D4+	A4	D7+	J6	D10+	D9
D4-	B4	D7-	H6	D10-	D8
D5+	J4	D8+	A8	D11+	F9
D5-	H4	D8-	B8	D11-	F8
D6+	A6	D9+	J8		
D6-	B6	D9-	H8		

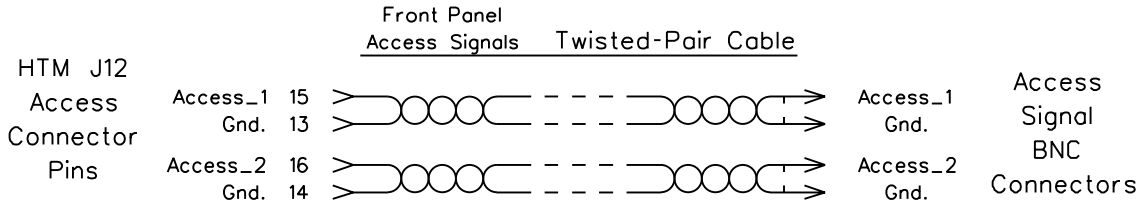
Transmitter MiniPOD TWS Bus Connections to the HTM's ZYNQ FPGA

Bi Dir Serial Data	FPGA Pin: AJ16 IO_L4P_T0_10
Serial Data Clock	FPGA Pin: AK13 IO_L1P_T0_10
Low --> Interrupt	FPGA Pin: AF18 IO_L15P_T2_DQS_10
Low --> Reset	FPGA Pin: AJ14 IO_L3P_T0_DQS_10

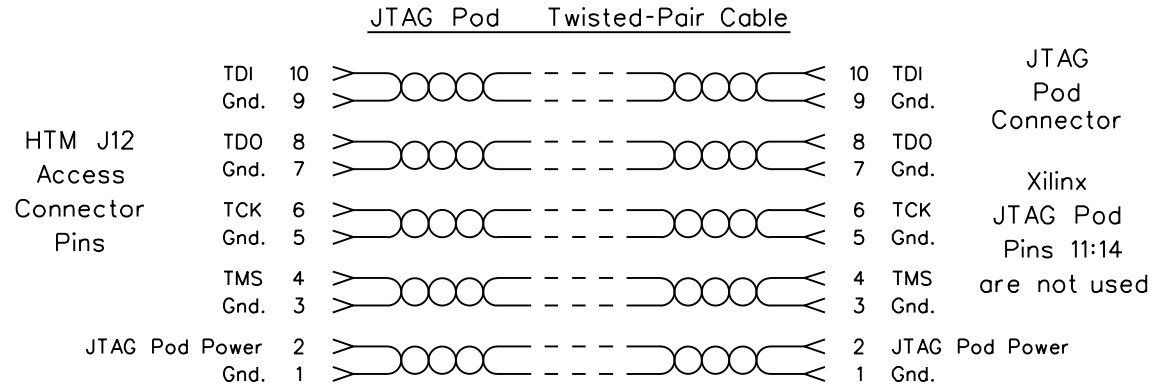
MiniPOD Trans. Data Signal	Pin	Polar	Mezzanine Connector	HTM's ZYNQ FPGA Pin	Signal
D0+	D1	X	J1-22	R4	MGT TX P1 112
D0-	D2	X	J1-24	R3	MGT TX N1 112
D1+	F1	—	J1-26	P2	MGT TX P2 112
D1-	F2	—	J1-28	P1	MGT TX N2 112
D2+	A2	—	J1-18	T2	MGT TX P0 112
D2-	B2	—	J1-20	T1	MGT TX N0 112
D3+	J2	—	J1-30	N4	MGT TX P3 112
D3-	H2	—	J1-32	N3	MGT TX N3 112

HTM Card Front Panel Connectors and Cables





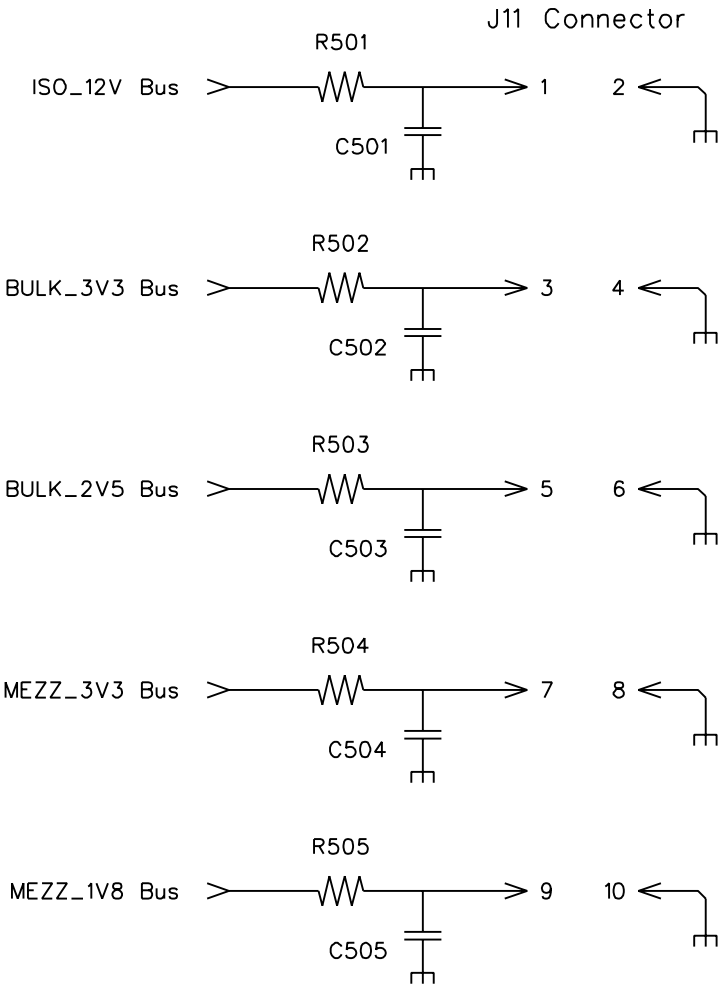
J12 Access Connector Pins 11 and 12 Have No Connecton.



HTM Drw: 14
Rev. 3-July-2018

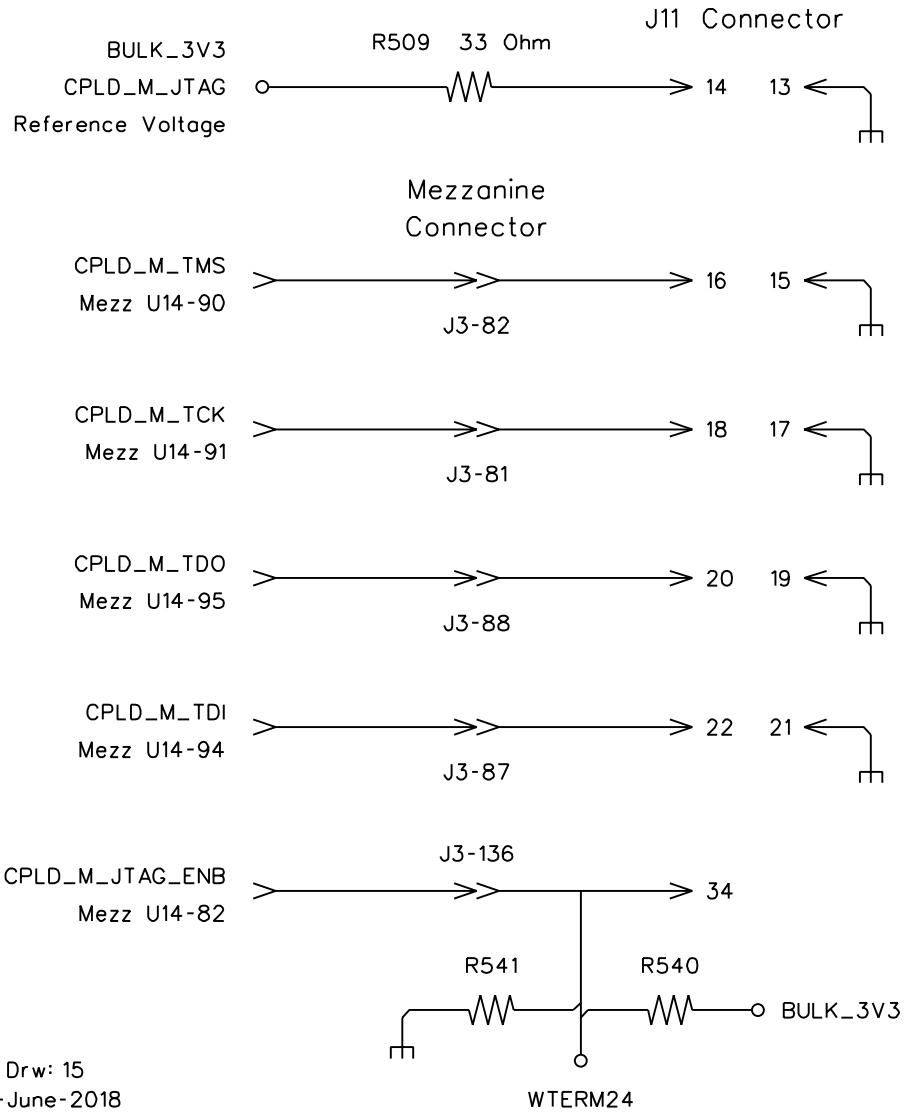
HTM Card J11: PS Monitor / Mezz CPLD JTAG

Power Supply Monitor Points



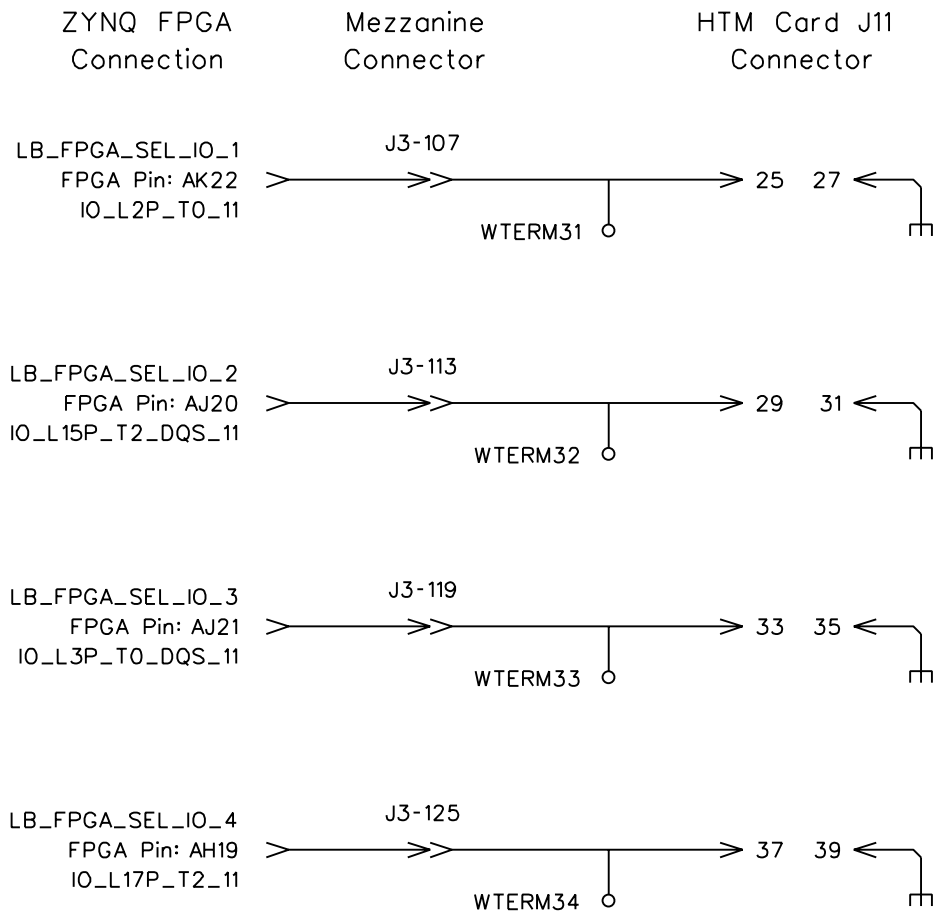
R501 : R505 110 Ohm J11-11, J11-12
C501 : C505 220 nFd No Connection

Mezzanine CPLD JTAG



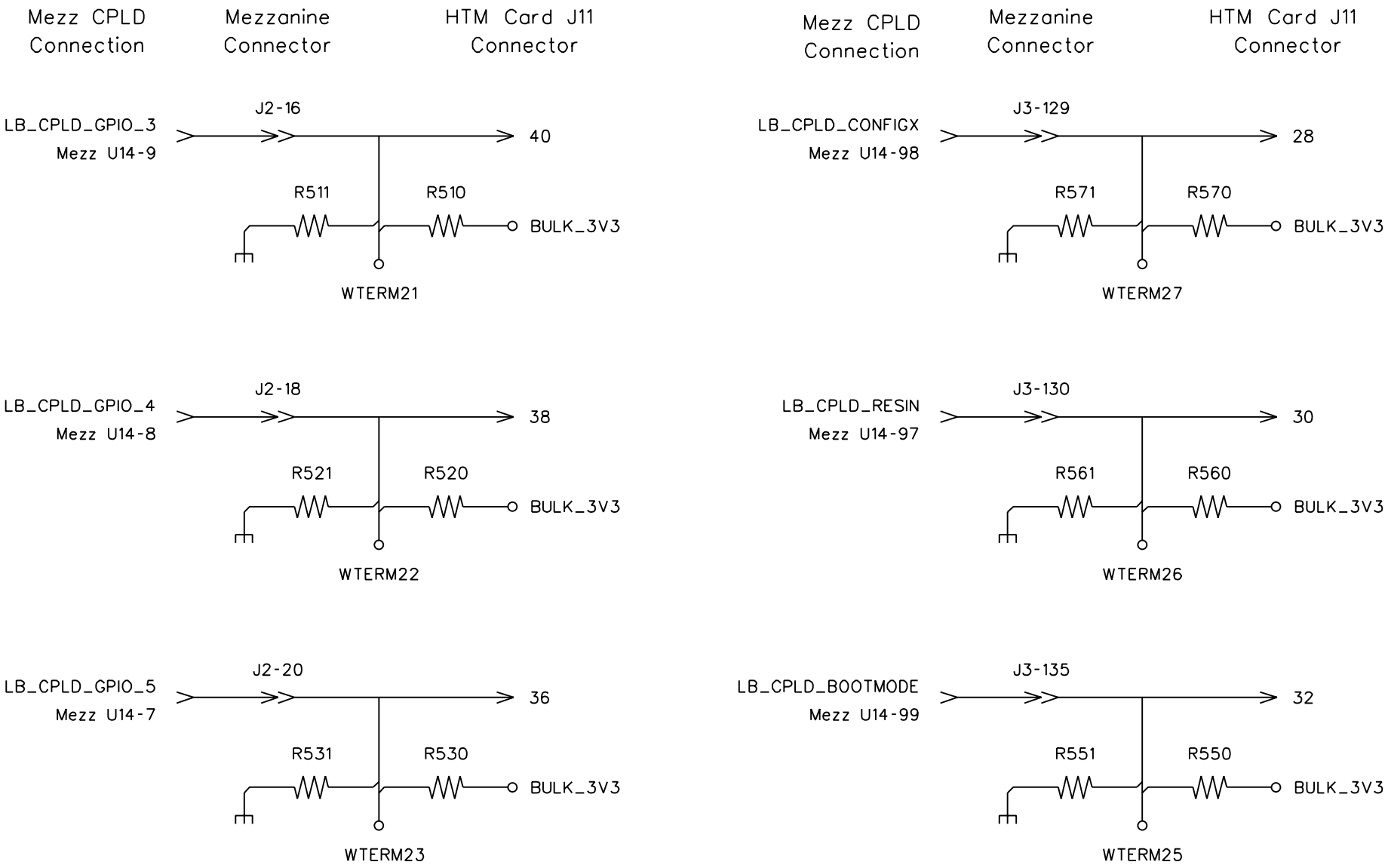
HTM Drw: 15
Rev. 5-June-2018

HTM Card J11: Life Boat FPGA Select I/O Connections



J11-23, J11-24 No Connection

HTM Card J11: Life Boat CPLD Connections

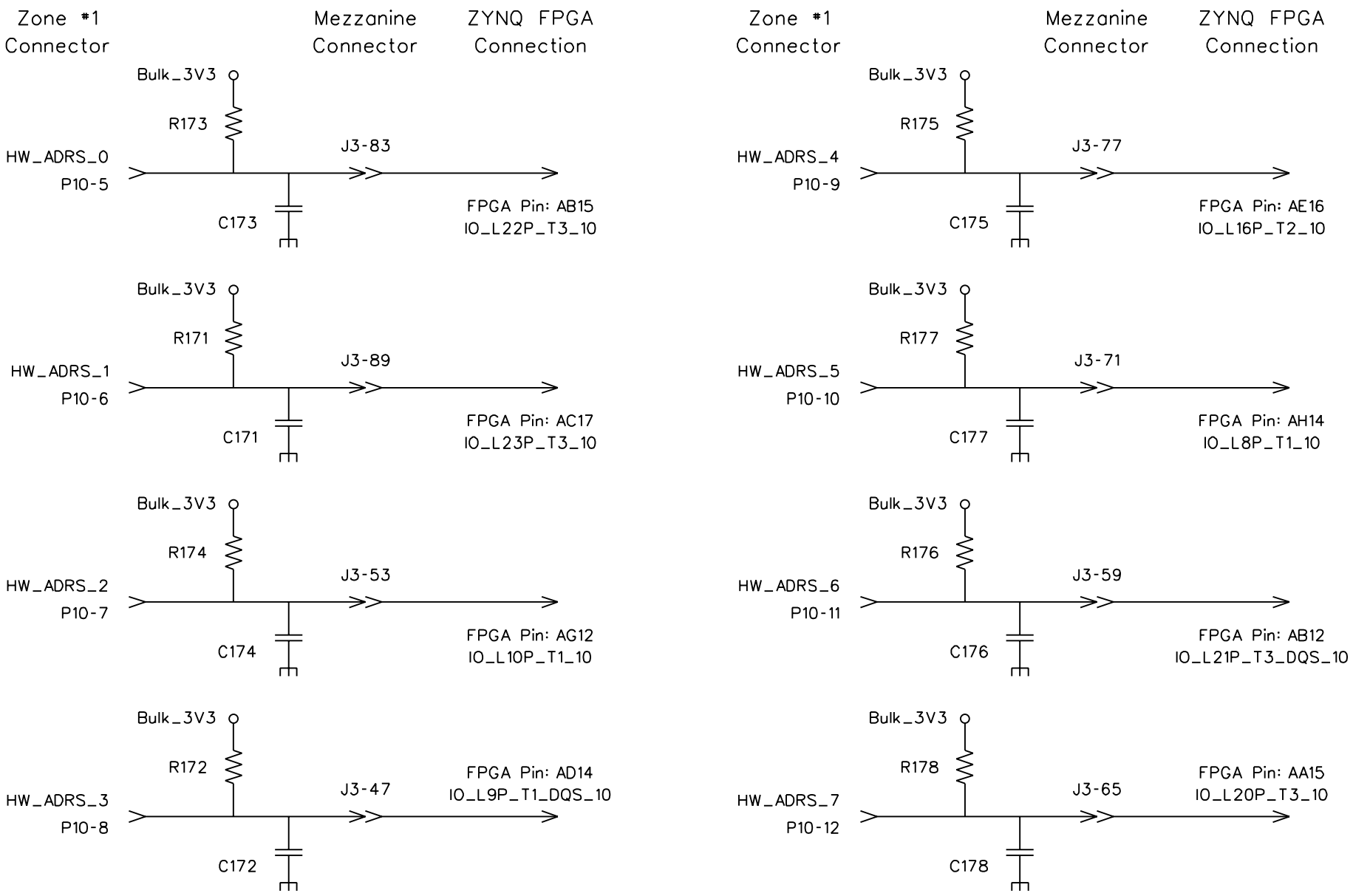


None of the Resistors shown on this page are installed during production assembly.

HTM Drw: 17

Rev. 7-June-2018

HTM Card Hardware Address to Mezz FPGA



Resistors 1k Ohm
Capacitors 100 nFd

The Hardware Address Consists of: 7 Address Bits: ADRS0:ADRS6 plus Odd Parity Bit ADRS7

HTM Drw: 18
Rev. 8-June-2018

HTM Card RJ45s for ATCA Backplane Ethernet

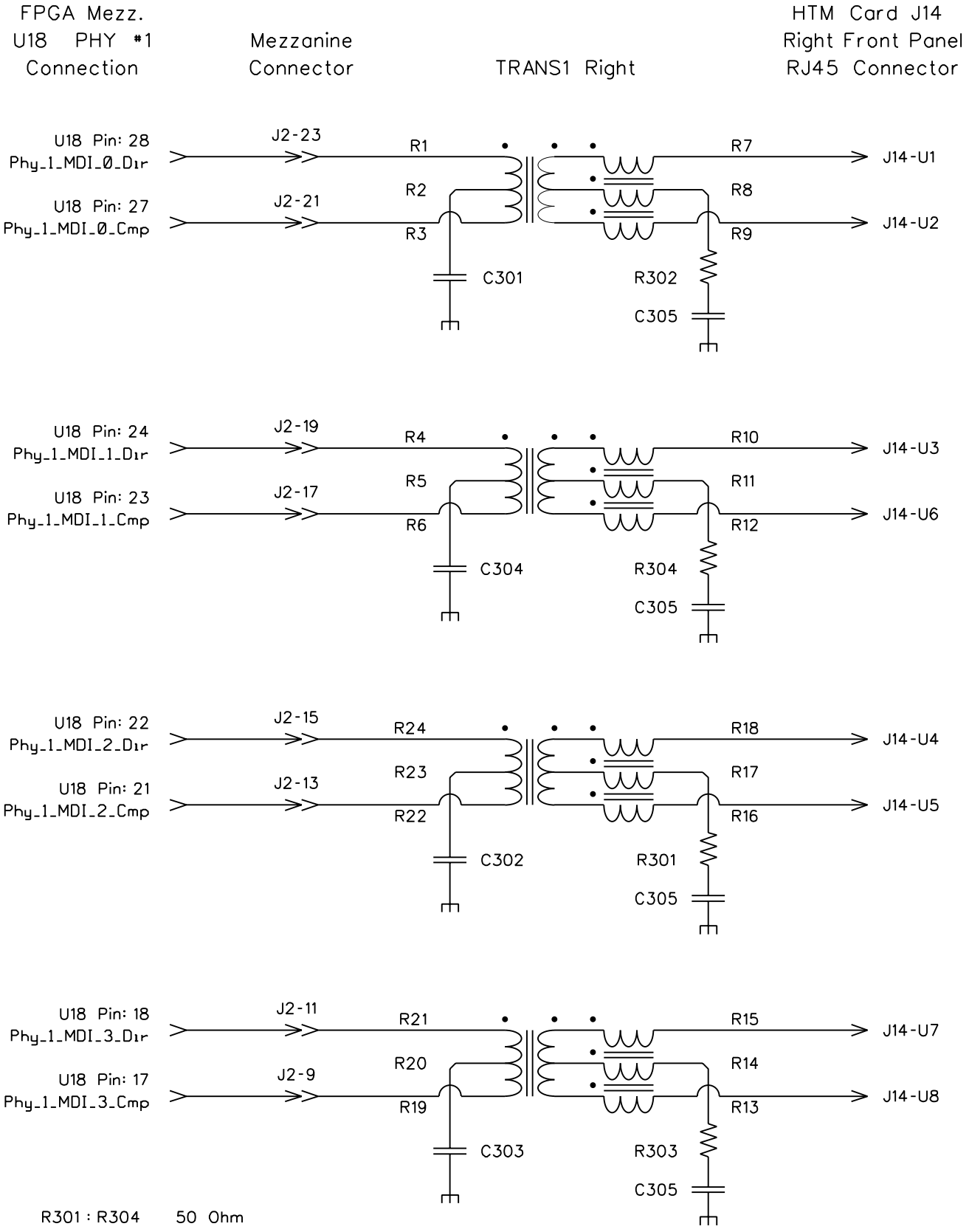
Hub #1 Backplane Ethernet

Backplane ATCA J23 Connector		HTM Card J13 Left Front Panel RJ45 Connector
J23-A5	Hub_1_Enet_D0_DIR	J13-L1
J23-B5	Hub_1_Enet_D0_CMP	J13-L2
J23-C5	Hub_1_Enet_D1_DIR	J13-L3
J23-D5	Hub_1_Enet_D1_CMP	J13-L6
J23-E5	Hub_1_Enet_D2_DIR	J13-L4
J23-F5	Hub_1_Enet_D2_CMP	J13-L5
J23-G5	Hub_1_Enet_D3_DIR	J13-L7
J23-H5	Hub_1_Enet_D3_CMP	J13-L8

Hub #2 Backplane Ethernet

Backplane ATCA J23 Connector		HTM Card J13 Right Front Panel RJ45 Connector
J23-A6	Hub_2_Enet_D0_DIR	J13-U1
J23-B6	Hub_2_Enet_D0_CMP	J13-U2
J23-C6	Hub_2_Enet_D1_DIR	J13-U3
J23-D6	Hub_2_Enet_D1_CMP	J13-U6
J23-E6	Hub_2_Enet_D2_DIR	J13-U4
J23-F6	Hub_2_Enet_D2_CMP	J13-U5
J23-G6	Hub_2_Enet_D3_DIR	J13-U7
J23-H6	Hub_2_Enet_D3_CMP	J13-U8

HTM Card FPGA Processor Ethernet

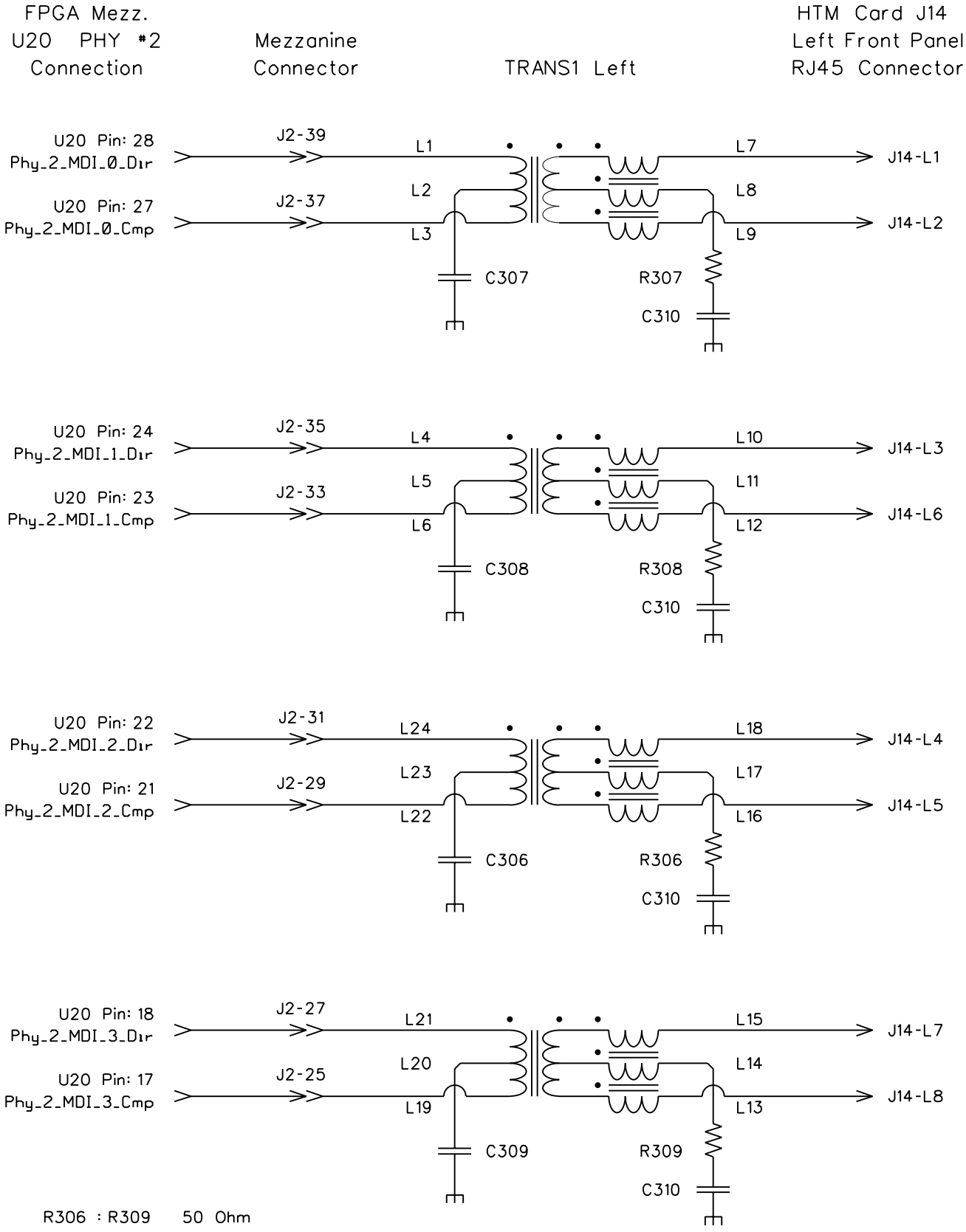


R301 : R304	50 Ohm
C301 : C304	100 nFd
C305	1 nFd

Magnetics
Pulse HX5201NL

HTM Drw: 20
Rev. 12-June-2018

HTM Card FPGA Logic Ethernet

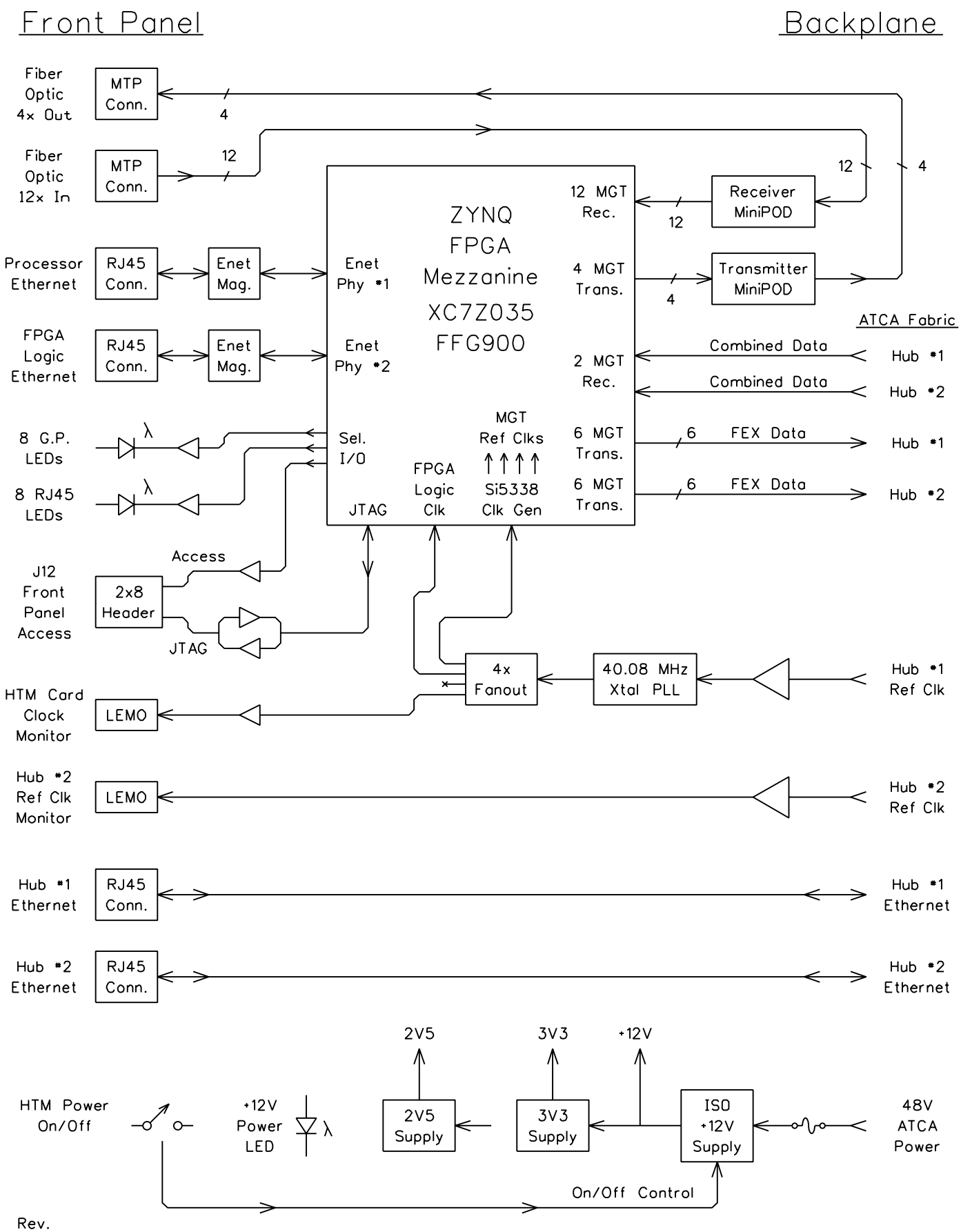


R306 : R309 50 Ohm
C306 : C309 100 nFd
C310 1 nFd

Magnetics
Pulse HX5201NL

HTM Drw: 21
Rev. 13-June-2018

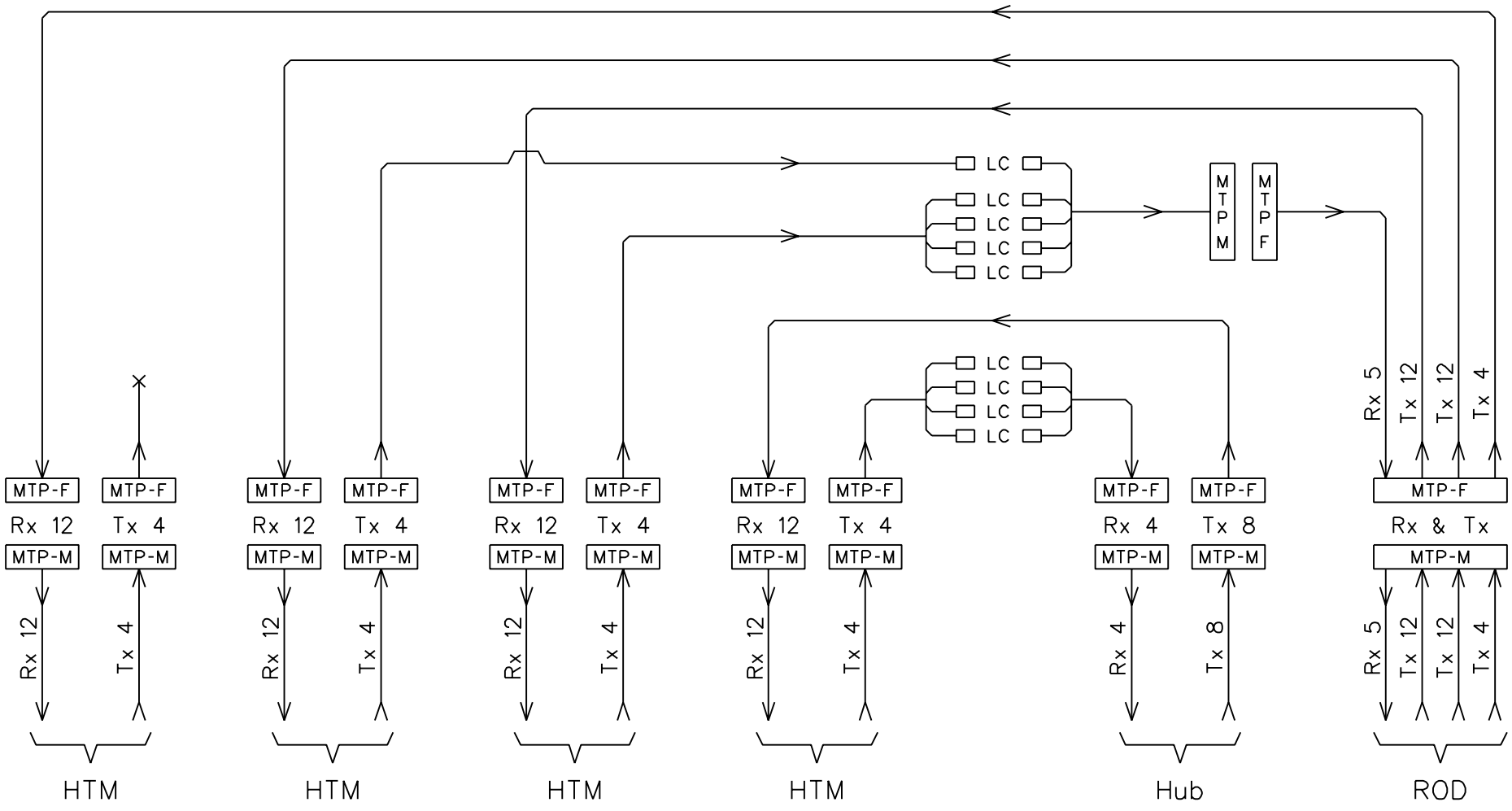
HTM Card Block Diagram



Rev.
24-June-2018

HTM Drw: 22

Fiber Optic: Four HTM Cards - ONE Hub/ROD



HTM Drw: 23

Rev. 11-July-2018