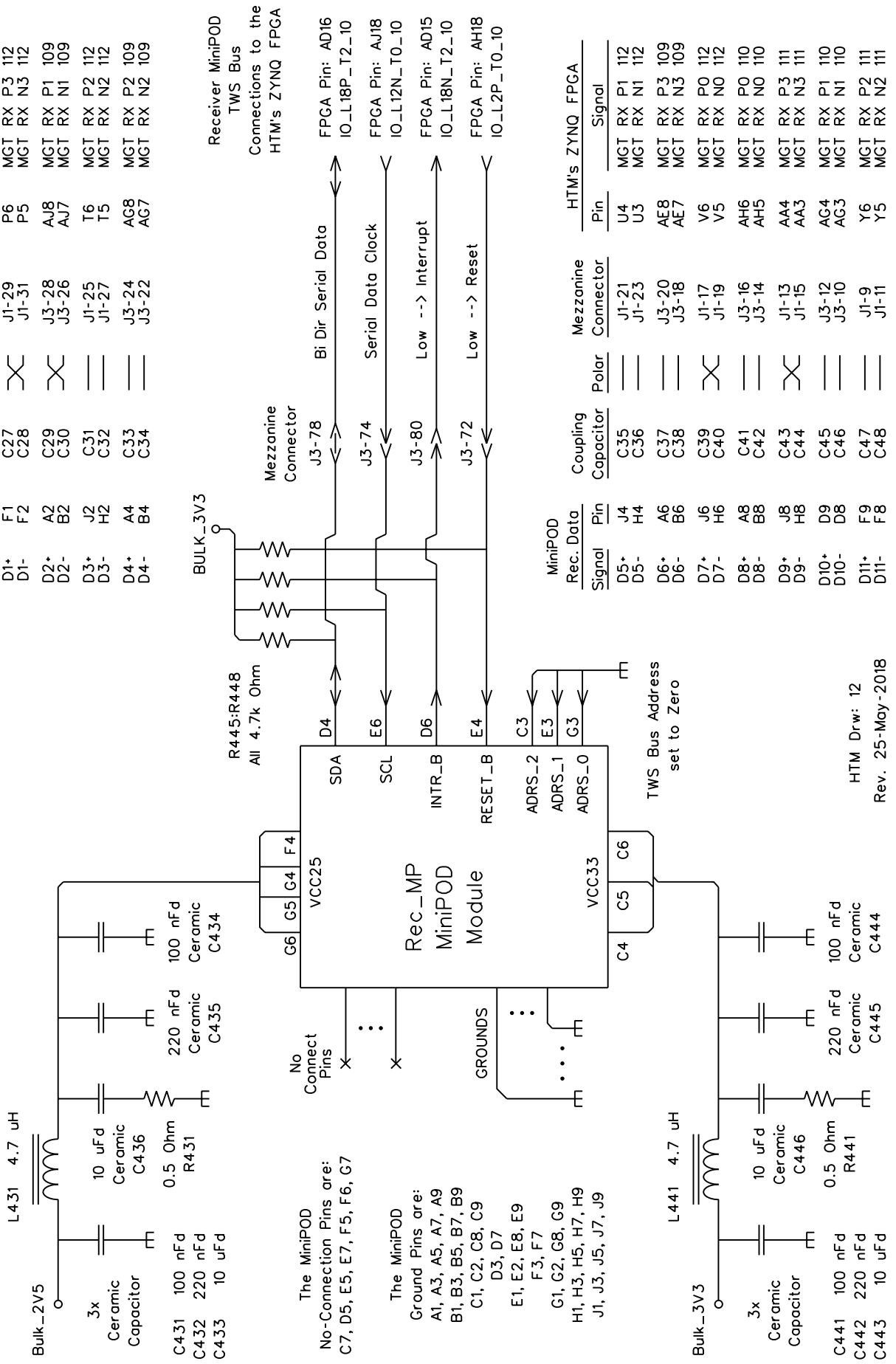


HTM Receiver MiniPOD



The MiniPOD No-Connection Pins are: C7, D5, E5, E7, F5, F6, G7

The MiniPOD Ground Pins are: A1, A3, A5, A7, A9 B1, B3, B5, B7, B9 C1, C2, C8, C9 D3, D7 E1, E2, E8, E9 F3, F7 G1, G2, G8, G9 H1, H3, H5, H7, H9 J1, J3, J5, J7, J9

MiniPOD		Coupling		Mezzanine		HTM's ZYNQ FPGA	
Rec. Data	Pin	Capacitor	Polar	Connector	Pin	Signal	
D0+	D1	C25	—	J3-32	AH10	MGT RX PO	109
D0-	D2	C26	—	J3-30	AH9	MGT RX NO	109
D1+	F1	C27	⊗	J1-29	P6	MGT RX P3	112
D1-	F2	C28	⊗	J1-31	P5	MGT RX N3	112
D2+	A2	C29	⊗	J3-28	AJ8	MGT RX P1	109
D2-	B2	C30	⊗	J3-26	AJ7	MGT RX N1	109
D3+	J2	C31	—	J1-25	T6	MGT RX P2	112
D3-	H2	C32	—	J1-27	T5	MGT RX N2	112
D4+	A4	C33	—	J3-24	AG8	MGT RX P2	109
D4-	B4	C34	—	J3-22	AG7	MGT RX N2	109

Receiver MiniPOD Connections to the HTM's ZYNQ FPGA

FPGA Pin: AD16 IO_L18P_T2_10

FPGA Pin: AJ18 IO_L12N_T0_10

FPGA Pin: AD15 IO_L18N_T2_10

FPGA Pin: AH18 IO_L2P_T0_10

MiniPOD		Coupling		Mezzanine		HTM's ZYNQ FPGA	
Rec. Data	Pin	Capacitor	Polar	Connector	Pin	Signal	
D5+	J4	C35	—	J1-21	U4	MGT RX P1	112
D5-	H4	C36	—	J1-23	U3	MGT RX N1	112
D6+	A6	C37	—	J3-20	AE8	MGT RX P3	109
D6-	B6	C38	—	J3-18	AE7	MGT RX N3	109
D7+	J6	C39	⊗	J1-17	V6	MGT RX PO	112
D7-	H6	C40	⊗	J1-19	V5	MGT RX NO	112
D8+	A8	C41	—	J3-16	AH6	MGT RX PO	110
D8-	B8	C42	—	J3-14	AH5	MGT RX NO	110
D9+	J8	C43	⊗	J1-13	AA4	MGT RX P3	111
D9-	H8	C44	⊗	J1-15	AA3	MGT RX N3	111
D10+	D9	C45	—	J3-12	AG4	MGT RX P1	110
D10-	D8	C46	—	J3-10	AG3	MGT RX N1	110
D11+	F9	C47	—	J1-9	Y6	MGT RX P2	111
D11-	F8	C48	—	J1-11	Y5	MGT RX N2	111