The Hub Test Module (HTM)

Version 0.9, 12/25/2017

1 Introduction

The purpose of this document is to describe the requirements and proposed implementation for the Hub Test Module (HTM).

2 Requirements

2.1 Example

Requirements for the HTM are specified in the following format:

HTM-### **Brief description of the requirement**

Detailed description of the requirement if necessary, optional 'nice to haves' that are related to the minimum requirement will be described here.

2.2 HTM Requirements

HTM-000 **The HTM shall fit in an ATCA slot.**

The HTM must fit in the envelope of one ATCA slot, as described in the ATCA specification. A full size board is preferred, such that it is easy to insert and remove HTMs in a fully populated shelf (2 Hubs, 12 HTMs)

HTM-005 **The HTM shall contain an FPGA of sufficient capability to fulfill all of its requirements**

General requirement indicating that we want the flexibility of an FPGA. Xilinx is preferred, so that we can hopefully leverage work from the Hub and FTM firmware.

HTM-010 **The HTM shall be powered from the ATCA backplane -48V power infrastructure**

No ATCA Power Entry Module, no Redundant Input Power, not Hot-Swappable. A or B power can be selected by populating the relevant fuses on the HTM.

HTM-015 **The HTM shall not require external connections during production testing.**

No external connections allowed during production testing. Ethernet and JTAG connectors will be present on the front panel. This requirement does not prevent the ethernet to ethernet connections on the front panel of the HTM.

HTM-020 **The HTM shall configure itself upon power-up.**

The firmware must be loadable onto the HTM itself, and it must boot into that firmware automatically upon power-up.

HTM-025 **The HTM shall provide 6 Multi-Gigabit Transceiver (MGT) channels of FEX-like data to each Hub via the ATCA backplane**

HTM-030 **The HTM shall receive 1 MGT channel of combined data from Hub1**

Optionally, the HTM could receive 1 MGT channel of combined data from Hub2 as well.

HTM-035 **The HTM shall be capable of receiving and validating the combined data**

HTM-040 **The HTM shall receive and lock to the 40.08 MHz LHC clock from Hub1, via the ATCA backplane.**

40.08 MHz clock from Hub2 to be routed to a pair of SelectIO pins, merely to check that it exists.

HTM-045 **The HTM shall generate a 320.64 MHz clock locked to the 40.08 MHz LHC clock from Hub1.**

HTM-050 **The HTM shall use the generated 320.64 MHz clock as a reference for its MGTs.**

HTM-055 **The HRM shall provide the 40.08 MHz and 320.64 MHz clocks to its FPGA for use as logic clocks.**

HTM-060 **The HTM MGTs shall operate at 6.4 Gbps minimum.**

Optionally, the HTM MGTs can operated at 9.8 to 10.2 Gbps.

HTM-065 **The HTM shall communicate with Hub1 via Ethernet over the ATCA backplane.**

Communicating to Hub2 via Ethernet over the ATCA backplane is desirable as well, but not a hard requirement.

HTM-070 **The HTM shall detect which ATCA slot it is in via the backplane hardware slot ID pins.**

HTM-075 **The HTM shall generate a MAC address from the hardware slot ID**

HTM-080 **The HTM shall generate a static IP address from the hardware slot ID**

HTM-085 **The HTM shall provide several status LEDs on the front panel.**

Specific LEDs TBD, ideas: standby and main power, main ethernet LED, and a small number of general Select IO LEDs.

3 Hardware Description

It is proposed that the HTM consist of the following:

1. One Trenz Electronic TE0782 XC7Z035-2FFG900I module, hereafter referred to as the 'FPGA module' or the 'TE0782'.
2. One carrier board with sufficient circuitry and mechanical hardware to support that module, hereafter referred to as the 'HTM carrier board'

3.1 Hardware Details - Mechanical

3.1.1 Envelope

The TE0782 is 8.5 cm square, has a PCB thickness of 1.7mm, and a mating height of 5mm when using standard connectors. This is well within the envelope of an ATCA slot.

3.1.2 Connectors

The TE0782 mounts to the carrier board via three high speed Samtec ASP-122952-01 Board-to-Board (B2B) connectors. HTM connector naming has been chosen to be consistent with the TEBT0782 base board. This makes the HTM consistent with the Trenz Electronic master pinout table, which is referenced above. Table 1 shows which TE0782 connectors mate to the three B2B connectors on the HTM.

Table 1: HTM and TE0782 Connector Mating

HTM Connector	TE0782 Connector
J1B	J2
J2B	J1
J3B	J3

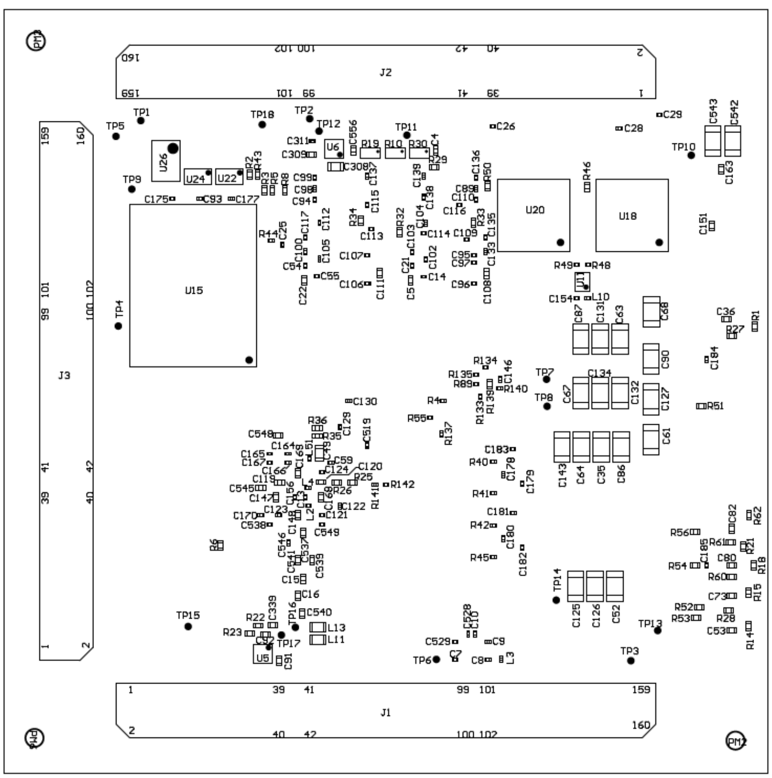

Figure 1: TE0782 Bottom View

Figure 1 shows the locations of the B2B connectors on the bottom side of the TE0782 module.

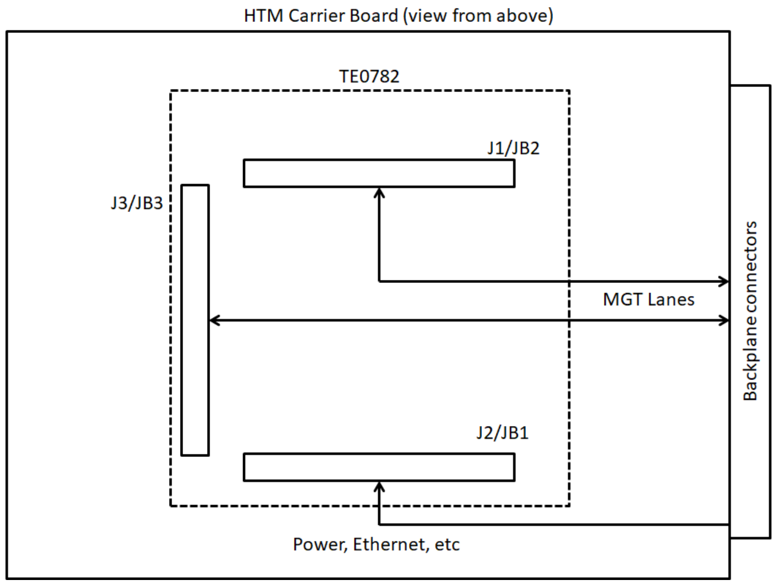

Figure 2: HTM TE0782 Module Orientation

Figure 2 shows a notional top view of the TE0782 module on the HTM carrier card.

The SelectIO lines on TE0782 J1 are 1.8V tolerant, while those on TE0782 J2 and TE0782 J3 are 3.3V tolerant.

JTAG will be exposed on the front panel, in case we need to load new firmware in-situ.

3.1.3 PCB Stackup

One big question surrounding the layer requirements for power purposes is the power consumption on the 12V rail. Currently, the TE0782 documentation lists "'TBD"' on this point. One approach could be to look up the maximum input current per pin on the B2B connectors, and multiply this by the number of 12V input pins. There is also a power estimator spreadsheet from Xilinx for the XC7Z035. My gut feeling is that two 1oz planes, or possibly even 0.5oz planes would be sufficient given that the module accepts 12V main power.

For routing the high speed traces, it is expected that four layers will be more than sufficient. If these are valid assumptions, a candidate stackup might look like:

high speed diff pairs 1 (TOP)
GND
high speed diff pairs 2
GND
Power 1
GND
Power 2
GND
high speed diff pairs 3
GND
high speed diff pairs 4 (BOTTOM)

3.2 Hardware Details - Electrical

TE0782 schematics are available here: https://www.trenz-electronic.de/fileadmin/docs/Trenz_Electronic/TE0782/REV02/Documents/SCH-TE0782-02-035-2I.PDF

The pinout table for the B2B connectors is available here: http://www.trenz-electronic.de/fileadmin/docs/Trenz_Electronic/Pinout/TE_MASTER_PINOUT.xlsm

3.2.1 Power

The TE0782 requires two input voltages, 3.3V Standby power for the on-board CPLD, and 12V Main Power for the rest of the board. The HTM carrier board must create these voltages from the -48V input power provided by the ATCA crate. It is proposed that -48V to 12V conversion use the same +12V isolated power module as the Hub design. The TE0782 draws 100 mA from the 3.3V rail. Thus, the LDO will dissipate: $(V_i - V_o)*I = (12v - 3.3V) * 0.1A = 0.87W$.

Note that in the connector pinout and the schematics, C3.3V is the input power to the CPLD, 3.3V is the output of one of the onboard power supplies (U16, LTM4644EY#PBF).

The 3.3V supply is provided by an LM1117T-3.3 LDO linear regulator.

The B2B connector pins for power are shown in Table 2

Table 2: TE0782 Power Pins

Power Rail	Pins
3.3V STBY	J2-147, J2-148
12V Main	J2-165, J2-166, J2-167, J2-168

Grounds are distributed through J1, J2, and J3.

3.2.2 Clocks

The TE0782 has an onboard Si5338 PLL for GTX clocking. This PLL can accept an input clock, and can be programmed via I2C. Currently the plan is to receive the clock from Hub1. There are no plans to clock the TE0782 from the Hub2 clock.

The onboard PLL will multiply the 40.08 MHz LHC reference clock to 320.64 MHz. Figure 3 shows this design.

In either case, either one or two differential clocks must be connected to the B2B connectors shown in Table 3.

Table 3: TE0782 Clock Inputs

Clock	Positive Pin	Negative Pin
Si5338 Input	J3-38	J3-40
GT REFCLK1	J3-37	J3-39
GT REFCLK2	J1-38	J1-40

Since we are using the Si5338 PLL, we will connect the 40.08 MHz LHC clock from Hub 1 to its input.
Prior to the carrier board arriving, the 25 MHz clock on the TE0782 module can be used to test basic functionality.

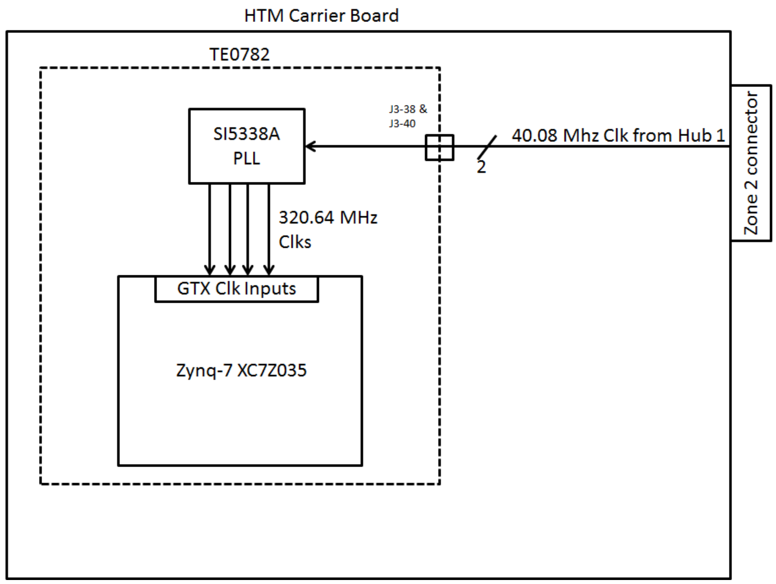

Figure 3: HTM Clock Design

3.2.3 MGTs

The TE0782 has 16 GTX Transceivers exposed on the high speed Samtec B2B connectors. These are capable of up to 12.5 Gbps.

The relevant pins on the B2B connectors for the MGTs are shown in Table 4

Table 4: TE0782 MGT pinouts

MGT #	Role	RxP	RxN	TxP	TxN
0	Hub 1 Tx0	J3-32	J3-30	J3-31	J3-29
1	Hub 1 Tx1	J3-28	J3-26	J3-27	J3-25
2	Hub 1 Tx2	J3-24	J3-22	J3-23	J3-21
3	Hub 1 Tx3	J3-20	J3-18	J3-19	J3-17
4	Hub 1 Tx4	J3-16	J3-14	J3-15	J3-13
5	Hub 1 Tx5	J3-12	J3-10	J3-11	J3-9
6	Hub 1 Combined Data	J3-8	J3-6	J3-7	J3-5
7	Not used	J3-4	J3-2	J3-3	J3-1
MGT #	Role	RxP	RxN	TxP	TxN
8	Hub 2 Tx0	J1-1	J1-3	J1-2	J1-4
9	Hub 2 Tx1	J1-5	J1-7	J1-6	J1-8
10	Hub 2 Tx2	J1-9	J1-11	J1-10	J1-12
11	Hub 2 Tx3	J1-13	J1-15	J1-14	J1-16
12	Hub 2 Tx4	J1-17	J1-19	J1-18	J1-20
13	Hub 2 Tx5	1-21	J1-23	J1-22	J1-24
14	Hub 2 Combined Data	J1-25	J1-27	J1-26	J1-28
15	Not used	J1-29	J1-31	J1-30	J1-32

The TE0782 MGTs are connected to backplane connector J23 via the carrier board as shown in Table 5

Table 5: TE0782 MGTs to Backplane

MGT #	Role	B2B-P pin	B2B-N pin	Backplane-P pin	Backplane-N pin
0	Hub 1 Tx0	J3-31	J3-29	J23-A4	J23-B4
1	Hub 1 Tx1	J3-27	J3-25	J23-E4	J23-F4
2	Hub 1 Tx2	J3-23	J3-21	J23-A3	J23-B3
3	Hub 1 Tx3	J3-19	J3-17	J23-E3	J23-F3
4	Hub 1 Tx4	J3-15	J3-13	J23-C3	J23-D3
5	Hub 1 Tx5	J3-11	J3-9	J23-G3	J23-H3
6	Hub 1 Combined Data	J3-8	J3-6	J23-G4	J23-H4
MGT #	Role	B2B-P pin	B2B-N pin	Backplane-P pin	Backplane-N pin
8	Hub 2 Tx0	J1-2	J1-4	J23-A2	J23-B2
9	Hub 2 Tx1	J1-6	J1-8	J23-E2	J23-F2
10	Hub 2 Tx2	J1-10	J1-12	J23-A1	J23-B1
11	Hub 2 Tx3	J1-14	J1-16	J23-E1	J23-F1
12	Hub 2 Tx4	J1-18	J1-20	J23-C1	J23-D1
13	Hub 2 Tx5	J1-22	J1-24	J23-G1	J23-H1
14	Hub 2 Combined Data	J1-25	J1-27	J23-G2	J23-H2

3.2.4 Ethernet

The TE0782 has two onboard Gigabit Ethernet Transceiver PHYs, though one is dedicated to the Cortex-A9 ARM MPCore. The other PHY is available to the FPGA directly, and will be sufficient to communicate to Hub1 via the backplane connector J23.

The TE0782 also has two onboard Ethernet MAC Address EEPROMs, one for each GigE channel.

Magnetics will be required for each Ethernet interface. The HTM carrier board will use the same Pulse Engineering HX5201NL magnetics as the Hub does.

Both Ethernet interface from the TE0782 will be routed to TE Connectivity 1-406541-1 RJ-45 connectors on the front panel of the HTM, via the HX5201NL magnetics. Both Ethernet interfaces from the backplane will routed directly to TE Connectivity 1-406541-1 RJ-45 connectors on the front panel of the HTM. This is shown in Figure 4.

The Ethernet pinout at the TE Connectivity 1-406541-1 RJ-45 connectors will be as shown in Table 6:

Table 6: TE0782 RJ-45 connector pinouts

RJ-45 Pin	Signal
1	A+
2	A-
3	B+
4	C+
5	C-
6	B-
7	D+
8	D-
9	Analog GND
10	Analog GND

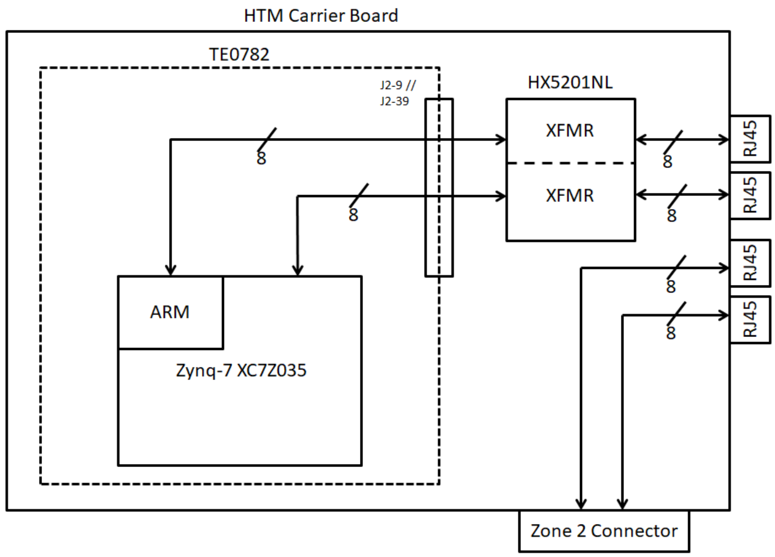

Figure 4: HTM Ethernet Lines

The LED signals for each Ethernet interface are routed to the FPGA. SelectIO lines will have to be used to illuminate LEDs on the carrier board for these signals.

The B2B connections for the Ethernet PHYs are described in Table 7

Table 7: TE0782 Ethernet pinouts

PHY1 Signal	Pin	PHY2 Signal	Pin
PHY1_MDI0_P	J2-23	PHY2_MDI0_P	J2-39
PHY1_MDI0_N	J2-21	PHY2_MDI0_N	J2-37
PHY1_MDI1_P	J2-19	PHY2_MDI1_P	J2-35
PHY1_MDI1_N	J2-17	PHY2_MDI1_N	J2-33
PHY1_MDI2_P	J2-15	PHY2_MDI2_P	J2-31
PHY1_MDI2_N	J2-13	PHY2_MDI2_N	J2-29
PHY1_MDI3_P	J2-11	PHY2_MDI3_P	J2-27
PHY1_MDI3_N	J2-9	PHY2_MDI3_N	J2-25

The L1Calo backplane specification defines Base Channels 1 and 2 are used for communicating to Hub 1 and Hub 2 respectively. These channels use the pins shown in 8

3.2.5 Hardware ID

Hardware ID pins from the backplane will be routed to selectIO lines via J2. These pins are tied to 3.3V via a 5k resistor, and to analog ground via a 1nF bypass capacitor. See requirements 2.298 and 2.299 in the ATCA base specification.

NOTE: The Hub uses 1k resistors and 100 nF capacitors for these lines.

Table 8: Backplane Ethernet Pinouts

Base Channel	Lane	Positive Pin	Negative Pin
1	0	J23-5A	J23-5B
1	1	J23-5C	J23-5D
1	2	J23-5E	J23-5F
1	3	J23-5G	J23-5H
2	0	J23-6A	J23-6B
2	1	J23-6C	J23-6D
2	2	J23-6E	J23-6F
2	3	J23-6G	J23-6H

4 Firmware Description

4.1 Configuration

The TE0782 has a 32 MB SPI flash available for configuration and/or bootloader storage. The First Stage Bootloader must exist on the SPI flash, and there is 4 GB of eMMC available for secondary boot.

4.2 Ethernet Control

TBD - expect to use similar IPbus infrastructure as the Hub, receiving commands from the backplane ethernet connection to Hub1. Also include dummy registers for Hub random register test through switch.

4.3 FEX Data Generation

TBD - Aurora-capable, also fixed lanes to emulate jFEX? Defined short and long duration patterns, pseudo-random patterns, eventually real-looking data.

4.4 Hub Combined Data Processing

TBD