TE0782 Basic-System

-Downloadable files are located below the description-

Short Description:

Zynq-PS with second Ethernet PHY over PL.

Currently implemented:

- USB 2.0(both)
- ETH (both)
- RTC

Release Notes and Known Issues:

- Boot process from QSPI
  - read image.ub from flash with uboot is slow. This effect occurs with uboot generate with 2017.1 petalinux

Launch:

1. Connect JTAG/UART on carrier.
2. Power on carrier.
3. Configure Flash with Boot.bin (<design_name>/prebuilt/boot_images/<short dir>/u-boot), image.ub is included into boot.bin. Use SDK or Vivado.
4. Power off/on carrier.
5. Open Serial console:
   - Windows: Open Serial Console (e.g. putty):COM Port(see device manager), Speed(115200).
   - Linux: Open Serial Console (e.g. minicom):COM Port(dmesg |grep tty) UART is *USB1, Speed(115200).
6. Wait until Linux boot finised(load image.ub from QSPI need a little bit time, see release notes).
7. ETH0 (PHY connected to PS MIOs)
   - Connect ETH cable.
   - type: udhcpc
   - or set IP manually
8. ETH1 (PHY connected to PL IOs)
   - Connect ETH cable.
   - type: ifconfig eth1 up
   - Note: output "xemacps e000c000.ethernet: Set clk to 0 Hz" can be ignored.
   - type: ifconfig eth1 <ip>

Excerpt of special Block-Design components/interfaces:

Component	Description
PS-MIOs	QSPI, I2C1, UART1, GPIO, SD1, USB0, USB1, ETH0, ETH1, DDR3

Xilinx-IP	GMII to RGMII
TE-IP	TE0782 System Control

Additional software application for SDK/HSI and Linux:

Application	Description
zynq_fsbl	TE modified Zynq FSBL for SI5338 Configuration (template in subfolder sw_lib)
hello_world	Xilinx Hello World Example
u-boot	Petalinux-Uboot (image.ub in <design_name>/prebuilt/os/petalinux/<short dir or default>)

Additional sources:

Name	Folder	Description
SI5338 Project	<design_name>/misc/si5338/	Clock Builder Desktop Project, with all CLKs enabled.
FSBL Template	<design_name>/sw_lib/	Modified FSBL Template for SDK/HSI
PetaLinux Project	<design_name>/os/petalinux	PetaLinux Project with ETH0,RTH1,USB0,USB1,RTC

Additional prebuilt-content (larger ZIP-file):

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA Configuration File
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Disclaimer:

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Files

Reference Design - Source Code only (1 Files)

te0782-test_board_noprebuilt-vivado_2017.1-build_04_20170830170858.zip

Size 1,48 MB / Modified 30.08.2017 - 18:09:00

Reference Design - Source Code and Configuration Files (1 Files)

te0782-test_board-vivado_2017.1-build_04_20170830170807.zip

Size 41,53 MB / Modified 30.08.2017 - 18:08:10

Other Files (0 Files)