TE0782 CPLD

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Overview

Firmware for PCB CPLD with designator U14. CPLD Device in Chain: LCMX02-1200HC

Feature Summary

- Power Management
- Boot Mode
- LED

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Description
BM0/MIO5	out	47	Boot Mode Pin
BM2/MIO4	out	48	Boot Mode Pin
BM3/MIO2	out	49	Boot Mode Pin
BOOTMODE	in	99	Boot Mode Pin from B2B / USED as Input to MIO9
CONFIGX	out	98	MIO8 to B2B
CPLD_GPIO0		12	/ currently_not_used
CPLD_GPIO1		11	/ currently_not_used
CPLD_GPIO2		10	/ currently_not_used
CPLD_GPIO3		9	/ currently_not_used
CPLD_GPIO4		8	/ currently_not_used
CPLD_GPIO5		7	/ currently_not_used
CPLD_IO		54	/ currently_not_used
DONE	in	34	FPGA Done Pin

Name / opt. VHD Name	Direction	Pin	Description
EN_1.0V_MGT / EN_1V0_MGT	out	20	Power control
EN_1.2V_MGT / EN_1V2_MGT	out	18	Power control
EN_1.8V	out	16	Power control
EN_1V	out	21	Power control
EN_3.3V	out	15	Power control
ETH1_RESET	out	53	ETH Reset
ETH1_RESET33	in	43	ETH Reset from MIO7
I2C_SCL	in	58	I2C CLK / currently_not_used
I2C_SDA	in	57	I2C / currently_not_used
INIT		36	/ currently_not_used
JTAGENB	in	82	Enable JTAG access to CPLD for Firmware update (zero: JTAG routed into CPLD logic, one: CPLD access)
LED1 / GLED	out	4	gren LED D2
LED2 / RLED	out	3	red LED D1
M_TCK	in	91	CPLD JTAG B2B
M_TDI	in	94	CPLD JTAG B2B
M_TDO	out	95	CPLD JTAG B2B
M_TMS	in	90	CPLD JTAG B2B
MIO8	in	38	used UART RS activity
MIO9	out	39	User IO, connected to BOOTMODE Pin on B2B

Name / opt. VHD Name	Direction	Pin	Description
MMC_RST	out	40	eMMC Reset
N.C. / dummy		1	used as dummy output
N.C.		2	/ currently_not_used
N.C.		27	/ currently_not_used
N.C.		28	/ currently_not_used
N.C.		29	/ currently_not_used
N.C.		30	/ currently_not_used
N.C.		32	/ currently_not_used
N.C.		41	/ currently_not_used
N.C.		42	/ currently_not_used
N.C.		59	/ currently_not_used
N.C.		60	/ currently_not_used
N.C.		61	/ currently_not_used
N.C.		62	/ currently_not_used
N.C.		63	/ currently_not_used
N.C.		64	/ currently_not_used
N.C.		65	/ currently_not_used
N.C.		66	/ currently_not_used
N.C.		67	/ currently_not_used
N.C.		68	/ currently_not_used

Name / opt. VHD Name	Direction	Pin	Description
N.C.		69	/ currently_not_used
N.C.		70	/ currently_not_used
N.C.		71	/ currently_not_used
N.C.		74	/ currently_not_used
N.C.		75	/ currently_not_used
N.C.		76	/ currently_not_used
N.C.		77	/ currently_not_used
N.C.		78	/ currently_not_used
N.C.		81	/ currently_not_used
N.C.		83	/ currently_not_used
N.C.		84	/ currently_not_used
N.C.		85	/ currently_not_used
N.C.		86	/ currently_not_used
N.C.		87	/ currently_not_used
N.C.		88	/ currently_not_used
N.C.		89	/ currently_not_used
N.C.		96	/ currently_not_used
OTG-RST	out	52	OTG Rest
OTG-RST33	in	45	OTG Reset from MIO0
PG_1.0V_MGT	in	19	Power control

Name / opt. VHD Name	Direction	Pin	Description
PG_1.2V_MGT	in	17	Power control
PG_1.8V	in	14	Power control
PG_1V	in	25	Power control
PG_1V5	in	24	Power control
PG_3.3V	in	13	Power control
PROG_B		35	/ currently_not_used
PS_POR	out	37	PS_POR_B (Power On Reset)
PS_SRST	out	51	PS_SRST_B (PS Reset)
RESIN	in	97	Reset from B2B
RTC_INT		31	/ currently_not_used

Functional Description

JTAG

Used only for Firmware Update. Zynq has dedicated JTAG connection.

Power

Power enables (EN_1V, EN_1V8, EN_3V3, EN_1V2_MGT, EN_1V0_MGT) are all enabled (constant 1).

Power goods (PG_1V, PG_1V5, PG_1V8, PG_3V3, PG_1V2_MGT, PG_1V0_MGT) are uses for System Reset and LED Monitoring.

Boot Mode

Is set fix to QSPI (MIO(5:3) = 100)

Reset

PS_SRST is main power failed or user reset (RESIN).

ETH1_RESET is main power failed and ETH1_RESET33 and DONE.

OTG_RST is main power failed and ETH1_OTG_RST33 and DONE.

MMC_RST is main power or mgt power failed.

LED

Red LED D1

Blink Sequency	Priority	Condition	Description
*ooooooo	1	PG_1V or PG_1V5 or PG_1V8 or PG_3V3 is zero	Main power problem
**oooooo	2	PG_1V2_MGT or PG_1V0_MGT is zero	MGT power Problem
***ooooo	3	B2B Main Reset is set (Zero)	User Main Reset
****oooo	4	FPG Done Pin is zero	FPGA part (PL) is not programmed
Blink	5		all Ready

Green LED D1

UART RX activity.

Appx. A: Change History and Legal Notices

Revision Changes

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
2018-03-13	v.3	REV01	RE02	@John Hartfiel	• REV01 , Firmware released 2016-06-27

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
2018-03-12	v.1			@John Hartfiel	• Initial release
	All			@John Hartfiel	

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