TE0782 TRM

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Overview

The Trenz Electronic TE0782 is a high-performance, industrial-grade SoM (System on Module) with industrial temperature range based on Xilinx Zynq-7000 SoC (XC7Z035, XC7Z045 or XC7Z100).

These highly integrated modules with an economical price-performance-ratio have a form-factor of 8,5 x 8,5 cm and are available in several versions.

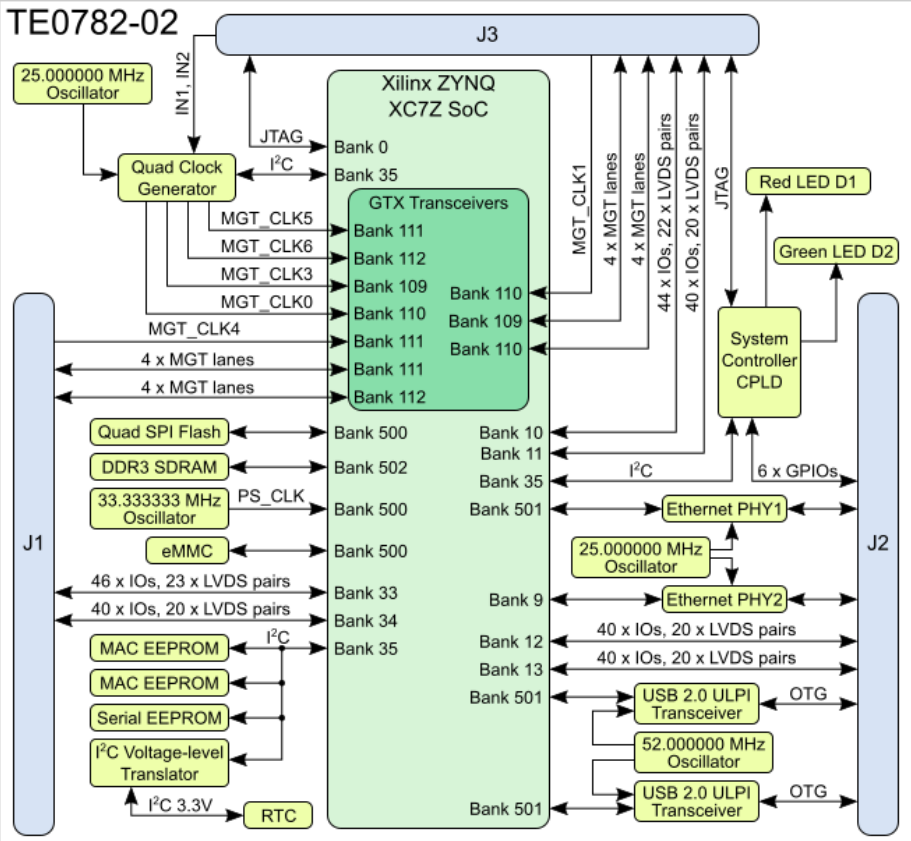
All parts cover at least industrial temperature range of -40°C to +85°C. The module operating temperature range depends on customer design and cooling solution. Please contact us for options and for modified PCB-equipping due increasing cost-performance-ratio and prices for large-scale order.

Key Features

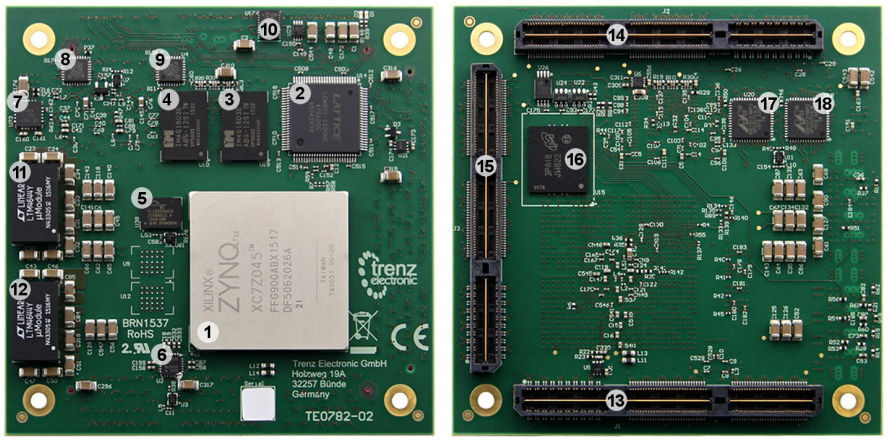
- Xilinx Zynq-7 XC7Z035, XC7Z045 or XC7Z100 SoC
- Rugged for shock and high vibration
- Large number of configurable I/Os are provided via rugged high-speed stacking strips
- Dual ARM Cortex-A9 MPCore
    - 1 GByte RAM (32-Bit wide DDR3)
    - 32 MByte QSPI Flash memory
    - 2 x Hi-Speed USB2.0 ULPI transceiver PHY
    - 2 x Gigabit (10/100/1000 Mbps) Ethernet transceiver PHY
    - 4 GByte eMMC (optional up to 64 GByte)
- 2 x MAC-address EEPROMs
- Optional 2 x 8 MByte HyperRAM (max 2 x 32 MByte) or optional 2 x 64 MByte HyperFLASH
- Temperature compensated RTC (real-time clock)
- Si5338 PLL for GTX transceiver clocks
- Plug-on module with 3 x 160-pin high-speed strips
    - 16 GTX high-performance transceiver
    - GT transceiver clock inputs
    - 254 FPGA I/O's (125 LVDS pairs)
- On-board high-efficiency switch-mode DC-DC converters
- System management
- eFUSE bit-stream encryption
- AES bit-stream encryption
- Evenly-spread supply pins for good signal integrity
- User LED

Assembly options for cost or performance optimization available upon request.

Block Diagram



Main Components



1. Xilinx Zynq XC7Z SoC (XCZ035, XC7Z045 or XC7Z100), U1
2. Lattice Semiconductor MachXO2 1200HC System Controller CPLD, U14
3. Intelligent Memory 4Gbit DDR3L-1600 SDRAM, U19
4. Intelligent Memory 4Gbit DDR3L-1600 SDRAM, U10
5. Spansion 32 MByte QSPI Flash memory, U38
6. SI5338A PLL programmable clock generator, U2
7. TI low-dropout linear regulator @1.5V, U23
8. Microchip USB3320C USB PHY transceiver, U8
9. Microchip USB3320C USB PHY transceiver, U4
10. Intersil ISL12020MIRZ Real Time Clock, U17
11. LT quad 4A PowerSoC DC-DC converter (1.0V), U13
12. LT quad 4A PowerSoC DC-DC converter (3.3V, 1,8V, 1.2V_MGT, 1.0V_MGT), U16
13. Samtec ASP-122952-01 160-pin stacking strip (2 rows a 80 positions), J1
14. Samtec ASP-122952-01 160-pin stacking strip (2 rows a 80 positions), J2
15. Samtec ASP-122952-01 160-pin stacking strip (2 rows a 80 positions), J3
16. Micron Technology 4 GByte eMMC, U15
17. Marvell Alaska 88E1512 Gigabit Ethernet PHY, 20
18. Marvell Alaska 88E1512 Gigabit Ethernet PHY, U18

Initial Delivery state

Storage device name	Content	Notes
24LC128-I/ST	not programmed	User content
24AA025E48 EEPROM's	User content not programmed	Valid MAC Address from manufacturer
eMMC Flash-Memory	Empty, not programmed	Except serial number programmed by flash vendor
SPI Flash OTP Area	Empty, not programmed	Except serial number programmed by flash vendor
SPI Flash Quad Enable bit	Programmed	
SPI Flash main array	demo design	
HyperFlash RAM	not programmed	
eFUSE USER	Not programmed	
eFUSE Security	Not programmed	

Signals, Interfaces and Pins

Board to Board (B2B) I/Os

I/O signals connected to the SoC's I/O banks and B2B connector:

Bank	Type	VCCIO Max	Connector	IO count	Differential	IO Voltage	Notes
10	HR	3.3V	J3	44	22	user	
11	HR	3.3V	J3	40	20	user	
12	HR	3.3V	J2	40	20	user	

Bank	Type	VCCIO Max	Connector	IO count	Differential	IO Voltage	Notes
13	HR	3.3V	J2	40	20	user	
33	HP	1.8V	J1	48	23	user	
34	HP	1.8V	J1	42	20	user	

For detailed information about the pin out, please refer to the Master pin-out table.

JTAG Interface

JTAG access to the Xilinx Zynq device is provided through B2B connector J3.

Signal	B2B Pin
TCK	J3-141
TDI	J3-147
TMS	J3-142
TDO	J3-148

JTAG access to the System Controller CPLD device is provided through B2B connector J3.

Signal	B2B Pin
M_TCK	J3-81
M_TDI	J3-87
M_TMS	J3-82
M_TDO	J3-88

⚠ JTAGENB pin in J3 should be kept low or grounded for normal operation.

System Controller CPLD I/O Pins

Special purpose pins to configure and operate the System Controller CPLD (IC U14):

Name	Connection	Note
CLPD_GPIO7	B2B	Function defined by CPLD Firmware (legacy name was BOOTMODE)
CLPD_GPIO6	B2B	Function defined by CPLD Firmware (legacy name was CONFIGX)
JTAGENB	B2B	Logic high enables CPLD JTAG pins, when low CPLD JTAG access is disabled
nRST_IN	B2B	Active low System-reset input (old name RESIN)

Name	Connection	Note
CLPD_GPIO0	B2B	Function defined by CPLD Firmware
CLPD_GPIO1	B2B	Function defined by CPLD Firmware
CLPD_GPIO2	B2B	Function defined by CPLD Firmware
CLPD_GPIO3	B2B	Function defined by CPLD Firmware
CLPD_GPIO4	B2B	Function defined by CPLD Firmware
CLPD_GPIO5	B2B	Function defined by CPLD Firmware
CPLD_IO	PL	

Some of the functions of the SoM are controlled by the System Controller CPLD and it's firmware. User can change this by using(creating) different firmware for the System Controller CPLD.

On-board LEDs

LED	Color	Connected to	Description
D1	Red	LED2	Function depends on System Controller CPLD firmware version.
D2	Green	LED1	Function depends on System Controller CPLD firmware version.

Clocking

Silicon Labs PLL Si5338 is used to supply reference clock for MGT banks. Optionally MGT reference clocks can also be supplied from the baseboard for any of the MGT banks. Reference clock for the Si5338 quad clock generator itself can be supplied by the on-board oscillator (U3) or from the baseboard.

Clock	Frequency	IC	Zynq PS / PL	Notes
PS CLK	33.333333 MHz	U61	PS CLK	PS subsystem main clock
ETH PHY reference	25.000000 MHz	U11	-	
USB PHY reference	52.000000 MHz	U7	-	
PLL reference	25.000000 MHz	U3	-	
GT REFCLK1	-	B2B connector	Bank 110, pin AC7/AC8	Supplied from baseboard.
GT REFCLK4	-	B2B connector	Bank 111, pin U7/U8	Supplied from baseboard.
Si5338 CLK0		U2	Bank 110, pin AA8/AA7	
Si5338 CLK1		U2	Bank 109, pin AF10/AF9	
Si5338 CLK2		U2	Bank 111, pin W8/W7	
Si5338 CLK3		U2	Bank 112, pin N8/N7	

Default MIO Mapping

MIO	Configured as	B2B	Notes

MIO	Configured as	B2B	Notes
0	USB Reset	-	CPLD used as level translator
1	QSPI0	-	SPI Flash-CS
2	QSPI0	-	SPI Flash-DQ0
3	QSPI0	-	SPI Flash-DQ1
4	QSPI0	-	SPI Flash-DQ2
5	QSPI0	-	SPI Flash-DQ3
6	QSPI0	-	SPI Flash-SCK
7	Ethernet Reset	-	CPLD used level translator
8	UART TX	JC3:129	output, muxed to B2B by the SC CPLD
9	UART RX	JC3:135	input, muxed to B2B by the SC CPLD
10	SDIO1 D0	-	-
11	SDIO1 CMD	-	-
12	SDIO1 CLK	-	-
13	SDIO1 D1	-	-
14	SDIO1 D2	-	-
15	SDIO1 D3	-	-
16..27	ETH0	-	Ethernet RGMII PHY
28..39	USB0	-	USB0 ULPI PHY
40...51	USB1	-	USB1 ULPI PHY
52	ETH0 MDC	-	-
53	ETH0 MDIO	-	-

Gigabit Ethernet

The TE0782 is equipped with two Marvell Alaska 88E1512 Gigabit Ethernet PHYs (U18 (ETH1) and U20 (ETH2)). The transceiver PHY of ETH1 is connected to the Zynq PS Ethernet GEM0. The I/O Voltage is fixed at 1.8V. The reference clock input for both PHYs is supplied from an on board 25MHz oscillator (U11).

ETH1 PHY connection:

PHY PIN	ZYNQ PS / PL	System Controller CPLD	Notes
MDC/MDIO	MIO52, MIO53	-	-
LED0	BANK35, Pin B12	-	-
LED1	BANK35, Pin C12	-	-
Interrupt	BANK35, Pin A15	-	-

PHY PIN	ZYNQ PS / PL	System Controller CPLD	Notes
CONFIG	BANK35, Pin F14	-	-
RESETn	-	Pin 53	ETH1_RESET33 (MIO7) -> CPLD -> ETH1_RESET
RGMII	MIO16..MIO27		-
MDI	-	-	on B2B J2 connector

ETH2 PHY connection:

PHY PIN	Zynq PS / PL	System Controller CPLD	Notes
MDC/MDIO	BANK35, Pin C17/B17	-	-
LED0	BANK35, Pin K15	-	-
LED1	BANK35, Pin B16	-	-
Interrupt	BANK35, Pin A17	-	-
CONFIG	BANK35, Pin E15	-	Pin connected to GND, PHY Address is strapped to 0x00 by default
RESETn	BANK35, Pin B15	-	-
RGMII	BANK9	-	-
MDI	-	-	-

USB Interface

The TE0782 is equipped with two USB PHY's USB3320 from Microchip (U4 (USB0) and U8 (USB1)). The ULPI interface of USB0 is connected to the Zynq PS USB0, ULPI interface of USB1 to Zynq PS USB1. The I/O Voltage is fixed at 1.8V.

The reference clock input of both PHY's is supplied from an on board 52MHz oscillator (U7).

USB0 PHY connection:

PHY Pin	Zynq PS / PL	CPLD	B2B Name (J2)	Notes
ULPI	MIO28..39	-	-	Zynq USB0 MIO pins are connected to the PHY
REFCLK	-	-	-	52MHz from on board oscillator (U7)
REFSEL[0..2]	-	-	-	000 GND, select 52MHz reference Clock
RESETB	MIO0	OTG_RESET33	-	OTG_RESET33 -> CPLD -> OTG_RESET
CLKOUT	MIO36	-	-	Connected to 1.8V selects reference clock operation mode
DP,DM	-	-	USB1_D_P, USB1_D_N	USB Data lines
CPEN	-	-	VBUS1_V_EN	External USB power switch active high enable signal
VBUS	-	-	USB1_VBUS	Connect to USB VBUS via a series resistor. Check reference schematic
ID	-	-	OTG1_ID	For an A-Device connect to ground, for a B-Device left floating

USB1 PHY connection:

PHY Pin	ZYNQ PS / PL	CPLD	B2B Name (J2)	Notes
ULPI	MIO40..51	-	-	Zynq USB1 MIO pins are connected to the PHY
REFCLK	-	-	-	52MHz from on board oscillator (U7)
REFSEL[0..2]	-	-	-	000 GND, select 52MHz reference Clock
RESETB	MIO0	OTG_RESET33	-	OTG_RESET33 -> CPLD -> OTG_RESET
CLKOUT	MIO48	-	-	Connected to 1.8V selects reference clock operation mode
DP,DM	-	-	USB2_D_P, USB2_D_N	USB Data lines
CPEN	-	-	VBUS2_V_EN	External USB power switch active high enable signal
VBUS	-	-	USB2_VBUS	Connect to USB VBUS via a series resistor. Check reference schematic
ID	-	-	OTG2_ID	For an A-Device connect to ground, for a B-Device left floating

The schematic for the USB connector and required components is different depending on the USB usage. USB standard A or B connectors can be used for Host or Device modes. A Mini USB connector can be used for USB Device mode. A USB Micro connector can be used for Device mode, OTG Mode or Host Mode.

I2C Interface

The on-board I^2C components are connected to bank 35 pins L15 (I2C_SDA) and L14 (I2C_SCL).

I^2C addresses for on-board components:

Device	IC	Designator	I2C-Address	Notes
EEPROM	24LC128-I/ST	U26	0x53	user data, parameter
EEPROM	24AA025E48T-I/OT	U22	0x50	MAC address EEPROM
EEPROM	24AA025E48T-I/OT	U24	0x51	MAC address EEPROM
RTC	ISL12020MIRZ	U17	0x6F	Temperature compensated real time clock
Battery backed RAM	ISL12020MIRZ	U17	0x57	Integrated in RTC
PLL	SI5338A-B-GMR	U2	0x70	
CPLD	LCMXO2-1200HC-4TG100I	U14	user	-

Pin Definitions

Pins with names ending with _VRN and _VRP are connected to Zynq PL HP bank special purpose pins VRN/VRP and can be routed to DCI calibration resistors on the baseboard. Otherwise they are useable as general purpose I/Os.

Bank 35 has 100 ohm DCI calibration resistors installed, it is also possible to "borrow" the DCI calibration from bank 35 for banks 34 and 33. For more detailed information about the DCI check Xilinx documentation.

On-board peripherals

Processing System (PS) Peripherals

Peripheral	IC	Designator	Zynq PS / PL	MIO	Notes
QSPI Flash	S25FL256SAGBHI20	U38	PS QSPI0	MIO1...MIO6	-
ETH0 10/100/1000 Mbps PHY	88E1512-A0-NNP2I000	U18	PS ETH0	MIO16...MIO27, MIO52, MIO53	-
ETH0 10/100/1000 Mbps PHY Reset			PS GPIO	MIO7	ETH1_RESET33 (MIO7) -> CPLD -> ETH1_RESET
ETH1 10/100/1000 Mbps PHY	88E1512-A0-NNP2I000	U20	BANK9, BANK35	-	PHY can be used with soft Ethernet MAC IP also
ETH1 10/100/1000 Mbps PHY Reset			BANK35, Pin B15	-	-
USB0	USB3320C-EZK	U4	PS USB0	MIO28...MIO39	-
USB0 Reset			PS GPIO	MIO0	OTG_RESET33 (MIO0) -> CPLD -> OTG_RESET
USB1	USB3320C-EZK	U8	USB1	MIO40...MIO51	-
USB1 Reset			PS GPIO	MIO0	OTG_RESET33 (MIO0) -> CPLD -> OTG_RESET
Clock PLL	Si5338	U2	BANK35, Pin L14/L15		Low jitter phase locked loop
e-MMC (embedded e-MMC)	MTFC4GMVEA-4M IT	U15	SDIO0	MIO10...MIO15	-
HyperFlash RAM	S26KS512SDPBHI00x	U9	BANK35	-	optional 2 x 8 MByte HyperRAM (max 2 x 32 MByte HyperRAM) or optional 2 x 64 MByte HyperFLASH
HyperFlash RAM	S26KS512SDPBHI00x	U12	BANK35	-	as above
EEPROM I2C	24LC128-I/ST	U26	BANK35, Pin L14/L15	-	-
EEPROM I2C	24AA025E48T-I/OT	U22	BANK35, Pin L14/L15	-	MAC Address
EEPROM I2C	24AA025E48T-I/OT	U24	BANK35, Pin L14/L15	-	MAC Address
RTC	ISL12020MIRZ	U17	BANK35, Pin L14/L15	-	Temperature compensated real time clock
RTC Interrupt	ISL12020MIRZ	U17	-	-	RTC_INT -> CPLD
UART			PS UART	MIO8, MIO9	forwarded to B2B by SC CPLD

RTC - Real Time Clock

An temperature compensated Intersil ISL12020M is used for Real Time Clock (U17). Battery voltage must be supplied to the module from the baseboard. Battery backed registers can be accessed over I^2C bus at slave address 0x6F. General purpose RAM is at I^2C slave address 0x57. RTC IC is supported by Linux so it can be used as *hwclock* device.

PLL - Phase Locked Loop

The TE0782 is also equipped with a Silicon Labs programmable clock quad generator Si5338A (U2). The Si5338 is accessible for programming over I^2C bus at slave address 0x70.

Input/Output	Default Frequency	Notes

Input/Output	Default Frequency	Notes
IN1/IN2	Externally supplied	Needs decoupling on base board
IN3	25.000000 MHz	Fixed input clock
CLK0 A/B	-	GT REFCLK0
CLK1 A/B	-	GT REFCLK3
CLK2 A/B	-	GT REFCLK6
CLK3 A/B	-	GT REFCLK5

MAC-Address EEPROM's

Two Microchip 24AA025E48 serial EEPROM's (U22 and U24) are used for storing globally unique 48-bit node addresses, are compatible with EUI-48(TM). The devices are organized as two blocks of 128 x 8-bit memory. One of those blocks stores the 48-bit node address and is write protected, the other block is available for application use. EEPROM's are accessible through I^2C nus at slave address 0x50 for MAC-Address1 (U22), 0x51 for MAC-Address2 (U24) .

Boot Process

TE0782's primary boot device is on-board SPI Flash. Boot from on-board eMMC is also supported (FSBL must be loaded from SPI Flash).

JTAG boot mode option is always available.

Power and Power-On Sequence

Input Power Supply

Power Rail	Net name	Voltage	I max	Notes
Standby power	C3.3V	3.3V	100mA	System Control CPLD power
Main power	VIN	12V	TBD	Main power for all on-board DC-DC regulators

Bank Voltages

Bank	Voltage	Voltage	Notes
0	3.3 V	-	FPGA configuration
502	1.5 V	-	DDR3-RAM port
109 / 110 / 111 / 112	1.2 V	-	MGT
500 / 501	3.3 V	-	MIO banks
9	1.8 V	-	ETH2 RGMII
10	user	3.3 V	B2B name: VCCIO_10
11	user	3.3 V	B2B name: VCCIO_11

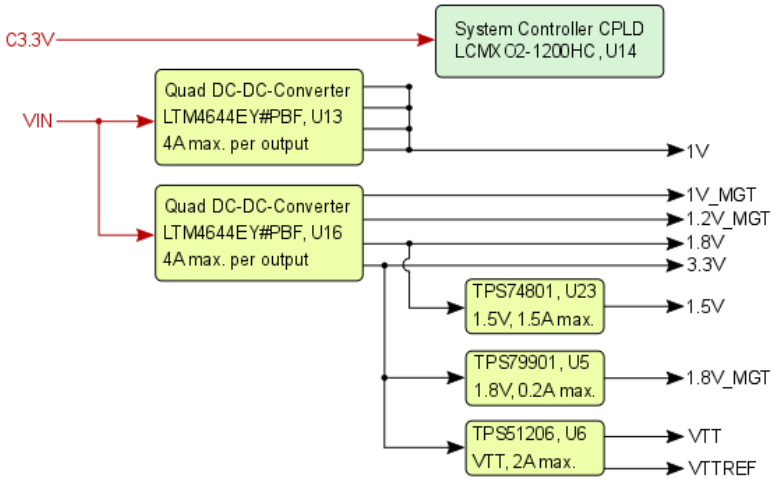
Bank	Voltage	Voltage	Notes
12	user	3.3 V	B2B name: VCCIO_12
13	user	3.3 V	B2B name: VCCIO_13
33	user	1.8 V	B2B name: VCCIO_33
34	user	1.8 V	B2B name: VCCIO_34
35	1.8 V	-	Hyper-RAM, Ethernet, I2C

Power-up sequence at start-up

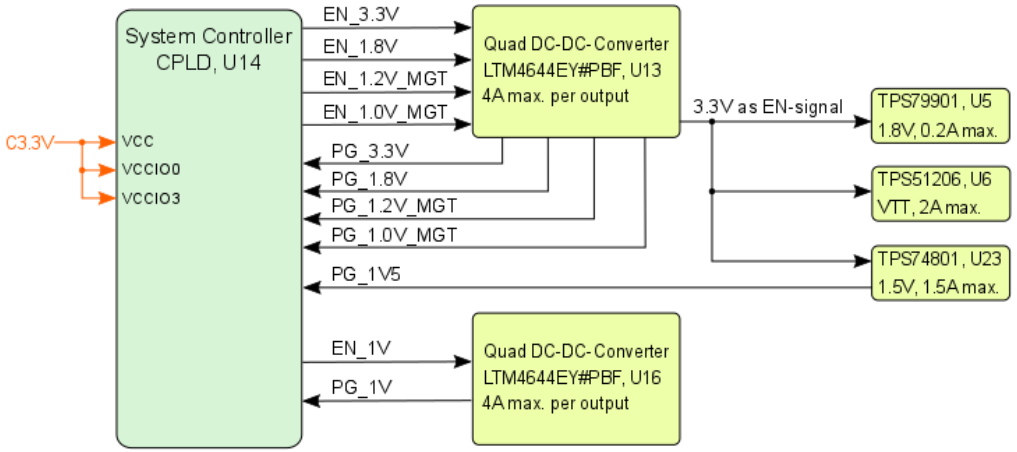
The Trenz TE0782 SoM is equipped with two quad DC-DC voltage regulators to generate required on-board voltage levels 1V, 3.3V, 1.8V, 1.2V_MGT, 1V_MGT. Additional voltage regulators are used to generate voltages 1.5V, VTT, VTTREF and 1.8V_MGT.

The power supply voltage 'C3.3V' of System Controller CPLD of the SoM have to be externally supplied with 3.3V nominal.

There are following dependencies how the initial voltages of the power rails on the B2B connectors are distributed to the on-board DC-DC converters, which power up further DC-DC converters and the particular on-board voltages:



Power-on sequence is handled by the System Controller CPLD using "Power good"-signals from the voltage regulators:



To avoid any damage to the SoM, check on-board voltages in steady state before applying VCCIO voltages to the SoC's I/O banks.

Voltage levels of the I/O signals must not get higher than VCCIO + 0.4V.

Board to Board Connectors

The TE0782 module has three 160-pin double-row ASP-122952-01 Samtec connectors on the bottom side which mate with ASP-122953-01 Samtec connectors on the baseboard. Mating height is 5 mm.

Variants Currently In Production

Module Variant	Zynq SoC	SoC Junction Temperature	Operating Temperature Range
TE0782-02-035-2I	XC7Z035-2FFG900I	-40°C to 100°C	Industrial grade
TE0782-02-045-2I	XC7Z045-2FFG900I	-40°C to 100°C	Industrial grade
TE0782-02-100-2I	XC7Z100-2FFG900I	-40°C to 100°C	Industrial grade

Technical Specification

Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
VIN supply voltage	-0.3	15	V	
VIN33 supply voltage	-0.5	3.75	V	
VBAT supply voltage	-0.3	6	V	
PL IO Bank supply voltage for HR I/O banks (VCCO)	-0.5	3.6	V	

Parameter	Min	Max	Units	Notes
I/O input voltage for HP I/O banks	-0.55	VCCO_X+0.55	V	
Voltage on module JTAG pins	-0.4	VCCO_0+0.55	V	VCCO_0 is 3.3V nominal
Storage temperature	-40	+85	C	
Storage temperature without the ISL12020MIRZ	-55	+100	C	

⚠ Assembly variants for higher storage temperature range on request

Recommended Operating Conditions

Parameter	Min	Max	Units	Notes	Reference document
VIN supply voltage	11.4	12.6	V		
VIN33 supply voltage	3.135	3.465	V		
VBAT supply voltage	1.8	5.5	V		
PL IO Bank supply voltage for HR I/O banks (VCCO)	1.14	3.465	V		Xilinx document DS191
I/O input voltage for HR I/O banks	(*)	(*)	V	(*) Check datasheet	Xilinx document DS191 and DS187
Voltage on Module JTAG pins	3.135	3.465	V	VCCO_0 is 3.3 V nominal	

⚠ Please check Xilinx Datasheet for complete list of Absolute maximum and recommended operating ratings for the Zynq device (DS181 Artix or DS182 Kintex).

Operating Temperature Ranges

Industrial grade: -40°C to +85°C.

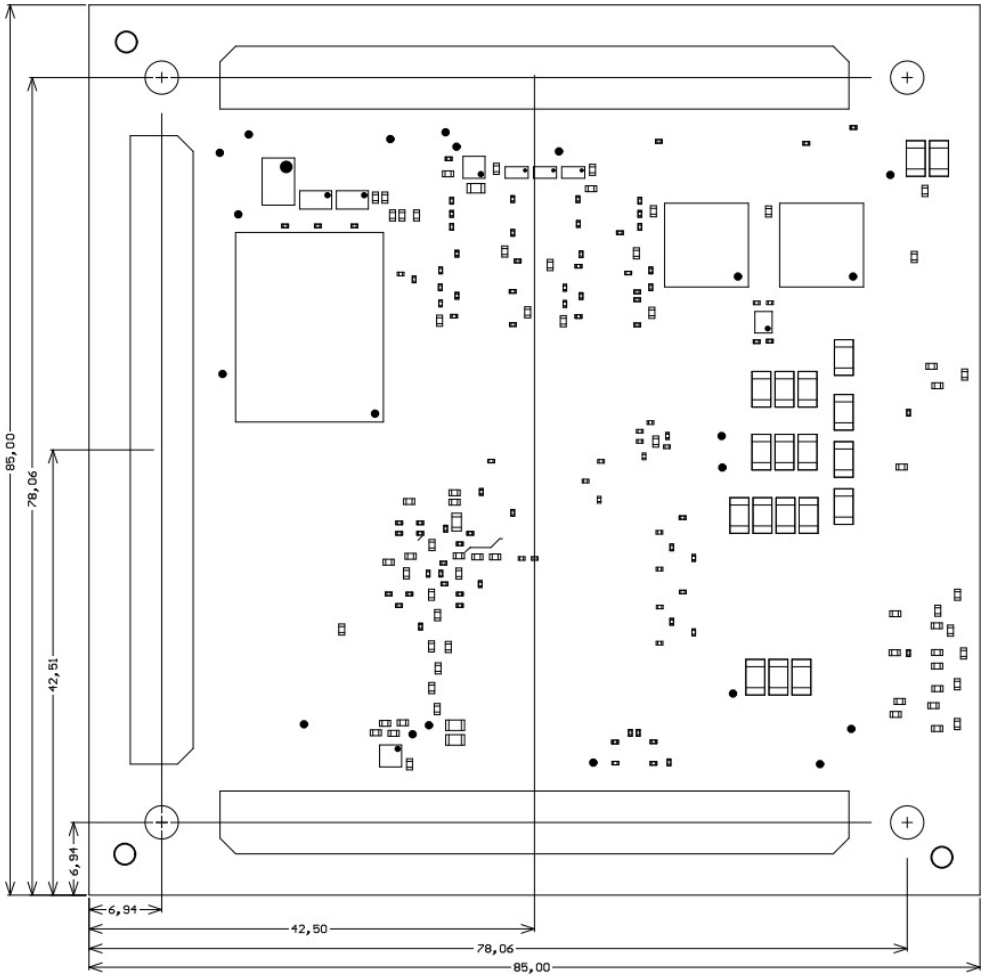
Module operating temperature range depends on customer design and cooling solution. Please contact us for options.

Physical Dimensions

Please download the assembly diagram for exact values.

- Module size: 85 mm × 85 mm.
- Mating height with standard connectors: 5 mm
- PCB thickness: 1,7 mm

All dimensions are shown in millimeters.



Weight

Weight	Part
60 g	Plain module

Revision History

Hardware Revision History

Date	Revision	Changes

Date	Revision	Changes
2015-05-27	02	First production release
	01	Prototypes

Hardware revision number is printed on the PCB board together with the module model number separated by the dash.

Document Change History

Date	Revision	Contributors	Description
2018-01-31	V21	Ali Naseri	updated Power section, added diagramms
2017-06-07	v19	Jan Kumann	Minor formatting
2017-05-23	V13	Jan Kumann	New block diagram. New product images. New physical dimensions drawing.
2017-01-24	V12	Ali Naseri	New numbered pictures describing main components. Added variants in production.
2016-06-27	v10	Ali Naseri, Jan Kumann	Initial release.

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WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.