MGT single channel (Control Signal list):

No	Name	Description	Dir	Size
1	init_done	This active-high signal indicates the mgt channel initialization is complete	IN	1-bit
2	init_retry_ctr	This signal indicates how many attempts were conducted to initialize the channel	IN	1-bit
3	gtpowergood	Power good indicator. When this signal asserts High, the clock output from IBUFDS_GTE3/4 will be ready after a delay of 250 µs.	IN	1-bit
4	txpmaresetdone	This active-high signal indicates TX PMA reset is complete	IN	1-bit
5	rxpmaresetdone	This active-High signal indicates RX PMA reset is complete	IN	1-bit
6	reset_tx_done	When asserted, this active-High signal indicates the transceiver TX has finished reset and is ready for use	IN	1-bit
7	reset_rx_done	When asserted, this active-High signal indicates the transceiver RX has finished reset and is ready for use	IN	1-bit
8	buffbypass_tx_done	Active-High indication that the transmitter buffer bypass procedure has completed	IN	1-bit
9	buffbypass_rx_done	Active-High indication that the receiver buffer bypass procedure has completed	IN	1-bit
10	buffbypass_tx_error	Active-High indication that the transmitter buffer bypass helper block encountered an error condition	IN	1-bit
11	buffbypass_rx_error	Active-High indication that the receiver buffer bypass helper block encountered an error condition	IN	1-bit
12	rxprbserr_flg	This Active-High signal indicates the prbs data error	IN	1-bit
13	rxprbserr_cnt	Error Counter	IN	32-bits
14	rxprbslocked	Output to indicate that the RX PRBS checker has been error free. Once asserted High, RXPRBSLOCKED does not deassert until reset of the RX pattern checker via a reset of the RX or a reset of the PRBS error counter	IN	1-bit
15	reset_master	Master reset (TX and RX)	OUT	1-bit

16	reset_tx_pll_and_datapath	User signal to reset the transmit data direction and associated PLLs of transceiver primitives. An active-High, asynchronous pulse of at least one gtwiz_reset_clk_freerun_in period in duration initializes the process	OUT	1-bit
17	reset_tx_datapath	User signal to reset the transmit data direction of transceiver primitives. An active-High, asynchronous pulse of at least one gtwiz_reset_clk_freerun_in period in duration initializes the process	OUT	1-bit
18	reset_rx_pll_and_datapath	User signal to reset the receive data direction and associated PLLs of transceiver primitives. An active-High, asynchronous pulse of at least one gtwiz_reset_clk_freerun_in period in duration initializes the process	OUT	1-bit
19	reset_rx_datapath	User signal to reset the receive data direction of transceiver primitives. An active-High, asynchronous pulse of at least one gtwiz_reset_clk_freerun_in period in duration initializes the process	OUT	1-bit
20	loopback	000: Normal operation 001: Near-end PCS Loopback 010: Near-end PMA Loopback 011: Reserved 100: Far-end PMA Loopback 101: Reserved 110: Far-end PCS Loopback	OUT	3-bits
21	txprbssel	Transmitter PRBS generator test pattern control: 4'b0000: Standard operation mode (test pattern generation is off) 4'b0001: PRBS-7 4'b0010: PRBS-9 4'b0011: PRBS-15 4'b0100: PRBS-23 4'b0101: PRBS-31	OUT	4-bits
22	rxprbssel	Receiver PRBS checker test pattern control. Only these settings are valid: 4’b000: Standard operation mode. (PRBS check is off) 4’b0001: PRBS-7 4’b0010: PRBS-9 4’b0011: PRBS-15 4’b0100: PRBS-23 4’b0101: PRBS-31	OUT	4-bits

		After changing patterns, perform a reset of the RX or a reset of the PRBS error counter (RXPRBSCNTRESET) such that the RX pattern checker can attempt to reestablish the link acquired. No checking is done for non-PRBS patterns		
23	txprbsforceerr	When this port is driven High, a single error is forced in the PRBS transmitter for every TXUSRCLK2 clock cycle. The output data pattern contains one error for every TXUSRCLK2 clock cycle while the port is asserted. When TXPRBSSEL is set to 4'b0000, this port does not affect TXDATA	OUT	1-bit
24	rxprbscntreset	Error flag and counter reset	OUT	1-bit