10/13/2016 by Pawel Plucinski
Target: VCU108 (UltraScale)

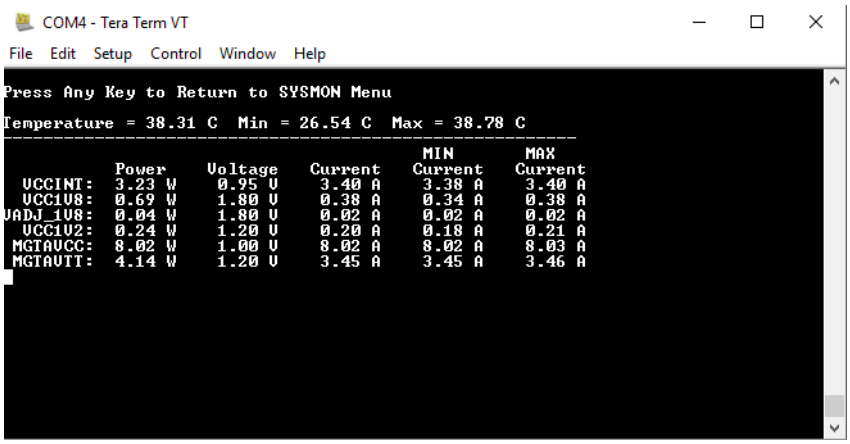
Power Estimation (VCU108) – the update

INTRODUCTION

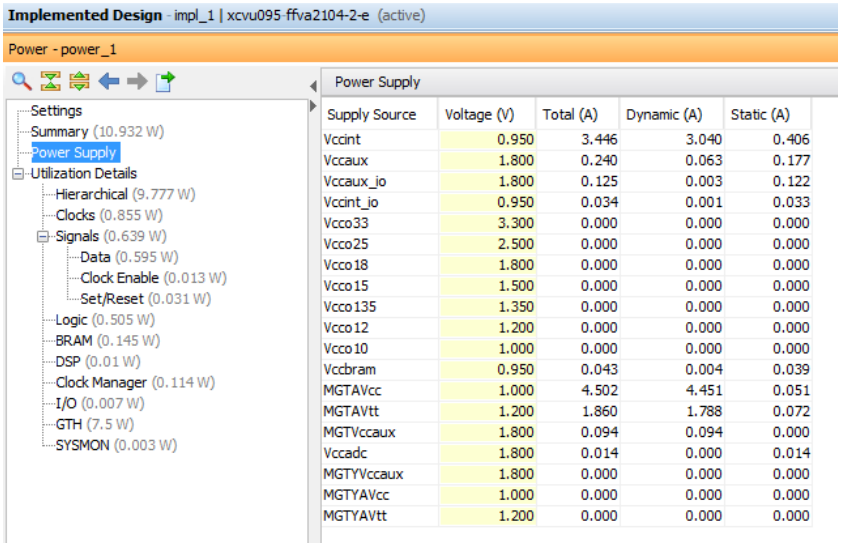
The Power Estimation for the MGTAVTT, MGTAVCC and VCCINT was done with the use of System Controller (Embedded System @ZYNQ) on the VCU108. The results demonstrates high discrepancy compared to the XPE/XPA-Vivado. The custom design with the SYSMON is implemented to verify numbers found with the System Controller.
Presented results corresponds to the configuration_1 (GTH, 28links @9.6 Gbps). The VCU108 board SYSMON ADC interface includes current measuring capability for all FPGA voltage rails. The rail current measurements are made available to SYSMON via an Analog Devices ADG707BRU multiplexer U75 (Figure 1-30 and Table 1 -37).
The design with the SYSMON allows to extract the raw ADC counts which after conversions corresponds to the measured currents and voltages. Table 1.37 summarizes the controlled rails.

RESULTS

Power Estimation – System Controller:



Power Estimation – Vivado (XPA):



Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	0.950	3.446	3.040	0.406
Vccaux	1.800	0.240	0.063	0.177
Vccaux_io	1.800	0.125	0.003	0.122
Vccint_io	0.950	0.034	0.001	0.033
Vcco33	3.300	0.000	0.000	0.000
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.000	0.000	0.000
Vcco15	1.500	0.000	0.000	0.000
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vcco10	1.000	0.000	0.000	0.000
Vccbram	0.950	0.043	0.004	0.039
MGTAVcc	1.000	4.502	4.451	0.051
MGTAVtt	1.200	1.860	1.788	0.072
MGTVccaux	1.800	0.094	0.094	0.000
Vccadc	1.800	0.014	0.000	0.014
MGTYVccaux	1.800	0.000	0.000	0.000
MGTYAVcc	1.000	0.000	0.000	0.000
MGTYAVtt	1.200	0.000	0.000	0.000

Power Estimation – SYSMON:

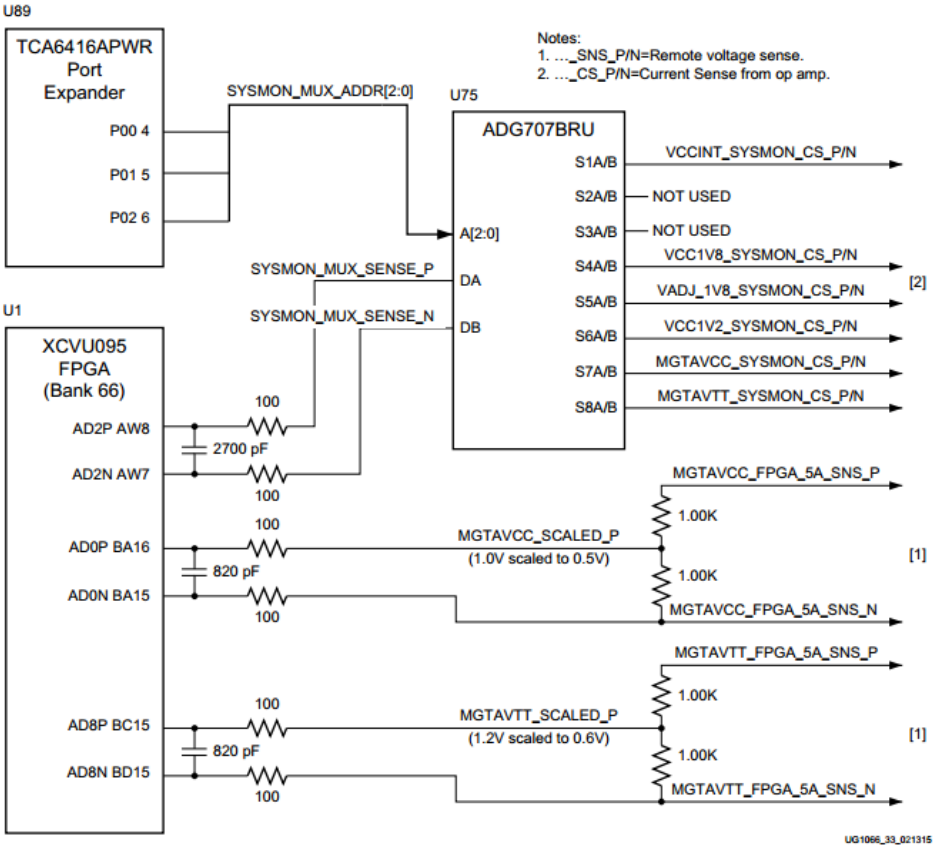


Figure 1-30: **SYSMON External Multiplexer Block Diagram**

Table 1-37: **SYSMON Measurements through MUX U75**

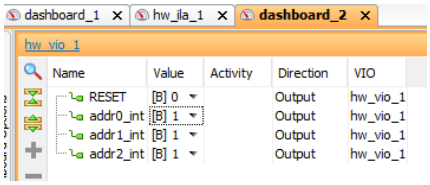
Controlled Rail Name	Regulator Reference Descriptor	Measurement Type	Nominal V_{OUT}	Current Range	I_{SENSE} Op Amp			Schematic Net Name	8-to-1 MUX U75		
					Reference Designator	Gain	V_O Range		Pin Number	Pin Name	A[2:0]
VCCINT_FPGA	U164	V	0.95V	N/A	N/A			SYSMON or MAXIM GUI	N/A		
		I	N/A	0-60A	U74	15	0-1V	VCCINT_SYSMON_CS_P	19	S1A	000
								VCCINT_SYSMON_CS_N	11	S1B	
VCC1V8_FPGA	U9	V	1.80V	N/A	N/A			MAXIM GUI ONLY	N/A		
		I	N/A	0-10A	U116	20	0-1V	VCC1V8_SYSMON_CS_P	22	S4A	011
								VCC1V8_SYSMON_CS_N	8	S4B	
VADJ_1V8_FPGA	U30	V	1.80V	N/A	N/A			MAXIM GUI ONLY	N/A		
		I	N/A	0-10A	U119	20	0-1V	VADJ_1V8_SYSMON_CS_P	23	S5A	100
								VADJ_1V8_SYSMON_CS_N	7	S5B	
VCC1V2_FPGA	U4	V	1.20V	N/A	N/A			MAXIM GUI ONLY	N/A		
		I	N/A	0-10A	U120	20	0-1V	VCC1V2_SYSMON_CS_P	24	S6A	101
								VCC1V2_SYSMON_CS_N	6	S6B	
MGTAVCC_FPGA	U166	V	1.00V	N/A	N/A			SYSMON AD0 or MAXIM GUI	N/A		
		I	N/A	0-17A	U118	54.4	0-1V	MGTAVCC_SYSMON_CS_P	25	S7A	110
								MGTAVCC_SYSMON_CS_N	5	S7B	
MGTAVTT_FPGA	U165	V	1.20V	N/A	N/A			SYSMON AD8 or MAXIM GUI	N/A		
		I	N/A	0-17A	U117	54.4	0-1V	MGTAVTT_SYSMON_CS_P	26	S8A	111
								MGTAVTT_SYSMON_CS_N	4	S8B	

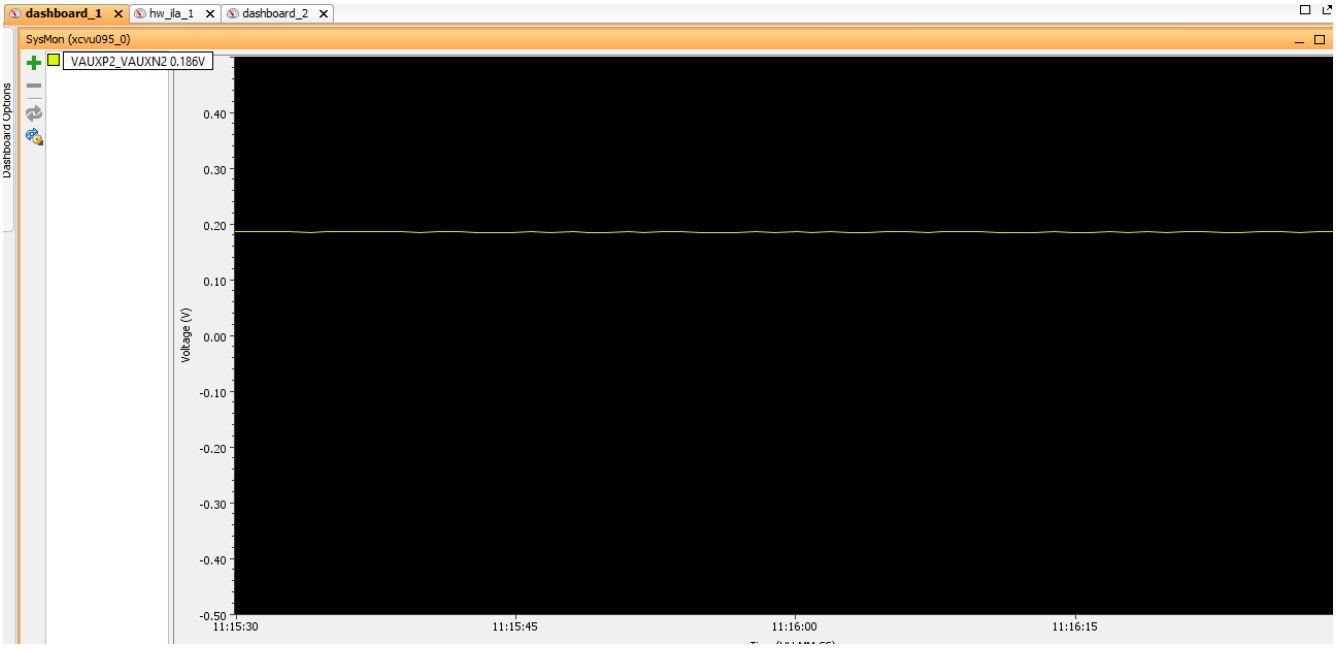
SYSMON: MGTAVTT_FPGA ADC (8-to-1 MUX U75, ADDR[2:0] = 111):

ADC conversion to currents:

$I = (ADC/2^{16})$ [V] x (17/0.93) [A/V]

I = (12183/65536) x (17/0.93) = 3.39 [A]



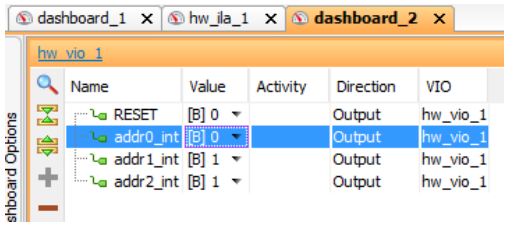


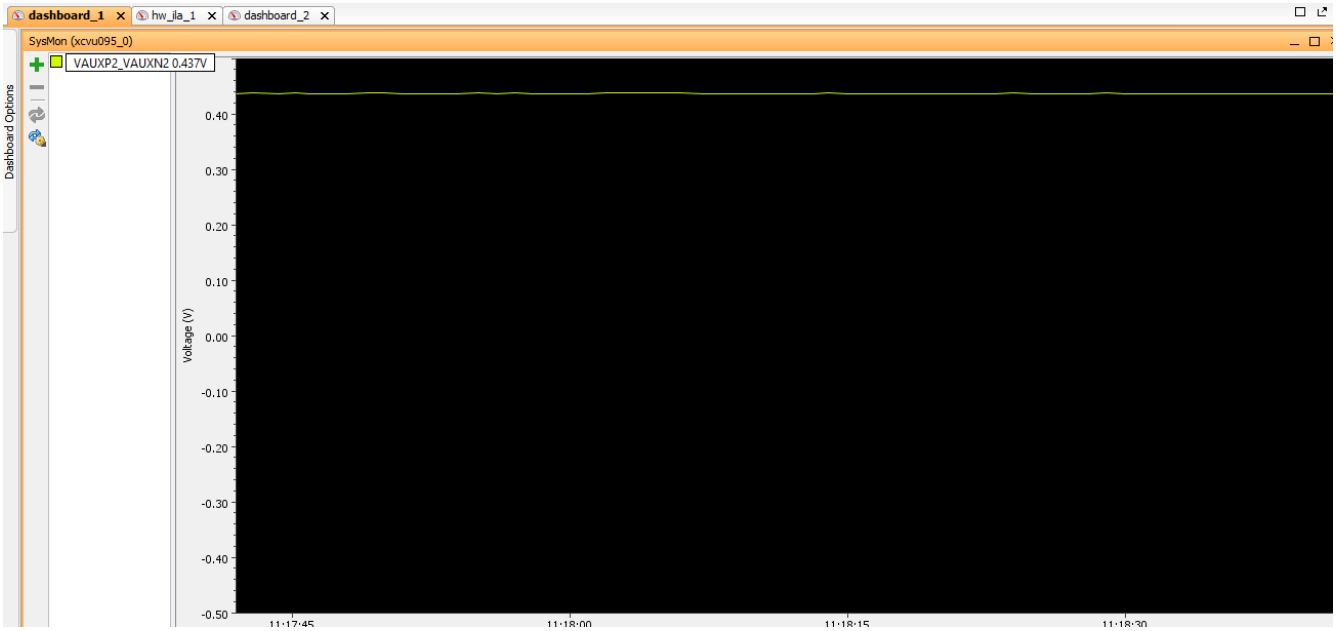
SYSMON: MGTAVCC_FPGA ADC (8-to-1 MUX U75, ADDR[2:0] = 110):

ADC conversion to currents:

$I = (ADC/2^{16})$ [V] x (17/0.93) [A/V]

I = (28684/65536) x (17/0.93) = 8 [A]



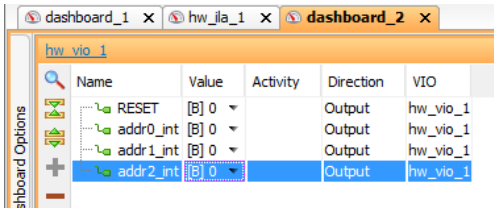


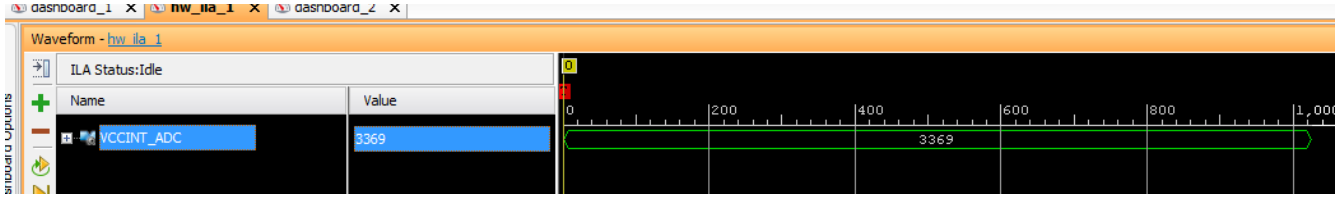
SYSMON: VCCINT_FPGA ADC (8-to-1 MUX U75, ADDR[2:0] = 000):

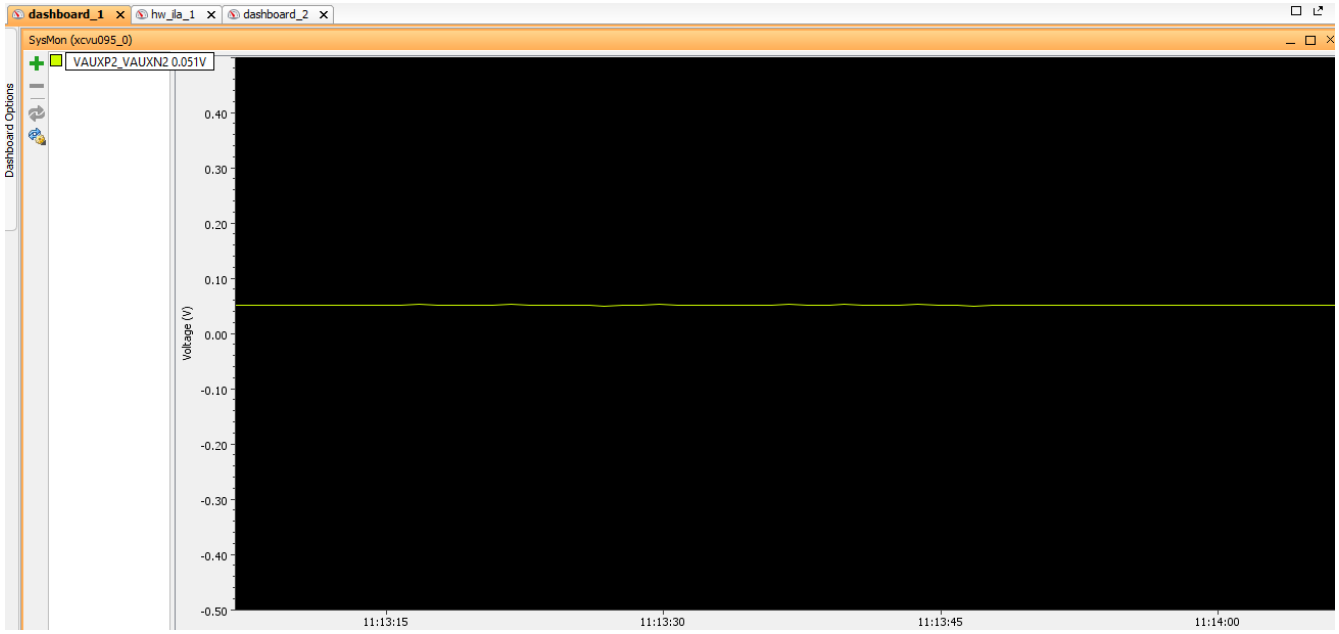
ADC conversion to currents:

$I = (ADC/2^{16})$ [V] x (60/0.9) [A/V]

I = (3369/65536) x (60/0.9) = 3.42 [A]







SUMMARY:

	MGTAVTT	MGTAVCC	VCCINT
SYSTEM CONTROLLER	3.45 A	8.02 A	3.40A
SYSMON	3.39 A	8.00 A	3.42 A
XPA (VIVADO)	1.86 A	4.50 A	3.44 A

Table 2: Measured (System Controller, SYSMON) and estimated (XPA) currents for the MGTAVTT, MGTAVCC and VCCINT.

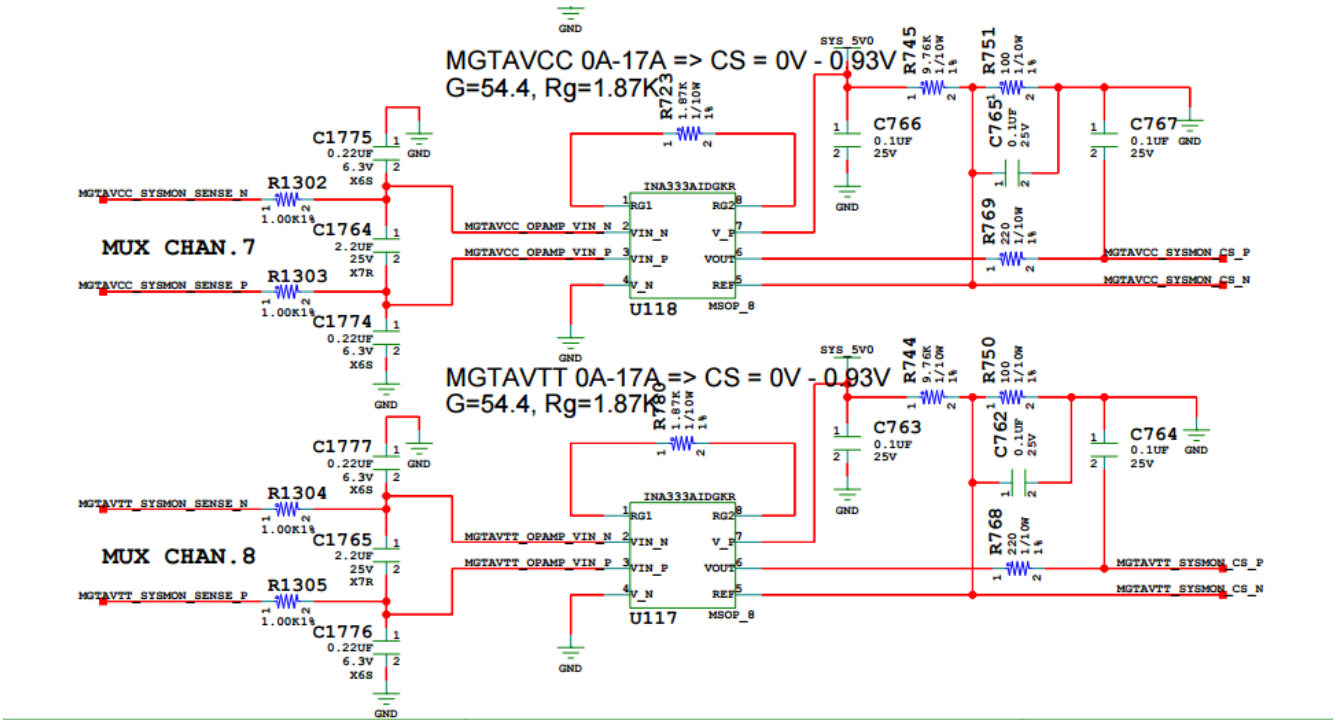


Figure 2: The scaling circuits; $G_{MGTAVTT}$ = (1 + 100kOhm)/R780 and $G_{MGTAVCC}$ = (1 + 100kOhm)/R723.

The collected results (Table 2) indicates that the origin of discrepancy is not related to the System Controller, because the measurement with the use of SYSMON provides the same results. Thus, the potential problem might be related to the scaling unit or the XPA estimator. I have checked (directly on the VCU108, rev: 1.0) that the resistance for R780 ad R723 is consistent with the documentation. Further examination is needed to fully eliminate the scaling as the potential problem.

In order to understand the origin of discrepancy, it's recommended to measure the output from U117 (amplifier, INA333) directly on board. Assuming the configuration_1 is being used in the test (GTH, 28 links @9.6 Gbps) and the XPA numbers are correct we should be able to monitor the output ca. 0.25V, and that corresponds to ca. 4.5A (MGTAVCC). If the measured output is higher ca. 0.43V (8 A) this would indicate the general issue with the XPA-Vivado estimator.