10/13/2016 by Pawel Plucinski Target: VCU108 (UltraScale)

#### Power Estimation (VCU108) - the update

### **INTRODUCTION**

The Power Estimation for the MGTAVTT, MGTAVCC and VCCINT was done with the use of System Controller (Embedded System @ZYNQ) on the VCU108. The results demonstrates high discrepancy compared to the XPE/XPA-Vivado. The custom design with the SYSMON is implemented to verify numbers found with the System Controller.

Presented results corresponds to the configuration\_1 (GTH, 28links @9.6 Gbps). The VCU108 board SYSMON ADC interface includes current measuring capability for all FPGA voltage rails. The rail current measurements are made available to SYSMON via an Analog Devices ADG707BRU multiplexer U75 (Figure 1-30 and Table 1 -37).

The design with the SYSMON allows to extract the raw ADC counts which after conversions corresponds to the measured currents and voltages. Table 1.37 summarizes the controlled rails.

#### RESULTS

#### **Power Estimation – System Controller:**

📒 COM4 - Tera Term VT	-	$\times$	
File Edit Setup Control Window Help			
Press Any Key to Return to SYSMON Menu		^	
Temperature = 38.31 C Min = 26.54 C Max = 38.78 C			
Power Voltage Current Current Current   UCCINT: 3.23 W 0.95 U 3.40 A 3.38 A 3.40 A   UCCIN8: 0.69 W 1.80 U 0.38 A 0.34 A 0.38 A   UADJ_108: 0.69 W 1.80 U 0.02 A 0.02 A 0.02 A   UCC102: 0.24 W 1.28 U 0.20 A 0.18 A 0.21 A   UCG102: 0.24 W 1.28 U 8.02 A 8.02 A 8.03 A   MGTAUCC: 8.02 W 1.20 U 3.45 A 3.45 A 3.46 A			
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#### **Power Estimation – Vivado (XPA):**

Implemented Design - impl_1   xcvu095-ffva2104-2-e (active)						
Power - power_1						
🔀 🖨 🗭 📑	Power Supply					
Settings   Summary (10.932 W)   Power Supply   Utilization Details   -Clocks (0.855 W)   -Clocks (0.855 W)   -Clocks (0.639 W)   -Clocks (0.639 W)   -Clock Enable (0.013 W)   -Set/Reset (0.031 W)   -Logic (0.505 W)   -BRAM (0.145 W)   -DSP (0.01 W)   -Clock Manager (0.114 W)	Supply Source Vccint Vccaux Vccaux_jo Vccau3 Vcca33 Vcco25 Vcco18 Vcco15 Vcco15 Vcco15 Vcco12 Vcco10 Vcco17 Vcco10 Vcco17 Vcco10 Vcco17 Vcco17 Vcco17 Vcco18	Voltage (V) 0.950 1.800 0.950 3.300 2.500 1.800 1.350 1.200 1.000 0.950	Total (A) 3.446 0.240 0.125 0.034 0.0000 0.0000 0.00000 0.00000 0.00000 0.00000 0.00000 0.00000 0.00000000	Dynamic (A) 3.040 0.063 0.001 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.00000 0.00000 0.0000	Static (A) 0.406 0.177 0.122 0.033 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000	
	MGTAVtt MGTVccaux Vccadc MGTYVccaux	1.200 1.800 1.800 1.800	1.860 0.094 0.014 0.000	1.788 0.094 0.000 0.000	0.072	
	MGTYAVcc MGTYAVtt	1.000	0.000	0.000	0.000	

## **Power Estimation – SYSMON:**



Figure 1-30: SYSMON External Multiplexer Block Diagram

Table 1-37: SYSMON Measurements through	MUX U75
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Controlled Dail	Regulator				ISENSE	Op An	np		8-to-1	MUX	U75								
Name	Reference Descriptor	Type	V <sub>OUT</sub>	Range	Reference Designator	Gain	V <sub>O</sub> Range	Schematic Net Name	Pin Number	Pin Name	A[2:0]								
		v	0.95V	N/A	1	N/A		N/A SYSMON or MAXIM GU		SYSMON or MAXIM GUI		N/A							
VCCINT_FPGA	U164			0.000			0.11	VCCINT_SYSMON_CS_P	19	S1A									
		1	N/A	0-00A	074	15	0-10	VCCINT_SYSMON_CS_N	11	S1B	000								
		v	1.80V	N/A	1	N/A	MAXIM GUI ONLY			N/A									
VCC1V8_FPGA	U9			0.100				VCC1V8_SYSMON_CS_P	22	S4A									
		1	N/A	0-10A	0116	20	0-10	VCC1V8_SYSMON_CS_N	8	S4B	011								
		v	1.80V	N/A	1	N/A		MAXIM GUI ONLY		N/A									
VADJ_1V8_FPGA	U30			0.100		20	20	20	2	20	20	20	20	0.11		VADJ_1V8_SYSMON_CS_P	23	S5A	
		1	N/A	0-10A	104 0119		0113		0-10	VADJ_1V8_SYSMON_CS_N	7	S58	100						
		v	1.20V	N/A	1	N/A		MAXIM GUI ONLY N		N/A									
VCC1V2_FPGA	U4			0.101	0.101	11120 20		0.11	VCC1V2_SYSMON_CS_P	24	S6A								
		1	N/A	0-104 0120		20	0-1V	VCC1V2_SYSMON_CS_N	6	S6B	101								
		v	1.00V	N/A	1	N/A		SYSMON AD0 or MAXIM GUI		N/A									
MGTAVCC_FPGA	U166			0.174			0.11	MGTAVCC_SYSMON_CS_P	25	S7A									
		1 N/A 0-17A 0118 54.4 0-1	54.4 0-1V	54.4 0-1V	MGTAVCC_SYSMON_CS_N	5	S7B	110											
		v	1.20V	N/A	1	N/A		SYSMON AD8 or MAXIM GUI		N/A									
MGTAVTT_FPGA	U165			0.174	11117		0.11	MGTAVTT_SYSMON_CS_P	26	S8A									
		1	N/A	0-1/A	011/	54.4	0-10	MGTAVTT_SYSMON_CS_N	4	S8B	111								

## SYSMON: MGTAVTT\_FPGA ADC (8-to-1 MUX U75, ADDR[2:0] = 111):

ADC conversion to currents:

 $I = (ADC/2^{16}) [V] x (17/0.93) [A/V]$ 

 $I = (12183/65536) \times (17/0.93) = 3.39 [A]$ 

6	) dasł	hboard_1 × 📧	hw_ila_1	🗙 🔊 di	ashboard_2	×
	hw	<u>vio 1</u>				
	٩,	Name	Value	Activity	Direction	VIO
and a share	X (金) + -	ն RESET Դա addr0_int Դա addr1_int Դա addr2_int	[B] 0 ▼ [B] 1 ▼ [B] 1 ▼ [B] 1 ▼		Output Output Output Output	hw_vio_1 hw_vio_1 hw_vio_1 hw_vio_1





# SYSMON: MGTAVCC\_FPGA ADC (8-to-1 MUX U75, ADDR[2:0] = 110):

ADC conversion to currents:

 $I = (ADC/2^{16}) [V] \times (17/0.93) [A/V]$ 

 $I = (28684/65536) \times (17/0.93) = 8 [A]$ 

8	dasł	nboard_1 🗙 🚳	hw_ila_1	🗙 🕥 d	ashboard_2	×
	hw	<u>vio 1</u>				
	٩,	Name	Value	Activity	Direction	VIO
2	$\mathbf{Z}$	ESET	[B] 0 🔻		Output	hw_vio_1
Ę.		ે ા addr0_int	[B] 0 🔹		Output	hw_vio_1
ŏ	7	ખ∿⊜ addr1_int	[B] 1 🔻		Output	hw_vio_1
ard	<b>*</b>	്… പം addr2_int	[B] 1 🔻		Output	hw_vio_1
oque	-					

6	S dashboard_1 x S hw_ila_1 x S dashboard_2 x								
	Wav	eform - <u>hw_ila_1</u>							
	₹	ILA Status:Idle		0					
ions	+	Name	Value		200	400	600	800	1,000
board Opt	-	MGTAVCC_ADC	28684			28684			



ADC conversion to currents:

 $I = (ADC/2^{16}) [V] \times (60/0.9) [A/V]$ 

 $I = (3369/65536) \times (60/0.9) = 3.42 [A]$ 

💿 da:	shboard_1 🗙 🏾 🕿	hw_ila_1	🛛 🗙 🕥 da	ashboard_3	2 X
hw	vio 1				
٩	Name	Value	Activity	Direction	VIO
oard Options	الله RESET مع addr0_int مع addr1_int مطdr2_int	[B] 0 ▼ [B] 0 ▼ [B] 0 ▼ [B] 0 ▼		Output Output Output Output	hw_vio_1 hw_vio_1 hw_vio_1 hw_vio_1





**SUMMARY:** 

	MGTAVTT	MGTAVCC	VCCINT
SYSTEM CONTROLLER	3.45 A	8.02 A	3.40A
SYSMON	3.39 A	8.00 A	3.42 A
XPA (VIVADO)	1.86 A	4.50 A	3.44 A

Table 2: Measured (System Controller, SYSMON) and estimated (XPA) currents for the MGTAVTT, MGTAVCC and VCCINT.



Figure 2: The scaling circuits;  $G_{MGTAVTT} = (1 + 100 \text{kOhm})/\text{R780}$  and  $G_{MGTAVCC} = (1 + 100 \text{kOhm})/\text{R723}$ .

The collected results (Table 2) indicates that the origin of discrepancy is not related to the System Controller, because the measurement with the use of SYSMON provides the same results. Thus, the potential problem might be related to the scaling unit or the XPA estimator. I have checked (directly on the VCU108, rev: 1.0) that the resistance for R780 ad R723 is consistent with the documentation. Further examination is needed to fully eliminate the scaling as the potential problem.

In order to understand the origin of discrepancy, it's recommended to measure the output from U117 (amplifier, INA333) directly on board. Assuming the configuration\_1 is being used in the test (GTH, 28 links @9.6 Gbps) and the XPA numbers are correct we should be able to monitor the output ca. 0.25V, and that corresponds to ca. 4.5A (MGTAVCC). If the measured output is higher ca. 0.43V (8 A) this would indicate the general issue with the XPA-Vivado estimator.