Spirent Communications

Performance Analysis Broadband Division -
Honolulu Development Center

PCB CAD Design Guidelines

Document 001-7001-001

Rev. A
18-Oct-02

Revision History

Revision	Description of Change	ECO
A	Initial Release	E03640-12

Miscellaneous Notes

1) Companies used to create these guidelines:

   TTM Technologies
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   Santa Ana, California 92704

   Velie Circuits
   Contact: Stuart Froman - (714) 751-4994; sfroman@velie.com
   1267 Logan Avenue
   Costa Mesa, California 92626

   Multek
   Contact: Tony DeSmet - (949) 609-7288; tony.desmet@multek.com
   40 Parker
   Irvine, California 92618

   Dynamic Details, Inc.
   Contact: Terry Talley - (714) 390-1700; ttalley@ah.ddiglobal.com or terrytal@pacbell.net
   1220 Simon Circle
   Anaheim, California 92806

   VIASYSTEMS Portland, Inc.
   Contact: Rey Sosa - (503) 672-4324; rey.sosa@viasystems.com
   9825 SW Sunshine Court
   Beaverton, Oregon 97005

   Fine Pitch
   Contact: Lawrence Lu - (408) 894-8393
   2265 Junction Avenue
   San Jose, California 95131

2) All dimensions given in this document are in inches unless otherwise specified.

3) "Standard" indicates the design guidelines in which all the current PCB manufacturers can build to; no additional costs should be encountered.

4) "Advanced" indicates the design guidelines in which only one or more PCB manufacturers have indicated the ability to meet. Additional cost, risk, and yield issues are associated with these figures. The trade-offs should be carefully weighed before pursuing this option.

5) This document is a snapshot of our current PCB manufacturer's and assembly houses' capabilities. It is generally agreed upon that technology moves too quickly to guarantee that all the recommendations given here are current. If there are any doubts, please feel free to contact the CAD department, PCB manufacturer, or assembly house to make sure before proceeding. There may not have been enough time to update this document with the new figures.

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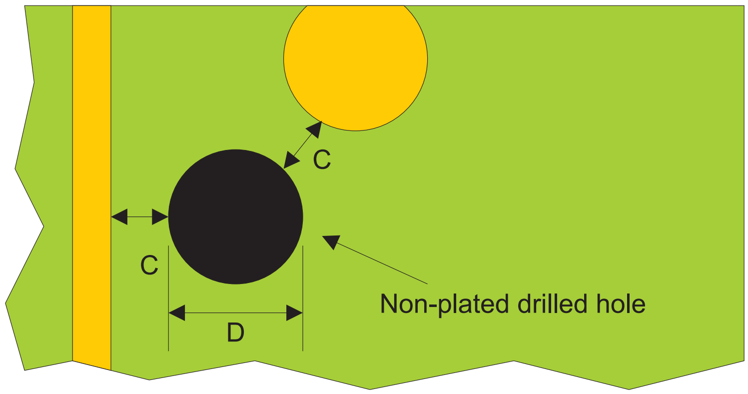
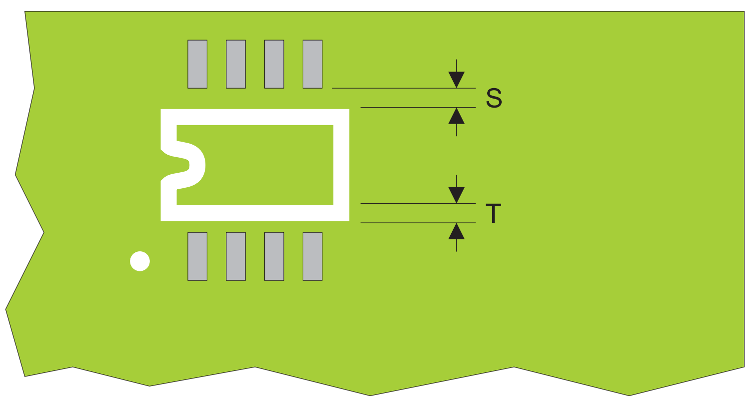
Non-Plated Holes



	Parameter	Standard	Advanced
C	Drill Hole Clearance	0.008	
D	Mechanically Drilled Hole (min.)	0.012	0.006 (*)

(*) Velie Circuits

Silkscreen/Legend



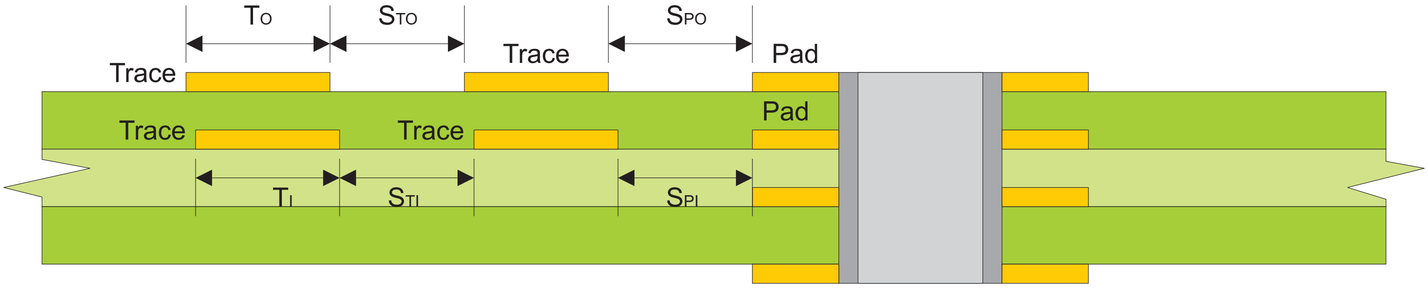
	Parameter	Standard	Advanced
T	Minimum Stroke Width	0.006	0.005 (**)
S	Minimum Spacing to Copper Pad	0.006	0.006
	Standard Colors	White or Yellow	N/A

Legends that violate the 0.006" clearance to copper pad will be clipped to provide the required clearance.

Below 6 mils, readability may become an issue; 10 mils was said to be the norm. 40 mils is usually considered to be the smallest, readable height for characters.

(**) Multek

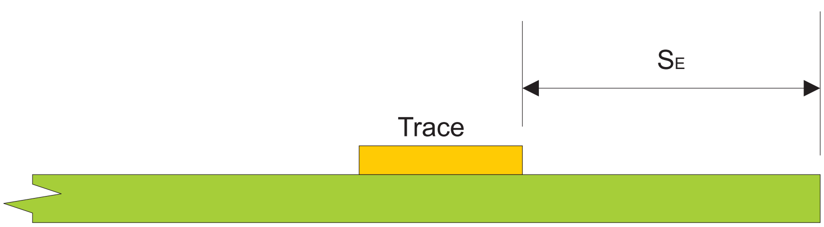
Trace Width and Spacing



	Parameter	Standard	Advanced
T_O	Trace Width (Outer Layer)	0.005	0.002 (*)
S_{TO}	Space Between Traces	0.005	0.002 (*)
S_{PO}	Space Between Trace and Pad	0.005	0.003 (*)
T_I	Trace Width (Inner Layer)	0.004	0.002 (*)
S_{TO}	Space Between Traces	0.004	0.002 (*)
S_{PO}	Space Between Trace and Pad	0.004	0.003 (*)

(*) Dynamic Details, Inc.

Trace to Board Edge

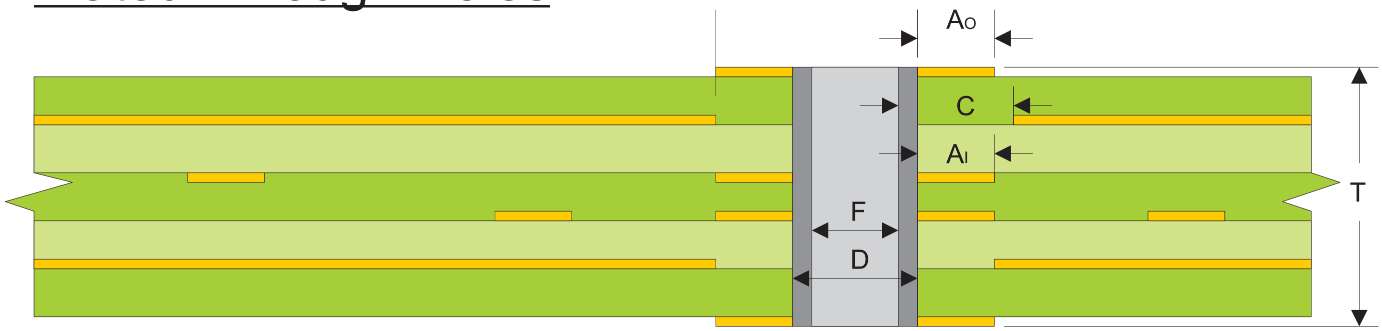


	Parameter	Standard	Advanced
S_E	Trace to Edge Spacing	0.010	0.006 (**)

(**) Velie Circuits

NOTE: If the PCB edge is to be de-tabbed or V-Scored, traces should be a minimum of 0.050" away from the edge. This is an assembly issue, not a PCB manufacturing issue.

Plated Through Holes

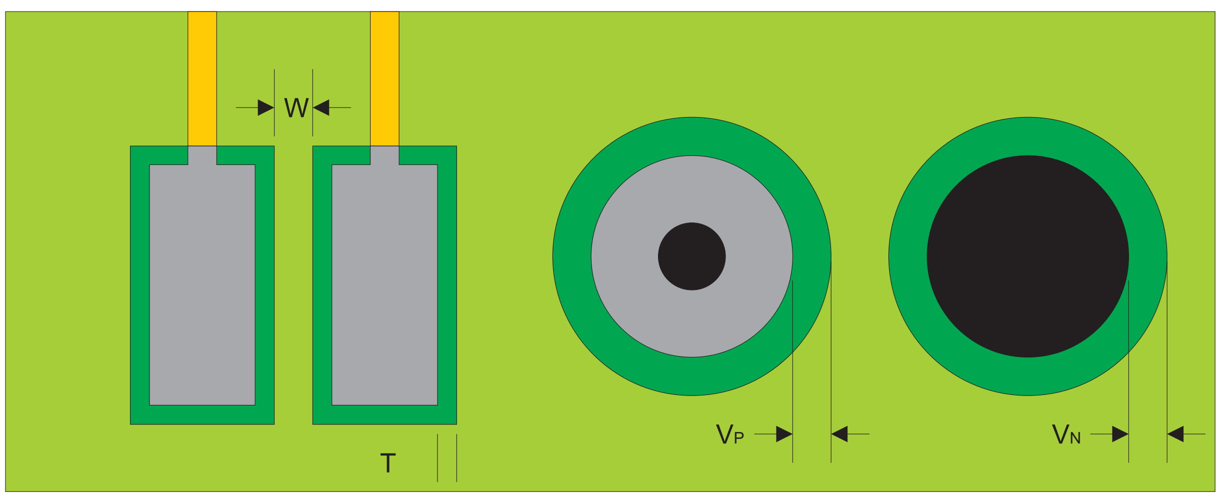


	Parameter	Standard	Advanced
T	Board Thickness (max.)	0.093	0.300 (*)
D	Min. Drill Hole Diameter	0.012	0.006 (**)
F	Min. Finish Hole Diameter	0.008	0.004 (**)
A_O	Min. Outer Layer Annular Ring	0.006	0.005 (*)
A_I	Min. Inner Layer Annular Ring	0.005	0.004 (***)
C	Clearance, Drill to Plane[1]	0.015	0.011 (**)
T/D	Max. Aspect Ratio	10:1	12:1
	Diameter Tolerance[2]	+/- 0.003	+/- 0.002 (***)
	Location Tolerance	+/- 0.005	+/- 0.003 (**)

(1) Plane clearance is normally specified as (pad diameter + XX mils; XX = 0.018" to 0.016") or (Drill diameter + YY mils; YY = 0.010"). The Clearance number was arrived at by adding 3 mil finish tolerance (can vary between 0.004 to 0.006) to the Inner Layer Annular Ring dimension and 5 mil (min) clearance between pad and plane.

(2) Diameter Tolerance is normally +/- 3 mils for 12 mil diameter holes or larger; +0/-10 mils for smaller holes.

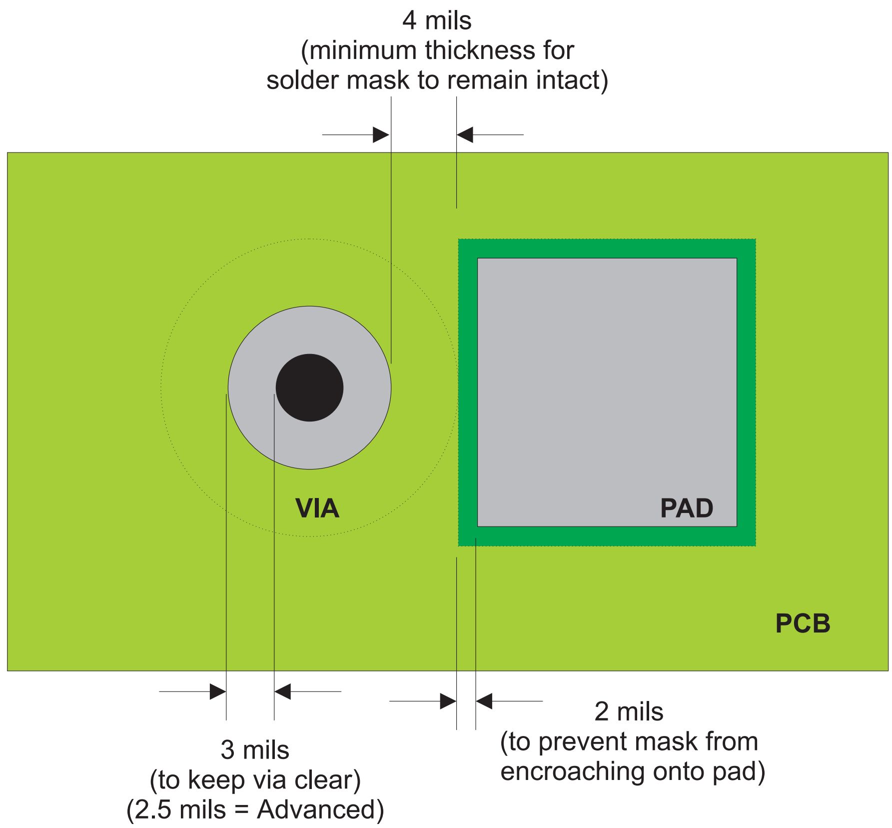
Solder Mask



	Parameter	Standard	Advanced
T	Registration Tolerance	0.003	0.002 (***)
W	Minimum Webbing	0.004	0.003 (***)
V_P	Via Clearance (PTH)	0.003	0.002 (***)
V_N	Hole Clearance (Non-PTH)	0.005	0.004 (***)

(*) Dynamic Details, Inc.
(**) Velie Circuits
(***) Multek

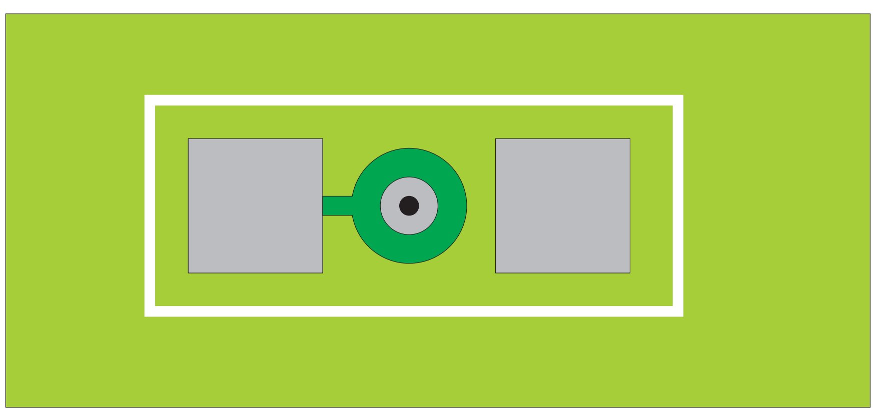
Encroachment of Solder Mask onto Via



Secondary Side

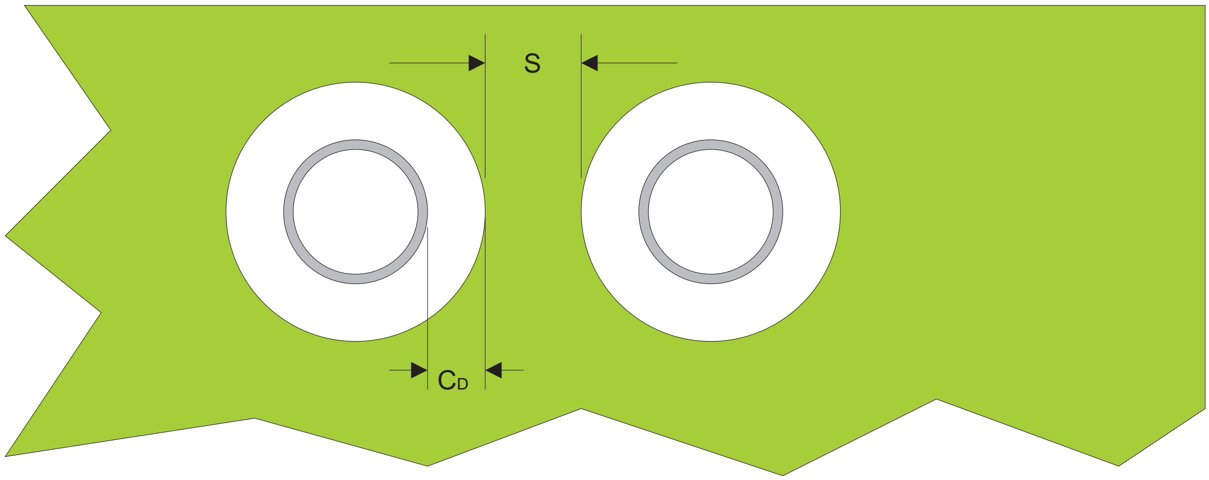
The distance between pad and via must be at least 25 mils to prevent bridging. The secondary side has the possibility of going through the wave so has a much greater restriction than the primary side (which will be reflowed).

Bad Idea



Placing a via in between pads of a component increases the chance of a solder bridge between the pad and via. Because the bridge will be hidden under the component after assembly, it could be difficult to inspect, find, and correct.

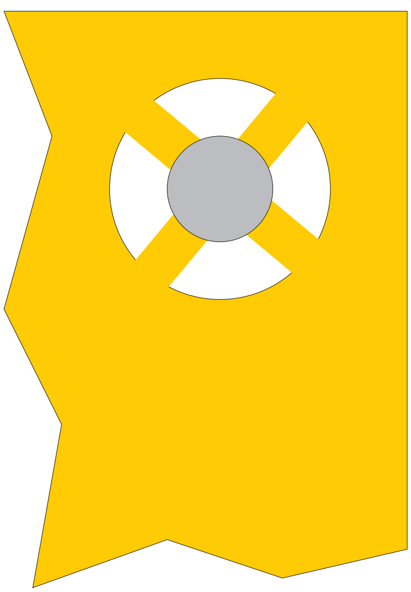
Anti-Pad/Plane Relief



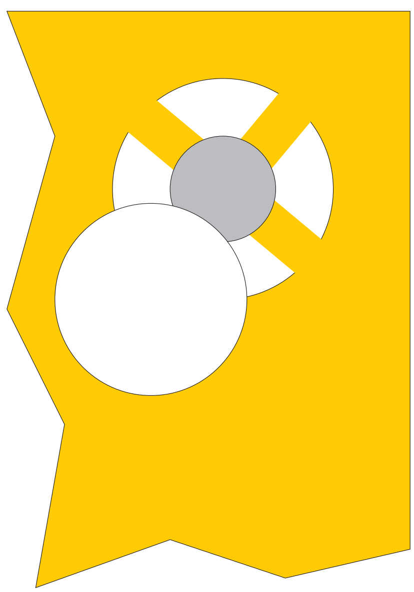
	Parameter	Standard	Advanced
C_D	Plane Relief (no pad)	0.010	0.007 (*)
S	Plane Clearance	0.005	0.005

(*) TTM Technologies

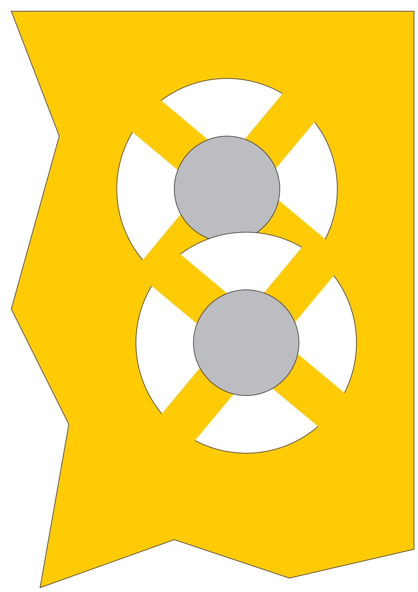
Thermals (Isotherms)



Preferred - Unhampered thermal making four connections with the plane layer.



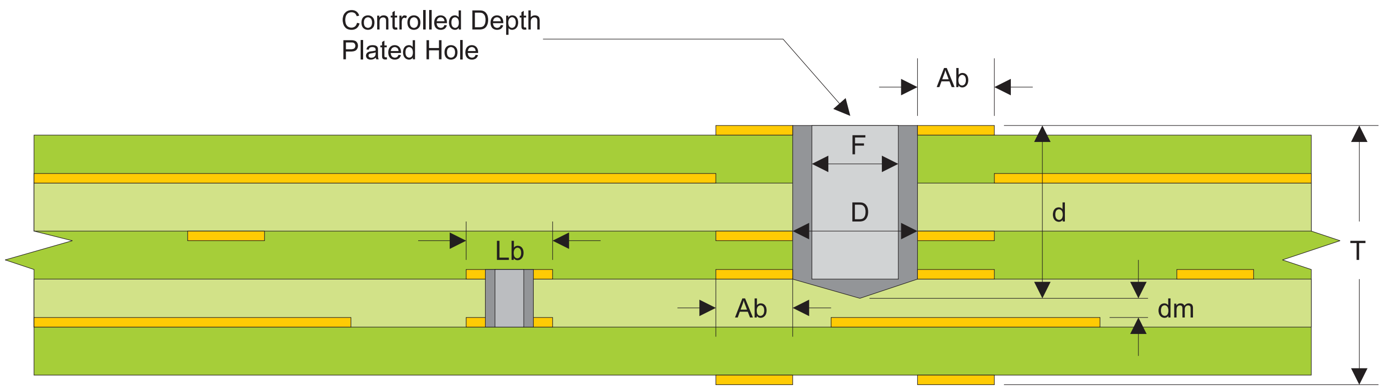
Avoid - Thermal overlapping a plane clearance and creating an annular ring problem. This design has the potential for increased fallout and reduced reliability.



Avoid - Overlapping thermals creating an annular ring violation. This design has a potential for increased fallout and reduced reliability.

Mechanical Blind and Buried Vias

Advanced Option (does not apply to Velie)

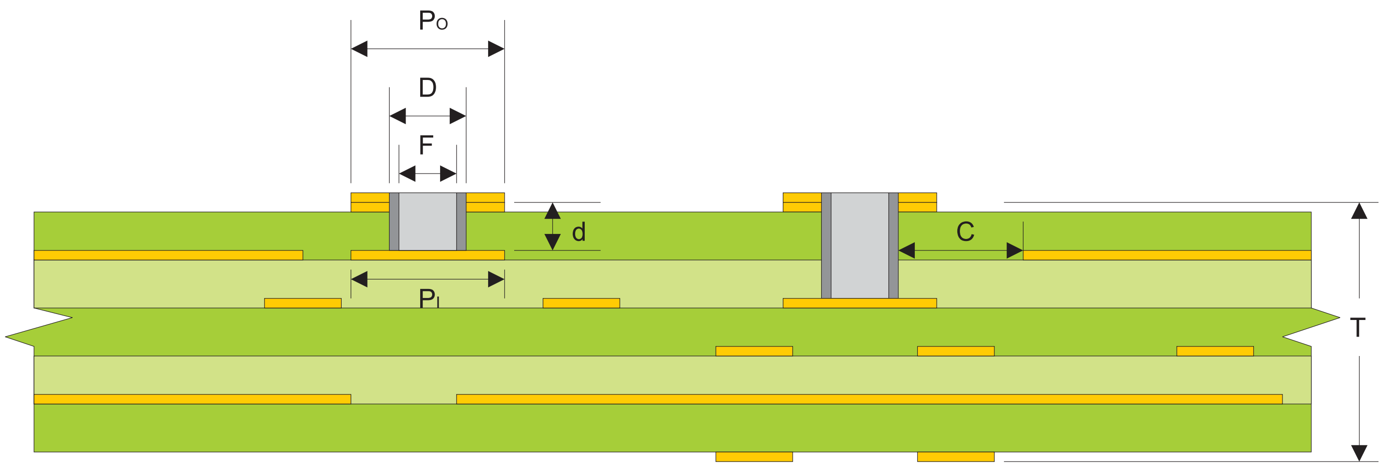


	Parameter	Standard	Advanced
T	Board Thickness (max.)	0.020-0.200	0.020-0.250
D	Min. Blind/Buried Via Drill	0.010	0.006
F	Blind/Buried Finished Diameter	0.008	0.004
d	Controlled Depth	AR Dependent	AR Dependent
dm	Controlled Depth Margin	0.005	0.005
AR	Blind AR = d/D (max.)	0.5	0.75
Ab	Min. Blind/Buried Annular Ring	0.005	0.004
Lb	Min. Blind/Buried Land	0.020	0.014

NOTE: AR = Aspect Ratio = Depth/Diameter

Laser Drilled Micro-Vias

Advanced Option (does not apply to Velie)



	Parameter	Standard	Advanced
D	Laser Drill Diameter	≥ 0.005	≥ 0.004
F	Finished Hole Diameter	≤ 0.004	≤ 0.003
d	Controlled Depth	AR Dependent	AR Dependent
P_O	Pad Diameter (Outer Layer)	D + 0.008	D + 0.004
P_I	Pad Diameter (Inner Layer)	D + 0.006	D + 0.004
C	Drill to Plane Clearance	0.010	0.006
AR	Blind AR = d/D (max.)	0.5	0.75
	Surface Copper Foil	1/4 oz. preferred	1/4 oz. preferred
	Surface Copper Plating	≥ 0.0005	≥ 0.0005
	Inner Layer Copper Foil	≥ 1/2 oz.	≥ 1/2 oz.

NOTE 1: AR = Aspect Ratio = Depth/Diameter

NOTE 2: By definition, a micro-via is a hole 6 mils or less in diameter.
From: "Extremely Dense Designs & DFM" by James C. Blankenhorn, SMT Plus, Inc. Oct. 2001.

Via Plugging/Filling

Advanced Option

1. Holes to be plugged must be specified on the drill chart to prevent errors.

2. Component, Solder, or both sides can be plugged. Plugging is not recommended for covering both sides of the via on a board; use filled holes instead. Air or moisture could become trapped inside causing blow-out during assembly.

3. With holes < 15 mils, simply screening LPI over the via, the via will "tent." However, after assembly (thermal stress, washing, vibration, etc.), there is no guarantee that the tent will remain intact. PCB manufacturers recommend either plugging or filling the vias. Delamination of the solder mask may result. Additionally, PCB vendors indicated that chemicals could become trapped in the tented via causing reliability problems and corrosion later in time.

4. There are some differences in terminology. Some vendors say "plugged" to mean one or both sides of the hole are plugged with epoxy. Some make the distinction that "plugged" is where only one side of the via is covered with epoxy; whereas "filled" is where both sides of the via are covered with epoxy.

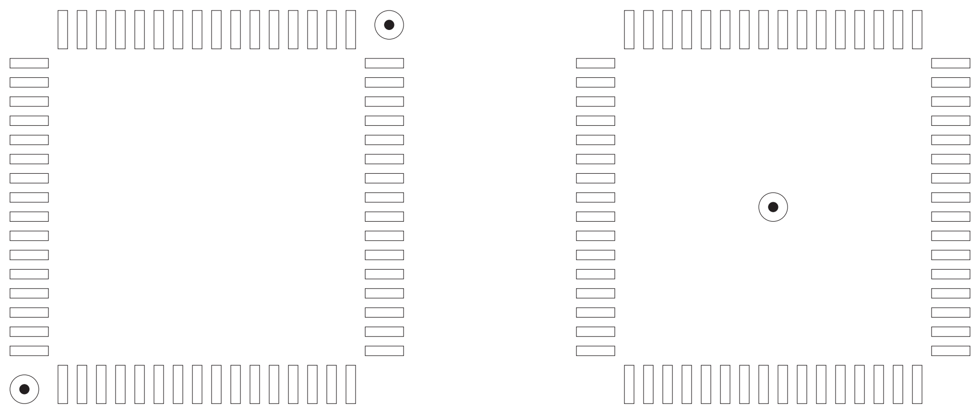
5. Plugged holes:
   a) Minimum hole diameter is 8 mils. The smaller the hole, the more difficult it is for the epoxy to flow into the hole.
   b) Maximum hole diameter is 20 mils. The larger the hole becomes, the more difficult it is to maintain 100% coverage.
   c) PCB vendors cannot guarantee that solder resist will not seep onto the other side of the board through the via. Therefore, this should not be used for covering the component side vias where access to the secondary side is required (as in ICT). Use filled vias with conductive epoxy for such applications.

6) Filled holes (an even more expensive option):
   a) Minimum hole diameter is 10 mils.
   b) Maximum hole diameter is 18 mils.
   c) Conductive or non-conductive epoxy can be used. Conductive epoxy can be used for areas requiring the component side to be covered but the solder side vias accessible for test points.

7) Possible alternatives to plugging is to use dry film to tent the vias on one side. Very few PCB manufacturers use dry film so it may be difficult to find such a manufacturer.
   NOTE: None of our current PCB manufacturers use dry film.

Fiducial Requirements

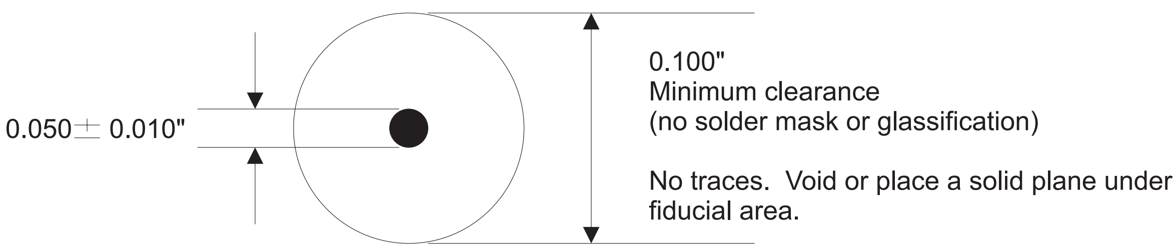
1. Local fiducials should be positioned in each fine pitch location to improve the placement accuracy of the device.



Preferred

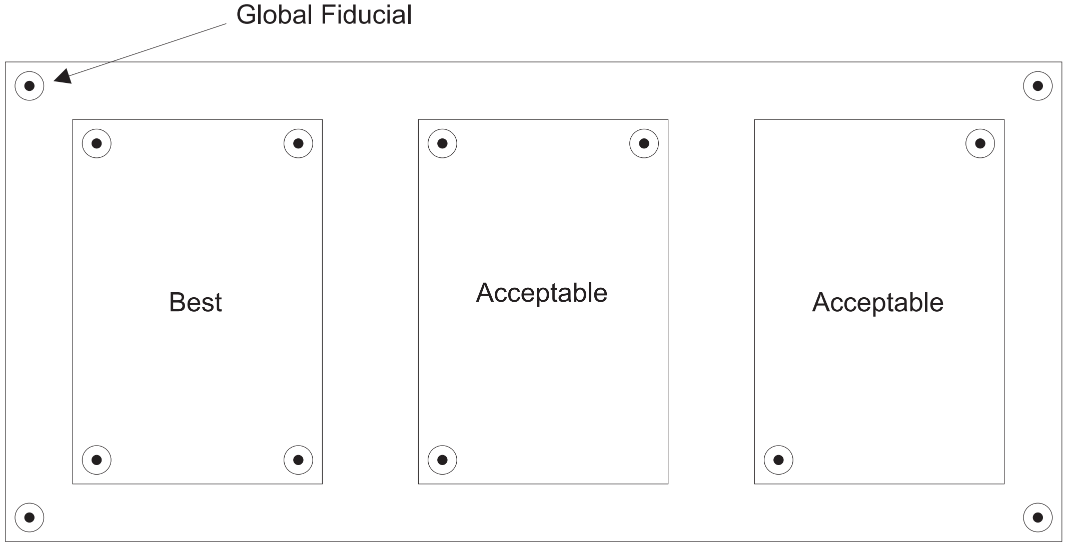
Acceptable

Recommended Fiducial Marking



2. Fiducials should be located in the corners of each image and in corners of the panel.
   Fiducials should be located as far apart as possible and should be in the same place on each axis.

   NOTE: When PCB's are panelized, PCB's should be centered in the "x" and "y" axis of the panel.



Tooling Holes

Two tooling holes per image within a PCB are needed for registration of the board for assembly processes and ICT test.

1. Recommended hole size is 0.125" +0.002"/-0.000"; 0.156" can also be used, if required. The hole should be non-plated.

2. The positional tolerance from tooling hole-to-tooling hole, center-to-center, should be +/-0.002".

3. The area over the tooling holes should be free of mechanical interference to a height of 1".

4. There must be a 125 mil annular ring free of components and test points around the tooling hole.

5. Tooling holes should be placed in diagonally opposite corners of the PCB.

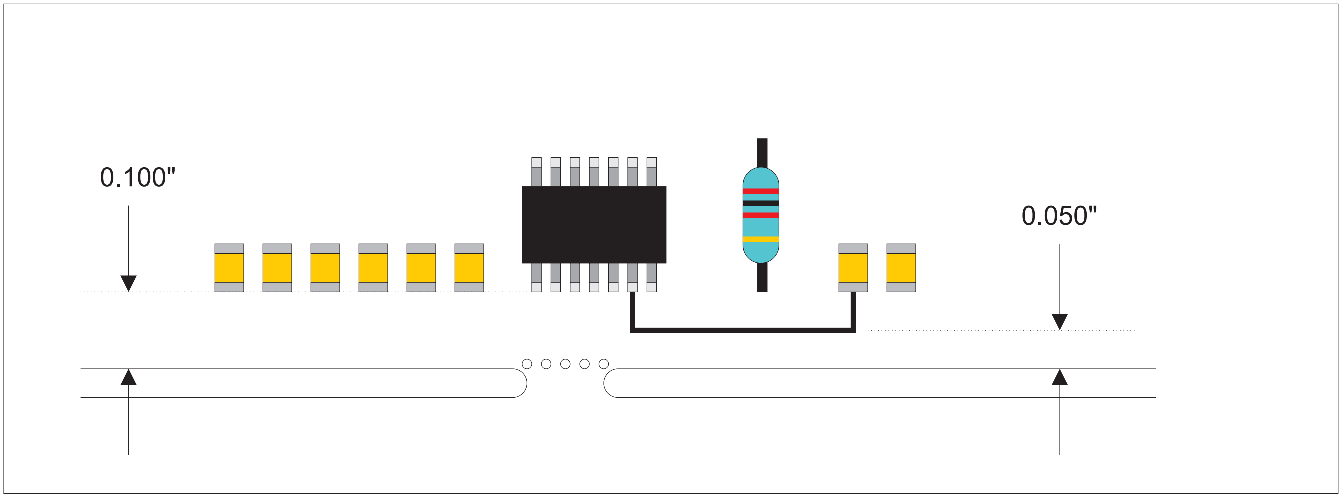
Depaneling/Tab Routing

Board assemblies can be de-tabbed using perforated breakaway tabs, v-grooves break away tabs, or hand-cutting with a de-tabbing tool.

For Tab and V-Score (i.e. PCB's that must be sheared along an edge):

1. Traces and vias should be a minimum of 0.050" away from routed/scored edge.
2. Components should be a minimum of 0.100" away from routed/scored edge.

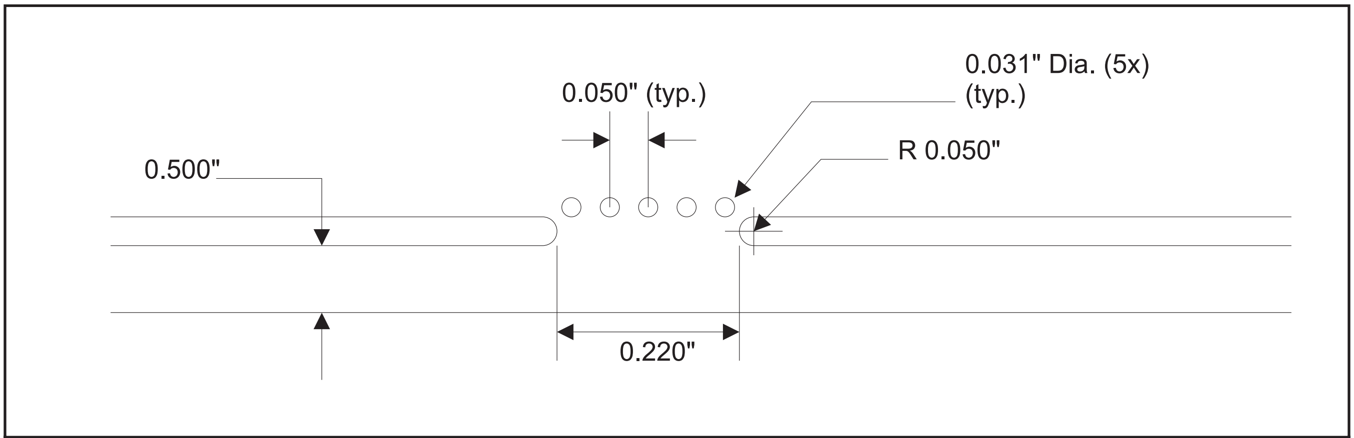
These rules are to help prevent components or board damage during the depaneling process and prevent flooding during the wave soldering process.

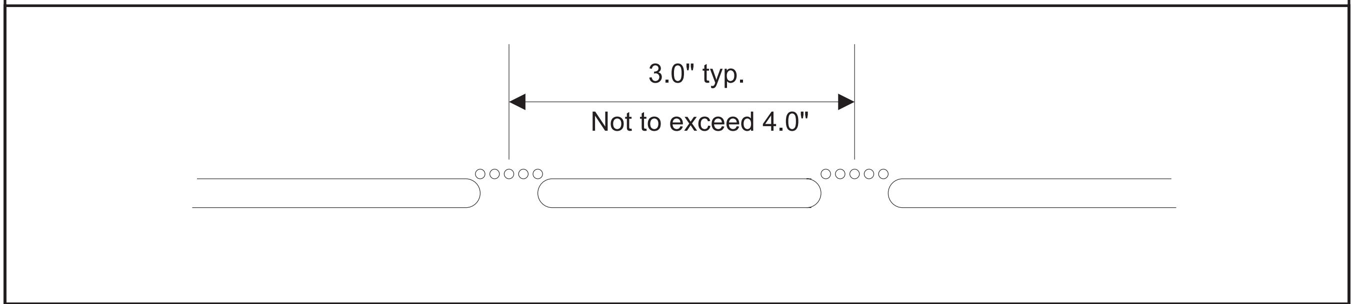


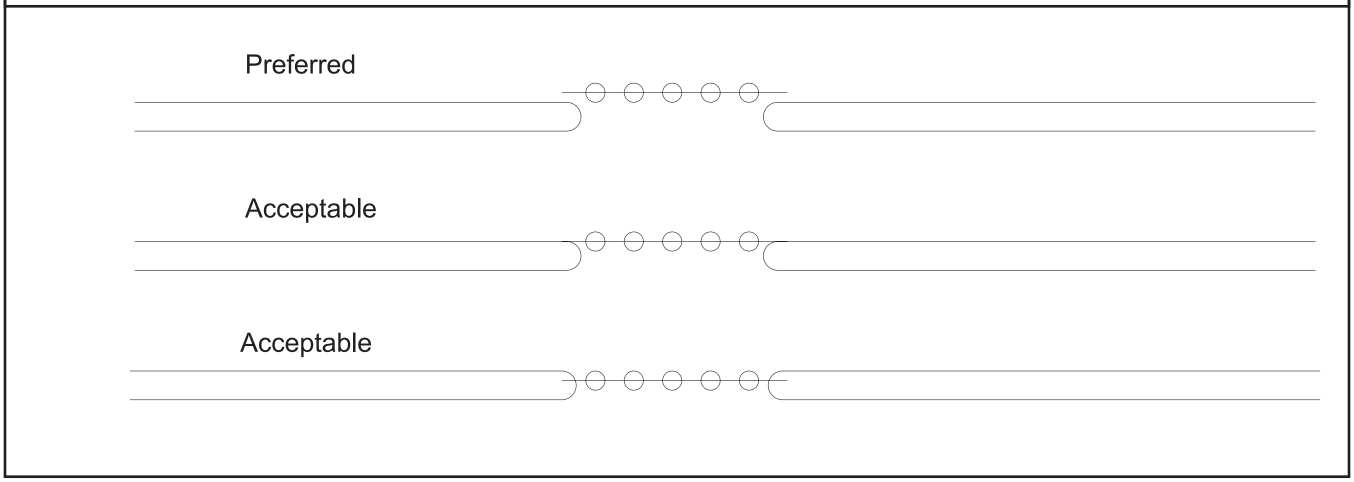
For 0.062" think (max.) Printed Circuit Boards:

1. Perforation holes should be typically spaced at 0.050" intervals.
2. Tab routed with 0.068 radius.
3. Routed slot should be 0.093" minimum, for single image panels. Use 0.125" routed slots when two or more boards are in a panel. This allows for more accurate edge dimensions.
4. 3.0" typical distance between tabs, not to exceed 4.0".
5. Place tabs approximately 1.00" from corners to reduce sagging during reflow or wave soldering.
6. Desirable to have at least one tab per side.
7. Slight inset of perforation is preferred; it provides an edge which requires little or no additional labor to clean up.

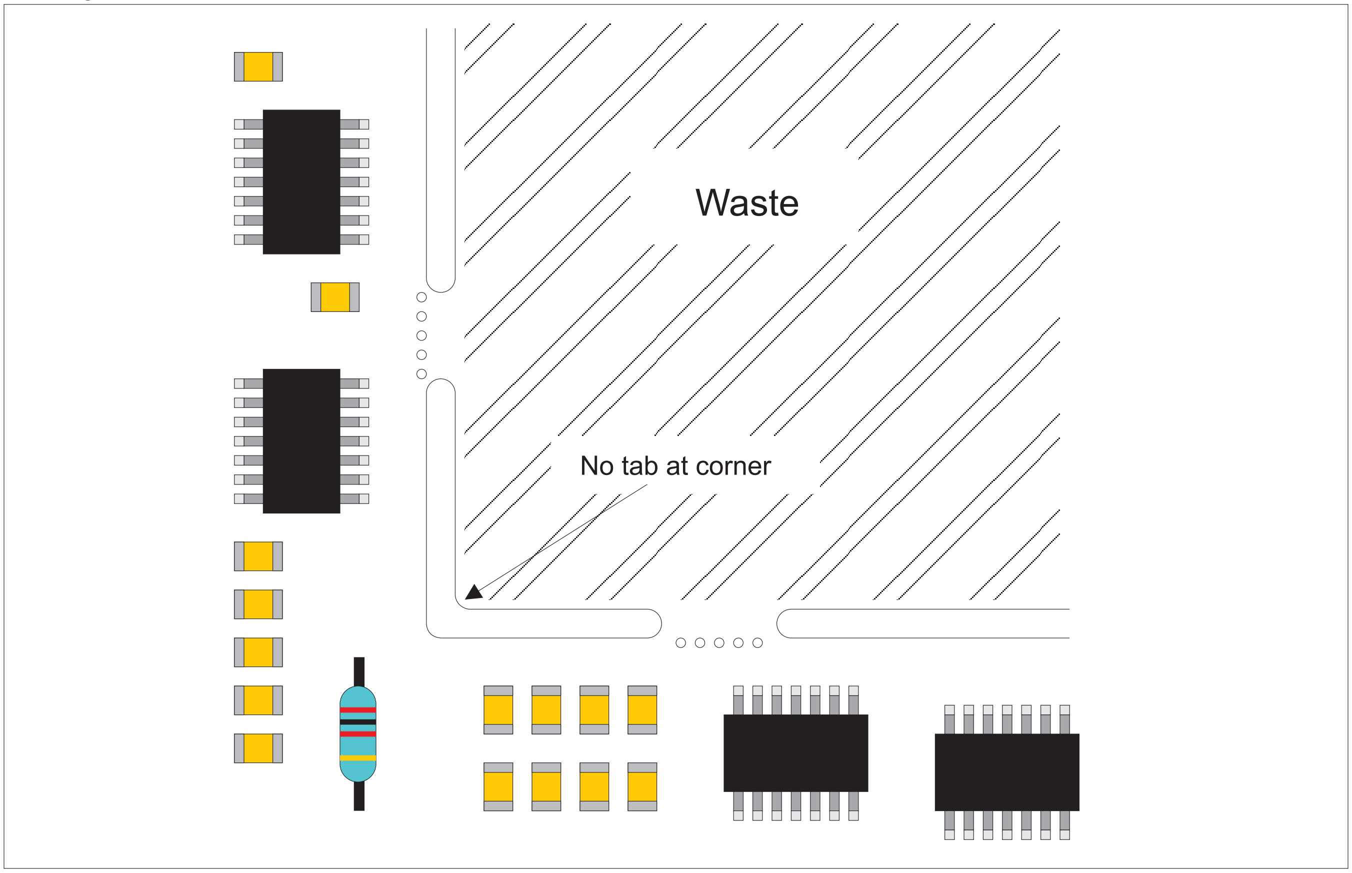
NOTE: Two parallel edges are required for a PCB to be processed in the SMT line. This is to prevent skewing through the conveyor system. **All odd shaped PCB's MUST have edge rails incorporated to meet this requirement. Custom reflow fixtures will be made if this requirement is not met.**





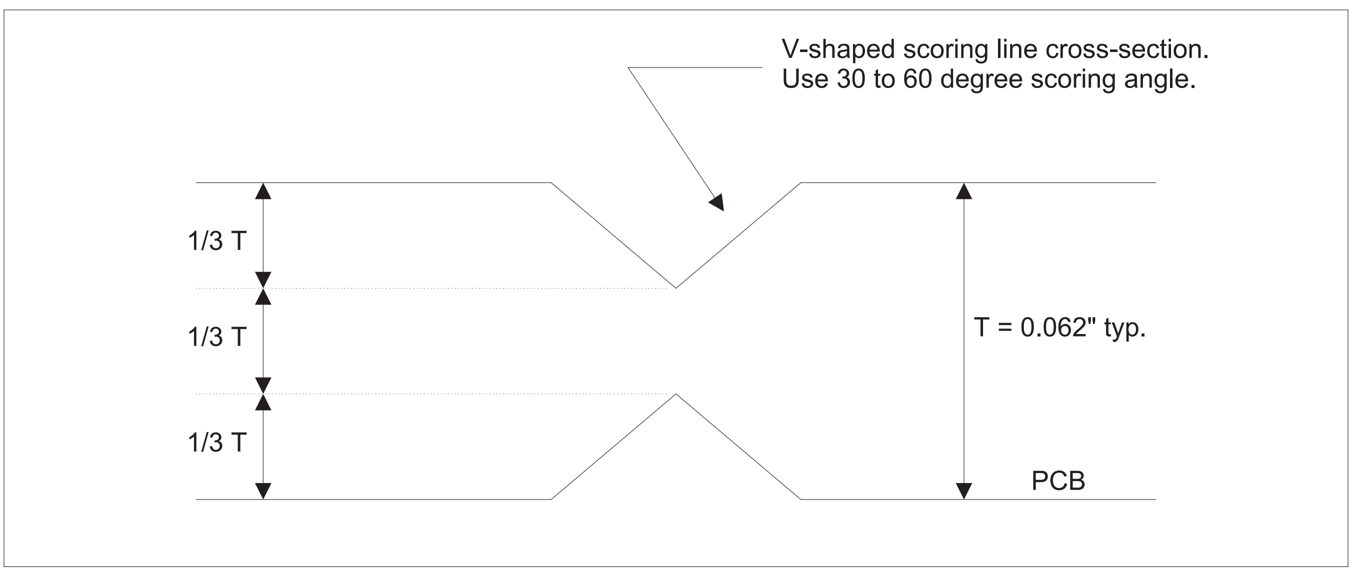


Routing to corners:



V-Score

All V-Score lines should follow the 1/3 rule illustrated in the diagram below.
NOTE: V-score cannot do 90 degree corners.



Test Points

Preferred:

ICT testing requirements

1. An area of 125 mils wide must be free of components and test pads around the edge of the board.
2. The test pad should be at least 40 mils in size; 75 mils is preferred.
3. The test pads should be no closer than 50 mils center-to-center; 100 mils is preferred. At 50 mils, there is an increase in false failures.
4. Test points should be on one side only. Two sides are possible but more expensive.
5. An 18 mil annulus free of components around each test pad is required.
6. A test point should be no closer than 25 mils (pad edge to center of via) from a via to prevent solder bridging.
7. Test points should be free of solder mask and ink.
8. Do not extend component pads to make test points. This may cause components to float.
9. 100% coverage for all nets on the design, including power, ground, and unused gates.
10. Fill through-holes with solder or solder resist; this is to provide a vacuum seal.

Less Than Ideal:

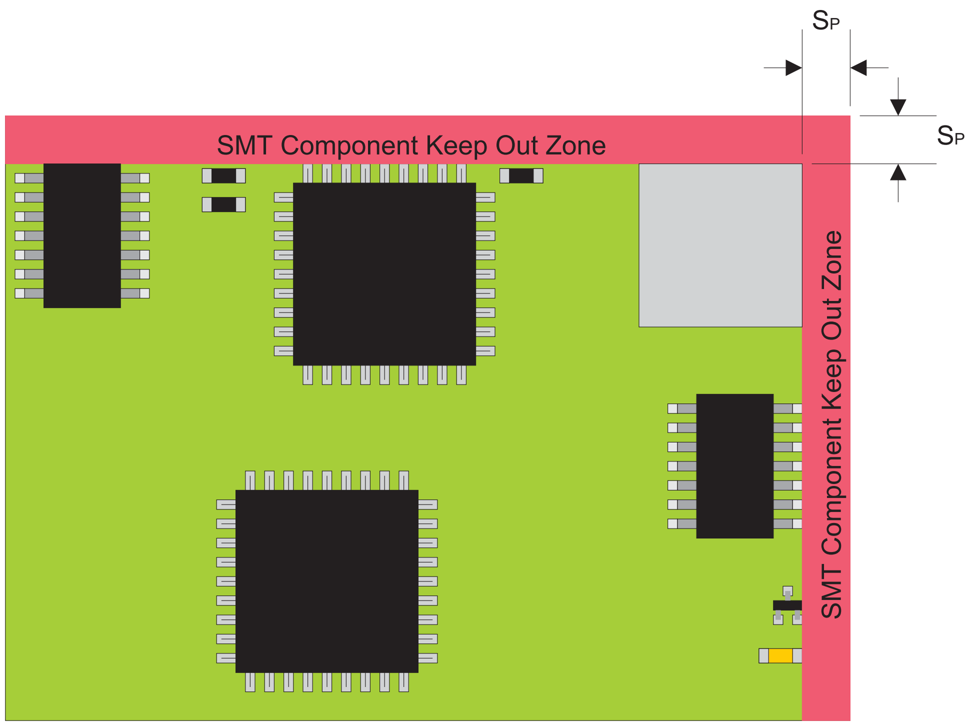
If ICT requirements cannot be accommodated, flying-probe test points should be attempted.

Caution: Flying-probe testing takes very long and is not for high volume modules or to be used on a production basis.

1. No component or test pad within 100 mils of the perimeter of the PCB.
2. Minimum size of the test pad is 28 mils. 20 is the lower limit before you start getting an increase in false failures. 10 mils is very unreliable and the assembly house should be contacted for a review of the locations.
3. Minimum pad spacing is 50 mils center-to-center (i.e. 25 mil spacing, pad edge-to-pad edge). This is to prevent bridging during wave soldering. If wave soldering will not be used, the minimum spacing is 40 mils (20 mil spacing between pads).
4. 18 mil annulus free of components around each test pad.
5. Test points should be free of solder mask and ink.
6. Do not extend component pads to make test points. This may cause the component to float.
7. 100% coverage for all nets is preferred, including power, ground, and unused gates. Engineering judgement should be used regarding which traces to verify (critical nets) if 100% coverage is not possible.

Parts Placement Rules

SMT Components to Edge



	Parameter	Standard	Advanced
S_P	Perimeter Component Keep-Out Zone (no components or test pads)	0.125	Negotiable (requires special fixtures)

Special Note: On the solder (secondary) side of the PCB, the long edge of the PCB must have a clearance of 0.300" on both sides. No SMT components should be placed there. Through-hole components that are to be hand-soldered or waved are okay.

The reason is that the solder screening machine has hold-downs which attach to the secondary side of the board to prevent the board from moving during the screening process. These hold-downs may damage any component in this area as the paste is screened onto the PCB.

SMT Component-to-Component Spacing

ALL DIMENSIONS IN TABLE OR IN MILS

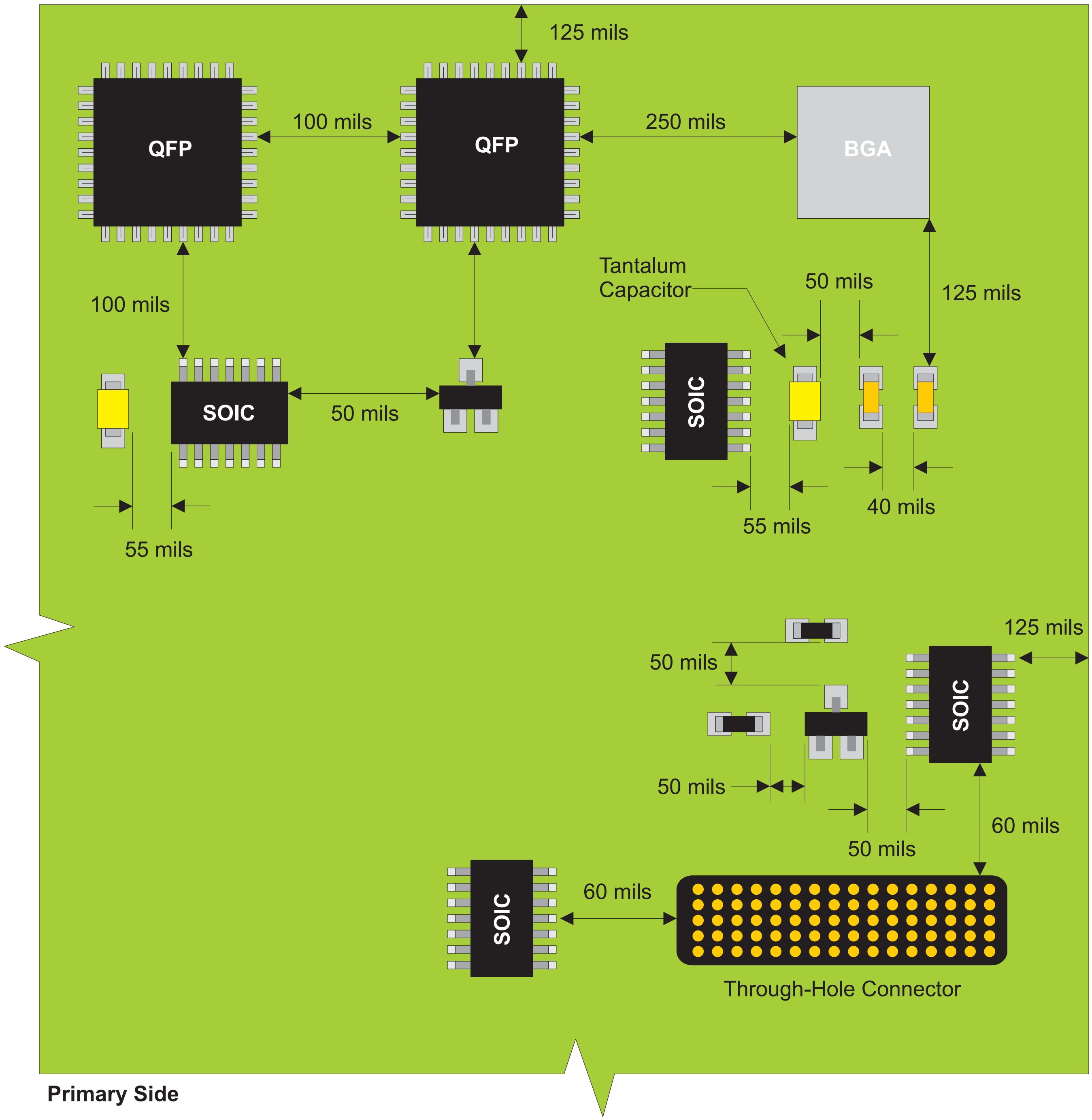
From \ To	Chip	Tantalum	SOIC	QFP/QFN	SOT23	PLCC	BGA	CSP	DIP*
Chip	40**	50	40	100	50	50	125	125	60
Tantalum	50	50	55	100	75	100	125	100	60
SOIC	40	55	50	100	50	100	125	125	60
QFP/QFN	100	100	100	100	100	100	250	250	100
SOT23	50	75	50	100	35	100	125	125	60
PLCC	50	100	100	100	100	100	125	125	60
BGA	125	125	125	250	125	125	250	250	125
CSP	125	100	125	250	125	125	250	100	125
DIP*	60	60	60	100	60	60	125	125	100

NOTE: Sockets (for PLCC and DIP) and connectors should be away from BGA and CSP components to prevent solder joint cracking due to possible stress exerted during second loading/removal of add-on cards or IC components.

(*) For primary side only. For secondary side, 0.125" clearance for all SMT components from DIP pins requiring selective wave solder fixture. Press fit connectors are an exception and do not require this clearance on the secondary side.

(**) Advanced Option - if absolutely necessary:
0402 components can be 20 mils apart.
0603 components can be 25 mils apart.
These numbers applies to Viasystems only and requires special setup on their side. Viasystems should be notified before the board is built.

SMT Component-to-Component Spacing Examples



NOTE: Distance is normally measured from pad edge-to-pad edge. However, in cases where the component's body exceeds the pad dimensions (e.g. tantalum capacitors), the distance is measured from the body edge to nearest feature (pad or component body).

Additional Secondary Side Restrictions

Component height restrictions on the secondary side of the board should be less than 0.120"; the preferred height is less than 0.090".

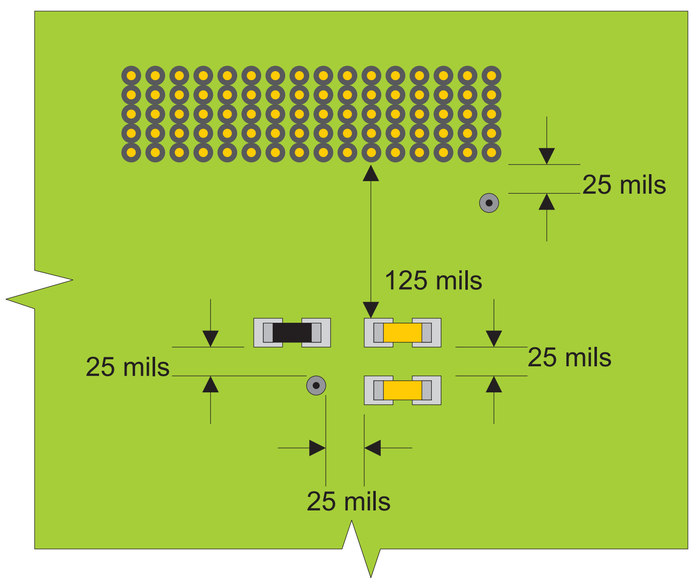
Components taller than 0.100" (e.g. tantalum capacitors or inductors) require 0.100" clearance (land-to-land) in all directions to prevent solder defects (skips and opens).

Minimum spacing of 0.025" between SMT components (land-to-land) is required in both directions to prevent bridging.

Minimum spacing of 0.025" land-to-annular ring (via or through-hole component) is required to prevent bridging.

Minimum spacing of 0.125" land-to-annular ring required between all SMT components and DIP pins requiring selective wave solder fixture. Press fit connectors are an exception and do not require this clearance on the secondary side.

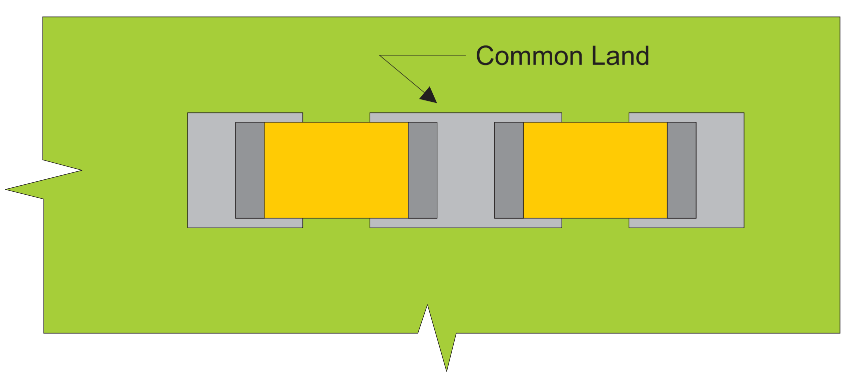
On the solder (secondary) side of the PCB, the long edge of the PCB must have a clearance of 0.300" on both sides. No SMT components should be placed there. Through-hole components that are to be hand-soldered or waved are okay.



Secondary Side

Bad Idea

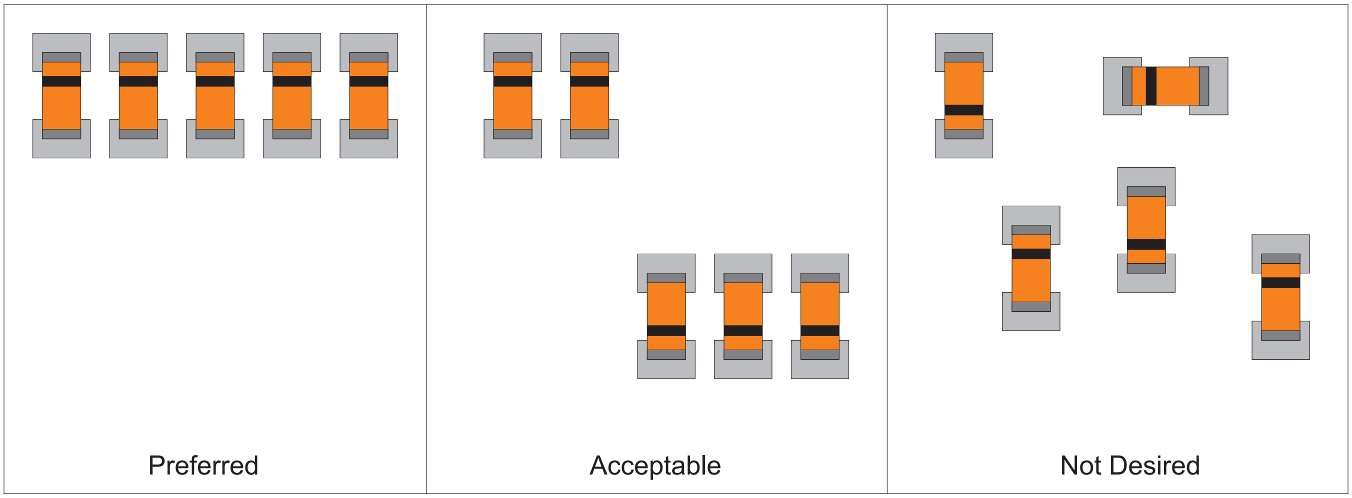
Only a single lead or termination should be placed on a land. Sharing a common land allows for one or both of the components to float during reflow. This causes unpredictable solder flow and part migration.



Component Orientation

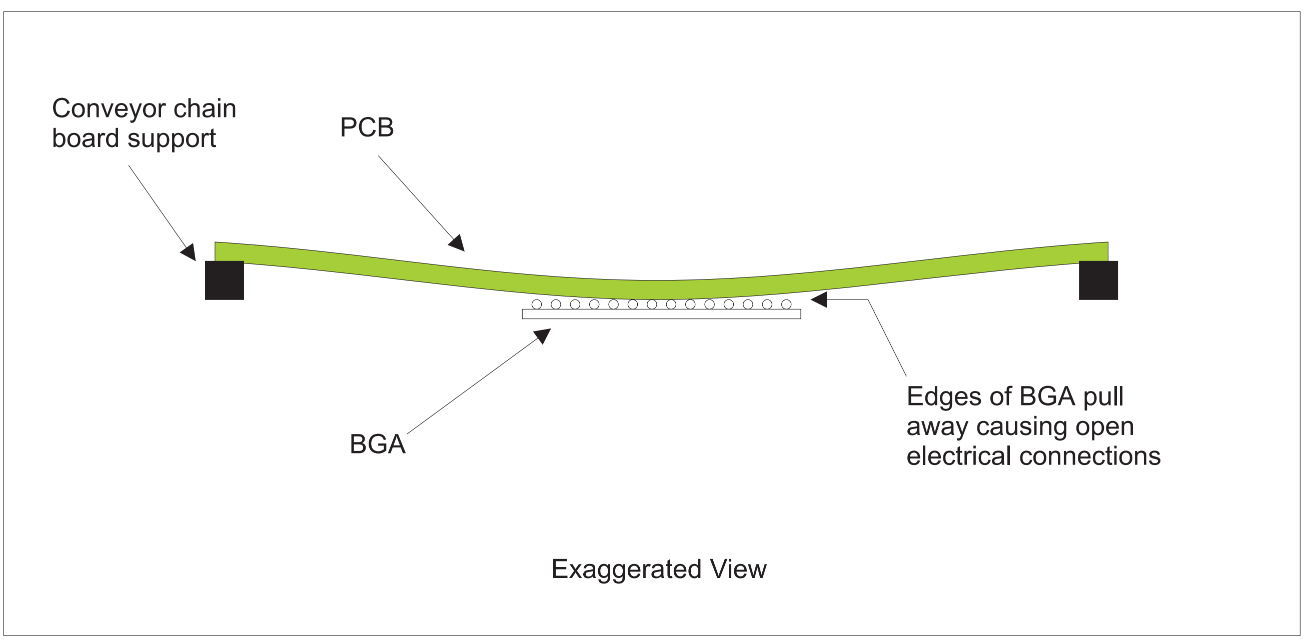
All polarized SMT and through-hole components should be placed in the same orientation and in only one axis. This facilitates easier visual inspection.

Where this is not practical, try to group components in the same orientation.



BGA's and QFP/QFN's

1. BGA and larger QFP devices (>100 leads) should not be placed in the center of the PCB. The maximum board warpage tends to be in the center of the PCB. The results can be open solder connections. For a standard 0.062" PCB, this becomes a concern when the surface area exceeds 25 in^2.



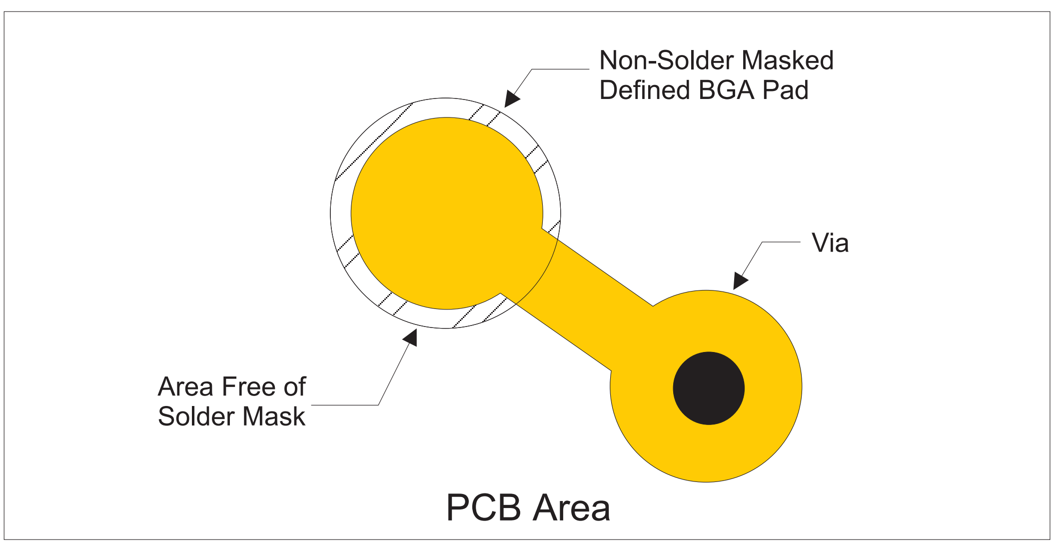
2. If BGA's are on both sides of the board, it is not recommended that the BGA's are positioned on top of each other. This method makes rework of a BGA extremely difficult. In addition, this method makes x-ray inspection of the solder balls very difficult.

3. BGA's should be placed on the top side of the PCB. This eliminates the possibility of open solder connections due to the weight of the part during second pass reflow.

4. CBGA's and QFN's should not be on the same PCB. The reason is that CGBA's and QFN's require different amounts of solder. (CBGA components require more solder paste than QFN components.) Because of this, a step-stencil or a separate solder stencil will need to be used for the CGBA to place the required amount of solder paste.

   Should CBGA's and QFN be placed on the same PCB, a minimum of 0.250" clearance around the CGBA is required to accommodate the solder stencil.

5. The traces that connect vias to BGA pads need to be masked off as a minimum to prevent solder from scavenging into the vias. The BGA pads are non-solder masked defined (i.e. solder mask opening is larger than the metal pad).



Required Files for PCB Fabrication

Required:

1. Gerber Files (RS-274-X or RS-274-D format)
   - All copper layers (including inner and outer layers)
   - Solder mask layers
   - Silkscreen/Legend layers
   - Via plugging layers (if applicable)
   - Solder paste layers (for board assembly)
   - Aperture list if apertures are not embedded in the Gerber data (i.e. not using RS-274-X)
2. Drill file with tool codes and X-Y coordinates for all holes (ASCII or EIA format).
3. IPC-D-356 netlist (used for continuity testing).
4. Readme File containing Engineering contact information and any special instructions.
5. Fab drawing
   - Board outline, dimensions, including cutouts, chamfers, radii, bevels, scores, etc.
   - Dimensions from a reference hole in the board to a corner or to two sides of the board outline.
   - A drill chart with the hole symbols on the drawing and the finished hole sizes
   - Material requirements
   - Finished board thickness and tolerance
   - Layer stack-up order
   - Controlled impedance requirements (if applicable)
   - Dimensioned array drawing if the design is to be shipped as a multiple-up array
   - Notes defining any other requirements or specifications pertinent to the design

Optional:

1. Valor ODB++ file - preferred by PCB vendors instead of Gerber format.
2. Check plots in Adobe PDF form. Incoming QC uses this to check PCB.

Required Files for PCB Assembly

Required:
1. Gerber files (RS-274-X or RS-274-D format) of
   - Inner and outer layers
   - Solder paste layers
2. Parts placement file (.CAD for Allegro; .ASC for Pads).
3. Assembly diagram.

Optional:
1. Valor ODB++ file

NOTE: The Hardware Engineer will provide additional files to the Contract Manufacturer (such as the assembly instructions and BOM) but those files are beyond the scope of this document. The listed files are what the PCB CAD department will provide.