LVDS Owner's Manual

Including High-Speed CML and Signal Conditioning

Fourth Edition

2008

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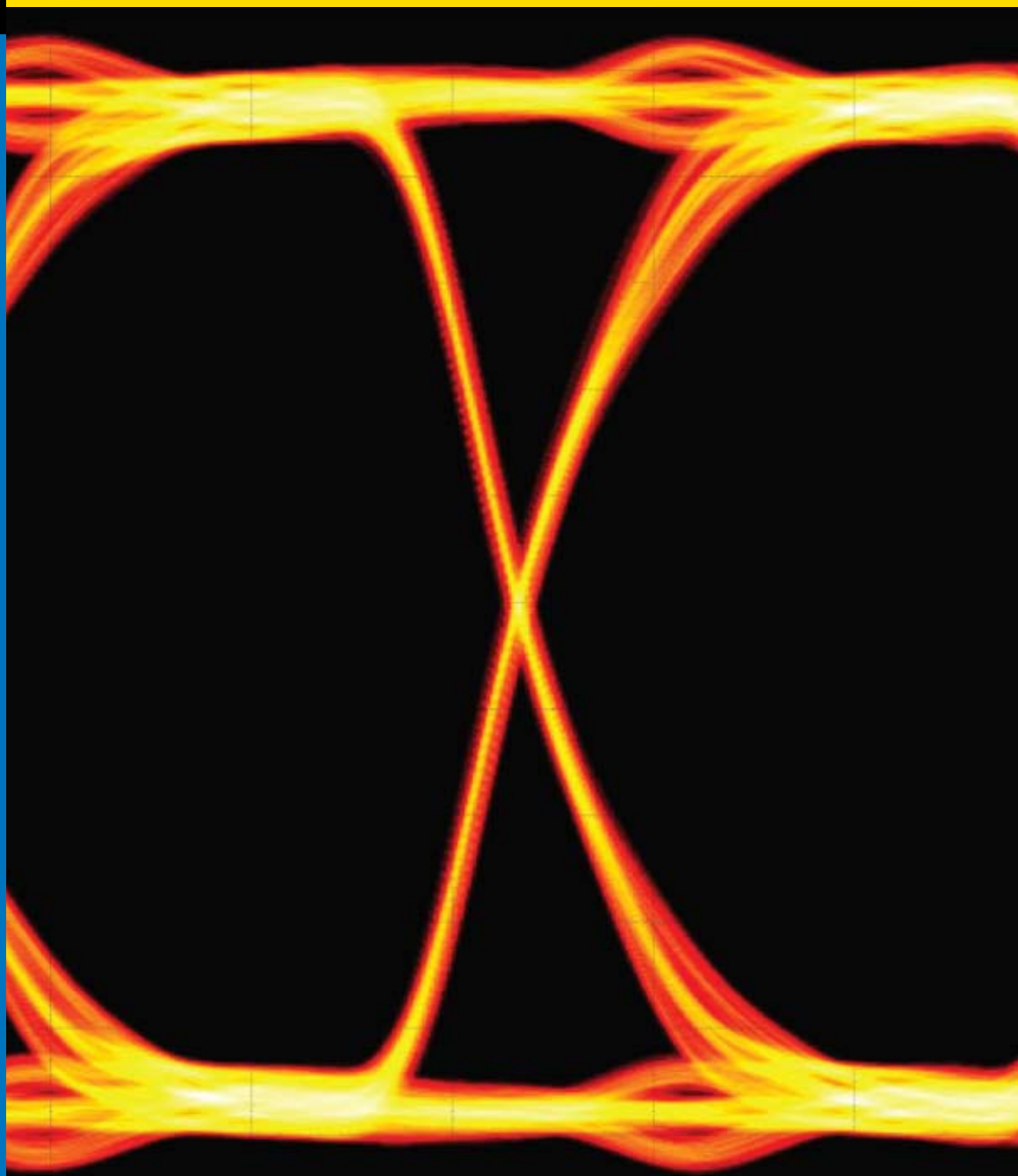

National Semiconductor

The Sight & Sound of Information

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Introduction

National Semiconductor's LVDS Owner's Manual, first published in spring 1997, has been the industry's "go-to design guide" over the last decade. The owner's manual helped LVDS grow from the original IEEE 1596.3-1996 Standard for Low-Voltage Differential Signaling (LVDS) for Scalable Coherent Interface (SCI) into the workhorse technology it is today.

LVDS is now pervasive in communications networks and used extensively in applications such as laptop computers, office imaging, industrial vision, test and measurement, medical, and automotive. It provides an attractive solution - a small-swing differential signal for fast data transfers at significantly reduced power and with excellent noise immunity. Along with the applications, LVDS continued to evolve over the last decade to meet specific requirements such as Bus LVDS and Multipoint LVDS. For example, the latest LVDS products are capable of data rates in excess of 3 Gbps while still maintaining the low power and noise immunity characteristics.

Today, many applications require even faster data rates and longer transmission paths. Therefore, designers should consider technologies such as Current-Mode Logic (CML) and signal conditioning for both LVDS and CML. That is why this new Fourth Edition includes practical design techniques for these technologies as well as LVPECL and LVCMOS.

This owner's manual provides useful and current information. It begins with a brief overview of the three most common high-speed interface technologies (LVDS (with variants B-LVDS and M-LVDS), CML, and LVPECL) a review of their respective characteristics, and a section on selecting the optimal technology for an application. The manual then covers relevant topics such as level translation, jitter, signal conditioning, and suggested design approaches. This practical information will help you select the right solution for today's interface design issues.

1.1 Differential Signaling Technology

There are plenty of choices when selecting a high-speed differential signaling technology. Differential technologies generally share certain characteristics but vary widely in performance, power consumption, and target applications. ***Table 1-1*** lists various attributes of the most common differential signaling technologies.

Table 1-1. Industry Standards for Various LVDS Technologies

	Industry Standard	Maximum Data Rate	Output Swing (V_{OD})	Power Consumption
LVDS	TIA/EIA-644	3.125 Gbps	± 350 mV	Low
LVPECL	N/A	10+ Gbps	± 800 mV	Medium to High
CML	N/A	10+ Gbps	± 800 mV	Medium
M-LVDS	TIA/EIA-899	250 Mbps	± 550 mV	Low
B-LVDS	N/A	800 Mbps	± 550 mV	Low

Industry standards bodies define LVDS and M-LVDS technologies in specifications *ANSI/TIA/EIA-644A* and *ANSI/TIA/EIA-899*, respectively. Some vendor datasheets claim LVDS I/Os (or pseudo-LVDS) but in fact may not meet the required common mode or some other important parameter. Therefore, compliance to the LVDS specification *TIA/EIA-644A* is an important consideration.

Current-Mode Logic (CML) and Low-Voltage Positive-Emitter-Coupled Logic (LVPECL) are widely used terms throughout the industry, although neither technology conforms to any standard controlled by an official standards organization. Implementations and device specifications will therefore often vary between vendors. AC coupling is used extensively which helps resolve threshold differences that might otherwise cause compatibility issues.

Note that all of the technologies listed are differential and thus share the advantages common to differential signaling such as excellent noise immunity and low device-generated switching noise.

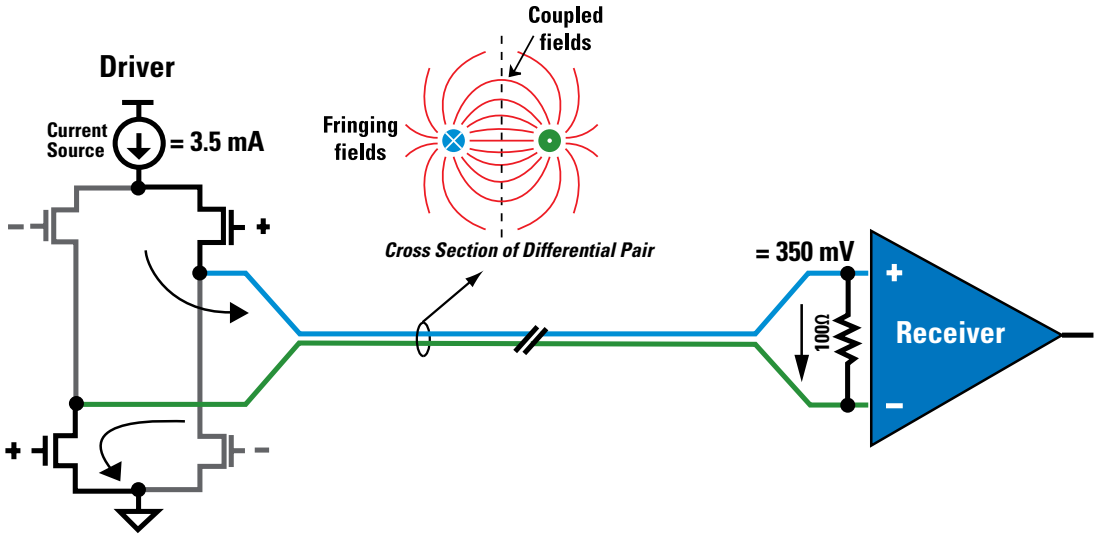


Figure 1-1. LVDS Driver and Receiver

A typical LVDS driver – receiver pair is shown in ***Figure 1-1***. A (nominal) 3.5 mA current source is located in the driver. Since the input impedance of the receiver is high, the entire current effectively flows through the 100Ω termination resulting in a (nominal) 350 mV voltage across the receiver inputs. The receiver threshold is guaranteed to be 100 mV or less, and this sensitivity is maintained over a wide common mode from 0V to 2.4V. This combination provides excellent noise margins and tolerance to common-mode shifts between the driver and receiver. Changing the current direction results in the same amplitude but opposite polarity at the receiver. Logic ones and zeros are generated in this manner. CML and LVPECL have a similar architecture but with different strength current sources and termination schemes.

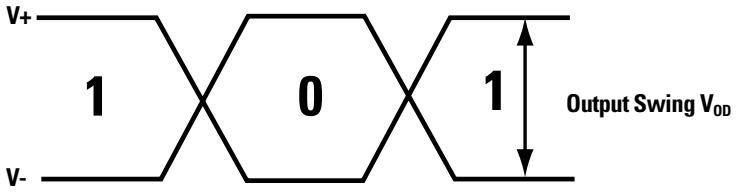


Figure 1-2. Differential Signaling

From this simple diagram in ***Figure 1-2***, the advantages common to all differential signaling technologies can be seen. First, note that the current source is always on and routed in different directions to drive logic ones and zeros. This always-on characteristic eliminates the switching-noise spikes and EMI resulting from turning high-current transistors on and off (as required in single-ended technologies). Secondly, the two lines of the differential pair are adjacent to each other providing a considerable amount of noise immunity. Noise from crosstalk or EMI that is absorbed in one of the pair will also appear in the adjacent line. Since the receiver responds to the difference between the two channels, "common-mode" noise that appears on both lines of the pair will cancel at the receiver. Also, as the two adjacent lines carry equal current, but in opposite directions, EMI generation is minimized.

1.2 LVDS – Low-Voltage Differential Signaling

The 350 mV typical signal swing of LVDS consumes only a small amount of power and therefore LVDS is a very efficient technology, delivering performance at data rates up to 3.125 Gbps. The simple termination, low power, and low noise generation generally make LVDS the technology of choice for data rates from tens of Mbps up to 3 Gbps and beyond.

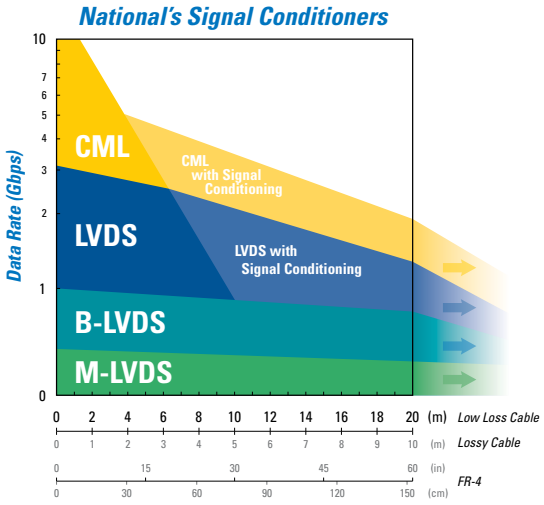


Figure 1-3. Typical Data Rates and Cable Drive Strength

For higher data rates, technologies such as CML or LVPECL are required. As shown graphically in ***Figure 1-3*** and ***1-6***, CML and LVPECL are capable of very high data rates in excess of 10 Gbps. Achieving these very high data rates requires extremely fast, sharp-edge rates and typically a signal swing of approximately 800 mV. For these reasons, CML and LVPECL generally require more power than LVDS.

Sharp, fast edge rates include a significant amount of very-high-frequency content – and since transmission loss in cables and FR4 traces increases with frequency, these technologies often require signal conditioning when driving long cables or traces. **See Interconnect Media, page 59**, for a more thorough discussion on signal attenuation and distortion in various cables and other media, including various signal-conditioning techniques such as pre-emphasis and equalization that help mitigate the effect of signal distortion in cables and traces.

1.3 CML – Current-Mode Logic

CML is a high-speed point-to-point interface capable of data rates in excess of 10 Gbps. As shown in ***Figure 1-4***, a common feature of CML is that termination networks are integrated typically into both drivers and receivers. CML uses a passive pull-up to the positive rail, which is typically 50Ω. Most implementations of CML are AC coupled, and therefore require DC-balanced data. DC-balanced data tests require data coding that contain, on average, an equal number of ones and zeros. (See **DC Balance, page 33**).

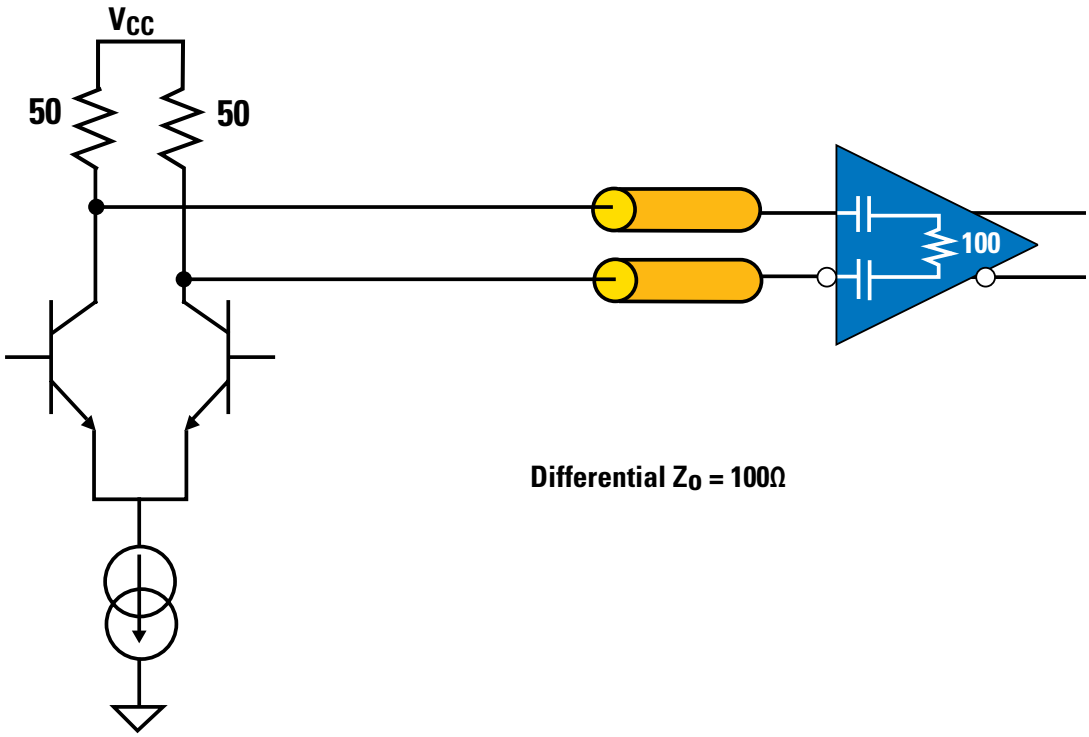


Figure 1-4. Typical CML Implementation

1.4 Low-Voltage Positive-Emitter-Coupled Logic

LVPECL and PECL are both offshoots of the venerable ECL technology first introduced in the 1960s. ECL is powered commonly between ground and -5.2V. Because of the negative rail requirements and ECL's incompatibility with other logic families, a positive rail technology was introduced known as Positive-Emitter-Coupled Logic (PECL). ECL, PECL, and LVPECL all require a 50Ω termination into a termination rail that is about 2V less than the most positive rail. ECL drivers are low-impedance open-emitter outputs that generate typically 700 mV to 800 mV. The output stage remains in the active region, preventing saturation, and results in very fast and balanced edge rates.

Positive features of LVPECL are the sharp and balanced edges and high drive capability. Drawbacks of LVPECL are relatively high power consumption and sometimes the need for a separate termination rail.

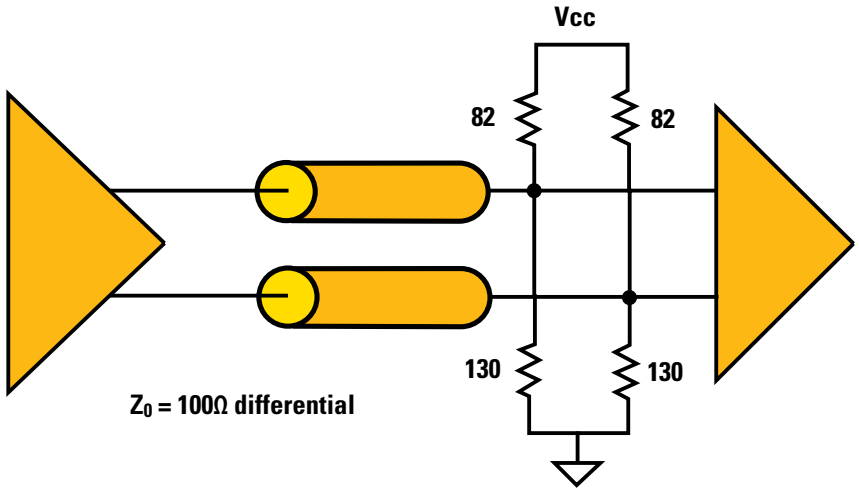


Figure 1-5. Typical LVPECL Implementation

1.5 Selecting an Optimal Technology

With the existence of various differential technologies, a need for some guidance in selecting an optimal signaling technology for an application is obvious. The following are the factors under consideration when selecting an optimal technology for a given application:

- Required bandwidth
- Ability to drive cables, backplanes, or long traces
- Power budget
- Network topology (point-to-point, multidrop, multipoint)
- Serialized or parallel data transport
- Clock or data distribution
- Compliance to industry standards
- Need or availability of signal conditioning

LVDS is the most common differential signaling interface. The low power consumption, minimal EMI, and excellent noise immunity are the features that have made LVDS an interface of choice for many applications. In addition, the LVDS wide-input common mode makes LVDS devices easy to interoperate with other differential signaling technologies. The latest generation of LVDS operates from DC to as high as 3.125 Gbps, allowing many applications to benefit from LVDS. These multi-gigabit LVDS devices feature pre-emphasis and equalization that enables signal transmission over lossy cables and printed circuit board (PCB) traces.

Applications requiring data rates greater than 3.125 Gbps will likely require CML signaling. In addition, certain communication standards (e.g. PCIe, SATA, and HDMI) mandate the use of specific signaling technologies or describe a set of conditions such as signal amplitude and reference to V_{CC}, consistent with CML.

For applications with data rates between 2 Gbps and 3.125 Gbps, the optimum choice will depend on the desired functionality, performance, and power requirements. For relatively short distance transmission where signal conditioning is not required the device power and jitter dominate, with CML generally having the lowest jitter and LVDS the lowest power.

For long-reach requirements, losses in the media dominate and the best choice is generally the device with the best signal-conditioning solution for the data rate and media. Both LVDS and CML use techniques such as equalization and pre-emphasis or de-emphasis, see **Signal-Conditioning Characteristics, page 63.** Understanding the loss characteristics of the transmission media and the best signal-conditioning solution will enable the user to select the appropriate device.

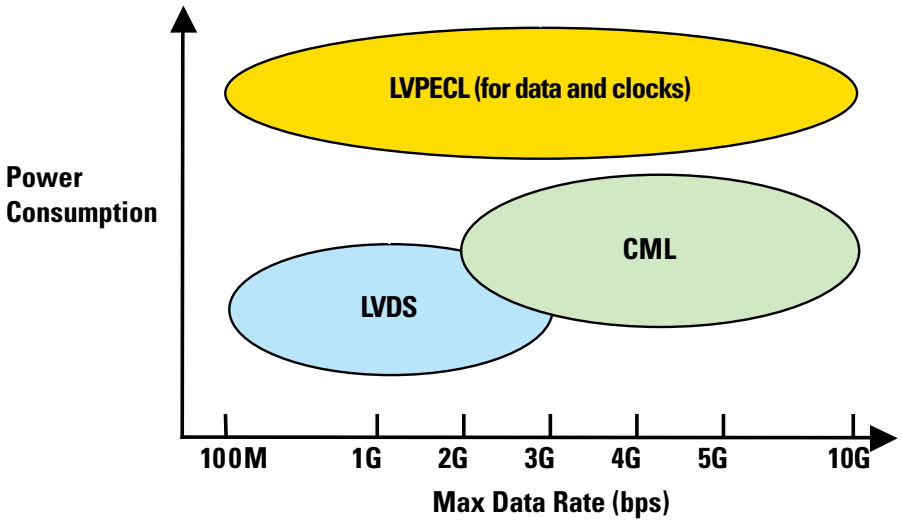


Figure 1-6. Typical Application Targets for Three Common Differential Signaling Technologies

The term “network topology” typically refers to a physical topology or an arrangement of network nodes (e.g. Ring, Mesh, Star, Bus, or Tree network topologies). This section discusses typical signal topologies or arrangements of signal drivers and receivers around a common interconnect or transmission medium (e.g. Printed Circuit Board (PCB) traces or copper cables). It also points out how common differential signaling may work in these arrangements and identifies optimal differential signaling technologies for each topology.

There are two fundamental topologies: point-to-point and multipoint. Point-to-point topology involves only one signal driver and one signal receiver; a multipoint topology may have multiple drivers and receivers.

2.1 Point-to-Point

As point-to-point topologies involve only a single driver and receiver pair, interconnecting media can be very simple and typically require a minimal number of transitions from one medium to the next (i.e. a transition from a printed circuit board to a cable via a connector). A minimal number of transitions usually means the signal path will likely have well-controlled impedance. A controlled-impedance environment allows very high signaling rates. While all differential signaling technologies may be used in links configured as a point-to-point topology, LVDS, CML, and LVPECL are designed for point-to-point signal transmission. Interface devices that feature LVDS, LVPECL, or CML have driver-output signals with fast edges that allow multi-gigabit transmission. These fast signal edges are very sensitive to any impedance discontinuities and demand careful interconnect designs.

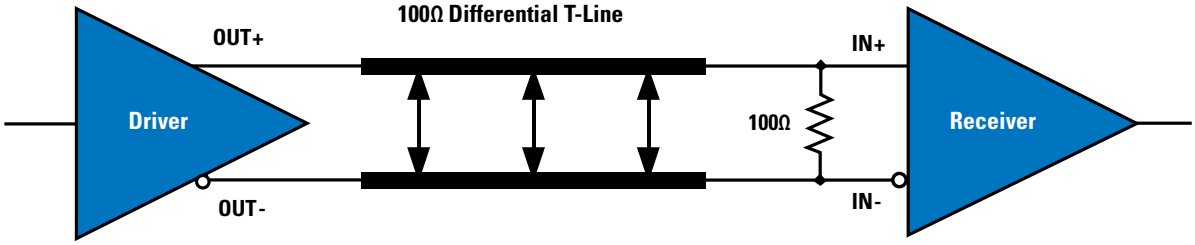


Figure 2-1. A Point-to-Point Topology

Figure 2-1 illustrates a typical LVDS driver and receiver pair in a point-to-point topology. Controlled impedance of the interconnect, proper driver load, and interconnect termination are the key points for consideration when designing for low-jitter signal transmission.

2.2 Multipoint / Multidrop

Unlike point-to-point topologies, multipoint topologies have multiple signal drivers and receivers all sharing a single interconnect. A variant of the multipoint topology where there is a single driver and multiple receivers is referred to as a "multidrop' topology (***Figure 2-2***).

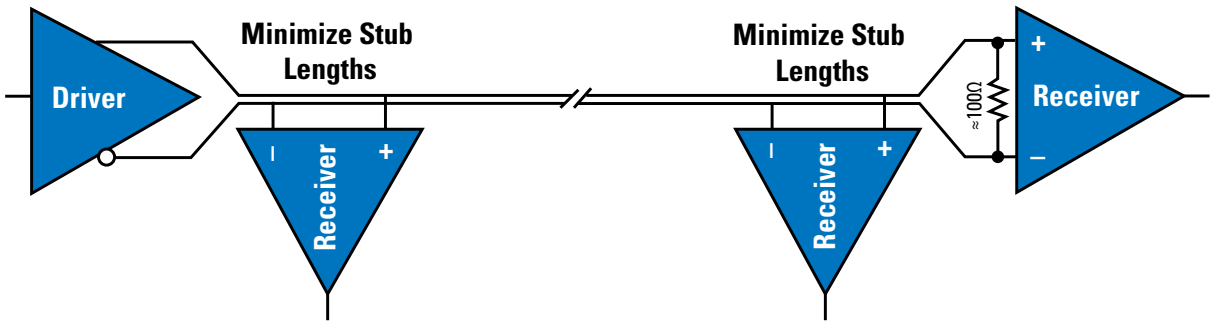


Figure 2-2. A Multidrop Topology

Figure 2-2 illustrates a typical multidrop topology. Terminating the signal bus on the far receiver side is advisable only when the signal driver is on the opposite end of the bus from the terminated receiver. In all other cases (e.g. driver connected to the middle of the bus), the bus needs to be terminated at both ends of the bus.

Another frequently implemented variant of the multipoint topology is "half-duplex" topology (***Figure 2-3***) which consists of two driver/receiver pairs that transmit and receive signals between two points over a single interconnect.

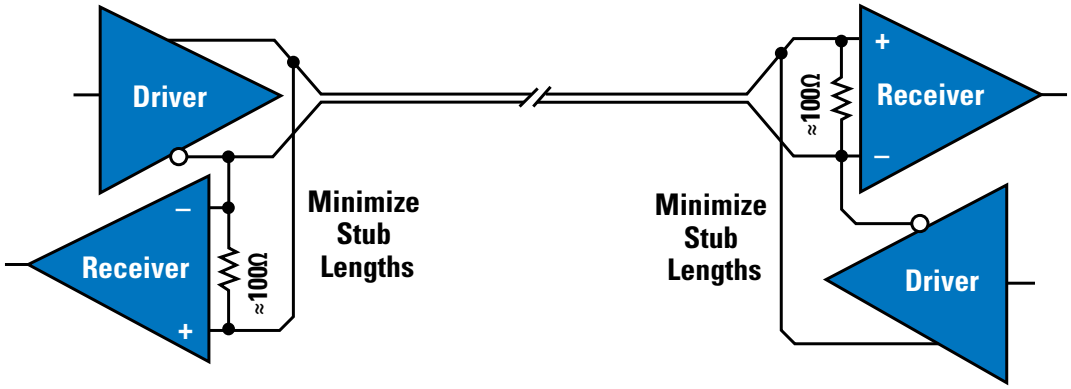


Figure 2-3. A Half-Duplex Topology

Physical connection of multiple drivers and receivers to a common signal bus presents unique challenges to successful multidrop-topology designs. The major challenge that system designers encounter are the impedance discontinuities that device loading and device connections (stubs) introduce on the common bus. Matching the impedance of the loaded bus and using signal drivers with controlled signal edges are the keys to error-free signal transmissions in multipoint topologies. Two versions of LVDS have been optimized for multipoint: Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS).

B-LVDS shares many of the characteristics of LVDS but has much higher current drive (10 mA typical) and controlled (slower) edge rates. B-LVDS is designed specifically for driving multiple loads and in a well-designed backplane can support up to 32 loads. B-LVDS-controlled edge rates help reduce reflections in multidrop configurations with multiple loads and associated stubs. The slower edges limit B-LVDS to slower data rates, typically below 1 Gbps.

The growth of B-LVDS in multidrop applications prompted the creation of an industry standard for an optimized version of LVDS intended for such networks. National Semiconductor co-authored the standard that became *TIA/EIA-899* and the technology Multipoint LVDS (M-LVDS). M-LVDS includes all of the desirable attributes for multidrop including increased drive, slow controlled edges, tighter input thresholds, and a wider common mode. M-LVDS is capable of driving 32 loads at speeds up to 250 Mbps.

2.3 SerDes Architectures

Two obvious ways to add bandwidth are to either increase the bus speed or add parallel channels. Prior to the advent of high-speed interface, the latter approach was often selected, resulting in very wide Low-Voltage Transistor-to-Transistor Logic (LVTTL) buses and backplanes. The technique of combining slower LVTTL signals into a single-bit stream (serializer), transporting the data at high speed and then redistributing at the receiver (deserializer), is very common and often referred to as Serializer/Deserializer (SerDes). The different SerDes architectures and advantages of each are covered in the **SerDes Architectures Section on page 19**.

2.4 Mixing Signaling Technologies

It is quite common for hardware platforms to have multiple signaling requirements for clocks, data, and control signals. In modular systems, card-to-card or box-to-box communication may involve different vendors and technologies. For these reasons, LVDS, LVPECL, and CML often coexist in the same platform, and translation between different signaling technologies is a necessary component of system design.

One approach to simplify translation is to AC couple the two networks using capacitors in each of the differential channels. This technique eliminates DC offsets and threshold differences, however AC coupling requires DC-balanced data. For non-DC-balanced data, various termination networks allow translation between technologies. For a full discussion on translation networks, see **Termination and Translation, page 31**.

2.5 Selecting an Interface Technology

The selection of an interface device or technology is an important one. Error-free and reliable signal transmission is a critical component of many systems. The first decisions are often the topology: Will the network be point-to-point or multidrop? Will SerDes be required? Bandwidth, power, and jitter budgets then need to be considered.

LVDS is the most common high-speed interface and has the dual advantages of low power and wide common mode. LVPECL generally uses additional power but supports very high data rates with excellent jitter. CML devices offer similar performance to LVPECL and have the advantage of a simple and usually integrated termination.

3.1 Introduction

Serial interconnects form the critical backbone of modern communications systems. The selection of the most appropriate Serializer/Deserializer (SerDes) will have a substantial impact on system cost and performance. While the maze of choices may seem confusing at first, SerDes devices fall into a few basic architectures, each tailored to specific application requirements. A basic understanding of the architectural differences enables the designer to quickly find the right SerDes for the application. In this section, four distinct SerDes architectures are examined and the vital role each fills in system design.

3.2 Parallel Clock SerDes

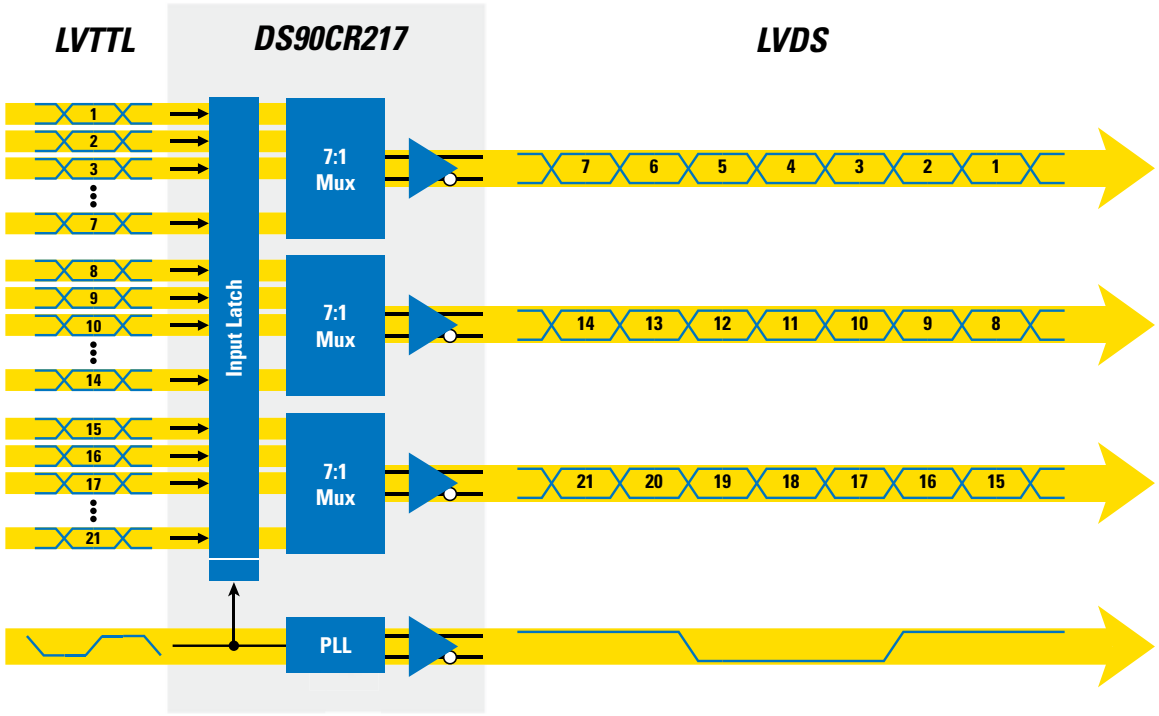


Figure 3-1. Parallel-Clock-Serializer Coding Example

Parallel clock SerDes are used normally to serialize "data-address-control" parallel buses such as PCI, UTOPIA, processor buses, and control buses. Rather than tackling the entire bus with one multiplexer, the parallel-clock-SerDes architecture employs a bank of n-to-1 multiplexers, each serializing its section of the bus separately. The resulting serial-data streams travel to the receiver in parallel with an additional clock-signal pair that the receiver uses to latch in and recover the data. Since clock and data travel on multiple pairs, pair-to-pair skew must be minimized for proper deserialization.

3.3 Embedded Clock (Start-Stop) Bits SerDes

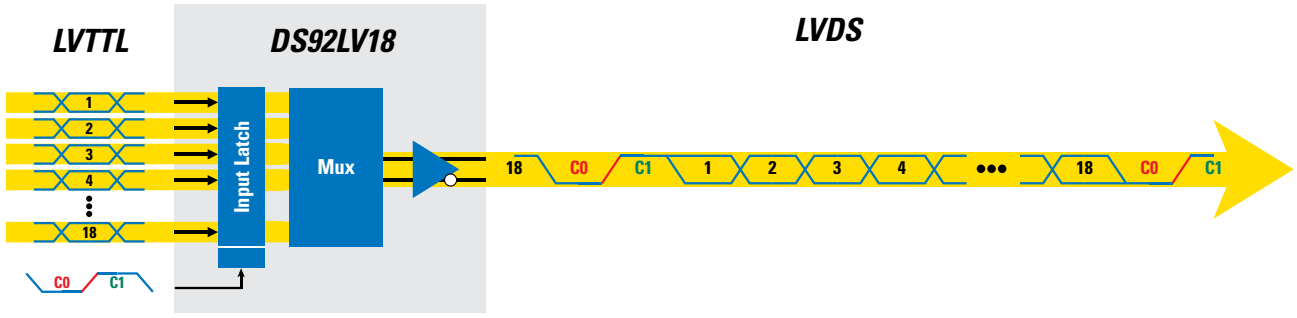


Figure 3-2. 18-bit Embedded-Clock-Bits-Serializer Coding Example

The embedded-clock-bits-architecture transmitter serializes the data bus and the clock onto one serial-signal pair. Two clock bits, one low and one high, are embedded into the serial stream every cycle, framing the start and end of each serialized word (hence the alternative name "start-stop bits" SerDes) and creating a periodic rising edge in the serial stream. One benefit of this architecture is data-payload word widths are not constrained to byte multiples; 10-, 16-, 18-, and 24-bit widths are popular bus widths.

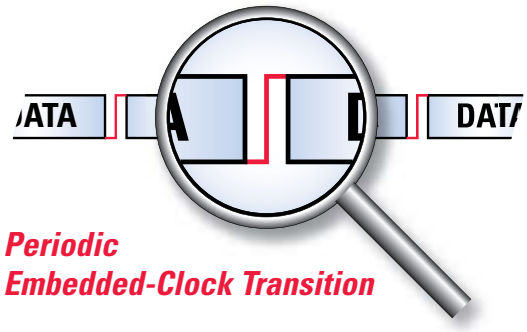
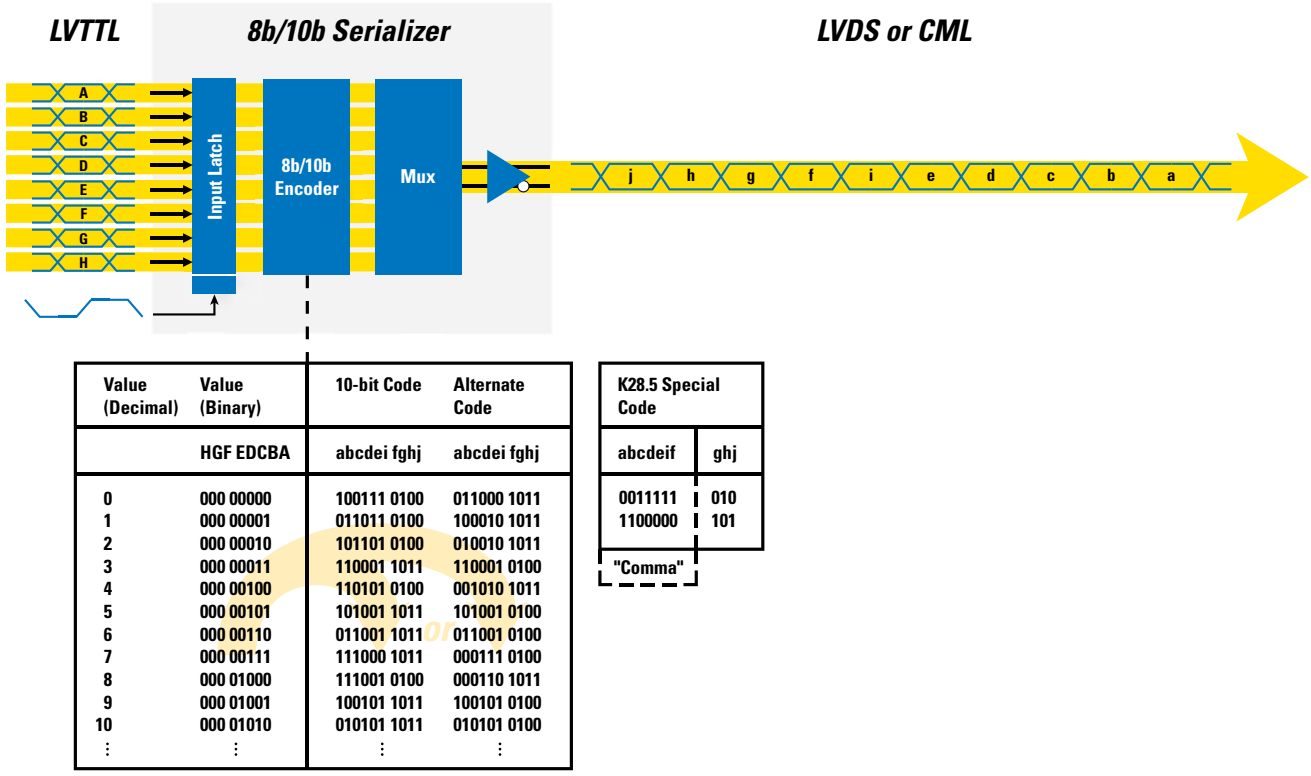


Figure 3-3. Periodic Embedded-Clock Transition

Upon power-up, the deserializer automatically searches for the periodic embedded-clock rising edge. Since the data-payload bits change value over time while the clock bits do not, the deserializer is able to locate the unique clock edge and synchronize. Once locked, the deserializer recovers data from the serial stream regardless of the payload-data pattern. This automatic synchronization capability commonly is called "lock to random data" and requires no external system intervention. This is an especially useful feature in systems where the receiver is in a remote module not under direct system control. Since the receiver is locked to the incoming embedded clock and not to an external reference clock, jitter requirements for both transmitter and receiver input clocks are relaxed significantly.

3.4 8b/10b SerDes



Value (Decimal)	Value (Binary)	10-bit Code	Alternate Code
	HGF EDCBA	abcdei fghj	abcdei fghj
0	000 00000	100111 0100	011000 1011
1	000 00001	011011 0100	100010 1011
2	000 00010	101101 0100	010010 1011
3	000 00011	110001 1011	110001 0100
4	000 00100	110101 0100	001010 1011
5	000 00101	101001 1011	101001 0100
6	000 00110	011001 1011	011001 0100
7	000 00111	111000 1011	000111 0100
8	000 01000	111001 0100	000110 1011
9	000 01001	100101 1011	100101 0100
10	000 01010	010101 1011	010101 0100
⋮	⋮	⋮	⋮

K28.5 Special Code	
abcdeif	ghj
0011111	010
1100000	101
"Comma"	

Figure 3-4. 8b/10b-Serializer Coding Example

The 8-bit/10-bit (8b/10b) serializer maps each parallel data byte to a 10-bit code and serializes the 10-bit code onto a serial pair. The 10-bit transmission codes were developed by IBM Corporation in the early 1980s and guarantee multiple edge transitions every cycle as well as DC balance (balanced number of transmitted ones and zeros). Frequent edge transitions in the stream allow the receiver to synchronize to the incoming data stream. DC balance facilitates driving AC-coupled loads, long cables, and optical modules. (See **DC Balance, page 33** for more information.)

In order for the receiver to locate the 10-bit code word boundaries in the serial stream, the transmitter first marks one boundary by sending a special symbol called a comma character. The unique bit sequence in this comma character never appears in normal data traffic and acts as a reliable marker for receiver code alignment. Once code alignment is accomplished, the receiver maps the 10-bit codes back to byte data, flagging an error if it detects an invalid 10-bit code.

The 8b/10b deserializer architectures use an external reference clock to recover the clock and deserialize the data stream. As a result, they require tight reference-clock source frequency and jitter control.

3.5 FPGA-Attach SerDes

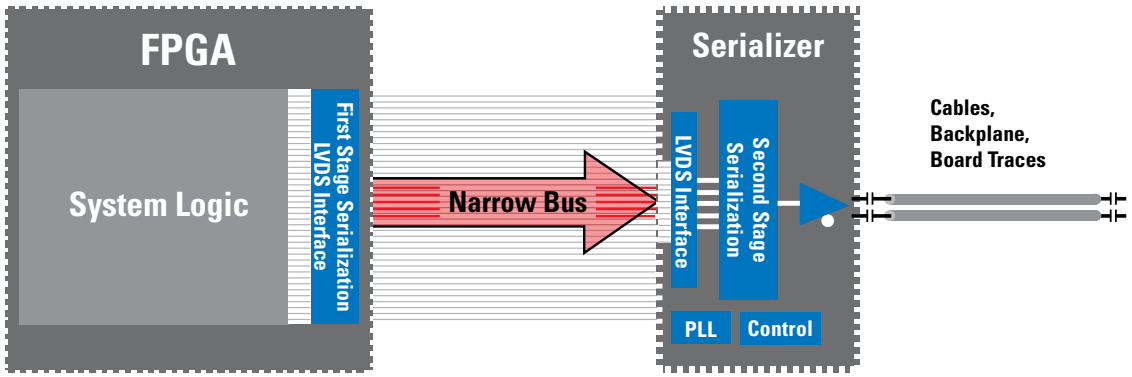


Figure 3-5. FPGA-Attach Serializer Optimizes the Analog-Intensive Functions

Over the past decade, FPGAs, largely due to their programming flexibility, have evolved to be the dominant way to implement digital logic. The FPGA-Attach SerDes complements this system architecture by providing all the analog-intensive functions like clock and data recovery, signal conditioning, clock synthesis, and jitter cleaning to support higher data rates over long, inexpensive interconnects like CAT-5 and coax cables.

This architecture implements the serialization and deserialization in two stages: the first stage combines several low-speed data bits to a few LVDS streams, and then the second stage multiplexes the LVDS streams onto one high-speed serial channel. A FPGA easily implements the first stage while an analog-optimized discrete SerDes handles the high-speed serialization.

The LVDS parallel interface of the FPGA-Attach SerDes enables higher data rates over fewer board traces while reducing the EMI, power, and noise sensitivity of the system. This eliminates the switching noise and skew associated with traditional single-ended interfaces like LVTTL.

SerDes devices in this family typically integrate signal-conditioning schemes like de-emphasis, DC balancing, and channel equalization. This optimizes the performance for the highest data rates and longest transmission paths.

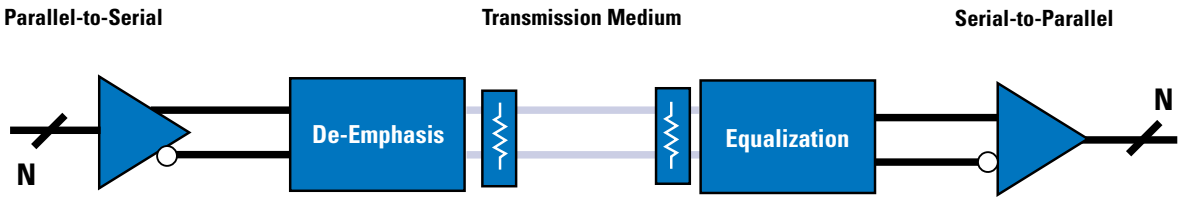


Figure 3-6. F PGA-Attach SerDes with Integrated Signal Conditioners

The popularity of FPGAs, desire to reduce board traces, and demand for higher bandwidth are resulting in growing adoption of this intelligently-partitioned architecture.

3.6 Applications

Parallel Clock SerDes

Parallel clock SerDes normally are used to serialize traditional wide "data+address+control" buses, acting as a "virtual ribbon cable" unidirectional bridge.

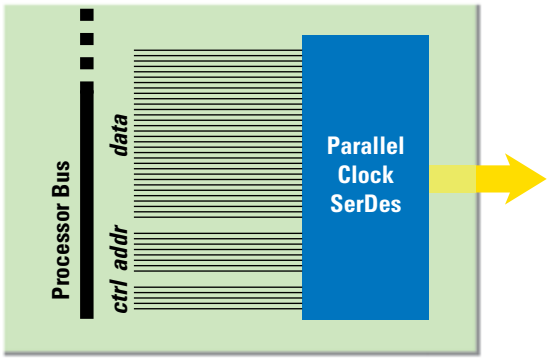


Figure 3-7. Parallel Clock SerDes Accommodate Traditional Wide Parallel Buses with Address and Control as well as Data Signals

The parallel clock SerDes delivers benefits over non-serialization such as fewer wires (especially grounds), lower power, longer cable-driving capability, lower noise/EMI, and lower cable/connector costs. Not being confined to using one serial pair, parallel clock SerDes can be made arbitrarily wide and also avoid the design issues associated with ultra-high-speed serial data rates. Parallel clock SerDes offer excellent price/performance and are often the only practical way to transmit a traditional wide parallel bus over several meters of cable. Common parallel-bus widths for these chipsets include 21-, 28-, and 48-bits.

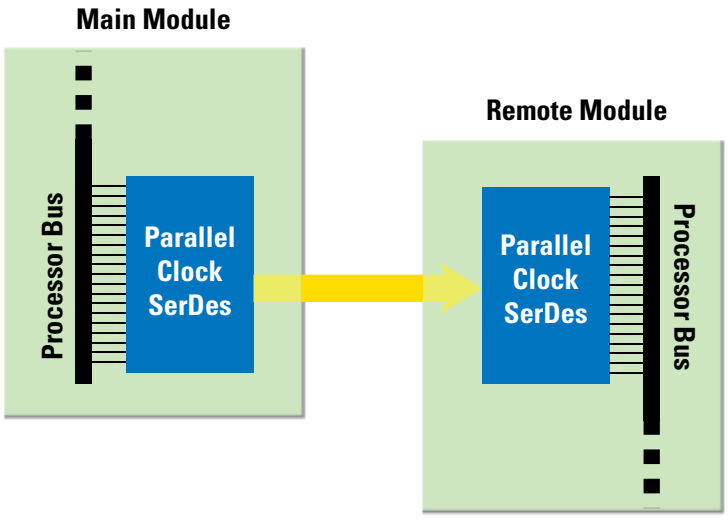


Figure 3-8. Unidirectional Rack-to-Rack Processor-Bus Extension

Common applications include laptop computer displays, rack-to-rack and shelf-to-shelf datacom/telecom interconnect, and video/camera links.

Embedded Clock (Start-Stop) Bits SerDes

Embedded clock bits SerDes are especially well suited to applications that transmit raw data plus other signals such as control, parity, frame, sync, status, etc. An application example for serializing 18 bits is shown in ***Figure 3-9***. The 18-bit transmitter serializes not only the data but also two extra bits of additional information such as parity and frame. These bits are serialized along with the data at the normal A/D sampling rate so no data buffering or extra logic is required.

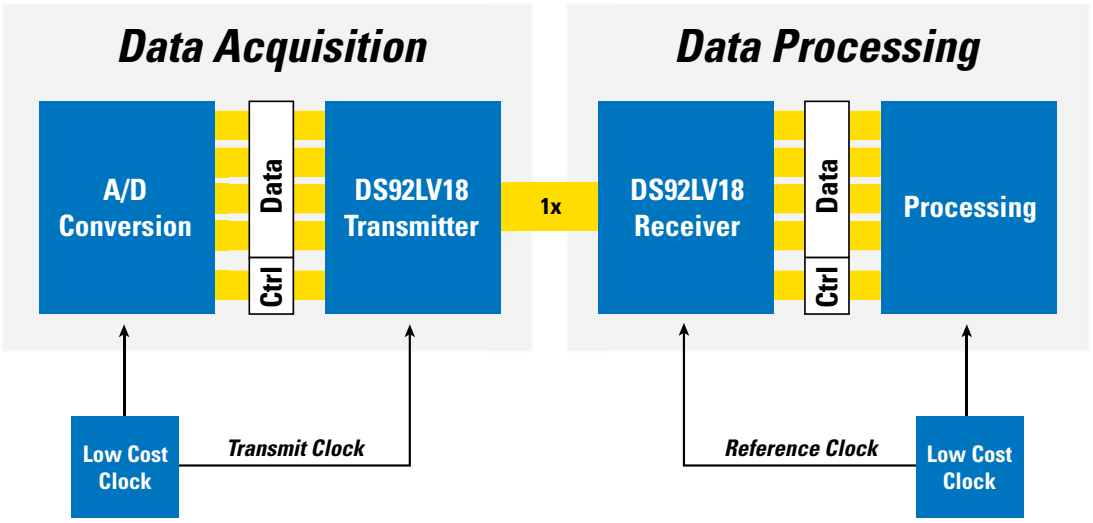


Figure 3-9. Signal-Processing System Implementation Based on DS92LV18 SerDes

Using a byte-oriented 8b/10b SerDes in the same application would be more complicated. The extra non-byte-oriented control information must be buffered and sent in byte format. A K28.5 comma character must be sent also at the start-of-link synchronization, requiring additional logic. These extra "non-data" bytes require the SerDes to operate faster than the data conversion rate, placing higher demands on backplane or cable design and also requiring some kind of idle insertion/deletion flow-control mechanism. While in data communications systems such buffering typically already exists, in many non-datacom applications this extra processing and buffering must be added.

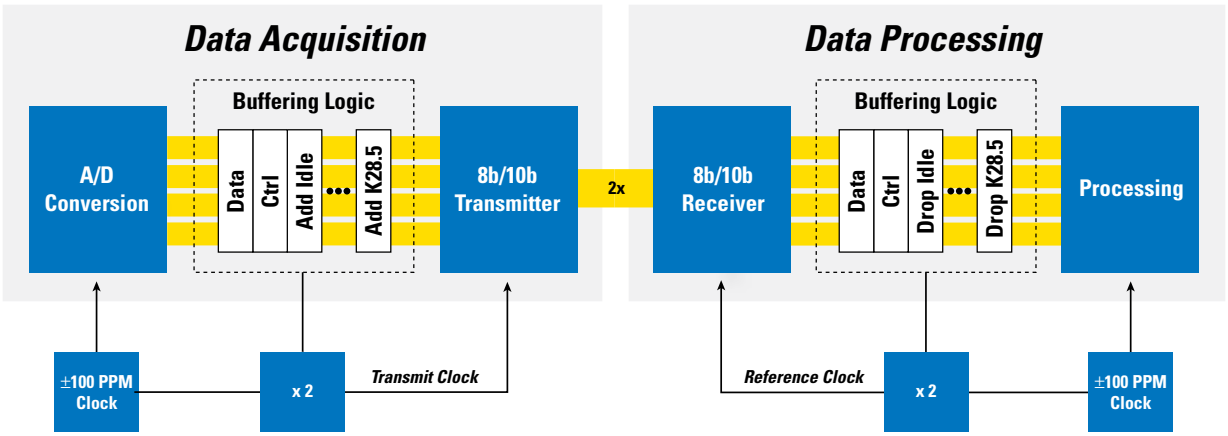


Figure 3-10. 8b/10b SerDes Implementation Example

Another feature of the embedded clock bits SerDes is automatic receiver lock to random data. This is an especially useful feature in systems where the receiver is in a remote module not under direct system control and also in systems where one transmitter broadcasts to multiple receivers. In the broadcast case, a new receiver module inserted onto the bus will lock to random data without the need to interrupt traffic to the other receivers by sending training patterns or characters.

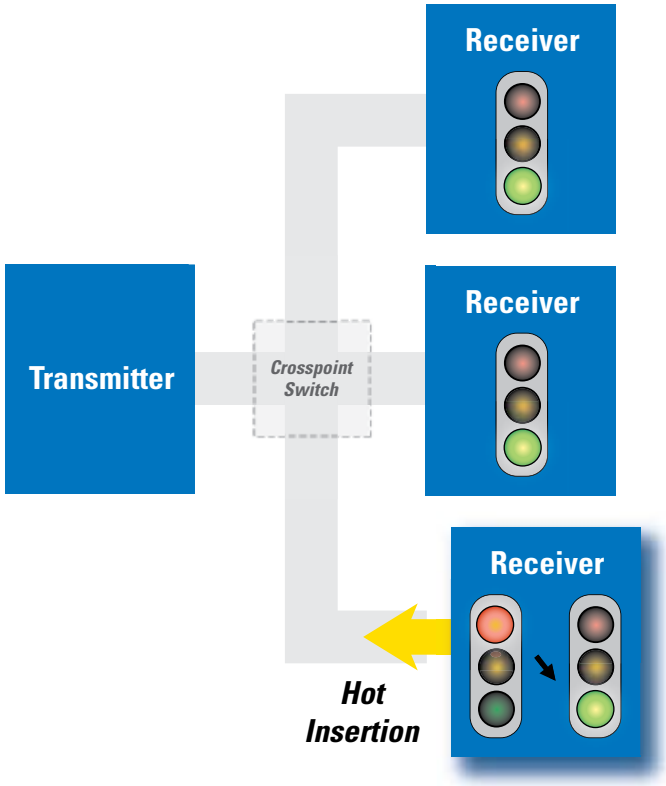


Figure 3-11. Automatic Receiver Lock to Random Data in a Broadcast Topology during Hot Insertion

The embedded clock bits deserializer locks to and tracks the incoming embedded-clock rising edge, requiring a reference clock only during initial synchronization to prevent lock to a false harmonic. This relaxes the jitter requirement on both transmit and reference clocks by at least an order of magnitude (*see Table 3-12*), reducing the cost of the clock oscillators and clock distribution networks. In many cases, an inexpensive PC-grade oscillator can be used to generate the receiver reference clock.

Table 3-12. Comparison Illustrating Relaxed Clocking Requirements of Embedded Clock Bits SerDes versus Typical SerDes Chipsets

Key Specifications	Embedded Clock Bits SerDes	Other SerDes
Serializer-Transmit-Input Clock Jitter	80 or 120 ps rms	5 or 10 ps rms
Deserializer Reference Clock vs. Serializer-Transmit Clock Disparity	± 50000 PPM	± 100 PPM

Embedded clock bits SerDes are well suited to non-byte-oriented applications such as applications requiring transmission of unpacketized raw data plus control signals. Examples include signal processing systems such as basestations, automotive imaging/video, and sensor systems where an analog-to-digital converter, camera, or image sensor communicates raw data with the processing unit at the other end of the link.

8b/10b SerDes

8b/10b SerDes are well suited to serializing byte-oriented data such as cell or packet traffic across a backplane, cable, and fiber. Many standards such as Ethernet, Fiber Channel, InfiniBand, and others use the popular 8b/10b coding at rates of 1.0625, 1.25, 2.5, and 3.125 Gbps, and many SerDes are available that span these data rates.

8b/10b coding has a maximum run length (the maximum number of consecutive ones or zeros in the serial stream) of 5 bits. This limits the spectral content of the serial stream, which can ease the task of suppressing electromagnetic radiation. For example, given a 1 Gbps line rate after 8b/10b coding, the maximum and minimum 1st harmonic frequencies are 1 GHz and (1 GHz)/5 = 200 MHz. (The maximum and minimum fundamental frequencies are therefore 500 MHz and 100 MHz, respectively.)

8b/10b serial streams are DC balanced, meaning the running disparity—or the number of ones sent minus the number of zeros sent—is on average equal to zero. 8b/10b data code words have a disparity of +2, 0, or –2, so the running disparity of an 8b/10b serial data stream always lies between +2 and –2.

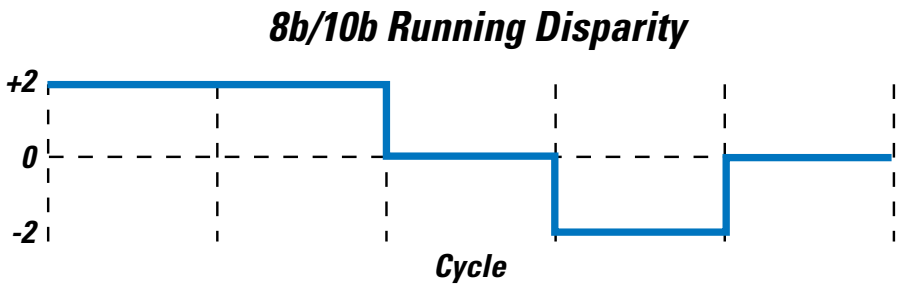


Figure 3-13. 8b/10b Running Disparity Example

DC-balance coding as well as short run length are necessary for reliably driving AC-coupled environments and fiber-optic modules. This is a major advantage of 8b/10b coding for optical serial interconnects. In addition, DC balance reduces Inter-Symbol Interference (ISI) to extend cable-drive capability.

8b/10b coding also provides a way to check errors and send control information. Error checking takes advantage of the fact that most of the possible 10-bit code permutations are not valid 8b/10b data code words. This allows 8b/10b deserializers to flag invalid codes and provide a level of error checking similar to using a parity bit. While this scheme does not count total bit errors, it is a good way to monitor serial link performance. In addition to data code words, many standards also define control words such as packet/frame markers, fault flags, and alignment characters. These control code words help systems assemble and disassemble packets, making 8b/10b coding very popular in communications data processing systems.

FPGA-Attach SerDes

The FPGA-Attach SerDes is well suited for applications that involve a FPGA and require serialization of high-speed data over lossy interconnects. The SerDes supports both AC-coupled and DC-coupled applications.

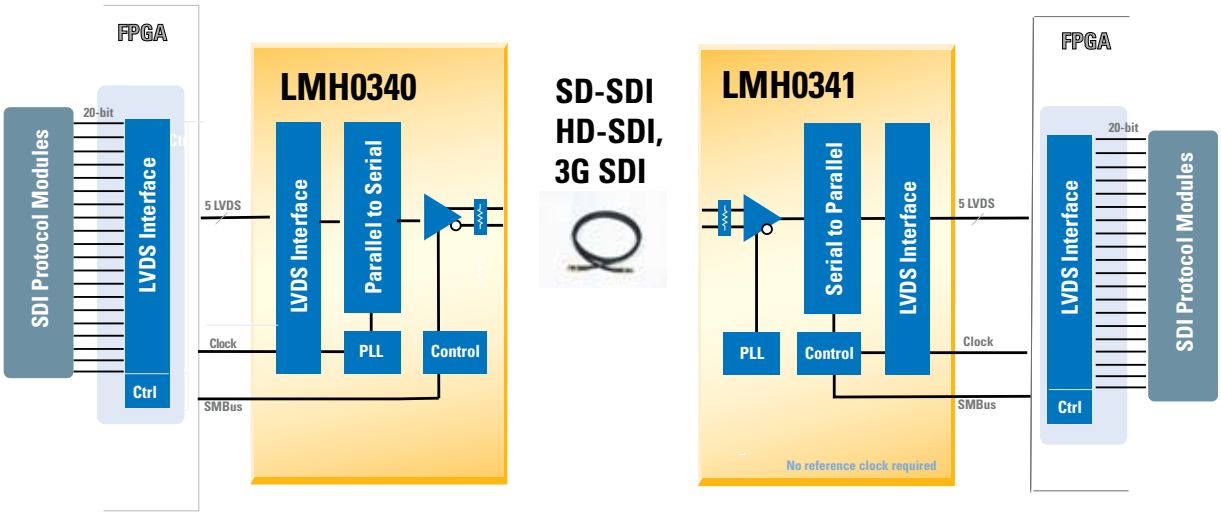


Figure 3-14. Serial Digital Video Transport Application using FPGA-Attach SerDes

The deserializer automatically locks to incoming data without an external reference clock or comma characters for easy "plug-and-go" operation. This makes the SerDes well suited to non-byte-oriented systems such as applications requiring transmission of unpacketized raw data. Examples include signal processing systems such as basestations, imaging/display, video, and sensor systems.

Integrated signal-conditioning schemes like transmit-side de-emphasis, DC balancing, programmable V_{OD}, and receive-side equalization make this a very attractive option for applications that require high data rates over inexpensive interconnects like CAT-5 cables and FR-4 backplanes. Furthermore, this integration reduces the overall system BOM and board components. Application examples include box-to-box interconnect, machine vision, LED walls, medical imaging, and various backplane applications.

3.7 Comparison Overview

Each SerDes architecture has its own advantages making it ideal for certain applications.

Parallel clock SerDes are inexpensive and conveniently serialize wide buses. They are inexpensive because they transmit the clock and data in parallel to the receive side so there is no clock recovery. However, this is also the major drawback because using multiple serial data and clock pairs requires careful wiring and low pair-to-pair skew.

Embedded clock bit SerDes are ideal for applications needing a couple of extra bits and/or the lock-to-random-data feature. They also have relaxed transmitter and reference clock requirements for systems with inexpensive clock sources. The lack of built-in DC-balance coding can be a disadvantage with AC coupling and when driving optical modules (note the 24-bit SerDes devices include built-in DC balancing, so this limitation only applies to 10-, 16-, and 18-bit SerDes).

8b/10b SerDes works well with byte-oriented cell or packet data. The 8b/10b coding allows for simple error checking and DC balance to reduce Inter-Symbol Interference (ISI) and drive AC-coupled interconnect and fiber optics. However, using 8b/10b SerDes with bus widths that are not byte multiples requires extra design effort to pack the bus into bytes and run the SerDes link with the increased speed.

Table 3-15. Comparison Overview of Advantages/Disadvantages of SerDes Architectures

Technology	Advantages	Disadvantages
Parallel Clock SerDes	Serializes wide buses Low cost Automatic transmitter/receiver sync	More pairs/wires needed Tight pair-to-pair skew requirements
Embedded Clock (Start-Stop) Bits SerDes	10-, 16-, 18- and 24-bit widths available Lock-to-random-data capability Relaxed clocking requirements	No inherent DC balance Not well suited for AC-coupled or fiber applications (except 24-bit devices)*
8b/10b SerDes	DC-balance coding Works well in AC-coupled and fiber environments Widely available	Byte-oriented Tight clocking requirements Requires comma for sync
FPGA-Attach SerDes	LVDS “parallel” interface lowers board traces, EMI, and power FPGA-friendly interface Lock to “any” data Integrated signal conditioners No external reference clock	Requires small “glue” code inside FPGA

**Note the 24-bit SerDes has DC balance and Thus is Appropriate for AC-Coupled or Fiber Applications.*

FPGA-Attach SerDes is ideal for applications that include a FPGA and need to drive high data rates over inexpensive interconnects like CAT-5 cables and FR-4 backplanes. The LVDS “parallel” interface reduces the number of I/Os, power, EMI, and noise sensitivity of the system. The deserializer automatically locks to incoming data without an external reference clock or comma characters for easy “plug-and-go” operation.

3.8 Summary

Over the past ten years, several SerDes architectures have flourished to meet the diverging needs of a growing number of applications. The popularity of FPGAs, desire to reduce board traces, and demand for higher bandwidth is resulting in growing adoption of intelligently-partitioned architectures like the FPGA-Attach SerDes. Understanding the advantages and disadvantages of each allows the designer to fit the SerDes to the application to maximize performance and minimize system cost and complexity.

To achieve optimum performance, high-speed interconnects must be treated as transmission lines. Care must be taken to avoid impedance discontinuities and an appropriate termination network is essential. A proper termination matches the effective impedance (Z_L) of the transmission media thereby minimizing reflections. Though the overall intent of the termination network may always be the same, a considerable number of variables must be considered when deciding on the appropriate termination scheme.

Asking some simple questions can yield important information, for example:

- Is the termination external or internal to the driver or receiver?
- Is the topology point-to-point or multipoint?
- Is the termination DC- or AC (capacitively)-coupled?
- Is the termination also acting as a failsafe or translation network between different technologies?

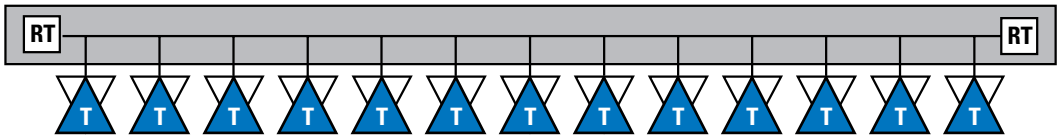
Internal terminations have the advantage of terminating as close as possible to the receiver (minimizing stubs) and also saving board space and reducing component count. A drawback to internal terminations is reduced flexibility. For example, an internal AC termination assumes that incoming data will be DC balanced (see **DC Balance, page 33** for more on this subject). An LVDS receiver with an internal termination may be unsuitable in a multidrop configuration because of additional loading.

4.1 Terminations and Impedance Matching

To avoid reflections, the characteristic impedance Z_0 of the transmission medium must be consistent and equal to the load termination. This task is complicated when the signal path likely includes some combination of vias, connectors, traces, and cables. In addition, the load termination may also be part of a failsafe or translation network. Additional information on these subjects can be found in the **Design and Layout Guidelines Section, page 39,** which includes a discussion on transmission-line theory.

4.2 Multidrop and Multipoint

B-LVDS and M-LVDS both offer higher current drive than conventional LVDS, making these technologies capable of driving multidrop or multipoint applications. (Multidrop has one driver and multiple receivers; multipoint can have multiple drivers and multiple receivers.) In either case, the recommended configuration has matching terminations at each end of the backplane. The termination resistors are selected to match the effective impedance of the backplane. The characteristic impedance of the backplane may be 100Ω, but the additional loading due to connectors and cards may result in an effective impedance of considerably less. For example in the case of the popular Advanced Telecom and Computing Architecture (ATCA), the characteristic impedance of the backplane is 130Ω but because of the additional loading of the cards, each end of the backplane is terminated with 80Ω.



Note – the receivers shown must not have internal terminations.

Figure 4-1. Multipoint Termination Scheme

4.3 AC Coupling

AC coupling is a termination technique where capacitors are placed in series with both signals of the differential pair - in addition to the standard resistive load termination. There are several reasons why this approach is desirable, and these are related to performance, compatibility, and system issues. ***Figure 4-2*** shows an AC-termination scheme and the waveforms on each side of the capacitors. Note the capacitors will block the entire DC component of the signal and therefore only the incident leading and trailing edges will be observed at the receiver. The incident wave will charge the network and then the energy will slowly dissipate based on the RC-time constant.

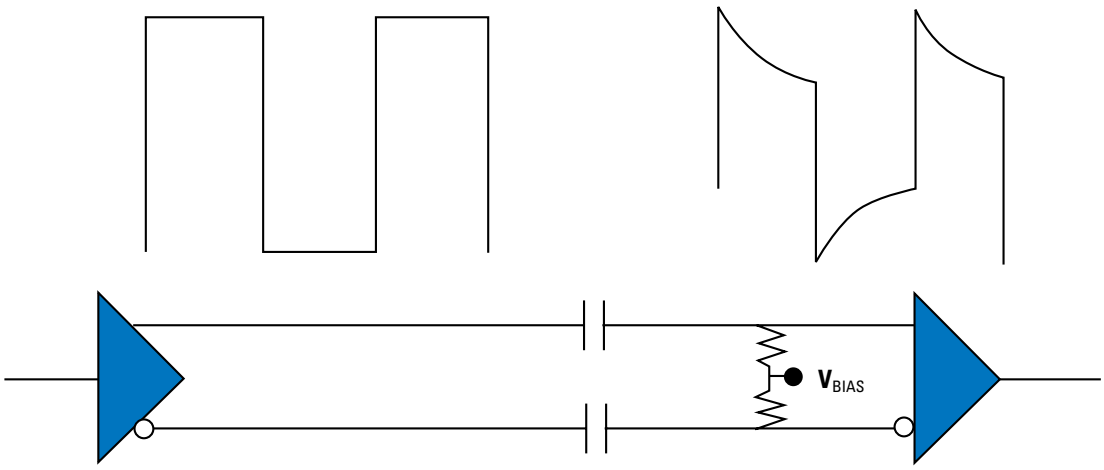


Figure 4-2. AC Coupling and Waveforms

The AC-coupling scheme shown in ***Figure 4-2*** offers the following advantages:

- The input waveform to the receiver will be centered at the bias voltage (V_{BIAS}). This enables the receiver to operate in the device "sweet spot" thereby reducing jitter and improving performance.
- Since CML and LVPECL are not industry standards, there are no hard rules for device thresholds. Assuming drivers and receivers may potentially be from different vendors, then AC coupling eliminates any threshold variation that may exist between different vendors.
- AC coupling eliminates any DC bias between driver and receiver – and therefore is very useful for translating between technologies. (This topic is covered in more detail later).
- Another reason for AC coupling is to guard against differences in ground potential between two cards or systems. If a cable connects two different pieces of hardware with different ground potentials, the voltage offset may affect the operation of the differential pair – or in extreme cases cause reliability issues. AC coupling eliminates the DC potential difference, thus eliminating this problem.

AC coupling is encountered generally with high signaling rates and with CML and LVPECL devices. In fact, many devices incorporate the capacitors into the internal receiver termination. However, one potential drawback with AC coupling is the need for DC-balanced data.

An innovative I/O architecture that demonstrates the benefit of both AC and DC coupling is the input stage of the DS64EV400 variable equalizer. This device tolerates threshold and common-mode-translation variations as seen in AC coupling, but does not require DC-balanced data.

4.4 DC Balance

DC balance refers to the difference between the absolute number of ones and zeros in a set of data, where an overall equal number of zeros and ones are considered "DC balanced". DC balance is important because when blocking capacitors are used, current only flows into the receiver termination network during transitions. Without transitions, the charge on the two receiver terminals will slowly decay towards the same value, thereby reducing noise margin.

Figure 4-3. AC-Coupled Differential Pair at Startup

Figure 4-3 shows an example of an AC-coupled circuit at startup. Initially both input terminals are at 1.2V. As the first positive transition bit arrives, each terminal follows the input waveform and makes a maximum excursion in opposite polarities. As the next negative transition bit arrives, there is very little differential voltage between the two terminals and a high likelihood of bit errors. After a sufficient number of balanced bits have been transmitted (equal numbers of ones and zeros), each receiver terminal transitions between 1.0V and 1.4V, resulting in the maximum noise margin. This example describes a startup condition but is similar to what happens with long strings of bits with the same polarity or unbalanced data. Unbalanced data reduces noise margin because the maximum differential between the receiver terminals is not maintained.

Various coding schemes such as the common 8b/10b ensure a high degree of DC balance. Although DC balance is used to describe an entire data set, there are other metrics that describe short-term deviations from ideal.

Value (Decimal)	Value (Binary)	10-bit Code	Alternative Code
	HGF EDCBA	abcdei fghj	abcdei fghj
0	000 00000	100111 0100	011000 1011
1	000 00001	011011 0100	100010 1011
2	000 00010	101101 0100	010010 0011
3	000 00011	110001 1011	110001 0100
4	000 00100	110101 0100	001010 1011
5	000 00101	101001 1011	101001 0100
6	000 00110	011001 1011	011001 0100
7	000 00111	111000 1011	000111 0100
8	000 01000	111001 0100	000110 1011
9	000 01001	100101 1011	100101 0100
10	000 01010	010101 1011	010101 0100
⋮	⋮	⋮	⋮

Figure 4-4. Example of 8b/10b Codes

Running Disparity (RD) is a calculation of the instantaneous deviation from DC balance. When considering a set of DC-balanced data, the maximum value of RD would then be the worst-case deviation from ideal at any point in time.

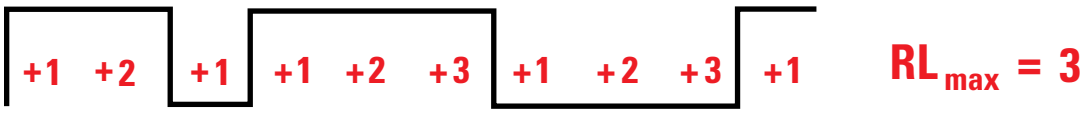


Figure 4-5. Example of Run Length

Run Length (RL) is the instantaneous number of consecutive similar bits. For an entire set of data, the maximum value of run length would again be the worst-case deviation from ideal.

Run length is an important parameter affecting jitter. Deterministic jitter is minimized when signal transitions cross the zero threshold at the exact bit width. Long run lengths result in RC decay that reduces the signal amplitude, therefore closing the eye – and resulting in increased deterministic jitter. A sufficiently large capacitor will help maintain signal amplitude.

Selecting a Capacitor

The RC time constant, bit width (f), and run length determine the amount of signal attenuation (droop) due to AC coupling. Smaller capacitors are desirable for board space reasons but larger capacitors will reduce signal droop. The following equation provides a rough approximation of the capacitor value that ensures only 0.25 dB signal droop (3%).

$$C = \frac{(7.8 \times \text{Run Length} \times \text{Bit Period})}{R}$$

Typical capacitor sizes for high-speed applications range between 0.1 µF and 0.01 µF.

4.5 Translation

It is common for systems to contain a mix of high-speed differential technologies making translation often necessary.

The most widely used differential technology is LVDS, and fortunately, it is the easiest to use when translation is necessary. LVDS inputs have the widest common-mode-input range of any of the high-speed differential technologies. This input flexibility allows National Semiconductor's LVDS products to interface directly with most CML and LVPECL devices.

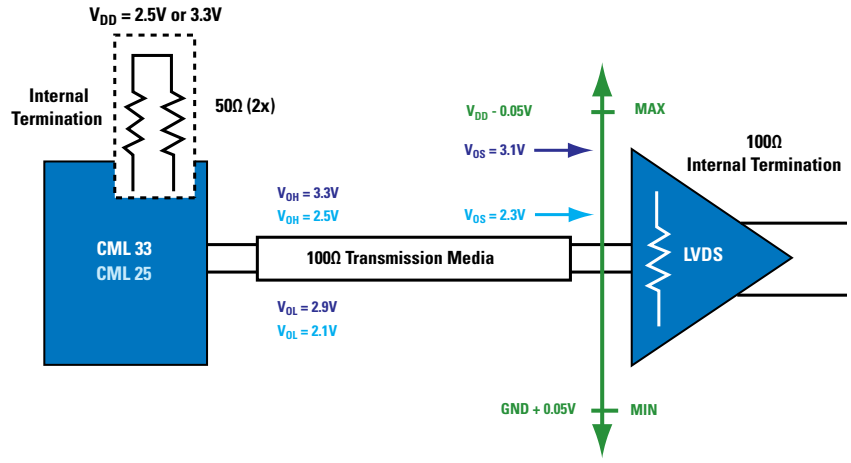


Figure 4-6. CML to LVDS

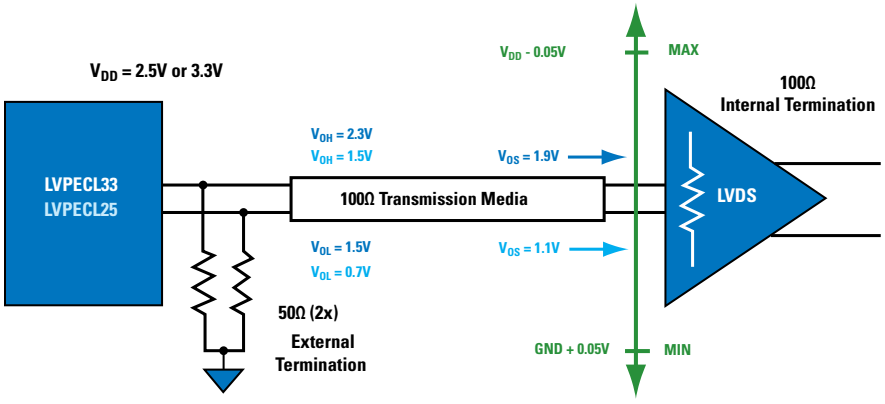


Figure 4-7. LVPECL to LVDS

Due to the wide range of input common-mode voltages, LVDS inputs can be considered a universal differential receiver.

The CML and LVPECL inputs often hold incoming signals to a much narrower input common-mode voltage. This can leave the LVDS output voltage outside the specified input range for CML receivers as shown in ***Figure 4-8***.

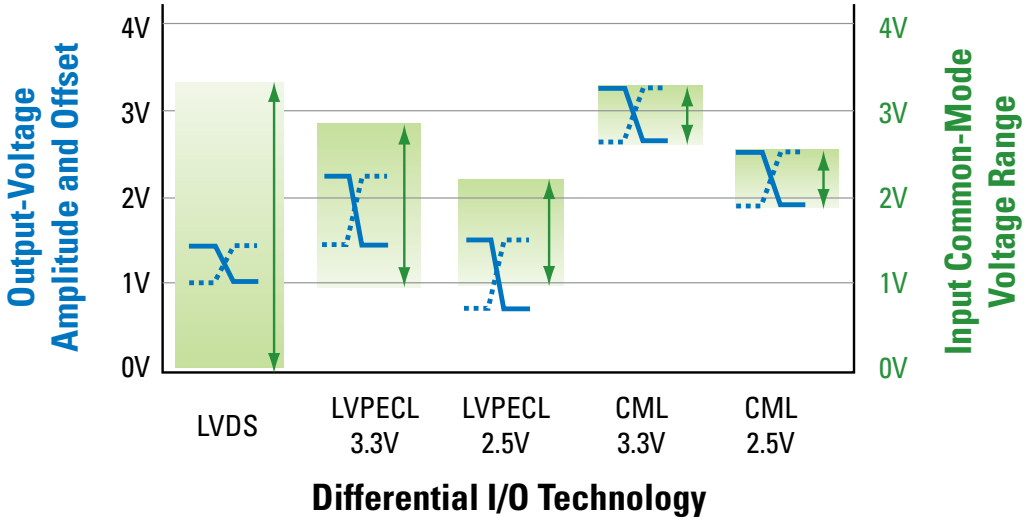


Figure 4-8. Differential Technologies

When translating differential signals from LVDS to LVPECL or CML, it is always important to investigate the input characteristics of the receiving device. LVPECL and CML I/O characteristics and termination schemes can vary from one device and manufacturer to another.

Based on datasheet specifications common to most IC vendors, the LVPECL and CML interfaces shown in ***Figures 4-9 and 4-10*** will be the best choice in the vast majority of cases. Specific LVPECL or CML devices may require some interface modifications for optimal performance.

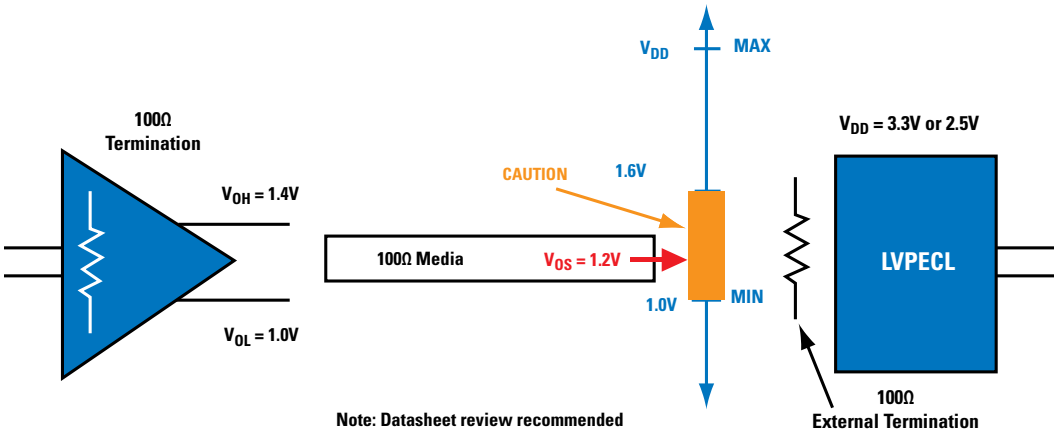


Figure 4-9. LVDS to LVPECL

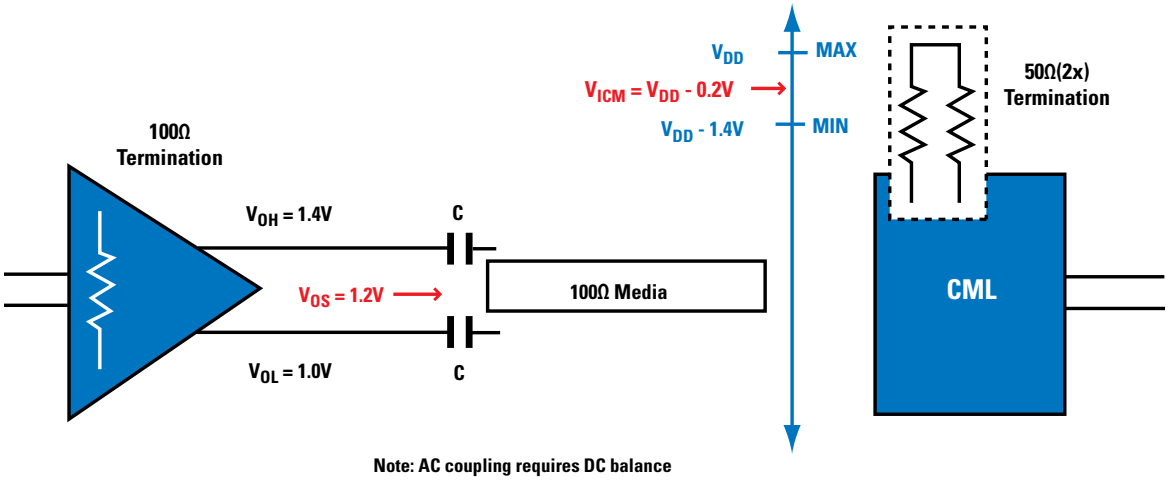


Figure 4-10. LVDS to CML

As shown in the previous figures, LVDS and other differential technologies can work together in a high-speed signal path. Three of the four interface possibilities with LVDS do not require any additional external components. In the final case where LVDS drives CML, most CML-only applications would already use AC coupling. AC coupling for high-speed signals does not represent a significant constraint in many applications since signal encoding has gained widespread market acceptance.

4.6 Failsafe

LVDS inputs often include a failsafe circuit that sets the corresponding output to a HIGH condition in the event of an open or short at the device input. Under normal conditions, internal failsafe circuits are sufficiently robust to prevent oscillations due to local cable faults or solder opens or shorts at the inputs. In very noisy environments or if a long cable is disconnected, the internal failsafe may not be sufficient to prevent oscillations. In this case, a shielded cable is recommended or a resistor network may be added to boost the strength of the internal failsafe.

Selecting a failsafe network is a compromise between ensuring sufficient margin to avoid possible oscillations and not impairing the balance and sensitivity of the receiver. **Application Note AN-1194, Failsafe Biasing of LVDS Interfaces**, provides a thorough discussion of this subject.

M-LVDS Failsafe

The TIA/EIA-899 (M-LVDS) standard describes a built-in failsafe required for type-2 receivers. Type-2 receivers include a 100 mV offset so the device switch point is offset from 0V by 100 mV. This is an effective failsafe but has the drawback of reducing noise margin and potentially affecting duty cycle in a clock application.

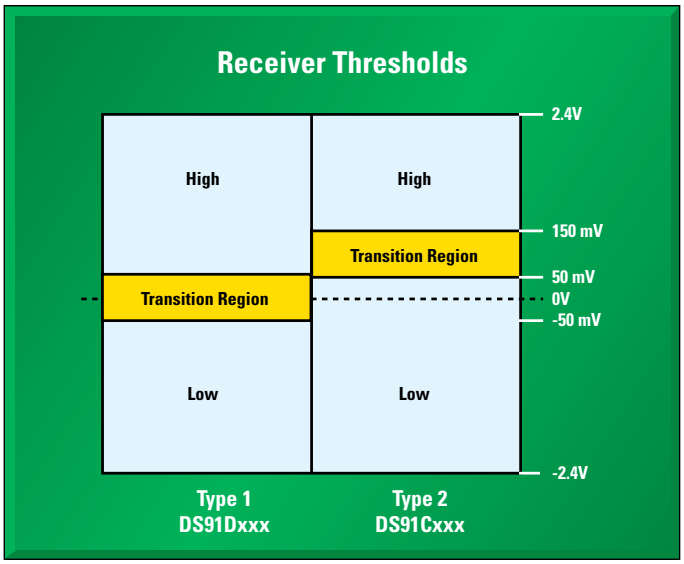


Figure 4-11. M-LVDS

The built-in offset also makes type-2 receivers ideal as the common receiver in "Wired–Or" logic applications. A wired-or enables multiple cards or devices to share a single differential pair for signals such as interrupts. If allowed to float the type-2 receiver will stay in a logic low state. Any device can then generate an interrupt by pulling the line to a logic high.

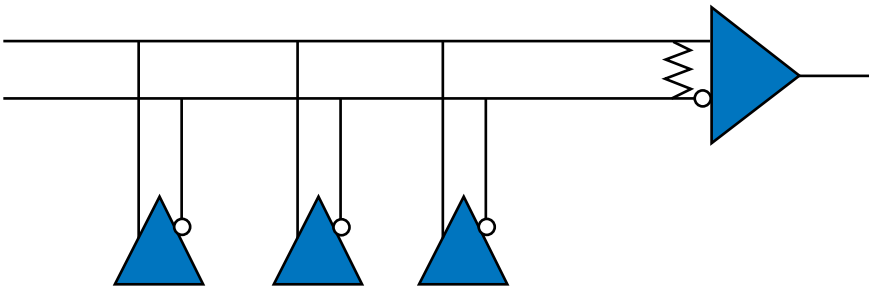


Figure 4-12. Example of Wired-Or Circuit

5.1 PCB Transmission Lines

Figure 5-1 depicts several transmission line structures commonly used in printed circuit boards (PCBs). Each structure consists of a signal line and a return path with uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The structure's dimensions along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. ***Figure 5-1*** shows examples of edge-coupled microstrips, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as "differential pair". The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent; for example, S is less than 2W, the differential pair is called a "tightly-coupled differential pair". To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

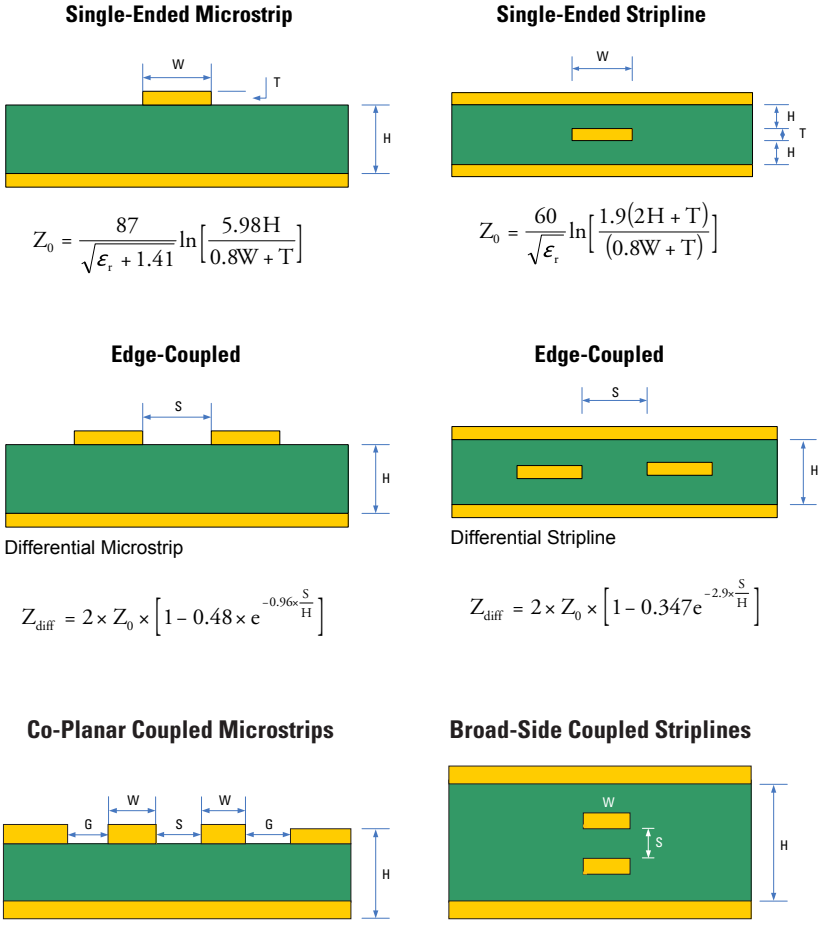


Figure 5-1. Controlled-Impedance Transmission Lines

5.2 Transmission Loss

At frequencies below approximately 1 GHz, transmission loss is dominated by skin loss that is proportional to the square root of the frequency. At higher frequencies, it is dominated by dielectric loss that is proportional to the frequency. The material properties of the board highly influence the transmission loss of the board trace. ***Figure 5-2*** shows the loss of 10-inch coupled microstrips of identical dimensions built with Nelco4000-6, Getek, and Roger materials.

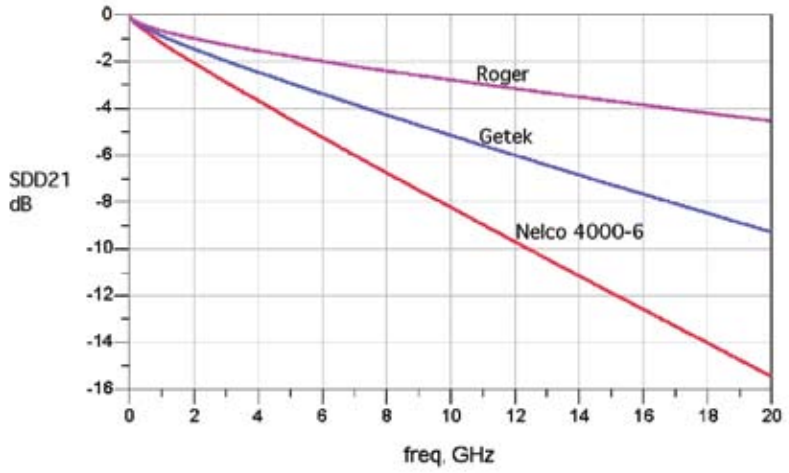


Figure 5-2. 10-Inch Microstrips Implemented with Different Board Materials

Figure 5-3 shows the loss of coupled microstrips and striplines of the same width implemented with Nelco4000-6 material. Striplines reside in the inner layer surrounded by the dielectric material that has higher dissipation than air. Striplines have higher dielectric loss than microstrips.

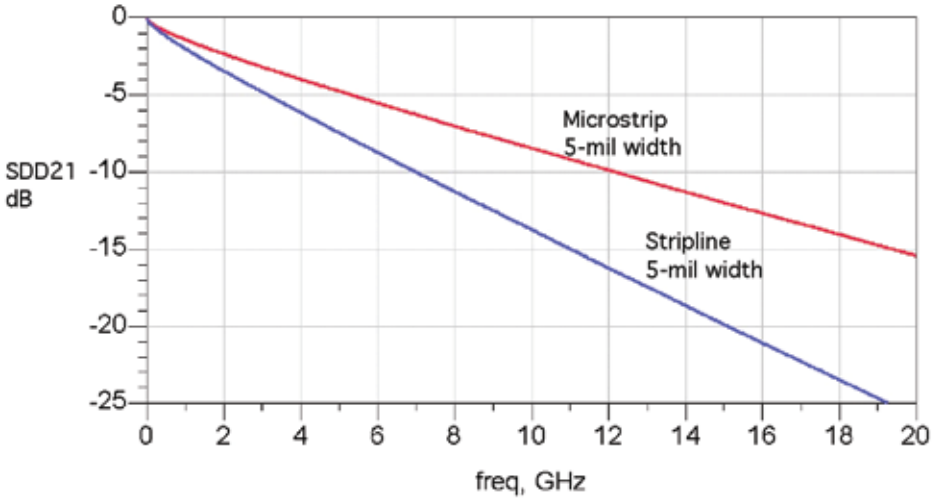


Figure 5-3. 10-Inch Coupled Microstrips and Striplines Implemented with Nelco4000-6

5.3 PCB Vias

Via is a term commonly used to refer to a plated through hole that connects signal traces on two layers of a printed circuit board. A via structure consists of donut-shaped pads, the plated cylindrical via barrel, and the clearance anti-pad at each power or ground layer. ***Figure 5-4*** depicts a 3-dimensional diagram of a via.

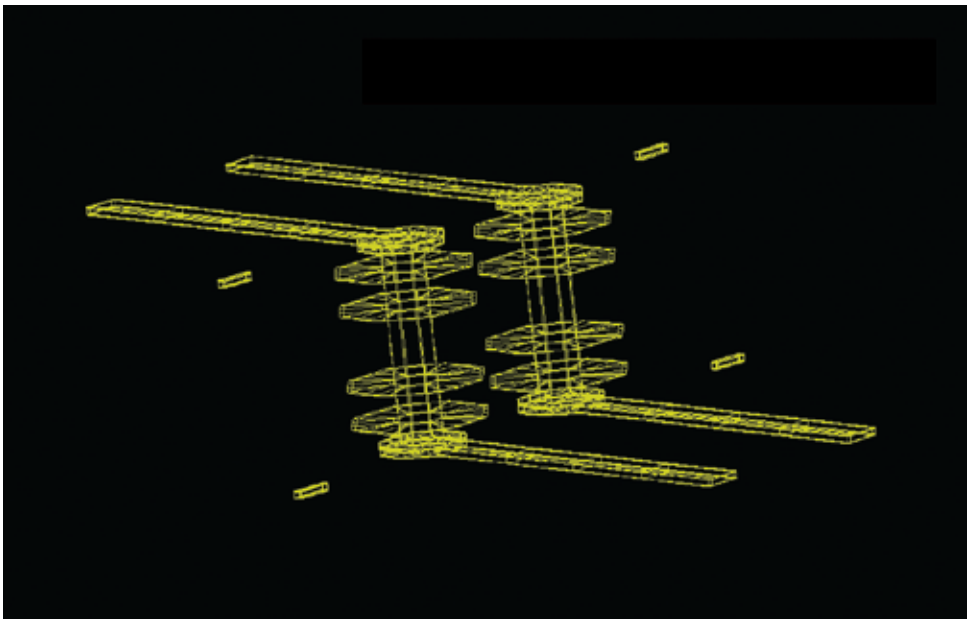


Figure 5-4. A 3-Dimensional Diagram of a Differential Via

The via's electrical behavior depends on the dimensions of the via, the stack-up of the board, as well as the board's material properties. The cylindrical barrel behaves as an inductor, while the pads and anti-pads have capacitive behavior. For a via with fine hole size, the overall effect of the via structure behaves as a small inductor. For a via with larger hole size and multiple power or ground layers, the via will exhibit capacitive behavior. With the help of a 3-D electromagnetic field solver, it is possible to design a via structure with controlled impedance.

Figure 5-4 illustrates a structure with two mutually-coupled differential vias with 100Ω differential impedance. In addition to the via dimensions, the distance between the two vias determines the mutual coupling and effect of the differential impedance.

For a signal via that connects from the top layer to an inner layer, the unused portion of the via that runs from the inner layer to the bottom layer creates a via stub. The via stub introduces added parasitic capacitance to the signal trace, reducing its bandwidth. For very-high-speed applications, an advanced board manufacturing process is used to precisely counter-bore the unused portion of the via. This counter-coring eliminates the existence of the via stub.

A buried via is used to connect two inner layers. The length of the via runs only through the dielectric that separates the two layers, thereby avoiding the creation of the via stub.

5.4 Backplane Subsystem

In a typical board, signals travel through an interconnect that consists of board traces, component landing pads, vias, and components. The parasitic capacitance of landing pads and vias introduces impedance mismatch from the characteristic impedance of the board trace. A change in trace width or spacing between a differential pair also creates an impedance mismatch. Excessive parasitic capacitance introduces insertion loss that is no longer linear with frequency, degrading the signal integrity of a high-data-rate transmission.

In a backplane subsystem, connectors link two cards together through an interconnecting backplane. ***Figure 5-5*** shows a simplified diagram of a typical backplane subsystem.

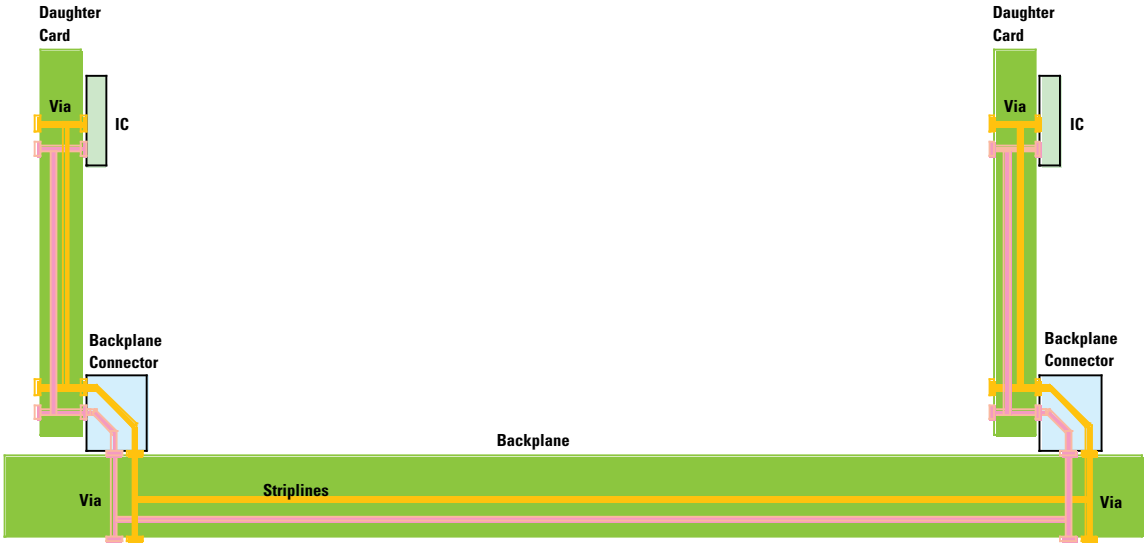


Figure 5-5. A Simplified Backplane Subsystem

For mechanical robustness, most backplane connectors are press-fit with plated through holes in a thick backplane. ***Figure 5-6*** illustrates the internal conductor structures in a backplane connector. A typical backplane may have a board thickness of 0.15 to 0.2 inches, and contains 10 to 20 layers for signal, power, and ground planes. The long vias with relatively large hole size (about 26 mil diameter) are highly capacitive and are notorious contributors to bandwidth reduction as well as crosstalk.

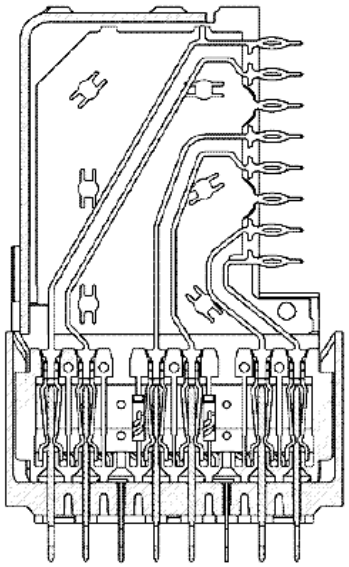


Figure 5-6. Cross-Section of VHDM HSD (Graphic Courtesy of Teradyne Inc.)

Figure 5-7 shows the transmission loss and crosstalk of a 20-inch backplane. In addition to the dielectric loss from board traces, there are losses caused by the parasitic capacitance of connectors, vias, via stubs, and component landing pads. The crosstalk from adjacent channels will negatively impact the Signal-to-Noise Ratio (SNR) of the victim line. Crosstalk is usually the factor that limits the maximum data rate of a backplane subsystem.

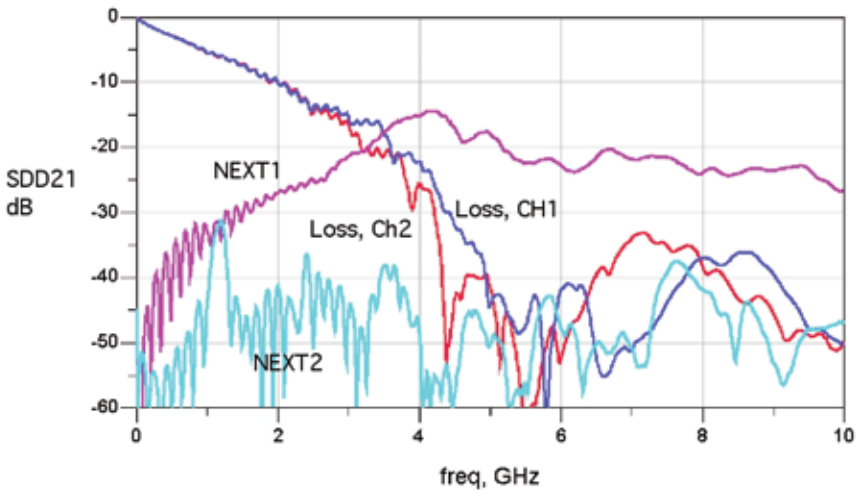


Figure 5-7. Transmission Characteristics of a 20-inch Backplane

5.5 Decoupling

Each power or ground lead of a high-speed device should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

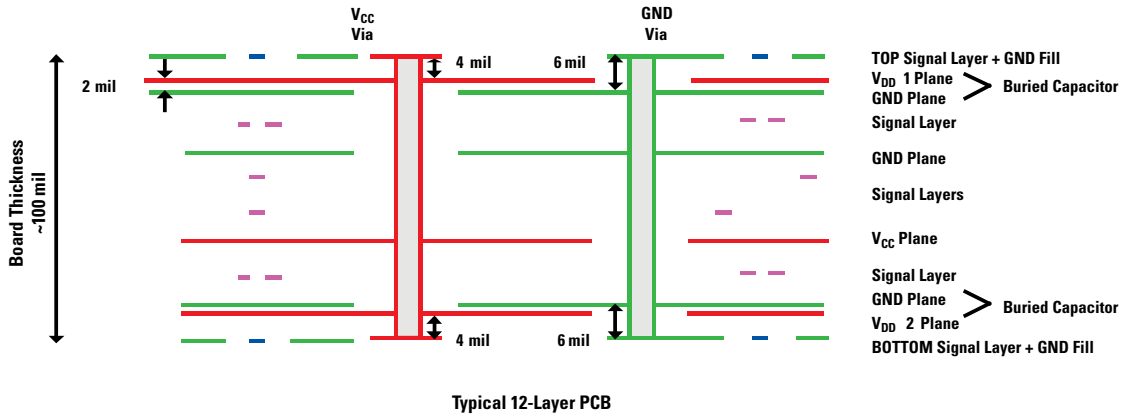


Figure 5-8. Low-Inductance, High-Capacitance Power Connection

Bypass capacitors should be placed close to V_{DD} pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402 or even 0201, or X7R surface-mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in ***Figure 5-8a***.

(a) (b)

Figures 5-8a and 5-8b. Typical Decoupling Capacitor Layouts

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 µF, and 0.1 µF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Refer back to ***Figure 5-1*** for some examples.

Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center dap must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the dap connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes (as shown in ***Figure 5-1***) creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility.

In many cases the GND dap that is so important for heat dissipation makes the optimal decoupling layout impossible to achieve due to insufficient pad-to-dap spacing as shown in ***Figure 5-8b***. When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the V_{DD} via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This will result in a poor solder connection.

6.1 Introduction

Referring to ***Figure 6-1***, jitter has both deterministic and random components. Deterministic Jitter (DJ) comes from system sources such as crosstalk, inter-symbol interference, and power-supply feed through. It is bounded, so it can be characterized by its peak-to-peak value. Random Jitter (RJ) comes from physical sources such as thermal noise, shot noise, and scattering in optical media. The classic way to characterize random jitter is through its probability density function, which is typically Gaussian in shape. Gaussian functions are infinite in extent, so the random component of total jitter is unbounded.

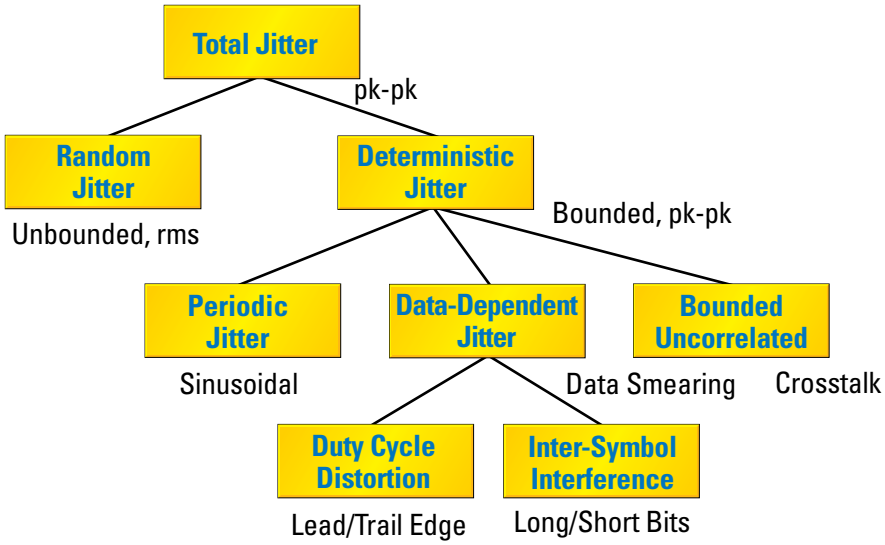


Figure 6-1. Jitter Components

Random Jitter Characteristics

Random jitter is characterized by a Gaussian distribution and is assumed unbounded. To measure these types of jitter, the distribution is quantified by the standard deviation and mean. Since RJ can be modeled as a Gaussian distribution, it can be used to predict peak-to-peak jitter as a function of Bit Error Rate (BER).

Common sources of RJ include shot noise, flicker noise, and thermal noise. Shot noise is broadband "white" noise generated when electrons and holes move in a semiconductor. Shot-noise amplitude is a function of average current flow. Flicker noise has a spectral distribution that is proportional to 1/f. The origin of flicker noise is a surface effect due to fluctuations in the carrier density as electrons are randomly captured and emitted from oxide interface traps. Thermal noise can be represented by broadband "white" noise, and has flat spectral density. It is generated by the transfer of energy between "free" electrons and ions in a conductor.

Deterministic Jitter

There is much more complexity in the deterministic types of jitter. There are data-dependent types such as Duty Cycle Distortion (DCD), which is the result of any difference in the mean time allocated for the logic states in an alternating bit sequence (e.g. 0,1,0,1). This can be caused by different rise and fall times and threshold variations of a device.

DCD and Inter-Symbol Interference (ISI) are functions of the data history that occur when the transition density changes, caused by the time difference that is required for the signal to arrive at the receiver threshold when starting from different places within the bit sequence (symbol). Also, ISI occurs when the transmission medium propagates the frequency components of data (symbols) at different rates; for example, when jitter changes as a function of edge density.

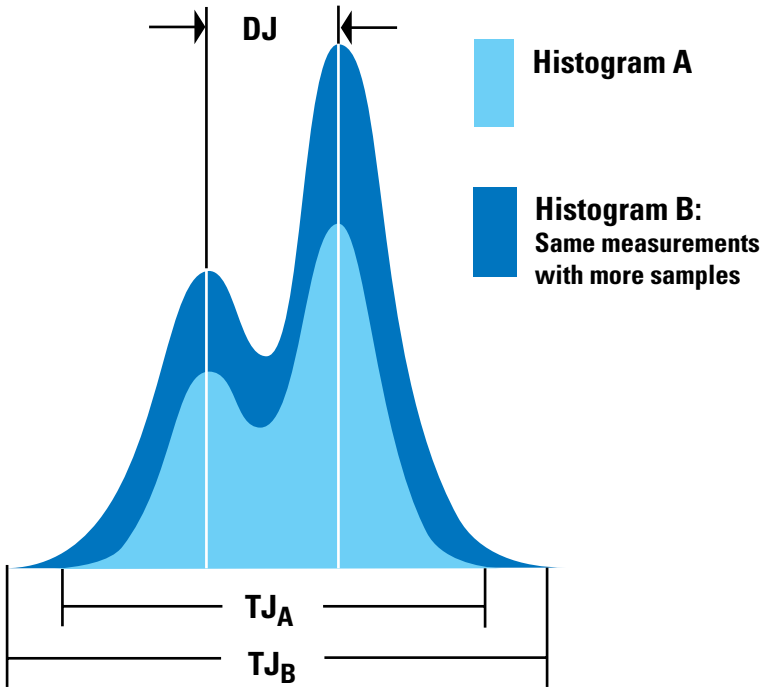


Figure 6-2. Total Jitter Histogram

The Total Jitter (TJ) histograms represent the Tj Probability Density Function (PDF), therefore if the DJ and RJ process are independent, the total PDF is the convolution of the DJ and RJ PDF. Removing DJ from the histogram would produce a Gaussian distribution. Adding DJ to the histogram broadens the distribution while maintaining Gaussian tails, effectively separating the mean of the left and right distributions. The difference between the two histograms means is the DJ, and the tail portions represent the RJ component. Since DJ is bounded, the value does not change as additional measurement samples are accumulated. The RJ component of the total jitter continues to increase as the sample size increases since random jitter is unbounded.

Duty Cycle Distortion

There are two primary causes of Duty Cycle Distortion (DCD) jitter. If the data input to a transmitter is theoretically perfect, but if the transmitter threshold is offset from its ideal level, then the output of the transmitter will have DCD as a function of the slew rate of the data signal's edge transitions.

The waveform represented by the dotted line in ***Figure 6-3*** shows the ideal output of a transmitter with an accurate threshold level set at 50% and with a duty cycle of 50%. The solid line waveform represents a distorted output of a transmitter due to a positive shift in the threshold level. With a positive shift in threshold level, the resultant output signal of the transmitter will have less than 50% duty cycle. If the threshold level is shifted negatively, then the output of the transmitter will have greater than 50% duty cycle.

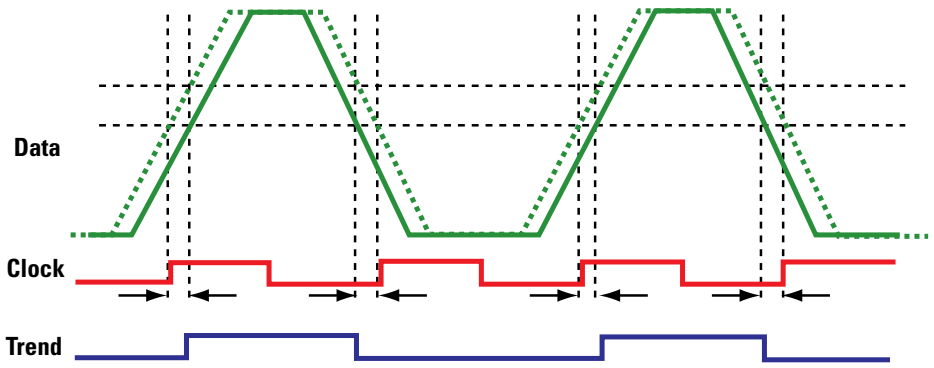


Figure 6-3. DCD Jitter Causes Timing Shifts

Measuring Time Interval Equivalent (TIE) relative to the software-generated best-fit clock results in a positive timing error on the rising edge of each data bit and a negative timing error on the falling edge of each data bit. The resultant TIE trend waveform will possess a fundamental frequency equal to half the data rate. The phase of the TIE trend waveform relative to the data signal will depend on whether the threshold shift is positive or negative.

With no other sources of jitter in the system, the peak-to-peak amplitude of DCD jitter will be theoretically constant across the entire data signal. Unfortunately, other sources of jitter such as ISI which almost always exist make it sometimes difficult to isolate the DCD component. One technique to test for DCD is to stimulate the system/components with a repeating 1-0-1-0… data pattern. This technique will eliminate ISI jitter and make viewing the DCD within both the trend and spectrum waveform displays much easier. Using the jitter spectrum display, the DCD component of jitter will show up as a frequency "spur" equal to half the data rate.

Another cause of DCD is asymmetry in rising and falling edge speeds. A slower falling edge speed relative to the rising edge will result in greater than 50% duty cycle for a repeating 1-0-1-0… pattern, and slower rising edge speeds relative to the falling edge will result in less than 50% duty cycle.

Inter-Symbol Interference

Inter-Symbol Interference (ISI), a form of Data-Dependent Jitter (DDJ), occurs when the bandwidth of the transmission medium and/or components is lower than the bandwidth of the transmitted signal. From a time-domain perspective, transmission-path bandwidth limitations slow down the edge rates of the transmitted signal. For a periodic signal such as a clock, this edge rate reduction will round signal edges and potentially attenuate the signal. For data, however, slower edge rates can affect actual 1-0 and 0-1 transition timing.

Consider the waveform in ***Figure 6-4***. The 1010 pattern prior to point "A" has uniform bit-pulse widths and transition timing. A series of consecutive 1s at point "A," however, charges the transmission medium to a higher voltage, requiring longer to transition to zero at point "B." This late transition to zero is then followed by an early transition to 1 at point "C" because the signal did not have time to reach a full steady-state low level.

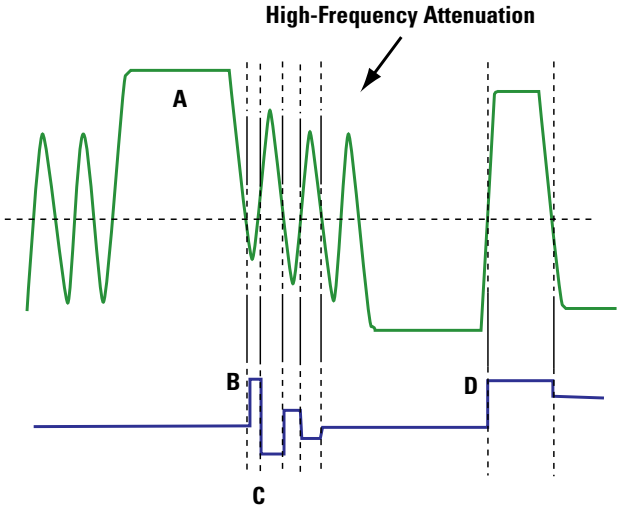


Figure 6-4. An Example of ISI-Pattern-Dependent Jitter and Reflections

The jitter caused by ISI is dependent on the pattern that is sent. Data patterns with longer run lengths will therefore tend to have higher jitter if the transmission medium bandwidth is limited. For example, in a bandwidth-limited situation, PRBS-23 (run length = 23) will exhibit slightly higher ISI DJ than PRBS-7 (run length = 7) or 8b/10b (run length = 5).

The negative peak amplitude of the next "0" bit preceded by a long string of "1s" will be attenuated for two reasons. First, the preceding long string of "1s" means the signal will take longer to transition to a true low level since the data signal starts from a higher initial level. Secondly, the following "1" bit causes the signal to reverse direction before it even reaches a solid low level. This reduction in signal amplitude will produce a negative timing error on the next transition to a "1" since the signal has a very short distance to travel to reach the threshold level. This is illustrated at point "C" on the jitter trend waveform.

The positive timing error illustrated at point "D" on the jitter trend waveform follows the same logic as the positive timing error at point "B" previously discussed. With a long string of "0s", the data signal has sufficient time to settle to a full steady-state low level. When this signal then transitions back to a high level, it again has a longer transition time to reach the threshold level, and therefore produces a positive timing error.

Reflections from transmission-path-impedance discontinuities and improper termination can also cause ISI. Impedance discontinuities not only reduce bandwidth, but their reflections can also affect transition timing if the reflected signal reaches the transmitter or receiver near or during an edge transition. The arrows in ***Figure 6-5*** show that reflections from one edge transition may not show up on the high-speed data signal until several bits later. If a reflection appears at the transmitter or receiver during an edge transition (point "C"), this will appear as DDJ on the signal eye pattern.

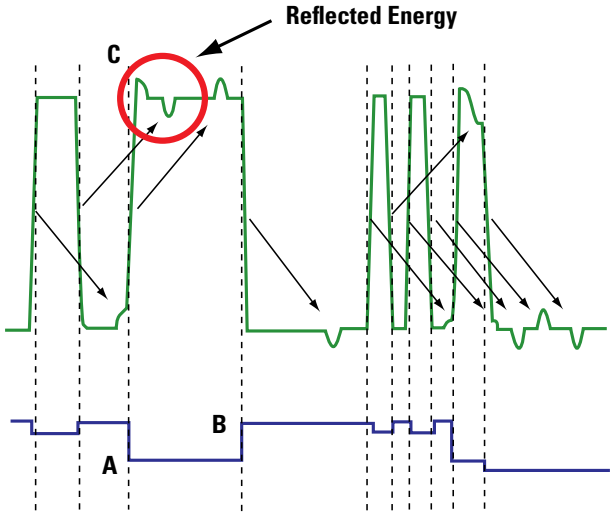


Figure 6-5. An Example of ISI-Pattern-Dependent Jitter and Reflections

Jitter due to reflections should be minimized by reducing impedance discontinuities and by using proper termination placed as close as possible to the end(s) of the transmission line. Jitter due to bandwidth limitations can be minimized by choosing a higher bandwidth-transmission medium and/or employing chips with transmit pre-emphasis and/or receive equalization.

Another common cause of ISI besides bandwidth limitations is signal reflections due to improper terminations or impedance anomalies within the physical media. Signal reflections will produce distortions in the amplitude of the data signal as shown on the right side of the figure. Depending on physical distances between impedance anomalies, reflections produced by one pulse may not appear on a high-speed data signal until several bits later in the serial pattern.

Periodic Jitter

Periodic Jitter (PJ) is also known as sinusoidal jitter and it repeats at a fixed frequency. PJ is quantified as a peak-to-peak number with a frequency and magnitude. This type of jitter is composed of repetitive effects not correlated to the data stream. The two prime offenders are crosstalk and switching-power-supply noise.

Figure 6-6. Example of Periodic Jitter

A special type of PJ called Spread Spectrum Clocking (SSC) is used in many computer interfaces such as PCI Express and Serial ATA to improve the EMI performance of the interface. It takes the form of Frequency Modulation (FM) of the data clock. This has the effect of spreading the radiated energy across more of the frequency spectrum and lowering the power at any one frequency. SSC also reduces the likelihood that the device will interfere with the operation of some other piece of equipment.

6.2 Additional Jitter Sources

Media over which data and clock are transmitted is generally the largest contributor of jitter in a link. However, there are some other contributors that, with careful design of the system, will remain small contributors to the jitter budget. This category of additional contributor can be classified under the umbrella of Deterministic Jitter (DJ) which includes additional Data-Dependent Jitter (DDJ) from input capacitance, Periodic Jitter (PJ) due to crosstalk of adjacent channels, and DDJ due to pattern dependencies. Eye diagrams will be used to analyze the different dependencies of the jitter.

Effect of Input Capacitance

Input capacitance is another source of ISI similar to the capacitance from a via or connector. This capacitance can affect serial or multipoint links by serving as a lowpass filter that slows down edge rates and adds jitter. For example at 1.5 Gbps, a 5 pF load due to the capacitance of an input will cause additional jitter at the input of a device when the device is driven by a 50Ω driver such as a self-terminated LVDS output. This jitter induced by input capacitance is related directly to the type of pattern and speed of the pattern applied.

To transmit zero jitter through a buffer, the buffer must have a small amount of equalization to counteract the jitter induced by the input capacitance. Keeping input capacitance as low as possible contributes to lower jitter and less eye noise and degradation.

FEXT/NEXT

Far-End Crosstalk (FEXT) and Near-End Crosstalk (NEXT) contribute to periodic jitter that can degrade system performance from adjacent channels of data and/or a clock. An aggressor channel can reduce the signal-to-noise ratio (SNR) of the victim channel thereby increasing the amount of DJ in the victim channel. There are two types of crosstalk: FEXT where crosstalk noise is injected into the victim channel at the far end of a channel and measured at a receiver, and NEXT where crosstalk noise usually from an adjacent transmitter is injected at the receive end and measured at the receive end. *Figure 6-7* illustrates NEXT where an adjacent transmitter adds crosstalk noise to a receive channel and FEXT where an adjacent transmitter on the far end can add crosstalk noise that is attenuated by the channel.

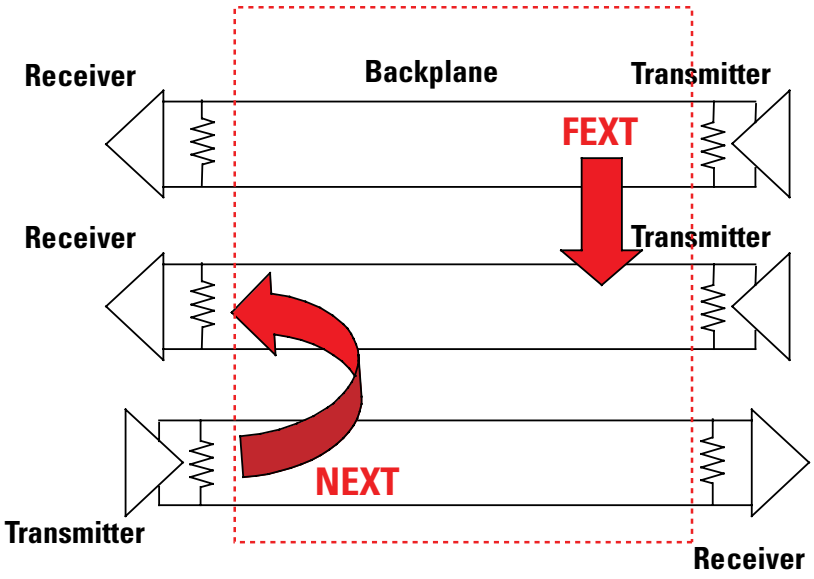


Figure 6-7. Far-End and Near-End Crosstalk Examples

Systems Susceptible to Crosstalk

Crosstalk becomes an increasing concern as boards are packed tighter, component pitches become smaller, and ever-higher frequencies are sent through connectors. ***Figure 6-8*** shows how NEXT can become a concern in a system. At lower frequencies, channel loss is relatively low so that the signal-to-noise ratio at the receiver is high. As frequencies increase so does the crosstalk, while the loss in the channel due to finer trace widths, vias, connectors, and other non-idealities increase as well. The result is receive SNR becomes lower, increasing jitter and closing the eye at the receiver.

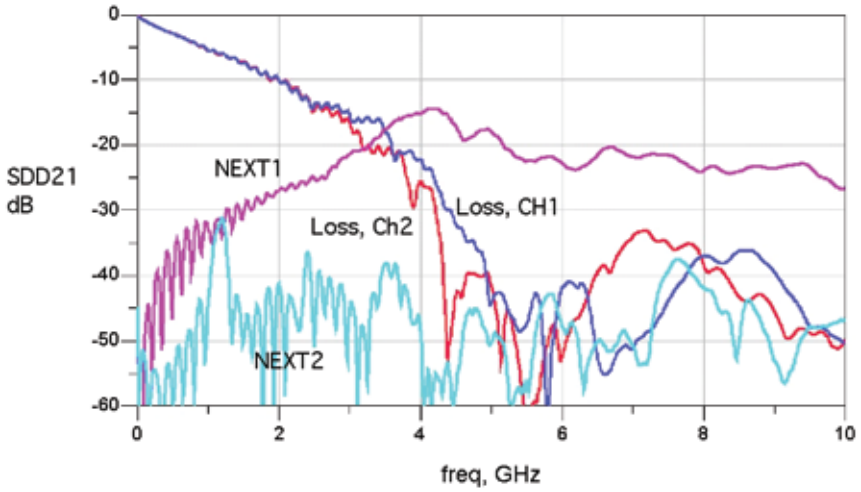


Figure 6-8. Example of Backplane Loss and Crosstalk SDD21 Characteristics

When using signal conditioning and considerable near-end crosstalk exists, consider using pre-emphasis on the transmitter end in the system to maintain a higher SNR on the receiver end rather than using equalization. The equalizer will boost the high-frequency components of the incoming signal regardless of whether it is a signal or crosstalk. On the other hand, adding pre-emphasis to a signal may increase the amount of NEXT with which a channel has to contend. Good board layout practices can reduce the amount of FEXT and NEXT in a system.

Bit Error Rate

Applications such as communications often must guarantee a very stringent Bit Error Rate (BER) such as less than 1-bit error in 10^{12} or 10^{15} bits. The total jitter will determine the extent of bit errors. Since total jitter includes random jitter, the established method to fully guarantee these bit error rates is by sending enormous amounts of pseudo-random data and validating each bit for errors in a technique known as Bit-Error-Rate Testing (BERT). BERT for large-bit error rates is time-consuming and is therefore impractical for everyday use. Instead, engineers use techniques such as eye patterns, eye masks, and bathtub curves to verify suitable signal integrity and then extrapolate to a bit error rate.

6.3 Pattern Dependencies and Eye Diagrams

Eye diagrams are a very good graphic illustrator of jitter and other observed receiver eye attributes. Qualitative measurements of receiver or transmitter eye characteristics such as rise/fall time, overshoot, ringing, loss, and zero-crossing jitter can be observed. For example, sending various data patterns with increasing run lengths of identical digits through FR4 media will give increasing amounts of ISI in the form of DJ due to the dielectric and skin-effect loss in the media.

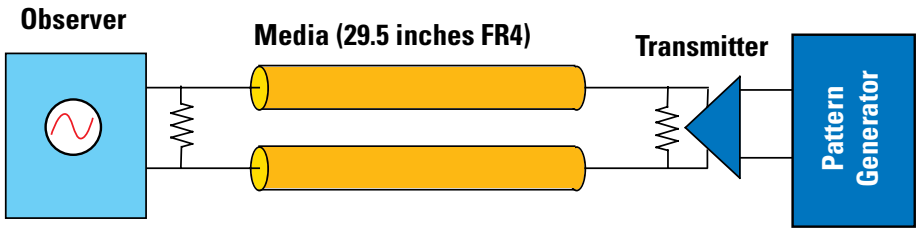


Figure 6-9. Block Diagram Figure Showing Eye Diagram Test Set-Up

As seen in ***Figure 6-10***, as the pattern run length increases, increasing amounts of jitter can be observed due to longer runs of identical digits. As an example, the K28.5 pattern from 8b/10b encoding is made up of run lengths of five followed by a run length of one, a Pseudo-Random-Bit Sequence of length seven (PRBS 7) pattern will have a maximum run length of seven ones followed by six zeros at some point in its pattern. Likewise, a PRBS 31 will have run lengths of 31 ones and 30 zeros.

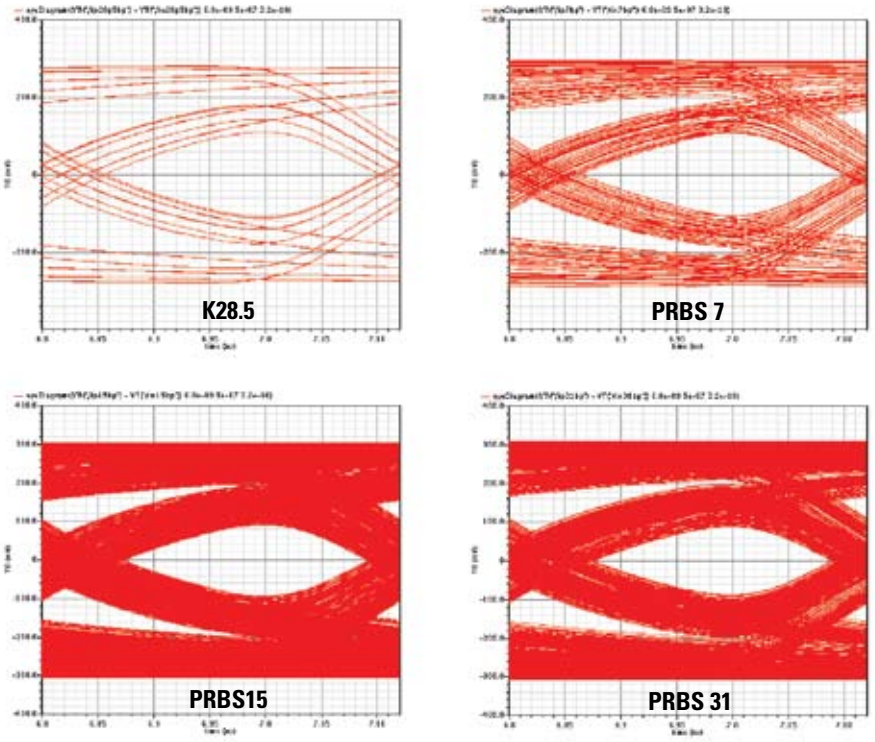


Figure 6-10. Eye Diagrams Showing Increasing Amount of DJ with Increased Run Lengths in Data Patterns

To illustrate further the degradation with pattern run length, the K28.5 pattern and the PRBS 31 pattern are compared in ***Figure 6-11*** where the degradation of the eye can be seen. The K28.5 pattern with its short runs of one and five does not stress the eye as much as the PRBS 31 pattern. The PRBS 31 pattern closes the eye by an additional 60 mV in the vertical and 83 ps in the horizontal direction of the eye. For this reason, the 8b/10b pattern is used in many applications to limit the runs of ones and zeros.

When looking at an eye pattern, it is important to be aware of the amount of time taken to acquire data points for the eye pattern to ensure the worst-case data-run length is captured. For a PRBS 31 pattern, the worst-case run lengths repeat only once per pattern, so for a 3.125 Gbps signal, a PRBS 31 repeats 320 ps x 2^{31} = 0.687s. Thus, to gather enough samples to populate an eye diagram will take a significant amount of time. This is the reason that alternate methods of analyzing the eye have been developed, such as bathtub curves.

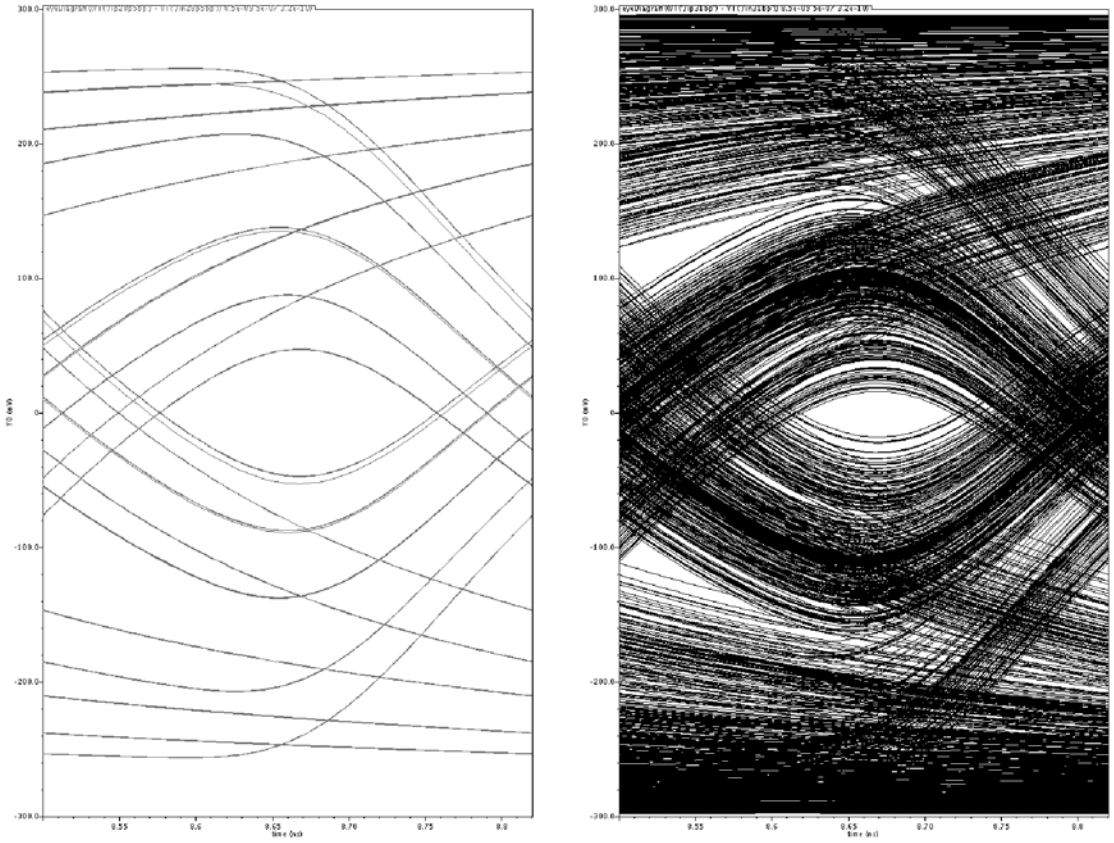


Figure 6-11. Comparison of a K28.5 Pattern (Left) with PRBS 31 Pattern (Right) after 41 Inches of FR4 Media. Plot Shows Degradation of Eye with Pattern Run Length.

Eye Masks

Eye masks, when used with eye diagrams, are another useful tool used in many standards to check for compliance of a signal. The eye mask is a specified voltage and time window that, when placed in the eye, will illustrate whether there is sufficient voltage and timing margin for the application. Standards such as InfiniBand, PCIe, SAS, 802.3, and others will define eye masks for transmitters and receivers, both optical and electrical.

As an example, ***Figure 6-12*** shows the 2.5 Gbps InfiniBand single data-rate-receiver eye mask. The individual standard should be consulted for the required number of samples to make up the eye mask. Some standards will define a required number of Unit Intervals (UIs) over which the eye must be sampled to ensure adequate coverage of deterministic and random jitter effects.

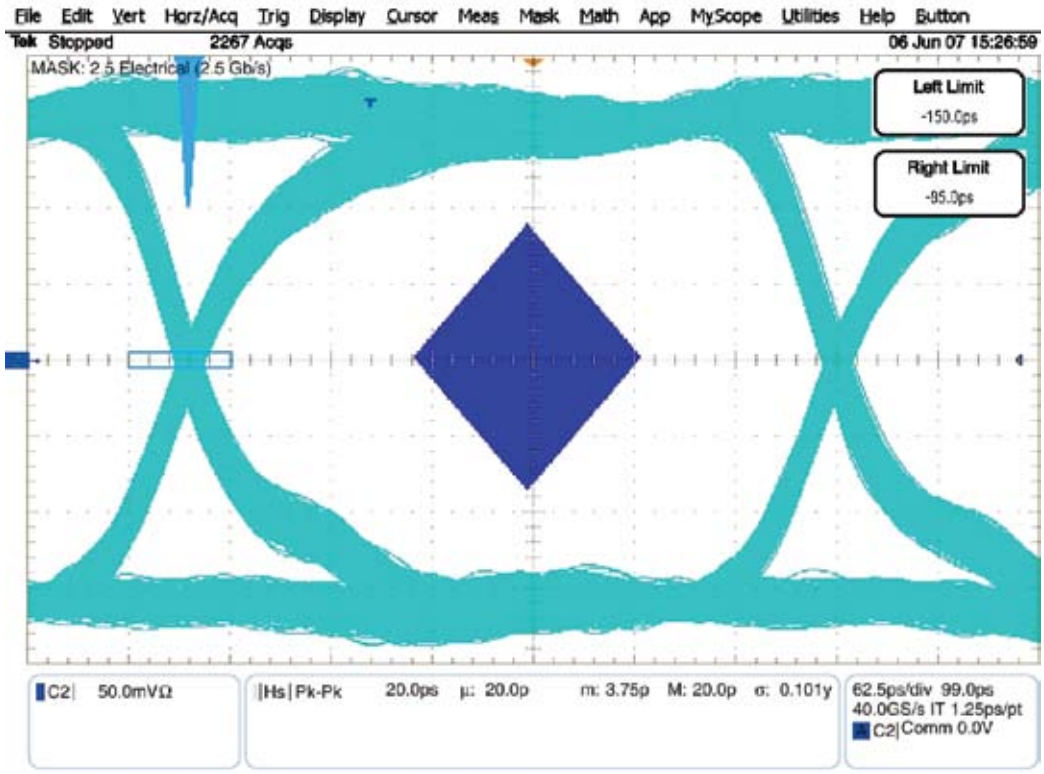


Figure 6-12. Eye Diagram with Infiniband 2.5 Gbps Receive Eye Mask

Bathtub Curves and Eye Contours

Another way to look at an eye is to look at an eye contour or a bathtub curve. The bathtub curve sometimes is referred to as a BERT scan. The bathtub curve is a graphical way to look at the eye diagram statistics in terms of BER versus time across the eye at the zero crossing of an eye diagram. A more in-depth description of a bathtub curve can be found in the document "T11.2 / Project 1316-DT/ Rev 2.0" (Fiber Channel-MJSQ).

As discussed in the previous section on jitter, random jitter is Gaussian, unbounded, and contributes to eye closure. The bathtub curve shows the statistics of BER and eye closure due to the random portion of the jitter. Patterns also affect eye closure so a sufficient amount of time to run patterns is needed to characterize the eye accurately to understand the worst case of pattern and random jitter.

To illustrate the amount of time to characterize an eye to the level of 10^{-12} at a date rate of 250 Mbps (the number of bits divided by the data rate), the time required will be determined at each data point on the bathtub curve: BER time = 10^{12} bits/250 Mbps = 40,000 seconds. Thus to use the bathtub curve, most engineers will characterize the eye to a level of 10^{-6} to 10^{-9} and extrapolate to 10^{-12}.

The eye contour shows similar eye diagram statistics to the bathtub curve, except with a more 3-D picture of what is happening to the eye at a lower BER. This can be helpful in determining how much margin a link has to an objective BER, and diagnosing an issue.

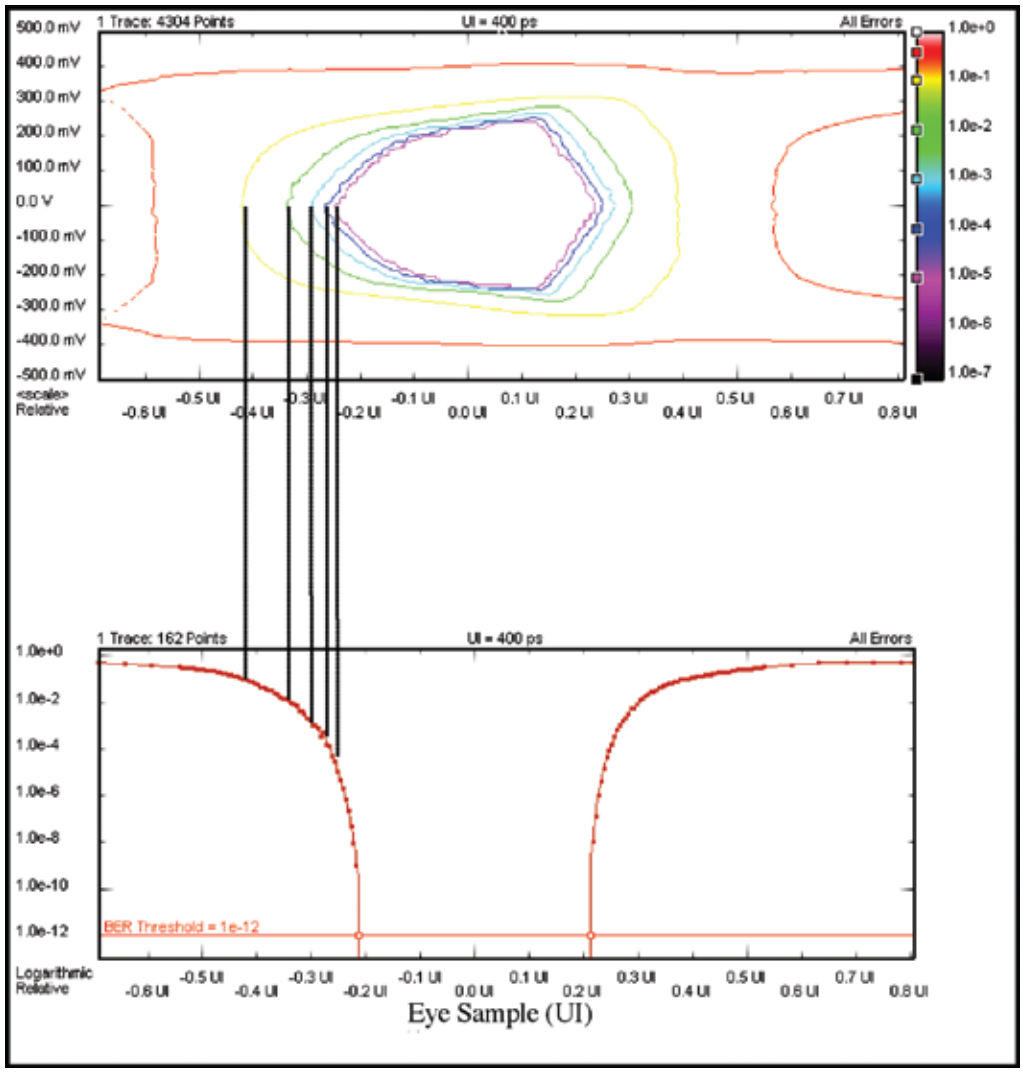


Figure 6-13. Correspondence of an Eye Diagram with BER Contours to a Bathtub Curve

When choosing cables and connectors for high-speed serial data transfer, it is essential to consider the effects media selection can have on system performance. Controlled-impedance media should be selected with (typically) a differential impedance of 100Ω. An appropriate connector with matching impedance is also imperative. The impact of these choices will be reviewed, including ways to compensate for the adverse effect of media distortion.

7.1 Physical and Electrical Cable Characteristics

The main detrimental effect of cable for high-speed serial data links is loss. Loss is the primary artifact that limits data rate. The loss is proportional to frequency and as data rates increase, the cable introduces more loss. The elements of the physical cable construction that control loss are length and gauge.

Table 7-1. Cable Specifications Affect Loss

Cable Specifications				
Gauge AWG	**Feet / Ohm**	**Ohms / 100 ft**	**Diameter in mils**	**Diameter in mm**
20	96.2	1.04	32	0.812
22	60.6	1.65	25.3	0.644
24	38.2	2.62	20.1	0.511
26	24	4.16	15.9	0.405
28	15.1	6.62	12.6	0.321
30	9.5	10.5	10	0.255
40	0.93	107	3.1	0.08

Table 7-1 lists different gauge cables, the associated cable diameter and mass. Lower-gauge cable, although better for signal quality, will be heavier and more expensive than higher-gauge cable and can be more awkward to use due to the torque affect. To help alleviate the rigidity, multi-strand copper cable is used to construct lower-gauge cable. ***Figure 7-2***, is an example of a typical DVI cable with a cut-away exposing a single differential pair. Depending on the gauge of the center conductor, the loss of the cable will vary.

As seen in ***Figure 7-2***, a shield surrounds the differential cable pair. A shield is used on higher-quality cables such as PCI-Express, SATA, DVI, and HDMI cables. The shield is the local return path for the signals traveling on the pair of cables. The closed return path is a low-impedance path that helps to limit the emitted energy from the cable pair to reduce crosstalk. The shield usually is made from foil, which is cost effective for cable manufacturers. There is also an outer shield that surrounds the bundle of pairs to minimize EMI. Braided wire usually is used as the outer shield.

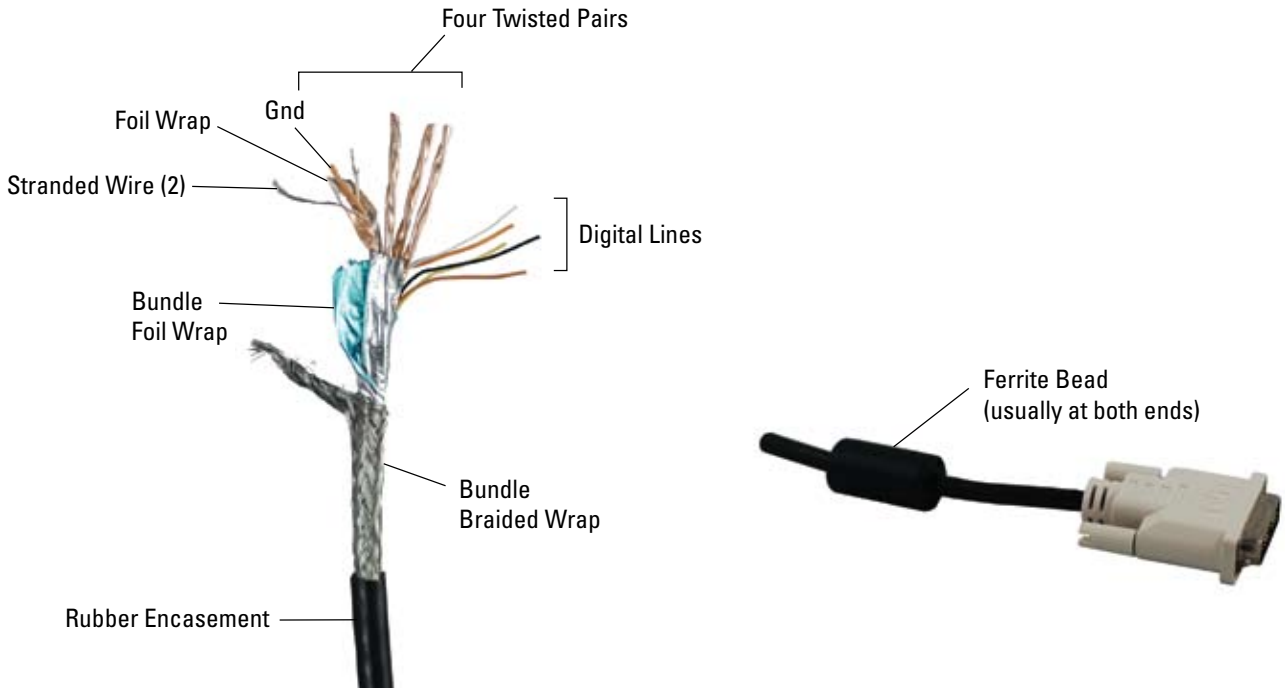


Figure 7-2. Stripped DVI Cable, Exposing Multiple Insulations

A single DVI wire pair is exposed in ***Figure 7-2***. Depending on the gauge of the center conductor, the loss of the cable will vary.

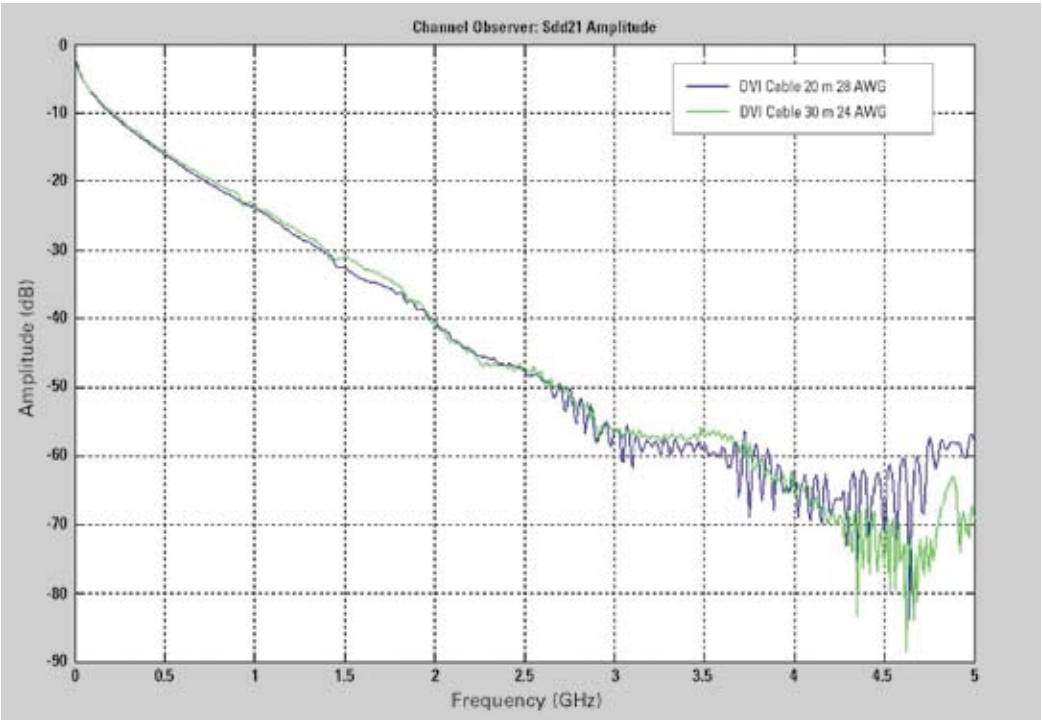


Figure 7-3. DVI Cable Loss vs. Wire Gauge

Using different quality DVI cables as an example, it can be seen that a 20-meter 28-AWG DVI cable has the same attenuation as a 30-meter 24-AWG DVI cable. Therefore, the easiest way to extend a link segment is to use a lower-gauge center-conductor cable.

The effect of crosstalk is important to consider when selecting different cable types. If the crosstalk between two adjacent pairs of cables is too high, then the SNR of the serial link will be compromised. As seen with the example using CAT-6 cable (***Figure 7-3***), the crosstalk limits the usefulness of the link segment to 1.2 Gbps. When compared to the same length of Inifiniband cable, the crosstalk effect stays 30 dB from the signal loss out to 5 GHz.

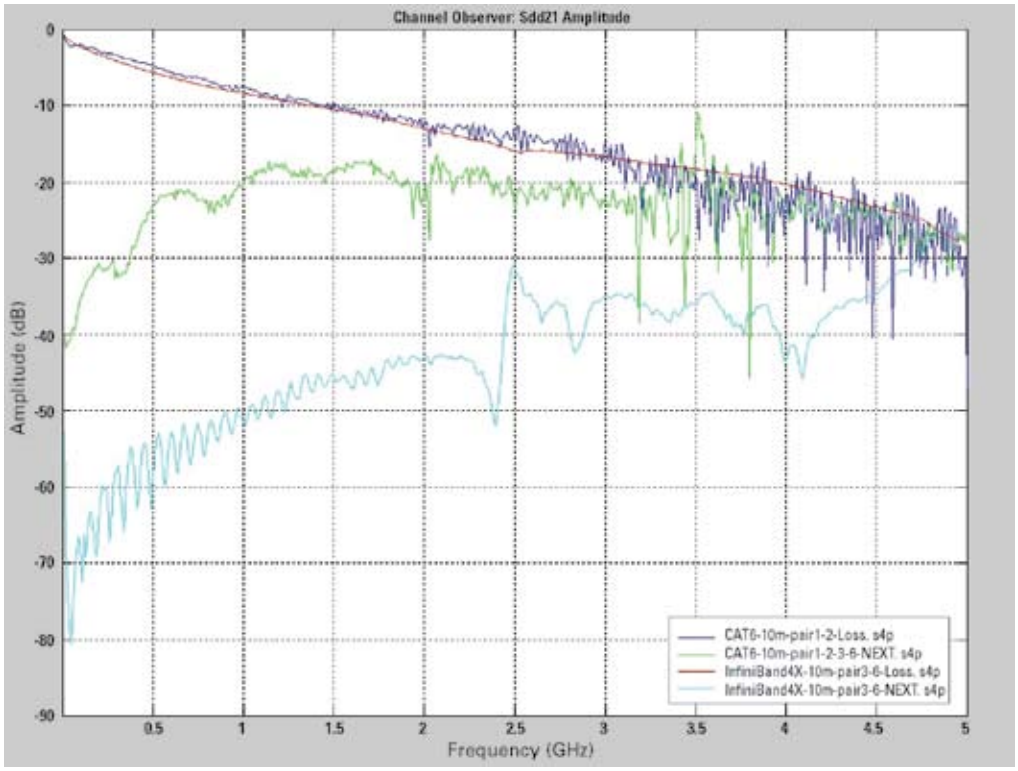


Figure 7-4. Infiniband and CAT-6 Cable Showing Cable-Type Crosstalk Differences

Low-cost twisted pair cables have been widely adopted across the industry to support higher data rates. Category 5-type cables provide four wire pairs per cable and are very cost effective, on the order of $0.20 cents per foot. The downside to twisted pair cables is skew. Both intra-pair and inter-pair skew plague twisted pair cables. The number of turns per pair of cable varies for each bundle and over 100 meters can vary by one meter. Further, when the individual pairs are manufactured, the length of each of the pairs is not controlled which creates intra-pair skew. Intra-pair skew introduces common mode to differential-mode conversion, which increases the signal loss at higher frequencies.

Cables that have tighter tolerance on skew are PCI-Express, SATA, Infiniband, DVI, and HDMI cables. Skew becomes more important to the application when all data lanes need to arrive at the destination on the same bit clock. Cable manufacturers are experimenting with new methods to control the inter-pair skew for high-data-rate applications like PCI-Express Generation 2 at 5 Gbps.

At each end of a cable is the connector. The connectors can cause electrical discontinuities (impedance mismatch), crosstalk, and added loss. For bi-directional link segments like SATA, pair isolation becomes the most-needed performance specification for the cable. SATA connectors minimize the crosstalk and EMI by having metal shielding around each pair and around the bundle. The technology advancement of the high-speed connectors has come a long way from the plastic RJ-45 connectors of the category cables, but given the cost effectiveness of the category cable, some manufacturers have developed high-speed connectors to reduce the crosstalk.

RJ-45 Cable

SATA Cable

DVI Cable Connector

HDMI Cable Connector

TeraCat-7 Connector

Figure 7-5. Cable End Examples – Not All are Suited for Highest-Speed Applications

Signal-conditioning devices can compensate for the linear insertion loss caused by the cable. When the connector introduces more loss or an impedance discontinuity, equalization and pre-emphasis cannot address the added effects. The bandwidth of the link segment can be determined by operating in the linear region of the media s parameter.

Table 7-6. Application-Driven Decisions Used When Selecting Cable Media

Cable Type	Cable Construction	Data Rates (Gbps)	Typical Markets	Gauge	Typical Media Lengths (meters)
Dual DVI	6 Data, 1 clock, 3 control	1.65	Consumer Digital Video	22, 24, 26, 28	5 to 30
HDMI	3 Data, 1 clock, 3 control	1.65	Consumer Digital Video	24, 26, 28	5 to 30
Category 5e	4 Data	Up to 3.125	Broad Market	26, 28	10
PCI-Express Gen2	X1, X2, X4, X8	5	PC	24, 26, 28	several feet, 10 meters
SATA-2	1 set bi-directional data pairs	3	Storage Applications	24, 26	several feet, 10 meters

7.2 Signal-Conditioning Characteristics

This section discusses various types of impairments faced by data bits as they originate from a source and travel over different types of media. Specific signal-conditioning techniques are used to address specific channel impairments.

Media Losses in Cables and PCB Traces

The most dominant loss comes from the limited bandwidth of cables and PCB traces that carry the data bits from point to point. These components create two different types of loss mechanisms: skin and dielectric. These frequency-dependent losses affect the signal differently and as such, there are different solutions for each.

1. **Skin Loss**: skin effect causes most of the high-frequency current to travel on the outer surface (skin) of the conductor. Consequently, the effective resistance of the conductor increases with frequency. Skin loss is directly proportional to the square root of signal frequency resulting in a more gradual frequency roll off.
2. **Dielectric Loss**: as a signal travels in a conductor that is insulated from another by a dielectric material, the dielectric material absorbs some of the signal. Dielectric loss is directly proportional to signal frequency resulting in a steeper frequency roll off.

Both skin loss and dielectric loss degrade the edge rate of high-frequency binary signals in the same fundamental way by introducing Inter-Symbol Interference (ISI), which spreads a single bit over many bit periods. However, they do affect the bits differently as described above. Furthermore, skin loss is the dominant loss mechanism in cables, while dielectric loss is more prevalent in PCB traces. Consequently, different types of compensation may be required to compensate completely for different media types.

There are two strategies to address and compensate for this kind of ISI. The first is to use better, lower-loss media and second, use signal-conditioning ICs to compensate for the signal. The choice of media is often constrained by material cost, by installation cost, and by the requirement for upgrading existing installations to work at higher data rates. By using signal conditioning and applying pre(de)-emphasis and equalization (EQ) techniques, higher performance can be achieved.

These two important signal-conditioning techniques allow customized tuning to modify the signal to eliminate losses due to media effects. Many signal-conditioning devices offer both techniques (EQ and PE/DE) in a single IC such as National's DS25BR110 and DS16EV5110, signal-conditioning chips with advanced features to compensate for media loss.

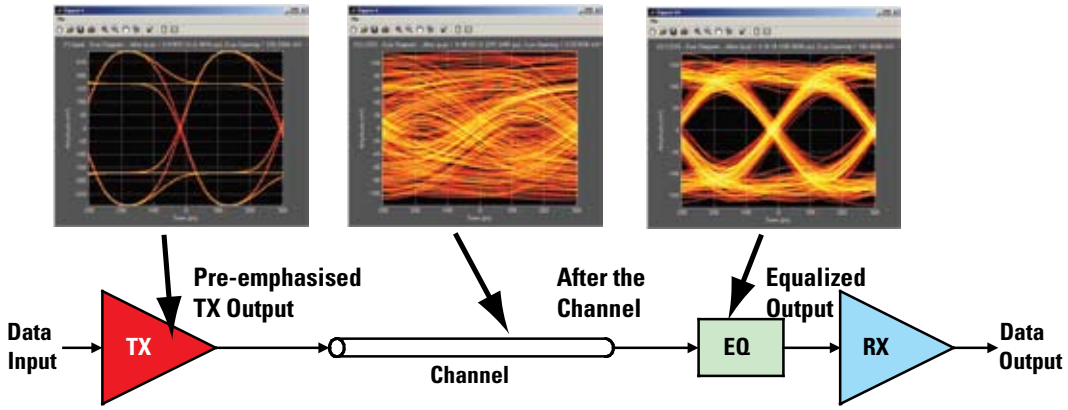
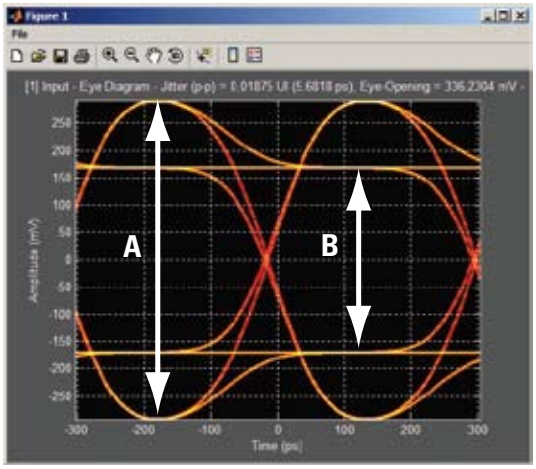


Figure 7-7. Signal Before and After Pre-Emphasis and Equalization is Applied

Pre-Emphasis and De-Emphasis Drivers

Pre-Emphasis (PE) and De-Emphasis (DE) techniques focus on the loss problem by applying frequency-selective attenuation to the data content at the transmit end. Media loss results in the slowing down of edges resulting in ISI. To compensate for this, pre-emphasis and de-emphasis drivers increase the energy in the edges (high-frequency component) relative to the flat portion of the waveform (lower-frequency component). Thus, the combined frequency response of the media and the PE/DE driver is relatively constant over frequency, which results in an open eye diagram at the end of the cable. (***See Figure 7-7***).



PE = 20 x log10(A/B): Transmit V_{OD} = B
DE = 20 x log10(B/A): Transmit V_{OD} = A

Figure 7-8. Different Parts of the Signal are Modularized

Pre-emphasis or de-emphasis usually is represented as a ratio of the peak-to-peak signal amplitude (A) to the peak-to-peak settled amplitude (B).

The difference between pre-emphasis and de-emphasis is in the way the frequency compensation is applied. In pre-emphasis, the edge energy is boosted by creating an overshoot on every edge. In de-emphasis, the edges are kept the same, but the settled amplitude is attenuated. The differences are listed in ***Table 7-9***.

Table 7-9. Differences Between Pre-Emphasis and De-Emphasis

Criteria	Pre-Emphasis	De-Emphasis
Typical signaling technology	LVDS	CML
Output peak-to-peak amplitude	Increased by PE ratio	Same as without DE
Power consumption	Higher	Same
Typical measurements	Positive dB (+3 dB)	Negative dB (-3 dB)
Receive eye opening	Same as without PE	Reduced by DE ratio

Pre-emphasis and de-emphasis width is determined in two ways – by an analog time constant or by a delay block related to data width (usually derived from a digital clock). In most signal-conditioning ICs that do not try to recover accurate timing information (clock), pre- and de-emphasis widths are limited between approximately half the bit width to approximately one full bit width.

Equalization

Equalization works at the receive end by selectively boosting the high-frequency data, thus compensating for the media's high-frequency roll off. An RLC network in the equalizer circuit implements a high-pass filter that has a frequency response (ideally) exactly opposite to the media loss that the equalizer is attempting to compensate (***Figure 7-10***).

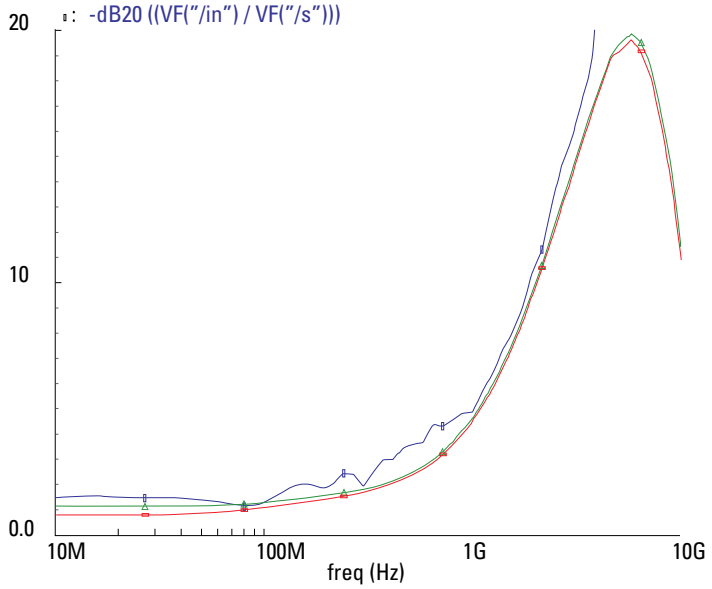


Figure 7-10. Inverse Channel Response (Blue) and Matching Equalizer Response (Green)

Two Types of Equalizer Circuits

The two types of equalizer circuits can be divided into two broad categories: passive circuits and active circuits. Passive circuits work by attenuating low frequencies. Active circuits work by amplifying high frequencies and require power to achieve the amplification. The active equalizers can be characterized further under three types – fixed, variable, and adaptive.

Passive: Power-Saver Equalizers

Power-saver equalizers from National (e.g., DS38EP100, DS80EP100) are unique solutions that equalize cables and backplane traces up to very high data rates without requiring any power supply connection and therefore without burning any DC power. Power-saver equalizers enable several new applications such as equalized backplanes and equalized cables/ connectors.

Power-saver equalizers achieve this performance by attenuating low-frequency components by only using on-chip resistors, inductors, and capacitors. As a result, these equalizers work equally well with all signaling technologies (LVDS, CML, and LVPECL). The waveforms at the receive end are similar to the ones achieved using de-emphasis drivers, i.e., the receiver sees an open eye but with reduced amplitude.

Power-saver equalizers offer several advantages:

- Flexible placement – can be placed anywhere in the data path (e.g., on the backplane in the middle of the data path)
- Bi-directional – data may pass in either direction
- Completely linear – multiple power-saver equalizers may be cascaded and can be followed up with active equalizers to restore signal levels

Active Equalizers

Active equalizers, as the name implies, use active transistors to gain up signals at high frequencies without attenuating low frequencies. This scheme works better with low-signal amplitudes; for example, de-emphasis drivers or LVDS drivers without PE. In addition, most active equalizers can tolerate high-input amplitudes just as well. Within the equalizer chip, there are several gain stages that 'square-up' the signal and restore it to full amplitude (***Figure 7-11***). This restoration is a non-linear process and therefore active equalizers should not be cascaded back to back.

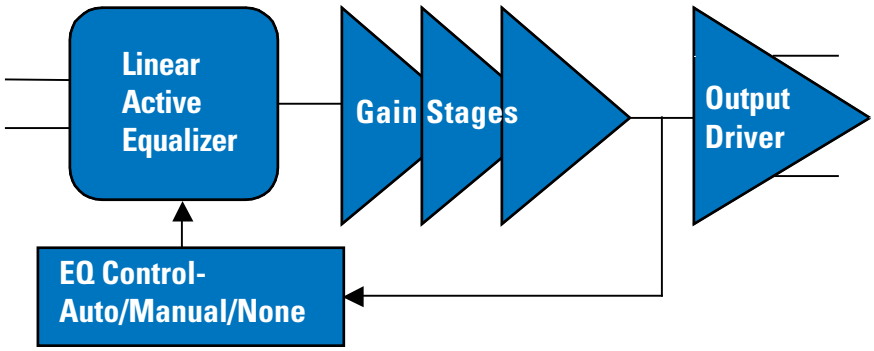


Figure 7-11. Active-Equalizer Topology

Since the equalizers are seldom ideal, there is always some leftover ISI. This leftover ISI gives rise to output jitter and is referred to as residual deterministic jitter. Well-designed equalizers will reduce incoming jitter to less than 0.2 UI. A Unit Interval (UI) is equal to the time period of one bit at the desired data rate.

Fixed Equalizers

Fixed equalizers are designed to equalize a fixed, predetermined length of cable up to a specified data rate. Fixed equalizers offer a preset equalization curve and often are quoted as providing a certain amount of boost (measured in dB) at a fixed, specified frequency.

The output jitter of these equalizers is optimized for a fixed channel and will degrade if the channel is too short or too long as compared to the reference channel targeted by the equalizer. Fixed equalizers should be used when the transmission channel is well known and does not vary.

Variable Equalizers Allow Control

Variable equalizers are useful when the transmission channel length varies from system to system and when the equalization setting must be retained independent of the data rate. These equalizers allow the system designer some manipulation of the equalization circuit, and variable equalizers (as well as fixed equalizers) are quite independent of the actual data patterns running through them.

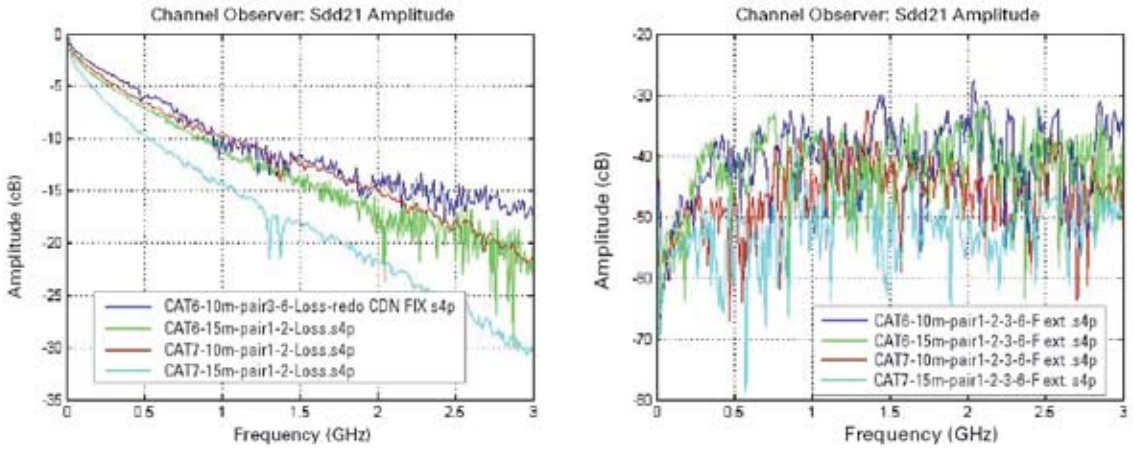
Configurations between multiple predefined equalization curves are set using CMOS pins on the device (e.g., DS25BR100) or by using serial-bus access (e.g, SMBus for DS64EV400). This allows a single equalizer chip to equalize different lengths of media (cable or trace) without the jitter degradation when using fixed equalizers. However, the system designer must set/program the correct equalization curve based on the channel loss.

Adaptive Equalizers

Adaptive equalizers use some internal algorithms to try to determine independently and automatically the optimum amount of equalization needed for the media that is connected to the adaptive equalizer. Often times, such an algorithm requires intimate knowledge of the cable type, data rate, and data patterns (such as 8b/10b). As a result, adaptive equalizers work well over a limited set of media types, data rates, and data patterns. Adaptive equalizers are necessary when the media length varies considerably and cannot be well constrained by the system designer. National's LMH0344, LMH0034, and DS15EA101 are good examples of very advanced adaptive equalizers that automatically equalize varying cable lengths of co-axial and CAT-5 cables.

Crosstalk

As discussed previously in the FEXT/NEXT section, crosstalk refers to undesired coupling from a signal source to the data bits of interest. Crosstalk typically occurs when multiple data streams are routed in close proximity and couple (via EMI) to each other. In cables, crosstalk is the result of running several conductors in the same cable. In the case of connectors, crosstalk occurs due to the physical design of the connector.



Figures 7-12. Examples of Crosstalk Observed in Different Media

Crosstalk becomes significant at higher data rates and often is the limiting factor when transmitting multiple lanes of data in the same cable or connector. As can be seen from the ***Figures in 7-12***, at 3 GHz, crosstalk is almost equal to the received signal. Crosstalk is especially poor when data is flowing in both directions in the same cable or over the same connector. In this scenario, the received signal experiences the attenuation from the cable but the near-end crosstalk couples in at full strength.

It requires complex DSP techniques and knowledge of the aggressor signals to compensate for crosstalk. It is very difficult to correct for crosstalk at higher data rates where complex DSP techniques are impractical. Crosstalk cannot be corrected by equalization. In fact, linear equalization boosts the high-frequency crosstalk along with the desired signal.

Therefore, the best strategy to address crosstalk remains that of prevention. The system designer should use the slowest possible edge rates. This limits the energy at high frequencies and reduces crosstalk. However, too slow of an edge rate increases ISI and attenuates the desired signal. The trade-off must be evaluated carefully. Typically, the edge rate should be no slower than one third of the bit period. The system designer should choose cables where conductor pairs are shielded individually, and use high-performance, low-crosstalk connectors.

Reflections

Reflections are a result of sending high-frequency, sharp edges through impedance discontinuities that exist in a channel. In a well-terminated channel with no impedance discontinuities, signals travel from the transmitter and are absorbed completely by the receiver. When properly (ideally) terminated, there are no reflections. However, if the signal encounters a discontinuity, part of the signal reflects back toward the source.

For instance, if the source termination is matched improperly to the load, the signal will reflect back toward the transmitter. The receiver will then receive multiple copies of the same signal, attenuated at different times. Such multiple arrivals at the receiver result in ISI. These discontinuities are often a result of connectors, PC-board vias, and improper termination resistors. Another source of reflection is poor return loss from integrated circuits, due to high capacitance (also refer to the section **Effect of Input Capacitance, page 53**) or due to improper termination on the high-speed I/O pins.

Linear equalizers cannot predict where in the signal path a discontinuity may happen. Furthermore, with long channels, the reflections take a relatively long time to reach the receiver. It is difficult to distinguish reflected signal from desired signal without using DSP techniques. As a result, none of the high-speed equalizers compensate for reflections.

As with crosstalk, the best strategy to address reflections is to use higher-performance connectors and employ high-frequency design practices. System designers should carefully review the return loss and input-capacitance specification of the circuits used. Typically, the return loss at the data rate should be better than -10 dB and input capacitance should be below 2 pF. National offers several signal-conditioning ICs that meet these requirements, e.g., the DS25BR100 family and DS64EV400. Finally, slowing down the edge rates significantly reduces reflections as shown in ***Figure 7-13***.

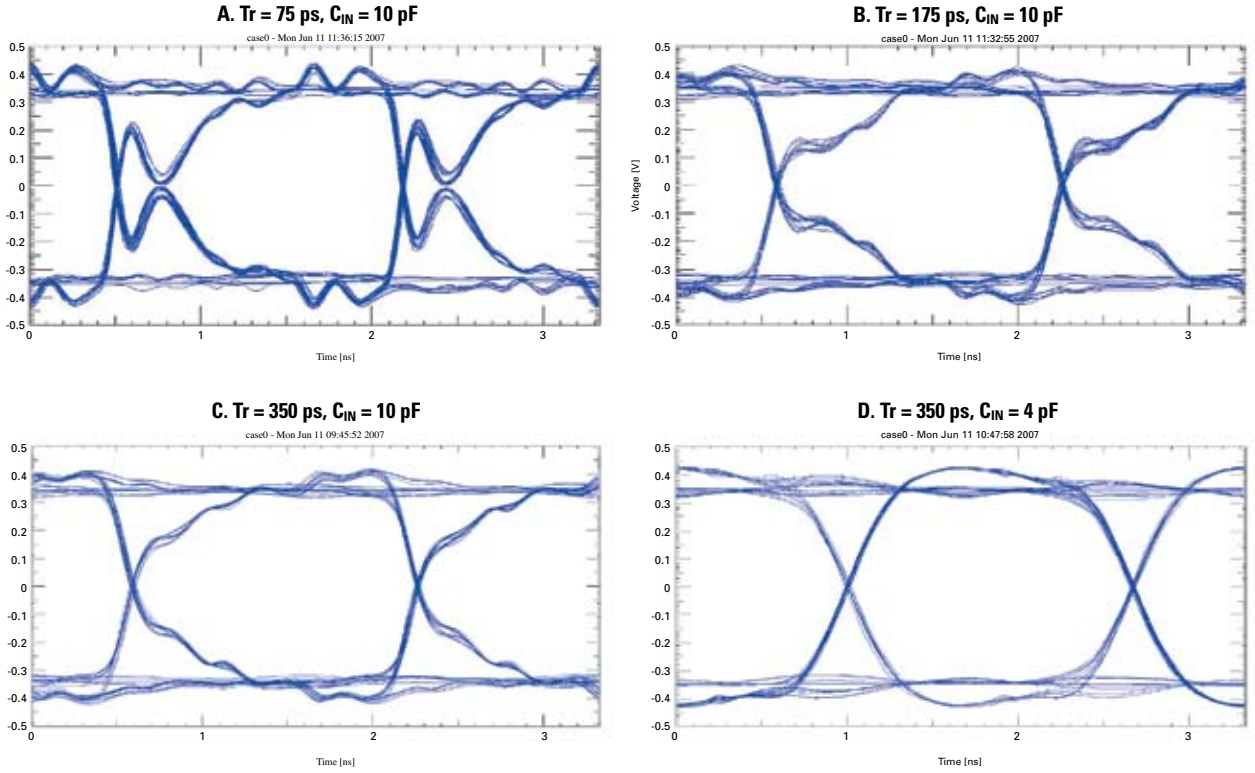


Figure 7-13. Effect of Edge Rate on Receiver Input Eye Diagram.
Data Rate = 600 Mbps. Waveforms Based on IBIS Model Simulations.

7.3 Using Pre- and De-Emphasis and Equalizers Together

Both pre- and de-emphasis (PE/DE) and equalizers (EQ) try to correct the problem of ISI by using PE/DE at the driver end and EQ at the receive end. If both the driving and the receiving ends can be defined by the system designer, it is possible to use both PE/DE and EQ in the same receive chain to obtain improved performance. However, there are several things to consider, including the PE/DE driver characteristics, transmission media, and receive-equalizer characteristics.

These system parameters must all match. A mismatch may result in increased residual deterministic jitter. Secondly, the system designer must be aware of extra reflections and crosstalk. A PE/DE driver introduces more high-frequency energy that can result in crosstalk, reflections, and electromagnetic radiations. These high-frequency artifacts are then gained up by the receive equalizer. Finally, pre-emphasis requires higher power in the driver.

Therefore, a good strategy is first to use maximum receive equalization. If that is insufficient, start increasing the pre-emphasis levels. Helping to deal with these constraints is National's DS25BR100/110/120/150 family of buffers. These have several combinations of PE and EQ functions that can be used together in a system.

7.4 Random Noise

Random noise is a result of the random nature of electrons and the random obstacles that the electrons overcome as they carry information down electrical channels. All electrical components exhibit some degree of random noise that ultimately translates to a noise voltage and results in Random Jitter (RJ) on data edges. True random noise is often Gaussian in nature and is measured in rms or peak-to-peak quantities. The latter measurement makes an inherent assumption of Bit Error Rate (BER).

Random noise/jitter is not predictable and therefore cannot be compensated with equalization.

Sources of random jitter can be separated into three main system components: driver jitter, channel jitter, and receiver jitter. Driver jitter is determined by the purity of the clock source feeding the driver and the driver random noise itself. Well-designed driver subsystems will exhibit timing jitter less than 0.1 UI_{P-P}. Media channels are usually passive and do not contribute significantly to RJ by themselves. The receive equalizer has to gain up the signal that has been attenuated by the channel. In the amplification process, noise is gained up as well and results in an increase in RJ. A well-designed equalizer will exhibit an RJ of less than 0.2 UI_{P-P}.

It is worth reiterating that the receive equalizer does not reduce the random noise/jitter. While the DJ is reduced, the equalizer increases RJ. To better minimize random jitter, National's equalizers are manufactured using advanced bipolar processes and circuit techniques.

The largest source of random timing jitter is usually the clock generation (PLL) and Clock and Data Recovery (CDR) sections of a data path. The different nature of timing jitter is depicted in ***Figure 7-14***. Note that clock noise affects the eye opening in the horizontal (time) direction, but does not impact the eye opening in the vertical (amplitude) direction.

7.5 Re-clocking Receivers (Re-clockers)

In order to address Random Jitter (RJ), crosstalk, reflection, and residual Deterministic Jitter (DJ), the system designer must look toward a different class of signal-conditioning device, a re-clocker. A re-clocker examines the incoming data and aligns an internal, local clock source to the received data pattern. Once perfect alignment is achieved, the re-clocker uses this internal clock, often called recovered clock, to resample the incoming data. This process and associated circuits form the core of CDR systems.

The sampling (or re-latching or re-clocking) is performed by strobing incoming data exactly in the center of the eye opening and recording the result as a binary 1 or a 0. The ideal output of such a strobing circuit has neither amplitude jitter nor timing jitter. In practice, the internal clock source has timing jitter that results in some residual RJ. Furthermore, the clock-recovery circuit cannot align to incoming data in the presence of severe DJ and RJ. Due to the sampling process, a partially-closed, input eye pattern may result in a clean eye diagram at the output, but one that has bit errors.

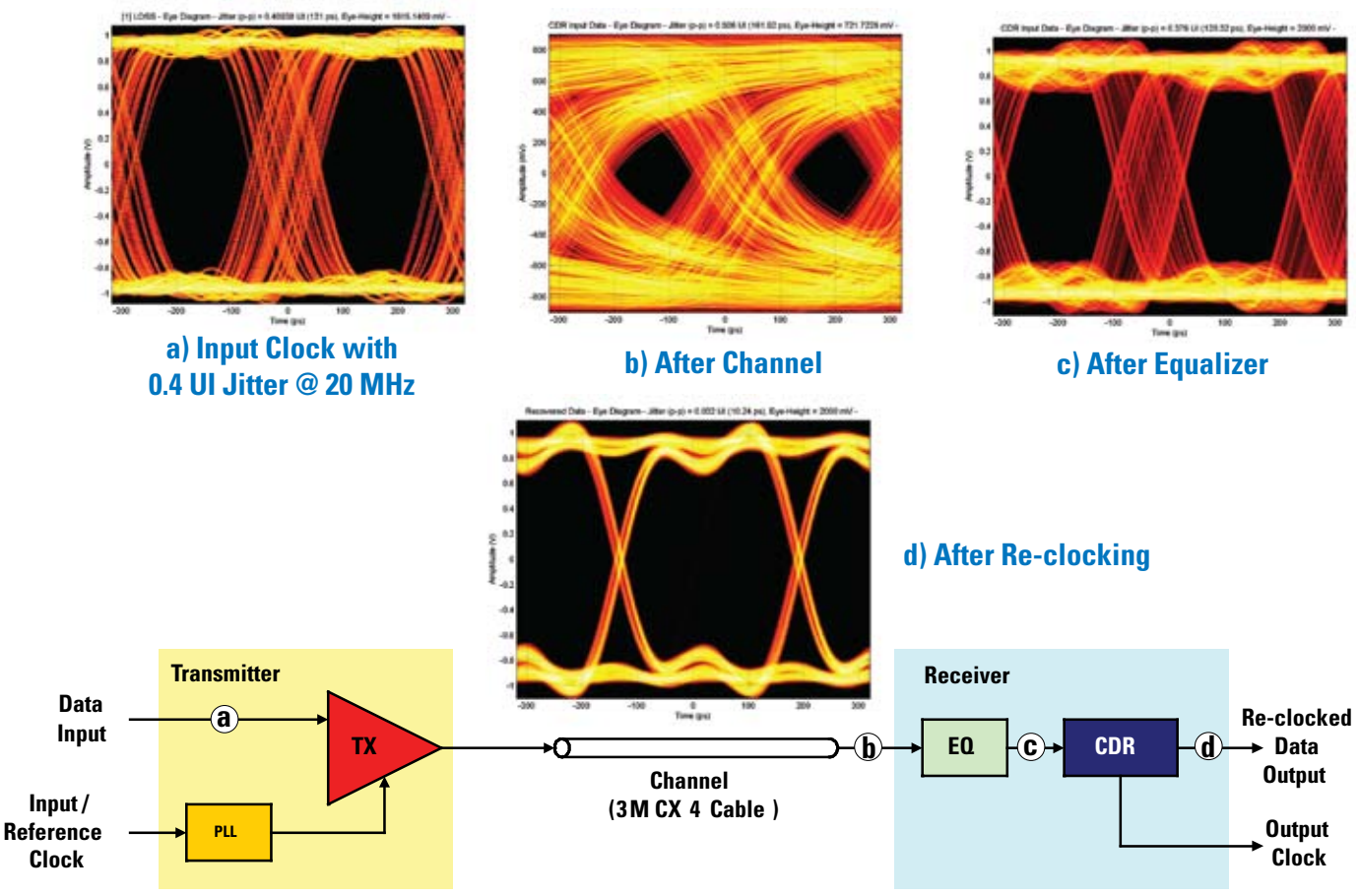


Figure 7-14. Recovered Signal Using Equalization and Re-clocking

Therefore, the system designer must rely on Bit Error Rate Tests (BERT) to ensure that the system is operating error free. The amount of incoming jitter that a CDR system can tolerate without introducing bit errors is known as Input Jitter Tolerance (IJT). State-of-the-art re-clockers such as National's LMH0346 can recover data in the presence of as much as 0.6 UI of jitter.

The jitter introduced due to channel ISI is often much more than what even the best CDR technology can handle. Therefore, in most applications, an equalized receiver or a pre-emphasized driver always precedes a re-clocker.

7.6 Bit Error Rate (BER) and Jitter (Random and Deterministic)

There are two types of jitter - Random (RJ) and Deterministic (DJ). DJ is a bounded quantity and is predictable. RJ, however, is a random quantity and typically follows a Gaussian distribution of zero mean and a sigma that is specified in the datasheet in root-mean-square (rms) seconds. Based upon the bit-error-rate requirements of a system, RJ must be carefully constrained. Assuming Gaussian distribution, in order to achieve a 1e-12 BER, the system designer must allow random jitter to spread by 14 sigma.

Similarly, for 1e-15 BER, a spread of 16 sigma must be budgeted. Furthermore, if there are multiple sources of jitter, all RJ contributors must be added in an rms fashion while DJ contributors must be added linearly as shown in ***Equation 7-15***. The total jitter must be less than the amount of jitter the downstream re-clocker or SerDes can handle, i.e., its IJT specification.

Equation 7-15. All contributors are added up for the total jitter value:

$$\text{Total Jitter (TJ)} = N_{sigma} \times \text{sqrt}(RJ_1^2 + \ldots + RJ_n^2) + DJ_1 + \ldots + DJ_n < \text{IJT(receiver)}$$

Lossy Media Compensated by Equalization

To illustrate the effect of the signal-conditioning features, examine the eye diagrams of signals going through lossy media. The attenuation and bandwidth limitation of a long PCB trace or a cable is easily noticed when a fast signal in a pseudo-random pattern is run through it. The result is a vertically- and horizontally-closing eye pattern that can be seen in ***Figure 7-15***.

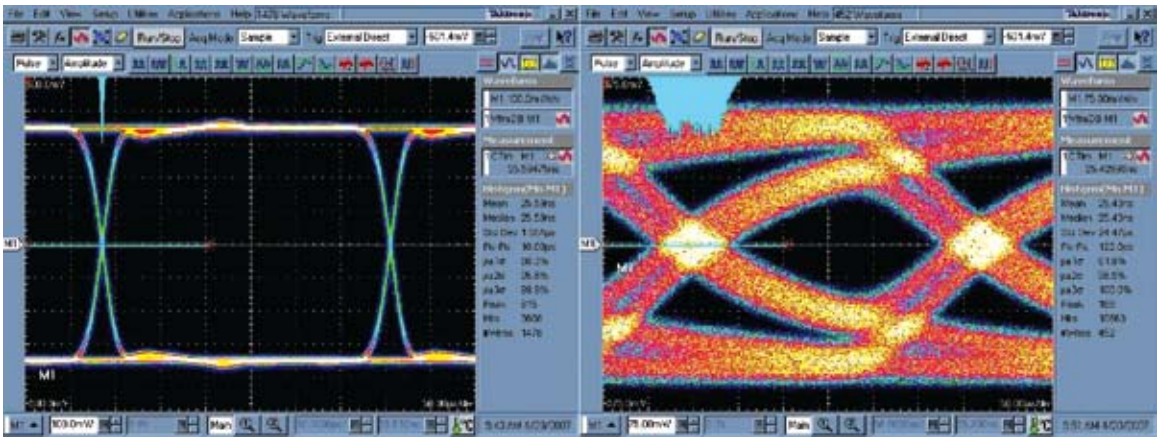


Figure 7-15. Generator-Created 3.125 Gbps Pseudo-Random LVDS Signal with No Media (Left) Going Directly to the Oscilloscope and the Same Signal Going Through 28" of FR4 Trace to the Oscilloscope (Right)

Input equalization is designed to match a specific lossy line that is attached to the input of the device. Equalized inputs try to compensate for the AC loss that the media introduced in the interconnect system. ***Figure 7-16*** shows before and after pictures of a signal going through a 28" FR4 trace and a device with input equalization. The 28" trace has approximately 8 dB of loss at 3.125 Gbps. The equalizer device has a gain-selected setting close to the inverse of the 8 dB loss of the trace, in our case around 7.5 dB.

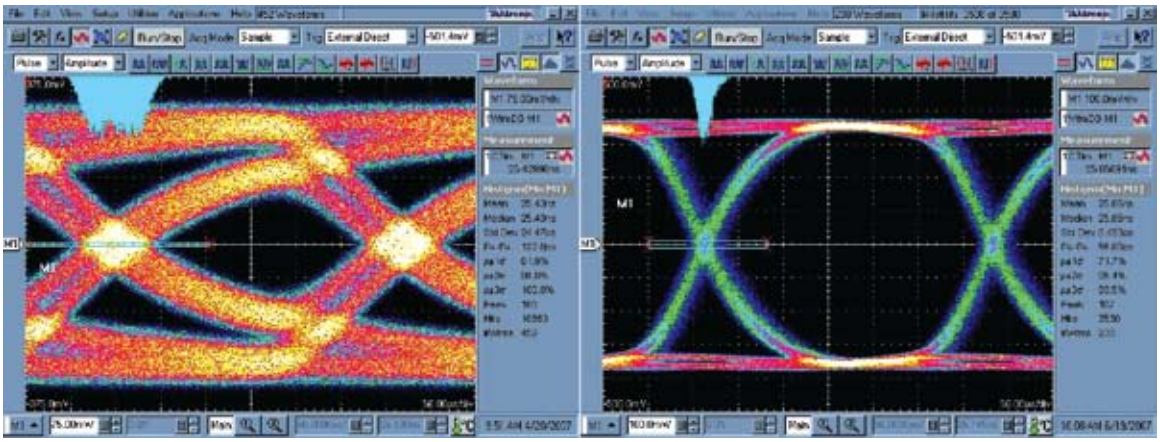


Figure 7-16. 3.125 Gbps Signal Going Through 28" of Differential FR4 Stripline on NRZ PRBS-7 Before (Left) Then After Equalizer Device (Right) (V: 125 mV / div., H: 50 ps / div.)

Equalizers can extend the cable medium to hundreds of meters. One application example would be when a long cable such as a DVI, CAT-5, or similar type is used as the medium. Next, ***Figures 7-17*** and ***7-18*** show an equalizer function in a cable environment with 200m of Belden cable before and after equalization is applied.

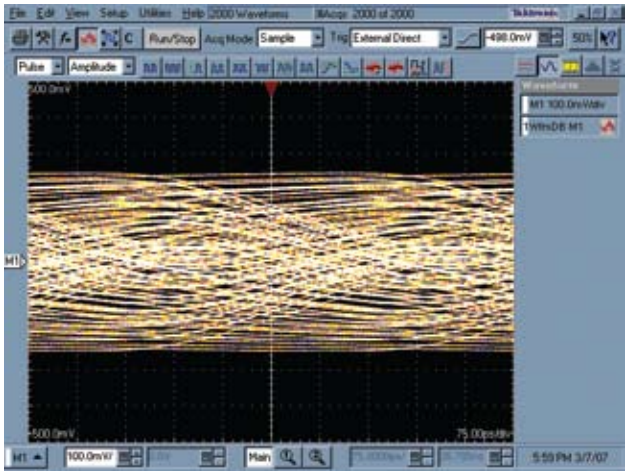


Figure 7-17. A 1.5 Gbps NRZ PRBS-7 after 200m of Belden 9914 Cable (No Correction); Scope: V:100 mV / DIV, H: 100 ps / DIV

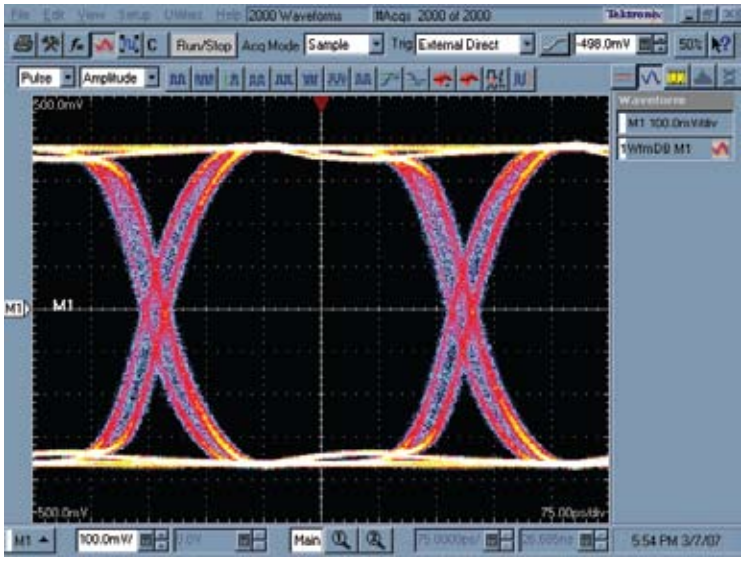


Figure 7-18. An Equalized 1.5 Gbps NRZ PRBS-7 After 200m of Belden 9914 Cable; Scope: V:100 mV / DIV, H: 100 ps / DIV

Pre-Emphasis Eye Diagrams

Output pre-emphasis is designed to extend the length of driven media by introducing a short boost in the output levels during the rise and fall transitions. Pre-emphasis devices usually have several settings to increase the pre-emphasis level from the original driver output level. ***Figure 7-19*** shows an example of before and after signals through the 28" FR4 trace.

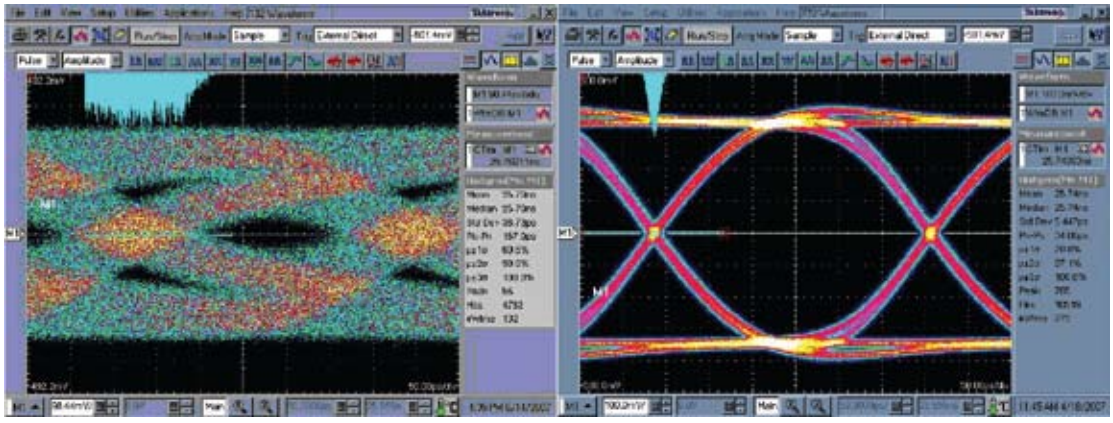


Figure 7-19. Output of 28" of Trace Driven by an Output Without Pre-Emphasis (Left) and by Output with 6 dB of Pre-Emphasis (Right)

PE/EQ Combination

Since pre-emphasis and equalization separately extend the reach of FR4 striplines to 30 to 40 inches, we can use a pair of transmit-receive devices to extend the media to 70 or 80 inches.

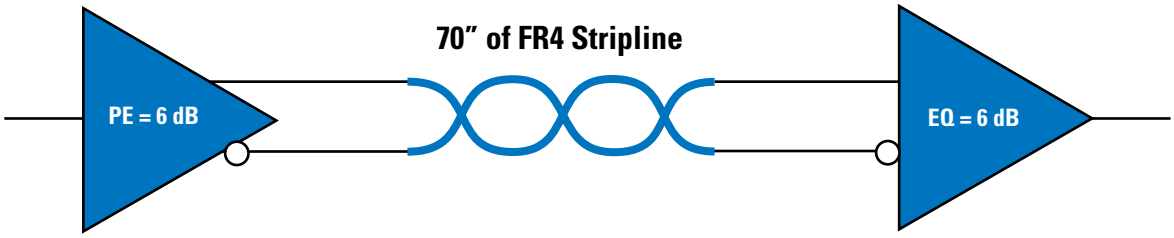


Figure 7-20. Output Pre-Emphasis Device Set to 6 dB PE Driving a 70" Trace into an Input Equalization Device Set to -6 dB EQ

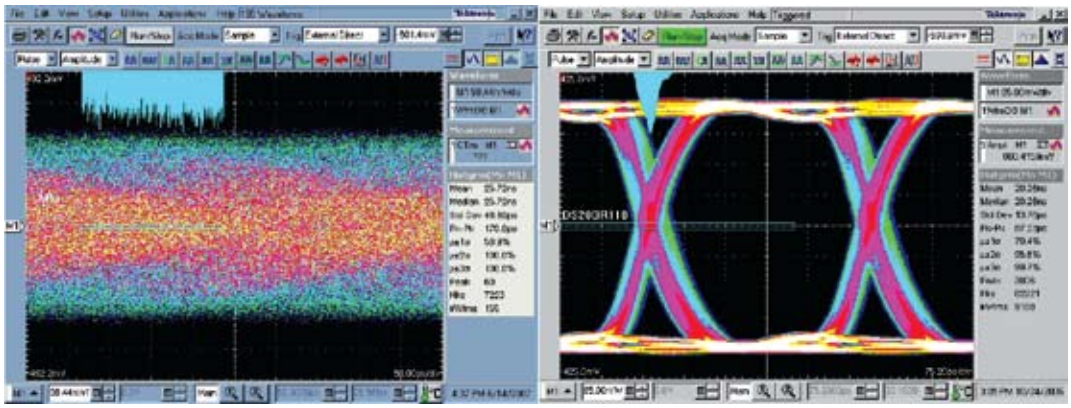


Figure 7-21. 70" of FR4 Trace Driven by 0 dB Pre-Emphasis (Left) and 70" Driven by 6 dB of Pre-Emphasis into 6 dB of Input Equalization (Right). (Plots Taken at 2.5 Gbps)

The complexity of high-speed interface design has made the use of modeling almost a necessity. Simulation tools using simple, accurate models for high-performance interface devices are readily available. Early in the design flow, simulations may be useful to obtain an approximate understanding of the challenges and potential shortfalls in a design. At this stage, it is more important for ease of use and quick results than absolute accuracy. Later, as the design becomes more concrete, simulations are required to provide a very close representation of actual system performance.

8.1 Input/Output Buffer Information Specification

Input/output Buffer Information Specification (IBIS) files have become the basic ingredient in generating fast, accurate behavioral simulations.

The IBIS model meets four essential criteria:

- The models are standardized and straightforward to create for semiconductor vendors and do not reveal specialized vendor IP.
- IBIS models are accurate and based on SPICE, bench results, or both.
- Many analog simulators and electronic design automation (EDA) tools support IBIS models.
- IBIS behavioral models do not have convergence problems in simulation and produce quick and accurate results.

IBIS is an approved industry standard, known as *ANSI/EIA-656-A*, and enjoys wide support among semiconductor and EDA vendors. An IBIS behavioral model contains I-V and V-T data representing buffer inputs and outputs in ASC-II text format. This data, along with additional information required by the standard is used to model the analog I/O behavior of the device. IBIS files include data for typical, maximum, and minimum values to allow modeling of both typical and worst-case performance.

The IBIS standard version 1.0 was released originally in 1993. With the current revision at 4.2, backwards compatibility has been maintained. Initially the standard was developed for single-ended technologies, and differential signals are handled by providing differential pin mapping. The differential pair is split into inverting and non-inverting pins and the simulation tool is aware that the pair is differential. However, the device IBIS file is extracted for each pin as if it was a single-ended device. The new IBIS revision (4.2) also allows inclusion and use of other simulator languages (e.g. SPICE) within the IBIS model. This new specification helps the modeling of non-linear signal conditioning like equalization and pre-emphasis.

There are various different model types available in the IBIS specification. Some examples are “input”, “input/output”, “3-state output,” and “open drain”. The two most common types for high-speed differential are “input” and “3-state output”.

8.2 Behavioral Diagram of IBIS

Figure 8-1 shows the "input" IBIS model structure for a typical receiver. RLC values for the package are represented by R_pkg, L_pkg, and C_pkg. The input Capacitance (C_{IN}) is the C_comp value and the device ESD structures are defined by the Power_Clamp and GND_Clamp.

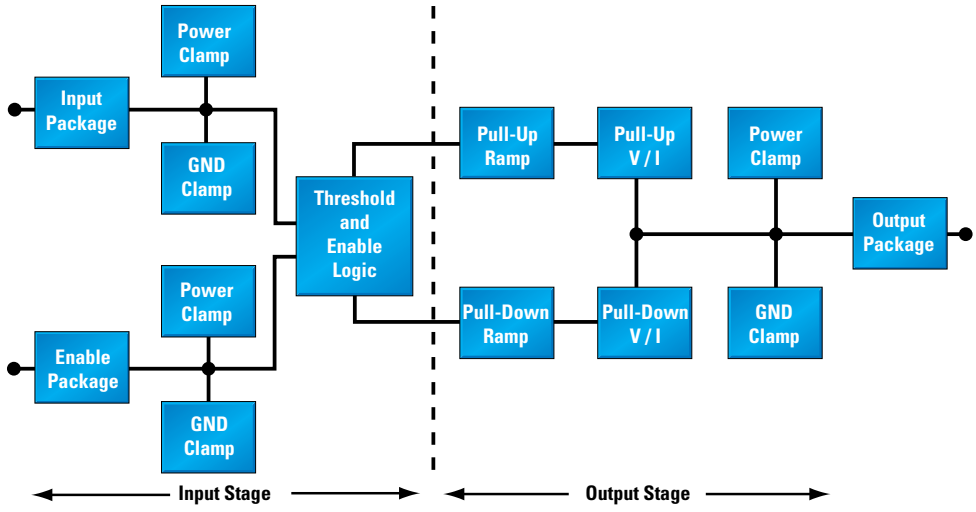


Figure 8-1. Input/output Buffer Information Specification

8.3 3-State Output Model

In a 3-state output, the output can be put into high impedance, as well as low and high states. The I-V data in the high-impedance condition is the power- and ground-clamp data. The power- and ground-clamp curves define the ESD structure of the output model and behave in the same manner as the clamps on the input. The device drive is modeled with three parameters for each of the high and low states. A V-I curve is provided for the high/low drive strength, a ramp term describes the slew rate for both rising and falling edges, and a rising/falling waveform value describes the transient output condition.

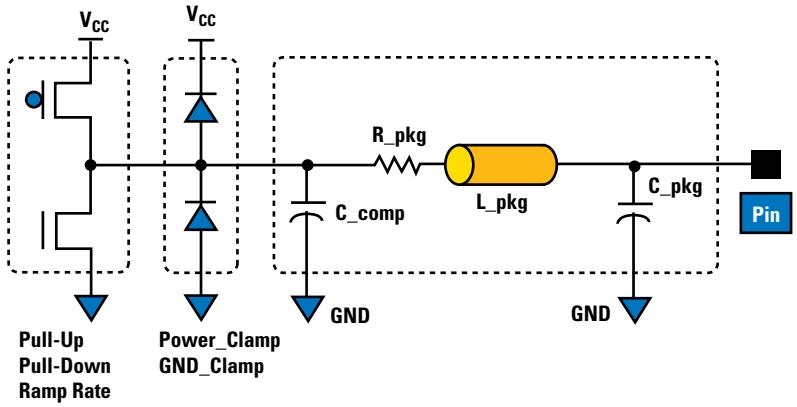


Figure 8-2. The IBIS 3-State Output Structure Model - The package characteristics and ESD structures are included and use the same notation as the input model

8.4 Creating IBIS Models

An IBIS model can be created from lab bench results, SPICE simulation data, or a combination of both. Although bench testing measures the actual performance of the device silicon, there are a couple of disadvantages to this approach. First, it is difficult to approximate process corners using bench results, and second, it is difficult to distinguish the package characteristics as required by IBIS.

At National Semiconductor, IBIS files are generated first using the most accurate SPICE netlists, including typical, maximum, and minimum values. Typical values are nominal V_{CC}, room temperature, and nominal process. Minimum values are weak process, high temperature, and minimum V_{CC}. Maximum values are strong process, cold temperature, and maximum V_{CC}. The SPICE-generated models then are verified by comparing the V-I curves and data values with the actual performance of the device in a bench environment. Prior to release, the model is subjected to a syntax and IBIS parser check, and is then posted on National's website.

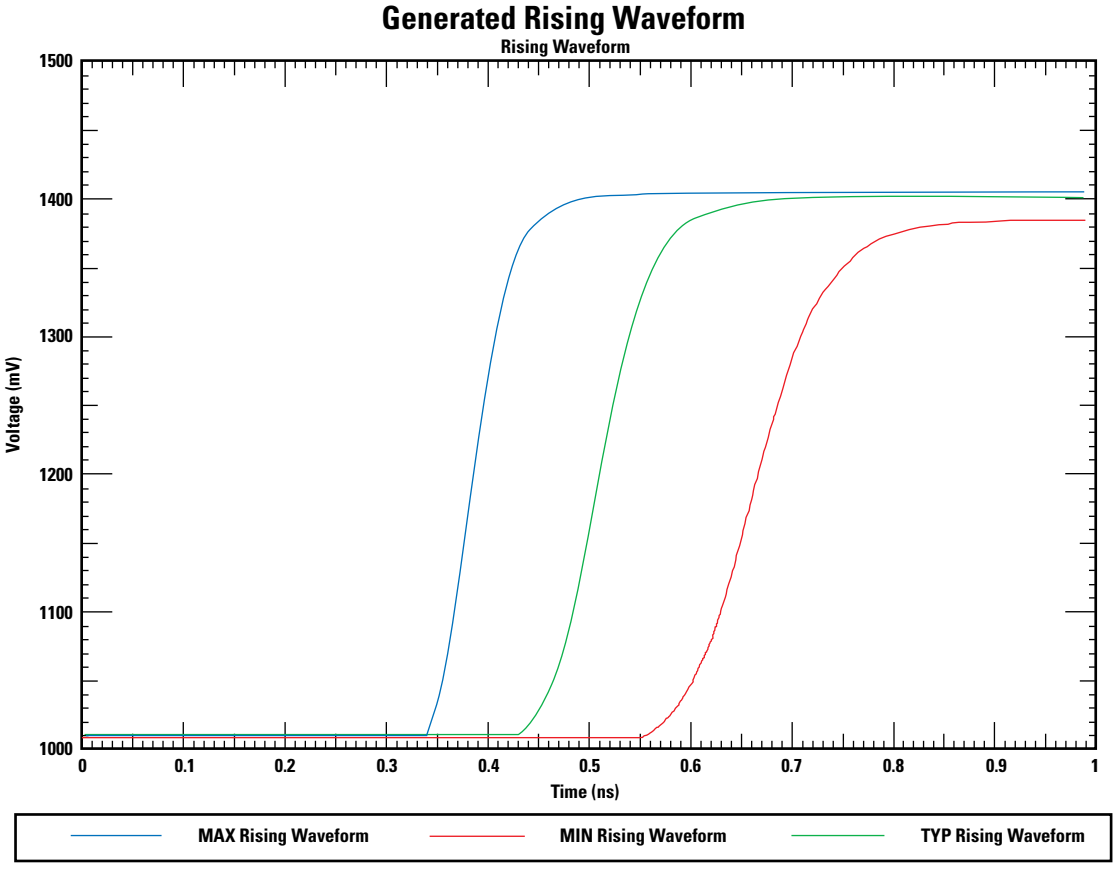


Figure 8-3. Typical Slew Rate Curve for IBIS Model of a LVDS Device

One limitation of IBIS models is that signal-conditioning features such as pre-emphasis are not well supported. For simulations that require these features, a more complex model may be required, such as SPICE (covered later in this section).

8.5 Scattering Parameters (S Parameters)

S parameters are properties used in communication systems to define and describe the electrical behavior of linear networks. S parameters are small signal representations of the network's response to steady-state stimulus.

While IBIS models provide simple yet accurate models for active ICs, S parameters are used to model the passive interconnect. The interconnect between a driver and receiver may be just a simple FR4 trace, or it might be complex, involving multiple connectors, different media, vias, and so forth. In either case, S parameters can be generated and used in simulation to create accurate signal-integrity models.

As with IBIS models, S parameters provide the advantages of an industry-standardized format, straightforward generation, and facilitate quick and accurate signal-integrity simulations. In the S parameter model, regardless of the complexity of the interconnect, the behavior at any node is predicted based on the stimulus at any other node.

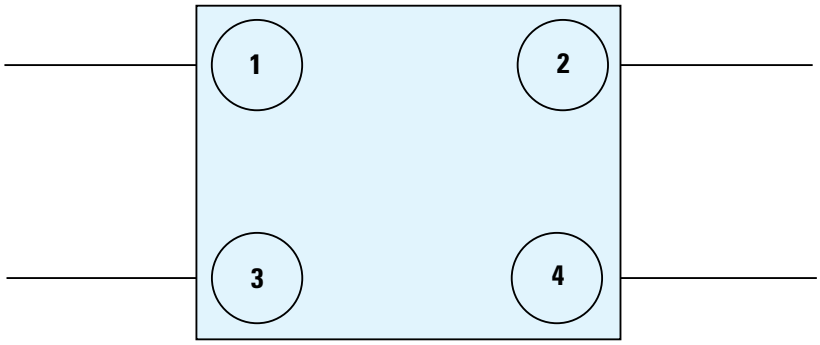


Figure 8-4. A Typical 4-Port S-Parameter Model

S parameters follow a naming protocol using two subscripts where the first digit represents the behavior at that specific node, and the second subscript, the node from where the stimulus is coming. For example, S_{21} would represent the response at node 2 to a defined stimulus at node 1. This interaction between each of the nodes can be recorded in a matrix format, in this case a 4 by 4. In the 4-port model shown in ***Figure 8-4***, the response to a stimulus at node 1 is described as follows:

S_{11} Reflection – this parameter describes the energy reflected back from the network to node 1.
S_{21} Insertion loss – this parameter indicates the amount of signal loss in the network as the signal propagates from node 1 to node 2.
S_{31} Near-end crosstalk
S_{41} Far-end crosstalk

S parameters are expressed in dBs and plotted versus frequency as seen in ***Table 8-5***; dB are calculated using the formula: dB = - 20log $_{10}$ (received signal/transmitted signal). Since S parameters are used to define passive networks, we can assume that the highest possible value would be 0 dB, i.e., no signal attenuation. Thirty percent attenuation would be -3dB, 50% would be -6 dB, and so forth.

Table 8-5. S Parameters Plot dBs versus Frequency

Normalized Rx Signal	Strength (dB)
1	0.0
0.7	-3.1
0.5	-6.0
0.25	-12.0
0.1	-20.0
0.05	-26.0
0.001	-60.0

In the example in ***Figure 8-6***, S_{21} (insertion loss) remains relatively flat until about 1 GHz and then the loss increases rapidly to about -25 dB at 10 GHz. This would be typical of transmission loss from source to receiver across a lossy media. S_{11} (reflection loss) is about -35 dB indicating consistent impedances across the network. S_{31} and S_{41} (near- and far-end crosstalk) are both below -50 dB, indicating minimal crosstalk.

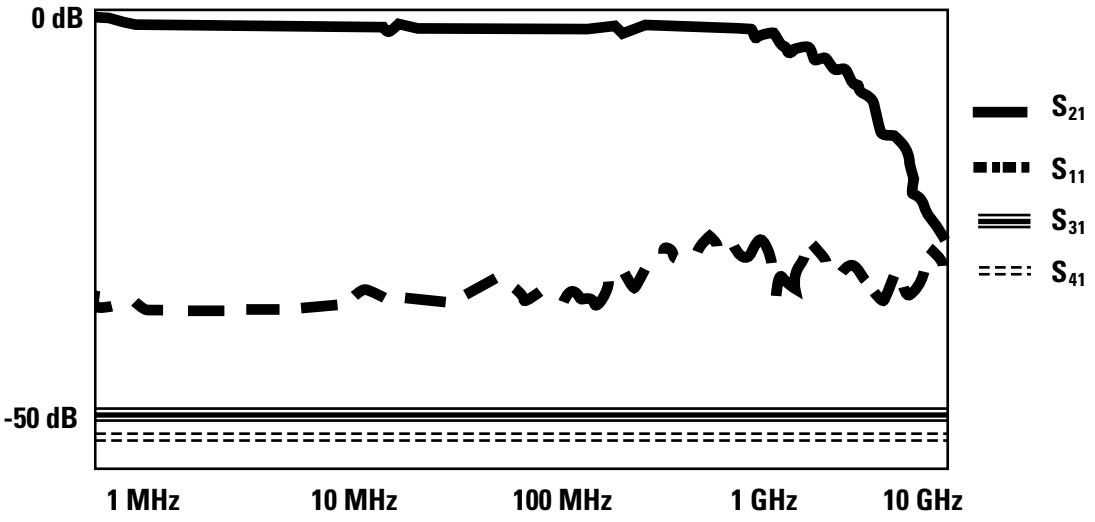


Figure 8-6. An Example of a Hypothetical Network with Stimulus Introduced at Node 1

S parameter models can be constructed with any number of ports; however, the application of most interest in this discussion is unidirectional point-to-point differential signaling. Although there are four potential ports in this instance, by referencing the two lines of the differential pair to each other, rather than ground, this model can be simplified to a 2-port model. For this simplified unidirectional model, the two parameters of most interest are S_{11} representing the reflection coefficient and S_{21} the insertion loss.

8.6 SPICE Models

Simulation Program with Integrated Circuit Emphasis (SPICE) is the pervasive IC modeling tool with over 30 years of industry usage. SPICE can be used to model a large inventory of passive- and active-circuit elements under various conditions including DC, AC, and transient stimulus. In simple terms, SPICE defines a network into a set of complex equations, and for given startup conditions and input stimulus, accurately predicts the circuit behavior.

SPICE uses an iterative approach to solving a large number of equations, and simulation times can be long and occasionally fail to converge. Dramatic increases in available computing power along with better circuit models have made these limitations less of a concern and SPICE is now capable of accurately modeling very large and complex analog networks.

Although SPICE provides superior models for active-circuit elements, IBIS models are generally more available. This is because SPICE models may contain proprietary vendor IP, and thus are frequently not provided, or only provided under NDA. Vendor-supplied SPICE models are often simplified versions that exhibit similar behavior but are altered to protect sensitive IP. SPICE simulations are also more complex and may take considerably longer than simulations using IBIS, which are often preferred for quick and relatively accurate simulations. When absolute accuracy is required, SPICE is the preferred tool.

9.1 Clock Distribution and Signal Conditioning

LVDS or CML often are used for distributing clocks, offering much better performance than single-ended solutions. Two basic architectures commonly are employed: point-to-point and multipoint.

Point-to-Point Clock Distribution

Also known as (1-n) or fan-out, the point-to-point architecture provides the lowest jitter and cleanest signals and is used for higher clock rates or for applications with the tightest jitter requirements.

The DS90LV110A is an example of a fan-out clock distribution device.

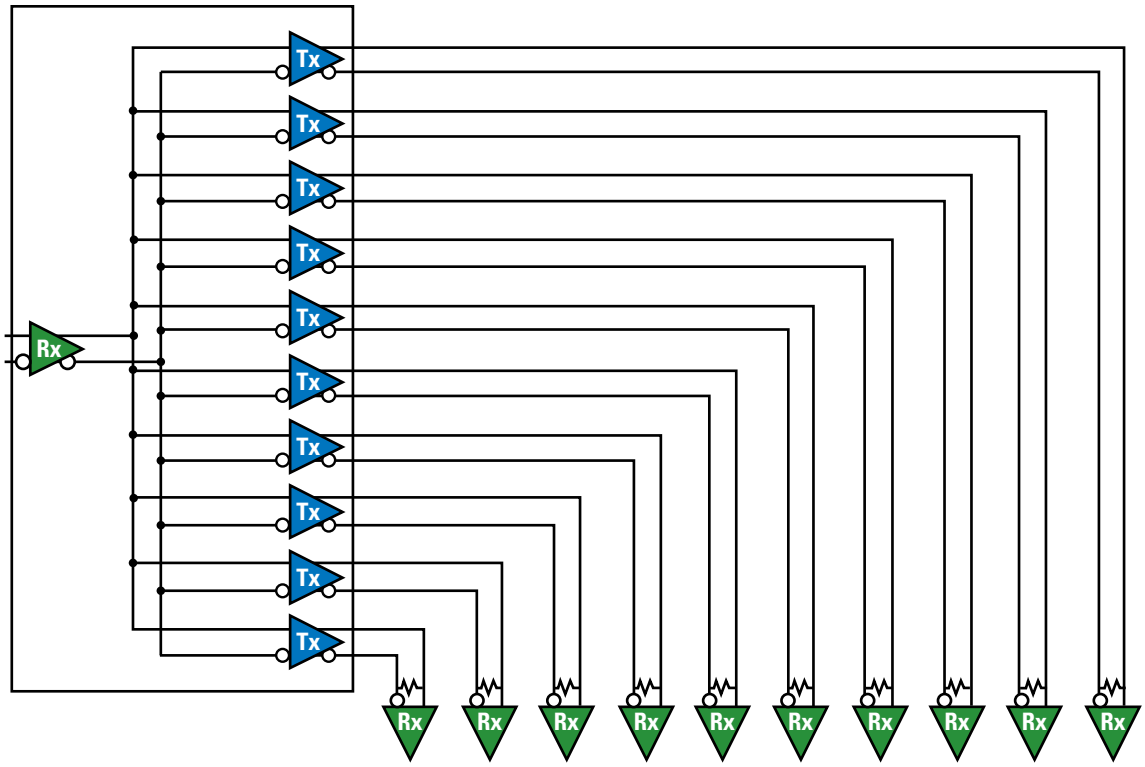


Figure 9-1. DS90LV110A 1-to-10 Fan-Out Buffer

Multipoint Clock Distribution

Multipoint clock distribution is an efficient and cost-effective solution in backplane environments. Multipoint solutions require the minimum amount of backplane traces or cabling and often support redundancy. An example is the Advanced Telecom and Computing Architecture (ATCA) that requires M-LVDS.

Multipoint configurations require B-LVDS or M-LVDS for additional drive. Multipoint works best when driving short distances and with very short stub lengths. Multidrop is similar to multipoint (***Figure 9-2***) but there is a single driver and multiple receivers.

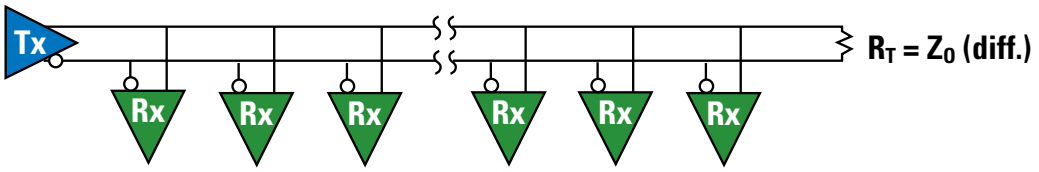


Figure 9-2. Multidrop Environment

A variety of devices support multipoint including National's DS92CK16 transceiver, which includes both B-LVDS drive for multipoint on the backplane and a 1-to-6 TTL fan-out buffer for the local card side. Other options are shown in ***Table 10-3***.

Table 9-3. Clock Distribution Selections

Device	F_{MAX} MHz	# of Rx	# of Tx	Comments
DS92LV010	75	1	1	TTL to B-LVDS, Drives up to 32 loads
DS91D176	125	1	1	TTL to M-LVDS, also DS91C176 with type-2 failsafe, DS91D180 full duplex
DS92001	200	1	1	LVDS to B-LVDS
DS92CK16	125	1	6 TTL 1 B-LVDS	Supports redundancy, can be master or slave
DS90LV110	400	1	10	Also available with failsafe, DS90LV110A
LMK01000 Family	1600	1	8	Extremely low 40 fs additive jitter, LVDS and LVPECL output options

Clock Conditioners

Signal-integrity clock devices such as the LMK family of devices designed by National offer a multitude of features to improve the clock performance of the system or backplane.

Table 9-4. Products for Clock Conditioning

Product ID	Clock Freq. (MHz)	LVDS Outputs	LVPECL Output	VCO	PLL	VCO Freq. (MHz)	MS Jitter (pS)
LMK04000 Family	0 to 800	5 to 7 LVDS, LVPECL, CMOS		Crystal	Integrated	1185 to 2160	0.2
LMK02000	0 to 800	3	5	External	–	–	0.2
LMK02002	0 to 800	0	4	External	–	–	0.2
LMK03000C	1 to 648	3	5	Integrated	Integrated	1185 to 1296	0.4
LMK03001C	1 to 785	3	5	Integrated	Integrated	1470 to 1570	0.4
LMK03002C	1 to 862	0	4	Integrated	Integrated	1566 to 1724	0.4
LMK03000	1 to 648	3	5	Integrated	Integrated	1185 to 1296	0.8
LMK03001	1 to 785	3	5	Integrated	Integrated	1470 to 1570	0.8
LMK03002	1 to 862	0	4	Integrated	Integrated	1566 to 1724	0.8
LMK03000D	1 to 648	3	5	Integrated	Integrated	1185 to 1296	1.5
LMK03001D	1 to 785	3	5	Integrated	Integrated	1470 to 1570	1.5
LMK01000	0 to 1600	3	5	–	–	–	0.04 (additive)
LMK01010	0 to 1600	8	0	–	–	–	0.04 (additive)
LMK01020	0 to 1600	0	8	–	–	–	0.04 (additive)

The LMK family of precision clock conditioners interface directly to the receiver in a multipoint or multidrop environment. Loads can affect the duty cycle, edge rate, and system margin, especially in multipoint environments that have up to thirty-two terminations. The LMK04000, LMK03000, and LMK02000 family of clock conditioners receive the dirty clock from the backplane and provide a cleaned and balanced clock of the same frequency or other related clock frequencies to various card slots. When clock cleaning or frequency multiplication is not required, the LMK01000 family can be used as ultra-low jitter-clock dividers and distributors.

For example, ***Figure 9-5*** shows a 122.88 MHz clock driven from slot 7 to slot 8 on a fully-loaded ATCA backplane. In this environment, the clock signal is experiencing bandwidth limitations and the duty cycle is 45% to 55%.

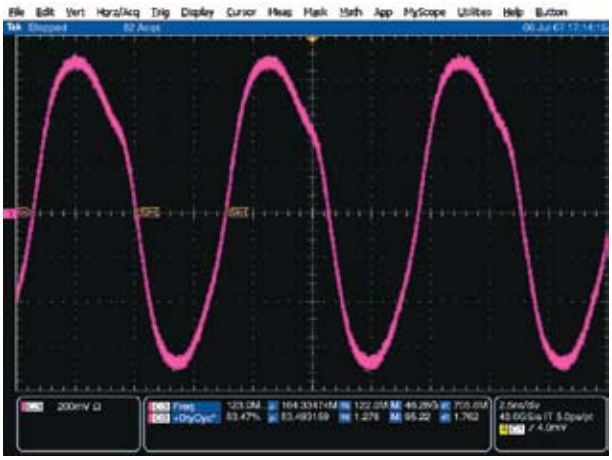


Figure 9-5. M-LVDS Clock Signal on a Fully-Loaded ATCA Backplane

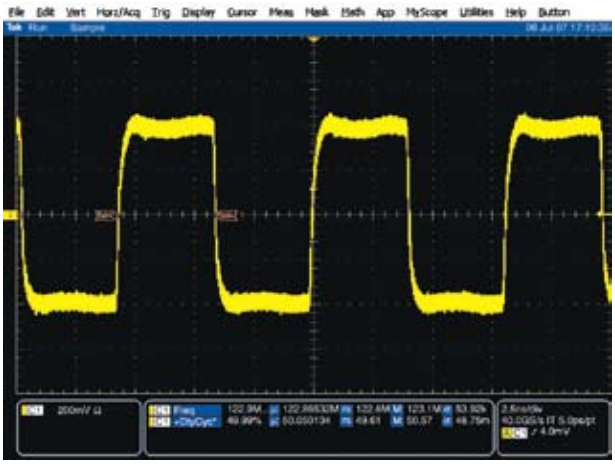


Figure 9-6. LMK03000 Clock-Conditioner Output

Note the duty cycle correction by the LMK03000 clock conditioner in ***Figure 10-6***. The LMK family of pin-compatible devices offers both LVDS and LVPECL outputs up to 785 MHz with industry-leading jitter performance. A variety of products in this family (***Table 9-4***) distribute up to eight clock signals to card applications requiring multiple clock frequencies free of duty-cycle distortion, with improved phase noise and very low jitter. The LMK04000 family has a cascaded PLL architecture for superior jitter cleaning without the need for an expensive VCXO.

10.2 System Clock Distribution

The Advanced Telecommunications and Computing Architecture (ATCA) and MicroTCA systems, along with many other communication systems, require synchronization of their internal interfaces and the external networks. The respective PCI Industrial Computer Manufacturers Group (PICMG) standards define synchronization-clock interfaces in these systems, and, as such, have assigned the task of distributing clock signals to ICs, which conform to the *TIA/EIA-899* standard (Multipoint Low-Voltage Differential Signaling or M-LVDS).

This section provides a quick overview of the AdvancedTCA- and MicroTCA-compliant clock-distribution networks. For the M-LVDS-clock-distribution design guidelines, refer to **Application Note AN-1503: "Designing an Advanced TCA-Compliant MLVDS Clock Network"**

ATCA-Synchronization Clock Interface

In an AdvancedTCA backplane, the clock-synchronization interface enables exchange of timing information between all slots in the backplane. It consists of three redundant clock busses: CLK1, CLK2, and CLK3. Each clock bus, together with connections to M-LVDS clock drivers/receivers/transceivers, forms a multipoint clock-distribution network. ***Figure 10-7*** illustrates six M-LVDS-clock-distribution networks that are formed when multiple line cards are installed in the backplane.

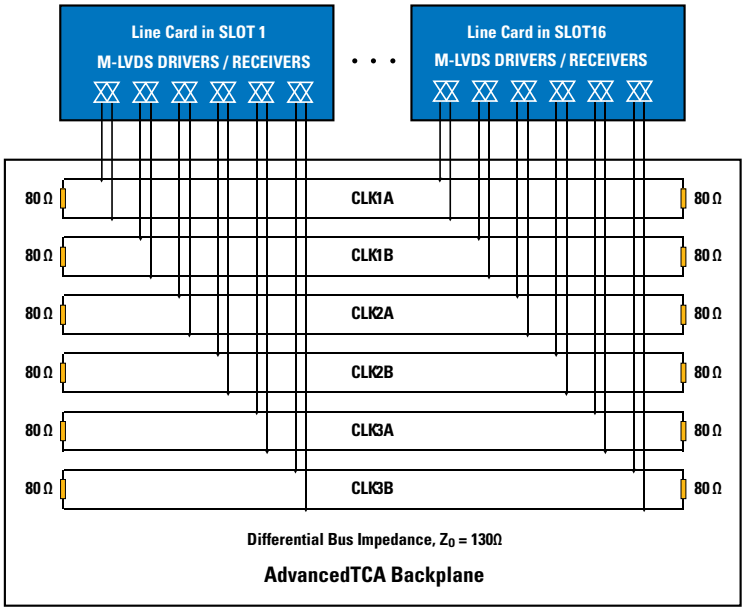


Figure 9-7. AdvancedTCA Clock-Distribution Interface Example

Short, narrow stubs coupled with signal drivers (i.e. M-LVDS line driver) that have a controlled-output edge rate are the key to increased noise margin and improved overall performance of any multipoint network. M-LVDS clock-distribution networks in AdvancedTCA backplanes benefit from those same methods.

MicroTCA-Synchronization Clock Interface

MicroTCA defines both non-redundant and redundant clocking architectures. The non-redundant architecture is for single MicroTCA Carrier Hub (MCH) systems as exemplified in ***Figure 9-8***. Note that the clock bus is terminated on the backplane at the MCH card and on the Advanced Mezzanine Card (AMC), and forms a point-to-point topology.

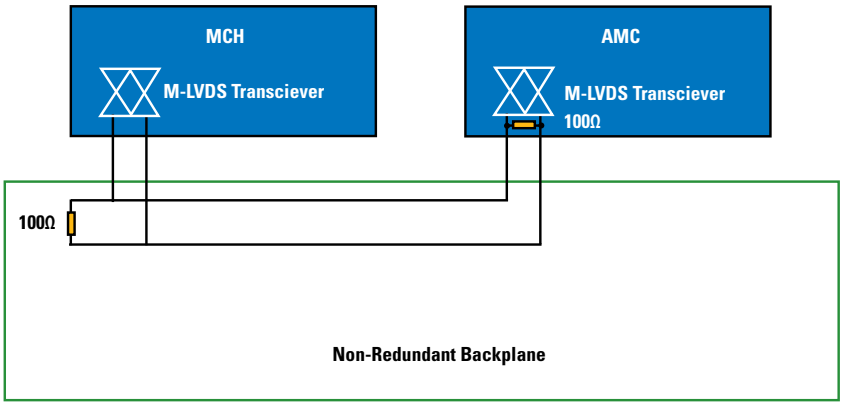


Figure 9-8. MicroTCA Non-Redundant Clock-Distribution Interface Example

The redundant clock architecture, as illustrated in ***Figure 9-9***, is for dual MCH systems that operate in a redundant manner. The effects of unterminated stubs in this multipoint topology variant are minimized with the use of series resistors. The controlled signal edges of M-LVDS devices further aid in distributing clocks to all cards within a system.

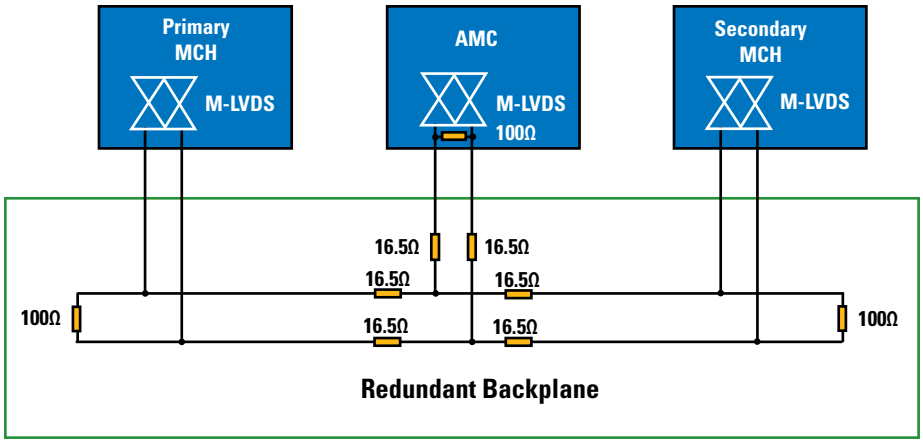


Figure 9-9. MicroTCA Redundant Clock-Distribution Interface Example

9.3 Complementing FPGA Performance

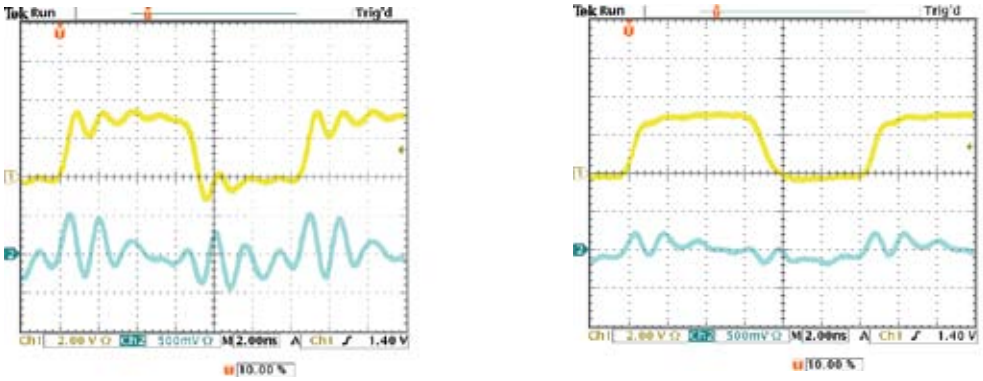
So much effort is spent in today's systems planning upgrades for growth, flexibility, and programmability that it is not surprising to see Field-Programmable Gate Arrays (FPGAs) populating communications, computing, industrial, and even space applications. FPGAs can be used successfully in many ways including high-speed interface, embedded microprocessors, and Digital Signal Processing (DSP).

With all of these advantages, there are also some limitations in using FPGAs. One challenge is meeting the *EIA-899* specifications for multidrop LVDS signaling. A large part of FPGA selection is based on control and management of the system interfaces. Having the right complementary support components helps the system meet these specifications.

Extending SerDes Enables FPGAs

The Altera Cyclone or Xilinx Spartan line of products are good examples of economical FPGAs intended for low-to-medium-speed applications. These FPGAs do not contain the advanced serialization or deserialization circuitry necessary for truly high-speed communications, and limit the maximum data rate to 640 Mbps. This makes the Cyclone and Spartan good candidates for an external SerDes interface. Using an external SerDes interface to a FPGA allows a parallel or multi-pair interface to be condensed to one or more high-speed signal pairs.

The external SerDes parallel interface increases the distance LVCMOS signals may travel across a backplane or ribbon cable by substituting a low-power, high-speed differential signal for the entire parallel interface. This reduces system EMI as well as the Simultaneous Switching Output (SSO) noise present in the system. SSO noise, also known as ground bounce, is a result of large instantaneous changes in current across the power/ground inductance of the IC. This potential problem becomes more and more serious as the number of active high-drive LVCMOS outputs on a FPGA design increases. In large FPGAs with several synchronous parallel interfaces, this phenomenon can result in poor system performance or intermittent data errors.



Active Outputs **Device Ground**

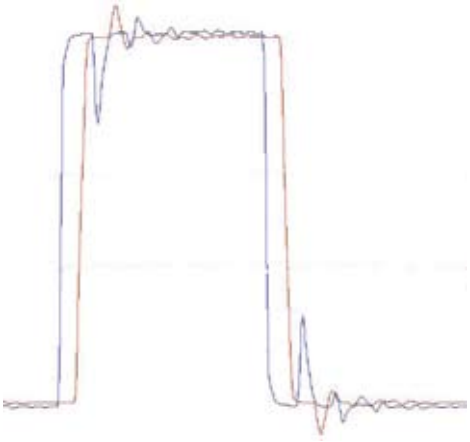
Figure 9-10. Noisy High-Drive LVCMOS Waveforms vs. Quiet Low-Drive LVCMOS Waveforms

Reducing FPGA drive current (***Figure 9-10***) generally improves the signal integrity and lowers the jitter of output clock and data signals. Excessive noise or jitter on the clock signal is a good indication of diminished FPGA PLL analog performance. In addition to the reduction in FPGA performance, analog devices located adjacent to the FPGA will be affected by the increase in ground noise.

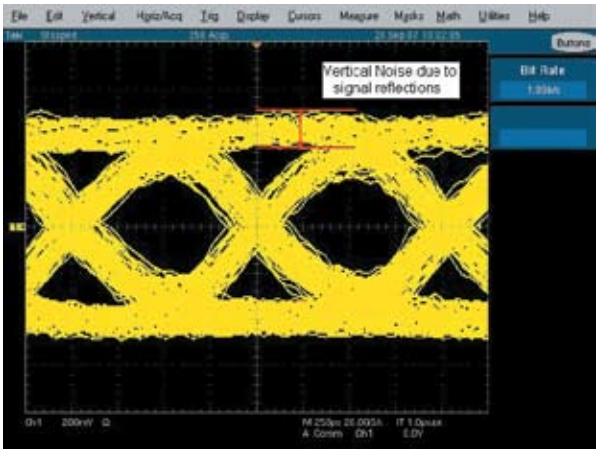
Load Capacitance is Critical

One factor often overlooked is the effect I/O capacitance can have on signal integrity at Gbps speeds. Some FPGAs suffer from having high I/O capacitance that becomes a major issue as the round-trip delay of the interface approaches or exceeds a single-unit-interval time of the transmitted data. Excess I/O capacitance will result in an impedance dip at the transmitter and receiver. Any reflections seen at these discontinuities will result in some portion of the energy reflected back onto the transmission media.

This process repeats as the transition energy encounters more impedance discontinuities until the energy fades into the background noise level after several round-trip-delay cycles. Due to the electrical length of the transmission line and bit width of the serial data, reflections from previous data transitions will impose themselves on subsequent data patterns. This additive energy increases jitter and reduces noise margins across the interface.



At 50 MHz, the simulation waveform shows reflections at the driver and receiver due to excess I/O capacitance, even with the transmission line properly terminated. These reflections will cause significant Inter-Symbol Interference (ISI) as the data rate is increased.



Increasing the data rate to 1 Gbps allows reflections from the driver and receiver to span almost 7 UI. The actual position of a signal at the receiver is being altered by any transitions during the previous seven data bits resulting in an eye diagram with a large DJ component.

Figure 9-11. Examples of ISI Due to the Effects of Load Capacitance

In order to reduce the negative effects of high I/O capacitance, the round-trip delay of the transmission media should be minimized; ideally, less than a single-bit width of the serial data. Reducing the length does not magically eliminate the bandwidth-robbing effects of a large, lumped capacitance. It places the capacitance in a very short transmission line, which allows for multiple data reflections to occur within a single bit period. With each reflection, the amplitude of the dynamic energy will be reduced, resulting in a higher-quality waveform at the receiving device.

LVDS Translation

Even though the FPGA LVDS architecture has limited headroom beyond 1 Gbps, discrete LVDS implementations can be used effectively to get data rates in excess of 3 Gbps. Using LVDS beyond 1 Gbps often involves mixing differential technologies and resolving design trade-offs over signal amplitude, output voltage, and translation.

The first hurdle to success is the assessment of signal amplitude (see ***Figure 9-12***). It often stems from the different way LVDS and many other differential interfaces are specified. For LVDS, the output amplitude or V_{OD} (as defined in *EIA/TIA-644A*) is the voltage difference across the driver outputs with a 100Ω load. Other differential standards have specified the output voltage amplitude as a peak-to-peak number. As an example, a 400 mV LVDS V_{OD} is exactly equal in amplitude to an 800 mV peak-to-peak CML output. (Refer to the **Translation Section, page 31** for further information).

As receivers, LVDS devices offer the greatest flexibility of any differential technology. The wide-input common-mode range easily spans the normal operating regions of 1.2V/1.5V/2.5V CML and LVPECL differential I/O. This allows for direct connection of most differential outputs to LVDS inputs, minimizing the PCB space and cost of multiple AC-coupling capacitors. The minimum LVDS output V_{OD} is specified to be 250 mV or 500 mV peak-to-peak. This output amplitude enables a low-EMI, low-power solution that can be coupled with output signal-conditioning features to drive extended lengths of cable or large backplanes.

The LVDS output drives a 1.2V common-mode voltage developed from an internal bandgap reference. This output can be DC coupled to many LVPECL inputs. Since the LVDS output-voltage swing does not meet the common-mode requirements specified, the CML inputs (with a limited common-mode range) will require an AC-coupled interface for the input.

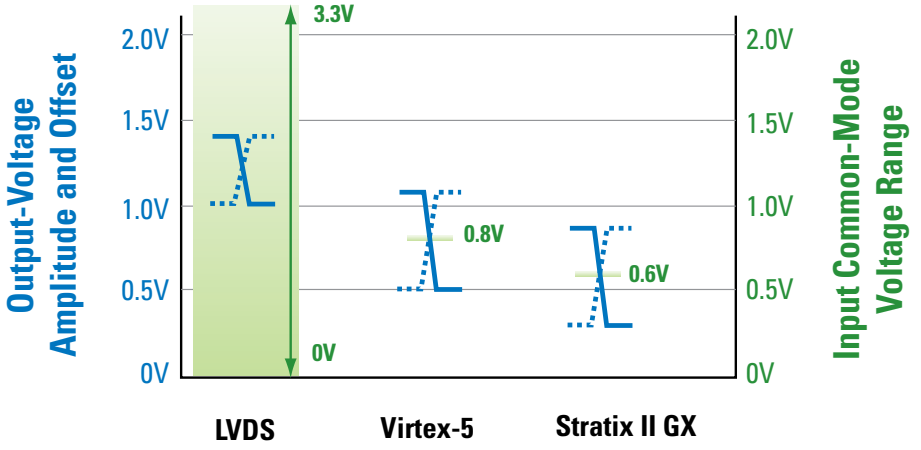


Figure 9-12. V_{OD} versus Input Common-Mode Range of Various Differential Interfaces

A low-power solution for redundancy, multiplexing, and distribution can be achieved with a combination of high-performance LVDS crosspoint switches and high-speed FPGA CML I/O.

LVDS inputs have been designed to work with peak-to-peak signal amplitudes of 200 mV to 1600 mV, but are optimized for signals in the 500 mV to 800 mV voltage range. Programming CML outputs for 600 mV to 800 mV will reduce transmit power expended by the FPGA-integrated SerDes and lower the overall EMI signature of the interface.

In summary, the high performance and flexibility of FPGAs often can be enhanced further by selecting the appropriate complementary devices. Simultaneous-switching output noise of low-cost Spartan and Cyclone devices can be reduced by using an external Ser/Des. FPGA cable reach can be extended using external signal conditioners. FPGA inputs with high-capacitive inputs can produce ringing and bit errors. These high C_{IN} can be effectively "hidden" using adjacent repeaters. Signals intended for multidrop can be buffered using high-drive B-LVDS or M-LVDS devices. These are all examples of external devices complementing FPGA performance and providing additional flexibility to design engineers.

9.4 Broadcast Video

Modern broadcast video relies on high-speed error-free transmission of serial digital video. Jitter reduction and minimized noise are essential ingredients in maintaining the necessary signal integrity. ***Figure 9-13*** shows a simplified 3 Gbps Serial Digital Interface (SDI) video router.

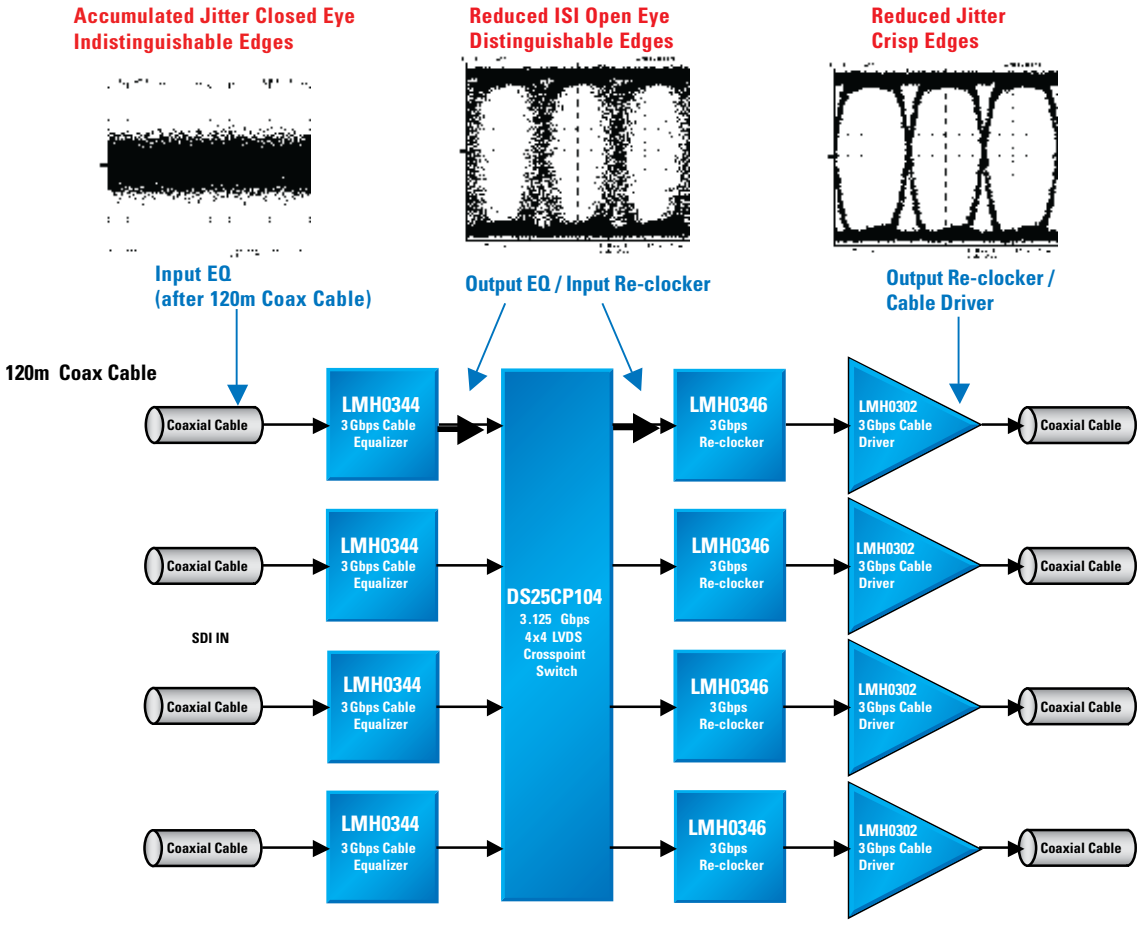


Figure 9-13. Simplified 3 Gbps Serial-Digital-Interface Video Router

High-speed data transmissions introduce several challenges for maintaining signal integrity. The 3 Gbps SDI router shown in ***Figure 10-13*** provides signal conditioning to reconstruct waveforms to their original integrity. The SDI equalizer opens the "eye" of the waveform and reduces ISI. National's LMH0344 adaptive cable equalizer automatically adapts and equalizes up to 120m of coaxial cable at 3 Gbps rates, 140m at HD rates, and 350m at SD rates.

The DS25CP104 4x4 LVDS crosspoint switch has selectable FR4 equalization and pre-emphasis to adjust conditioning for various system architectures. The SDI re-clocker reduces high-frequency jitter to provide crisp, clean edges, and the cable driver sets the appropriate amplitude and slew rates to meet SDI standards defined by the Society of Motion Picture and Television Engineers (SMPTE).

National offers a comprehensive portfolio of video products for SD, HD, and 3 Gbps SDI applications.

9.5 Extending the Reach of SerDes

Serializers and Deserializers (SerDes) are an integral piece of most of today's high-speed systems. One of the design constraints for these systems is the maximum transmission distance between a serializer and a deserializer. While most SerDes can support transmission over only several meters of cable, many systems require the transmission distance between a serializer and a deserializer to be tens and even hundreds of meters. The DS15BA101 and DS15EA101 is a cable-extender chipset that enables long-reach applications for SerDes chipsets as illustrated in ***Figure 9-14***.

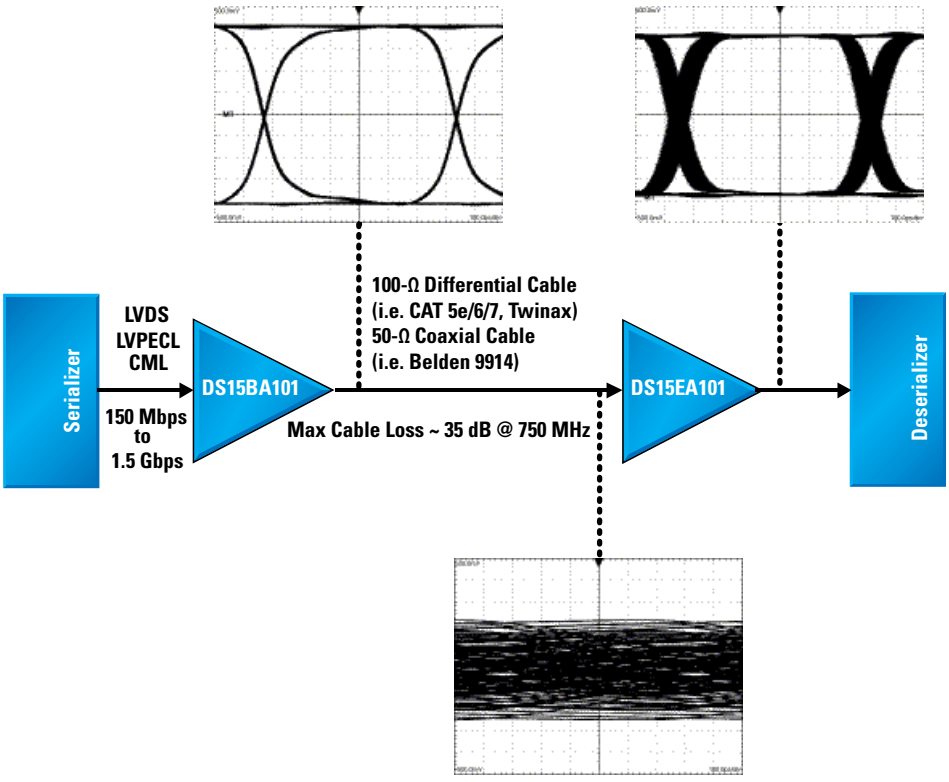


Figure 9-14. Typical Cable-Extender-Chipset Application

It is important to realize that automatic equalization is dependant on the signal amplitude at the transmitter end of the cable. The DS15EA101 device "assumes" that the amplitude of either single-ended (if equalizing coaxial cables) or differential-signal (if equalizing differential-balanced cables) cables is 800 mV p-p ±10%. The energy-detector circuitry in the DS15EA101 device senses the incoming signal amplitude and feeds this analog information to the automatic equalization-control circuitry that instructs the equalizer filter to apply a certain amount of gain to high-frequency components of a signal.

Any deviation from the optimal signal amplitude in either direction will cause the equalizer filter to assert either excessive or an insufficient amount of gain. This mismatch between the equalizer gain and cable's loss characteristics will result in sub-optimal equalizer performance, higher-output residual jitter, and ultimately, system bit errors. The DS15BA101 device is able to meet this DS15EA101 device's requirement in systems utilizing both 50Ω coaxial cables and 100Ω differential balanced cables (e.g. twin-axial and twisted pair cables) and needs to be used as a companion of the DS15EA101 device.

Identifying Cable-Extender-Chipset Benefits

While any SerDes chipset that transmits/receives serialized data that is within the 0.15 to 1.5 Gbps operating range may benefit from the cable-extender chipset, SerDes that operate with a single high-speed serial DC-balanced data stream (e.g. embedded clock SerDes) are best suited for coupling with the cable-extender chipset. SerDes that operate with multiple serial data and clock streams (e.g. parallel clock SerDes) may also benefit from the cable-extender chipset, however, these SerDes run into channel-to-channel skew issues before they encounter cable loss problems. ***Table 9-15*** lists selected National SerDes that may be coupled with the cable-extender chipset. For the full list of currently available SerDes, visit national.com/LVDS.

Table 9-15. Selected SerDes Pairs that Can Benefit from the Cable-Extender Chipset

SerDes Chipset	Clock Frequency Range (MHz)	Raw Serial Data Rate Range (Mbps)
10-Bit Embedded Clock SerDes		
DS92LV1021A/DS92LV1212A DS92LV1023E/DS92LV1224 SCAN921025H/SCAN921226H	16 to 40 40 to 66 20 to 80	192 to 480 480 to 792 240 to 960
16-Bit and 18-bit Embedded Clock SerDes		
DS92LV16 DS92LV18	25 to 80 15 to 66	450 to 1440 300 to 1320
24-bit Embedded Clock SerDes		
DS90C124/DS90C241 DS90C124/DS90C241 DS99R103/DS99R104	5 to 35 5 to 43 3 to 40	140 to 980 140 to 1204 84 to 1120

Typical Transmission Distance Gains

The DS15EA101 is an adaptive equalizer optimized for equalizing data transmitted over coaxial and differential-balanced copper cables. It automatically equalizes any cable length from zero meters to lengths that attenuate the signal by approximately 35 dB at 750 MHz. Depending on cable loss characteristics, transmission distance gains may range from several tens of meters to even few hundreds of meters. For more information about the cable-extender chipset, its typical performance with various cables, and reference design, check the following link: www.national.com/appinfo/lvds/drivecable02evk.html

Extending Signal Transmission with Conditioning

In applications where low-to-medium-quality cables are used, LVDS devices (and other high-speed interface devices) are limited to transmission distances of several meters. High-performance, low-loss cables may enable data transmission over longer distance, but these solutions increase the system cost.

The output-signal-conditioning technique used to improve LVDS performance is pre-emphasis. Pre-emphasis is a controlled amplitude and duration-output overdrive used to compensate for high-frequency losses and extend transmission distance over cables and backplanes. The simplest pre-emphasis scheme is full-first-bit pre-emphasis as shown in ***Figure 9-16***.

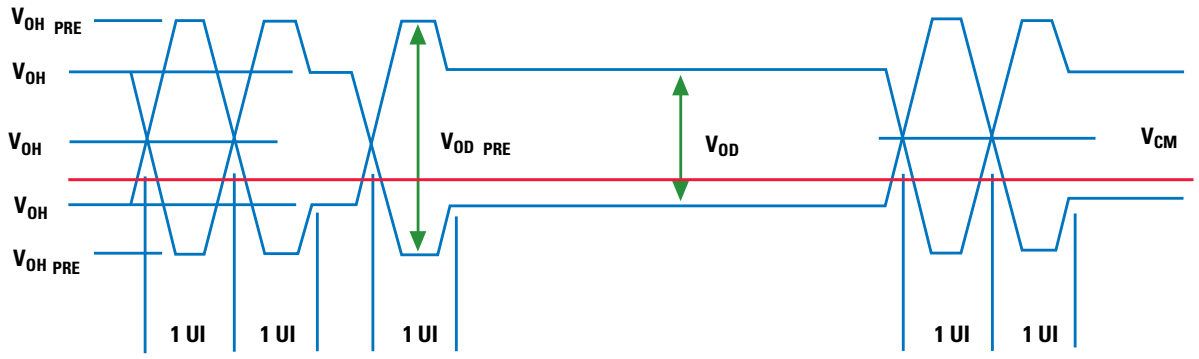
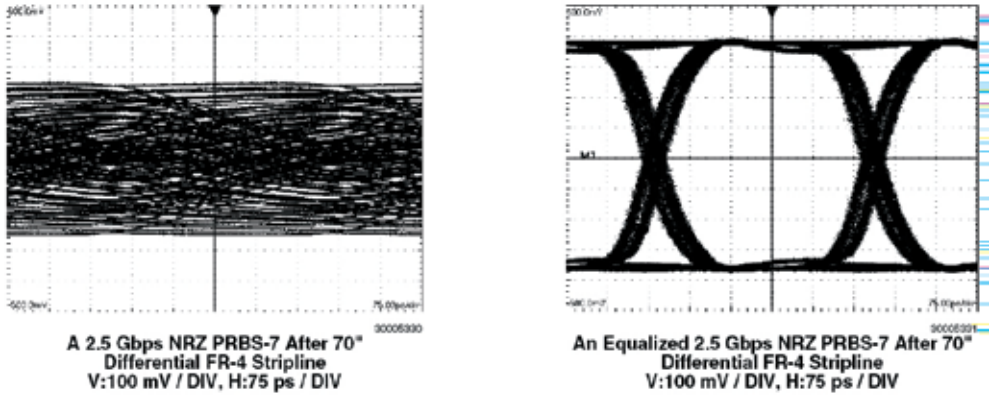


Figure 9-16. Pre-Emphasis Signal with 1 Gbps Timing

Equalization circuits are used to condition received signals. The equalizer is a function applied at the receiver to counteract the high-frequency degradation or loss across the transmission media. The equalizer flattens the transmission frequency response by acting as a high-pass filter that approximately complements the low-pass effect of the transmission medium within the data signal's frequency band. When properly tuned, equalization can significantly reduce the ISI effects from the transmission media as shown in ***Figure 9-17b***.



A) Measured at the Equalizer Input

B) Measured at the Equalizer Output

Figure 9-17. 2.5 Gbps NRZ Signal after 70" of FR-4 without Equalization (A) and with Equalization (B)

High-speed devices from National such as the DS25BR110 buffer feature a receiver-input equalization circuit to reduce the effects of frequency-dependent losses caused by the transmission medium (***Figure 9-17***). Multiple levels of equalization control ranging from 0 dB to 16 dB allow for easy optimization of signal quality across a broad range of typical transmission media lengths.

Power-Saver Equalizers

Another cable-extending option is a power-saver equalizer. Power savers require no power or ground connection but can produce as much as 7 dB relative boost. Power savers are especially well suited for placement in connectors as they provide equal boost in either direction and require no power or ground.

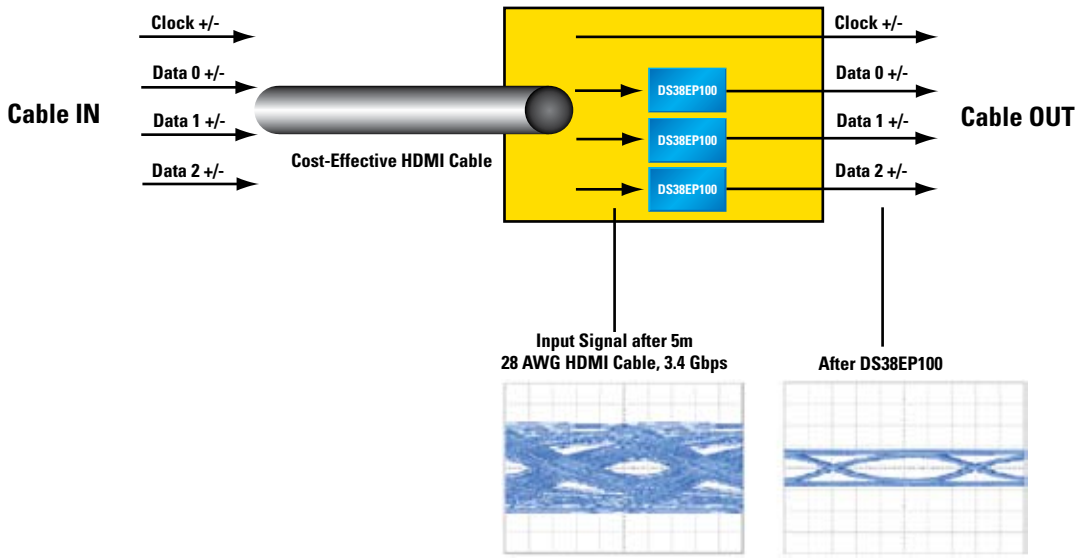


Figure 9-18. Power-Saver Equalization

9.6 M-LVDS: A High-Speed, Short-Reach Alternative to RS-485

Both *TIA/EIA-485-A* (RS-485) and *TIA/EIA-899* (M-LVDS) are popular electrical standards for binary data interchange over a multipoint differential bus. Both utilize differential signaling for low power, high speed, and excellent noise immunity for robust differential data transmission.

When it comes to driving signals over long cables, the larger swing of RS-485 along with a wider-input common-mode range help to achieve longer transmission reach. However, M-LVDS devices offer significant advantages such as higher speed, much lower power consumption, and radiated EMI. These key M-LVDS characteristics are beneficial in many applications.

Table 9-19. Comparison of Key Driver and Receiver Parameters

Parameter	RS-485	M-LVDS
V_{OD} [V]	1.5 to 5.0	0.48 to 0.65
I_{DD} [mA]	28 to 93	9 to 13
I_{OS} [mA]	<250	<43
t_{RISE} / t_{FALL} Typ [ns]	5 to 50	1 to 5
Data Rate Max [Mb/s]	40	250
V_{ID} [V]	0.4 to 5.0	0.1 to 2.4
V_{ICM} [V]	-5.0 to 12.0	-1.4 to 3.8

While RS-485 multipoint differential busses are long reaching and typically implemented with cables as transmission media, M-LVDS devices have found applications in backplane environments. A common application space that both interfaces share is a point-to-point signal transmission over long cables.

Figure 9-20 shows a typical cable length (CAT-5e) as a function of the bit-rate characteristic of RS-485 and M-LVDS point-to-point links. The sloped portion of the RS-485 curves is determined based on the maximum attenuation of 9 dB at the frequency of $1/t_{UI}$ in hertz, where tUI is a unit interval at a given signaling rate. This is an accepted industry guideline for determining the maximum signaling rate for the RS-485 point-to-point links. The flat portion of the RS-485 curve is based on the Ohmic loss of a typical CAT-5e cable (9Ω/100m), with the maximum allowed loss of 9 dB.

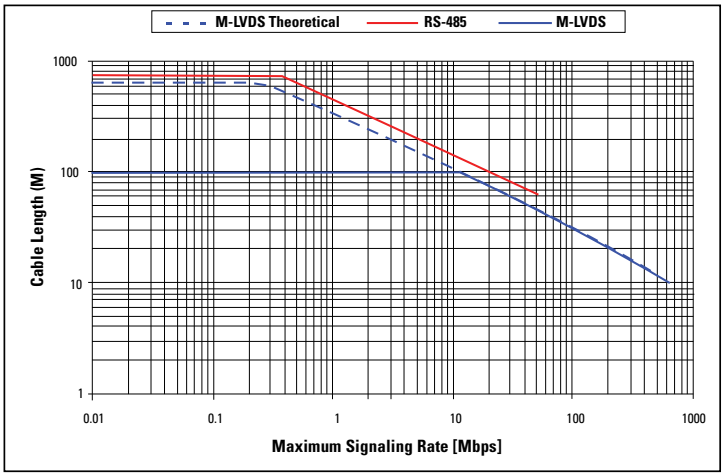


Figure 9-20. CAT-5e Length as a Function of Bit Rate for M-LVDS and RS-485 Point-to-Point Links

For networks that use interface ICs with reduced voltage swing for higher signaling rates (i.e. M-LVDS), the maximum attenuation of 6 dB at $1/t_{UI}$ hertz may be used as a general guideline when determining maximum signaling rate for a given cable length. The M-LVDS dashed curve is a product of such a guideline. Note that the M-LVDS receiver-input common-mode range of –1.4V to 3.8V makes M-LVDS a robust interface for connecting subsystems that may have a potential difference between their ground references of ± 1V. However, this relatively wide input common-mode range is generally sufficient for transmission distances of up to 100m.

Applications that have driver and receiver cards separated by more than 100m are likely to experience ground potential differences greater than ±1V. In such harsh environments, the recommended interface is the RS-485 with its input common-mode range of -7V to 12V that allows for ± 7V of unwanted voltage. At distances less than 100m, M-LVDS supports higher data rates with reduced power and EMI.

9.7 Redundancy

The term “high availability” refers to systems that must demonstrate very little downtime. An example is the famous “five 9s” from the Telecom industry where critical systems are required to be online 99.999% of the time. A common approach to ensure high availability is the use of redundancy, where each essential hardware component is twinned with a standby unit, ready to take over in the event of a failure. A simple redundant network is shown in ***Figure 9-21***.

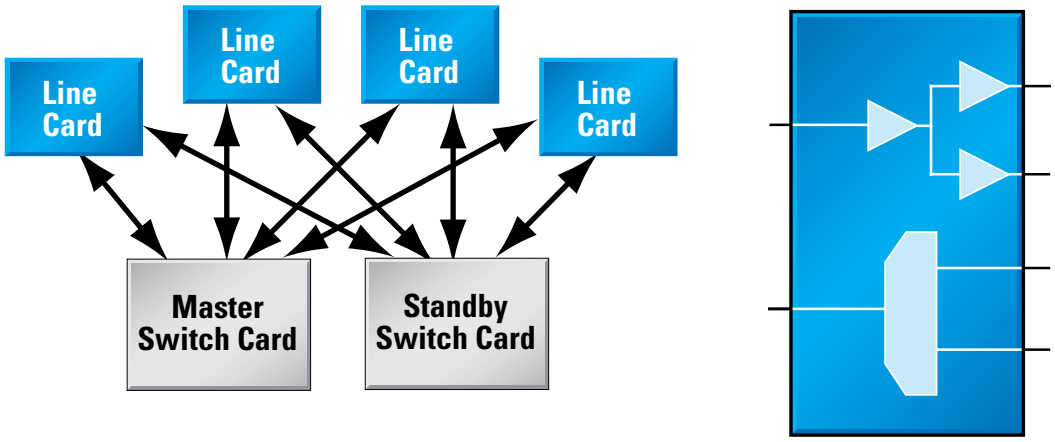


Figure 9-21. Simple Dual-Star Redundant Network

In this redundant network, each linecard requires a 1-to-2 select buffer to send signals to either switch card then a 2-to-1 mux receives the signals. A dedicated IC to provide this functionality is known as a “Mux/Buffer” and National offers this function in various speeds, grades, and configurations. (***See Table 9-22***)

Table 9-22. Mux/Buffer Product Table

Device	Data Rate (Mbps)	# of Channels	I/O	Features
DS08MB200	800	Dual	LVDS	800 Mbps Multiplexer/Buffer
DS15MB200	2000	Dual	LVDS	Pre-emphasis
SCAN15MB200	2000	Dual	LVDS	Pre-emphasis, JTAG
DS25MB100	2500	Single	CML	Equalization / Pre-emphasis
DS25MB200	2500	Dual	CML	Equalization / Pre-emphasis
DS40MB200	4000	Dual	CML	Equalization / Pre-emphasis
DS42MB200	4200	Dual	CML	Equalization / Pre-emphasis
DS42MB100	4200	Single	CML	Equalization / Pre-emphasis

9.8 Testability of High-Speed Differential Networks

Testability is an essential consideration in advanced system design. Testability directly affects time-to-market, product quality, and manufacturing costs. High-speed differential technology often represents a significant percent of the total nets in a system, making differential test a major concern.

The JTAG standard, IEEE1149.1 is used extensively in digital logic and can be used to test differential networks. In this case, each differential pair is treated as a single logic connection and a single JTAG-boundary-scan cell is used to force/sense the differential connection, as seen in ***Figure 9-23***.

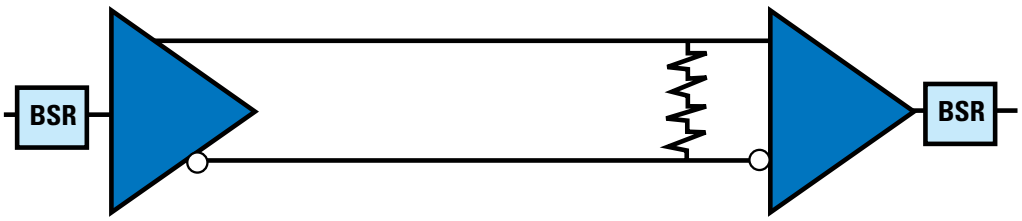


Figure 9-23. IEEE1149.1 JTAG Used for Differential Nets

Although this approach provides some test coverage, there are two major drawbacks. Most JTAG testing is performed at slow clock rates between 1 MHz and 15 MHz. Differential technologies are inherently fault tolerant, and will continue to operate to some degree even with gross faults such as a single open or short, or a missing termination resistor. At the slow JTAG test speeds, often a differential link will correctly pass ones and zeros even with these gross faults.

The second problem involves the very common AC coupling of differential nets. Since digital JTAG is a DC-based test, AC coupling eliminates IEEE1149.1 as a test possibility.

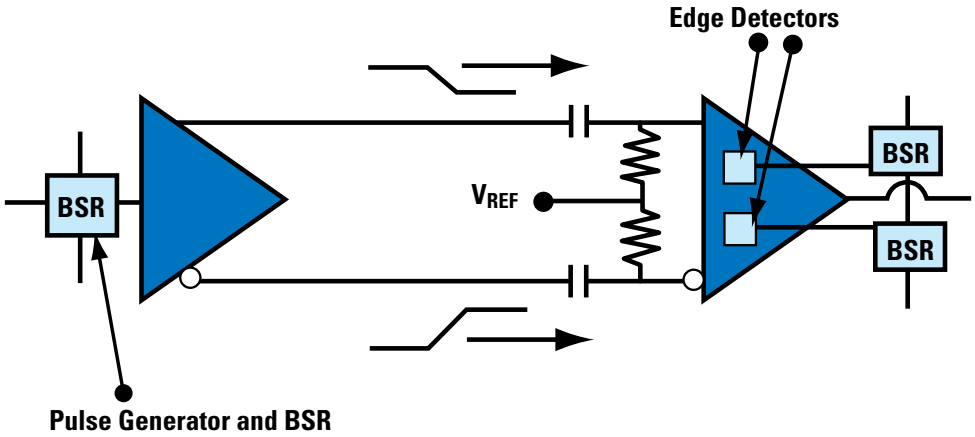


Figure 9-24. IEEE1149.6 Differential Test Standard

The solution (***Figure 9-24***) is the new standard, IEEE1149.6, which is fully compatible with the existing digital standard but specifically intended for high-speed differential. IEEE1149.6 assigns two boundary scan cells for each differential receiver, one cell for each line. In addition, rather than DC signals, IEEE1149.6 uses pulses to convey ones and zeros. The pulses travel directly through the AC termination.

This combination of dual cells and pulses enables IEEE1149.6 to provide accurate pass/fail information, but also diagnostics to the pin level. National Semiconductor currently supplies four devices compliant to the IEEE1149.6 standard.

Table 9-25. IEEE 1149.6-Compliant Devices

Device	Description
SCAN90004	Quad 1.5 Gbps LVDS buffer with pre-emphasis
SCAN90CP02	1.5 Gbps 2x2 crosspoint with pre-emphasis
SCAN15MB200	2.0 Gbps dual 2-to-1, 1-to-2 LVDS mux/buffer with pre-emphasis
SCAN25100	CPRI SerDes with integrated 30.72 MHz clocking and precision delay measurement

Functional Testing

The IEEE1149.6 standard does an excellent job detecting manufacturing defects such as opens and shorts, however it does not verify functionality, particularly at speed. Several of National's SerDes chipsets do include a test for functionality, including a short duration Bit-Error-Rate Test (BERT).

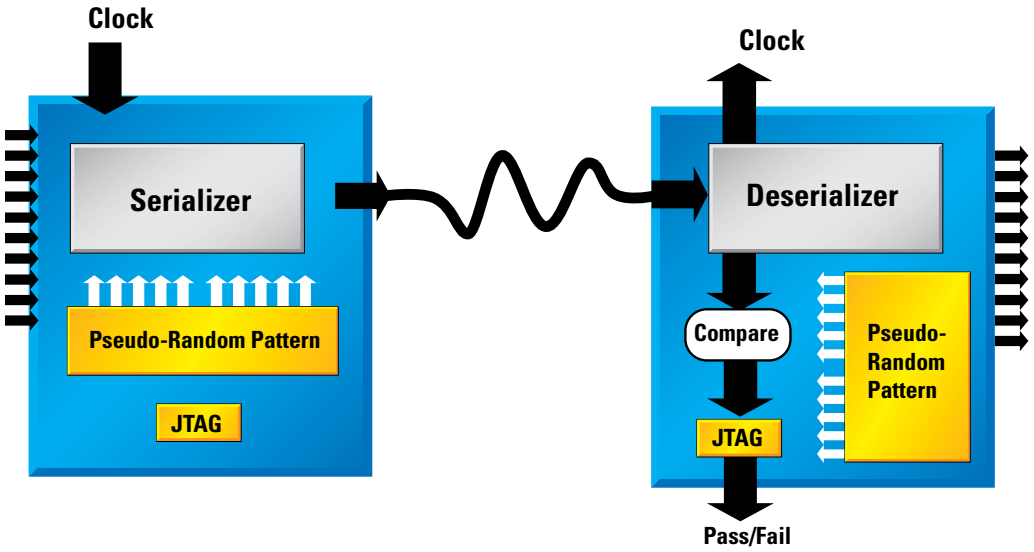


Figure 9-26. SerDes BERT Functionality

The BERT test is initiated on both devices with a JTAG BIST instruction. Pseudo-random patterns are generated simultaneously in both devices. In the serializer, the patterns are serialized, the clock embedded, and the bit stream sent across the differential link. In the deserializer, the received bits are deserialized, the clock recovered, and a comparison is made against every bit with a fail on zero bits. The test runs for 10^8 bits providing a mini at-speed BERT test. *Table 9-27* lists the SerDes chipsets offering this feature.

Table 9-27. IEEE1149.1-Compliant Devices with BIST

Device	Description
SCAN921023/921224	66 MHz 10-to-1/1-to-10 SerDes
SCAN921025/1226	80 MHz 10-to-1/1-to-10 SerDes
SCAN921260	66 MHz 6 channel 1-to-10 deserializer
SCAN926260	66 MHz 6 channel 1-to-10 deserializer
SCAN928028	66 MHz 8 channel 10-to-1 serializer

Loopback

Loopback is a diagnostic technique used to verify continuity between cards on a backplane. Devices with loopback support the option of routing the incoming signal back to the source. This feature is included in several of the mux/buffer functions.

9.9 DVI / HDMI

Digital Visual Interface (DVI) and High-Definition Multimedia Interface (HDMI) are two similar high-bandwidth standards for distributing uncompressed digital video. Both standards require three high-speed data channels and a clock channel to transmit 24-bit RGB color video. DVI and HDMI are very popular in PCs and consumer electronics.

High Data Rates and Longer Cost-Effective Cables

Higher-resolution displays continue to drive the need for greater bandwidth, and the latest HDMI 1.3 specification has increased the data rate from 1.65 Gbps to 3.4 Gbps per channel. Higher data rates result in increased attenuation and signal distortion due to the skin effect. In addition, users often desire longer cables than the standard 5m cable. Higher data rates and longer cables can be achieved using equalization.

Compensation for Skin Effects and Dielectric Losses

The DS16EV5110 is a video equalizer for DVI, HDMI, and CAT-5 cables, providing compensation for skin effect and dielectric losses. The DS16EV5110 equalizer dramatically extends the reach of DVI, HDMI, and CAT-5 cables at data rates from 250 Mbps to 2.25 Gbps.

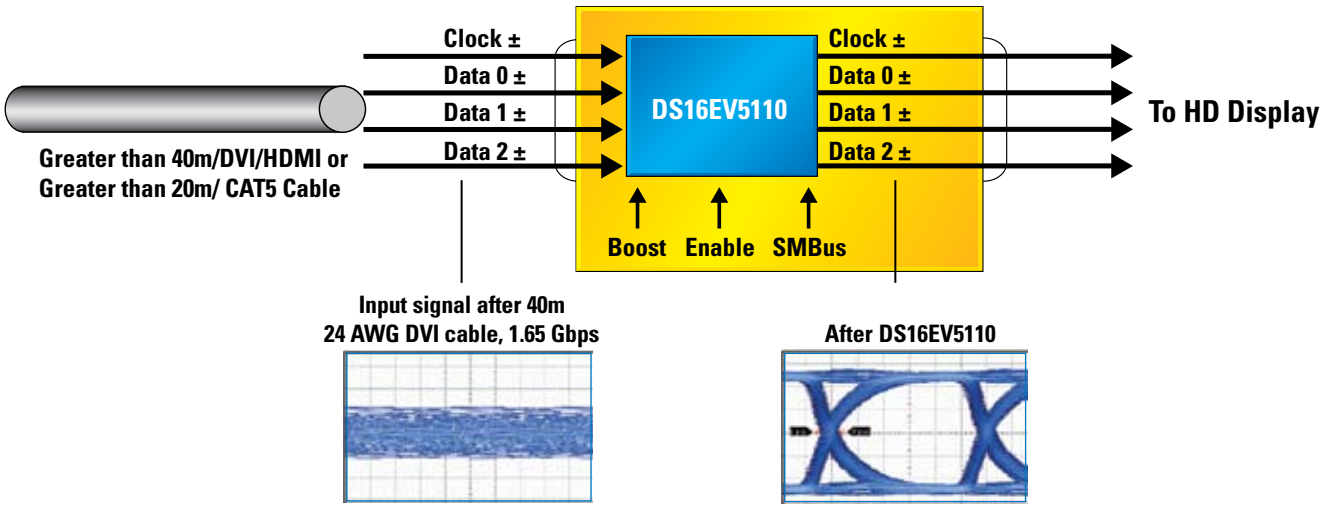


Figure 9-28. Using Signal-Conditioning ICs Extends Cable Performance

For more detailed information, please refer to **AN-1613 "Extending the Reach of HDMI, DVI, and CAT-5 Cables Using the DS16EV5110 Cable Equalizer."**

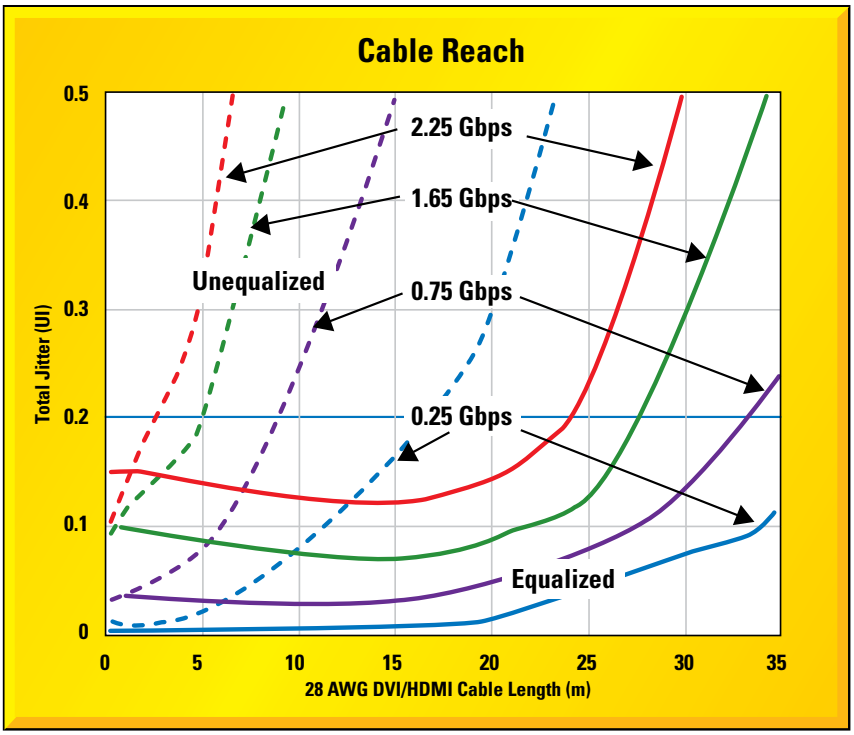


Figure 9-29. Different Cable Performance due to Correction-Enabled Signals

Appendix of Technical References

10.1 Websites and LVDS Applications

National's in-depth application site on signal conditioning provides the design community with the latest information on our expanding LVDS family.

LVDS Home Page:
national.com/LVDS

Interface Home Page:
national.com/appinfo/interface

Signal Conditioning Selection Guides:
national.com/whatsnew/files/national_analog_product_selguide.pdf

Cabling and High-Speed Effects:
www.informit.com/articles/article.aspx?p=101149&seqNum=8&rl=1

Clocking/Timing Solutions Website:
national.com/timing

Introduction to LVDS:
national.com/AU/design/1,4678,13_0_,00.html

Boosting FPGA and CPLD Performance for Off-board Data Transmission:
national.com/AU/design/0,4706,0_61_,00.html

Analog by Design:
national.com/nationaltv

WEBENCH® Online Tools:
national.com/webench

10.2 Analog Edge® and Signal Path Designer® Articles

May 2006
"Overcoming Impedance Discontinuities in High-Speed Signal Paths by Using LVDS" by Brian Stearns

July 2007
"Extending the Signal Path over Data Transmission Lines" by Lee Sledjeski

10.3 Outside Publications

EE Times Europe — April 2007
"3-Gbps SerDes Targets Professional and Broadcast Video Applications"

Electronic Products — October 2002
"LVDS Product Selection"

Systems Designline — May 2006
"Reduce Simultaneous Switching Output Noise with a Standalone SerDes Network"

Electronic Design Europe — Feb 2006
"LVDS Role in LCDs for Cars"

EPN Supplements — September 2007
"High-Speed Data Transfer for Infotainment"

10.4 Application Note References

App Note	Title
AN-759	Comparing EIA-485 and EIA-422-A Line Drivers and Receivers in Multipoint Applications
AN-903	A Comparison of Differential Termination Techniques
AN-971	Introduction to LVDS
AN-977	Signal Quality Eye Patterns
AN-1032	Introduction to FPD-Link
AN-1057	Ten Ways to Bulletproof RS-485 Interfaces
AN-1060	LVDS - Megabits @ Milliwatts (EDN Reprint)
AN-1084	Channel Link Parallel Application of Link Chips
AN-1085	PCB and Interconnect Design Guidelines
AN-1115	Bus LVDS and DS92LV010A XCVR
AN-1123	Sorting Out Backplane Driver Alphabet Soup
AN-1173	High-Speed Bus LVDS Clock Distribution Using the DS92CK16 Clock Distribution Device
AN-1194	Failsafe Biasing of LVDS Interfaces
AN-1217	How to Validate Bus LVDS SerDes Signal Integrity Using an Eye Mask
AN-1238	Wide Bus Applications Using Parallel Bus LVDS SerDes Devices
AN-1313	SCAN90CP02 Design for Test Features
AN-1327	Simplified Programming of Altera FPGAs using a SCANSTA111/112 Scan Chain Mux
AN-1340	Simplified Programming of Xilinx Devices Using a SCANSTA111/112 JTAG Chain Mux
AN-1376	External Serial Interface Reduces Simultaneous Switching Output Noise in FPGAs
AN-1380	Design Challenges in 5 Gbps Copper Backplanes
AN-1389	Setting Pre-Emphasis Level for DS40MB200 Dual 4 Gbps Mux/Buffer
AN-1398	Printed Circuit Board Design Techniques for DS40MB200
AN-1399	Enabling Redundancy in Multi-Gigabit Links with DS40MB200 Mux/Buffer
AN-1473	PCI Express Using National Semiconductor DS25MB100, DS25MB200, and DS25BR400
AN-1503	Designing an ATCA Compliant M-LVDS Clock Distribution Network
AN-1511	Cable Discharge Event
AN-1541	Driving Signals Over XAUI Backplanes Using DS42MB100, DS40MB200, or DS42BR400
AN-1613	Extending the Reach of HDMI, DVI, and CAT-5 Cables Using the DS16EV5110 Cable Equalizer
AN-1734	Using the LMK03000C to Clean Recovered Clocks

10.5 Index

10.6 Acronyms

AMC	*Advance Mezzanine Card*
AN	*Application Note*
ANSI	*American National Standards Institute*
ASIC	*Application-Specific Integrated Circuit*
ATCA	*Advanced Telecommunications and Computing Architecture*
B/P	*Backplane*
BER	*Bit Error Rate*
BERT	*Bit-Error-Rate Test*
B-LVDS	*Bus LVDS*
BTL	*Backplane Transceiver Logic*
CAT-3	*CAT-3 (Cable classification)*
CAT-5	*CAT-5 (Cable classification)*
CISPR	*International Special Committee on Radio Interference (Comité International Spécial des Perturbations Radioélectriques)*
D	*Driver*
DCD	*Duty Cycle Distortion*
DCR	*DC Resistance*
DE	*De-Emphasis*
DJ	*Deterministic Jitter*
DSP	*Digital Signal Processing*
DUT	*Device Under Test*
DVI	*Digital Visual Interface*
ECL	*Emitter-Coupled Logic*
EIA	*Electronic Industries Association*
EMC	*Electromagnetic Compatibility*
EMI	*Electromagnetic Interference*
EN	*Enable*
EQ	*Equalization*
ESD	*Electrostatic Discharge*
EVK	*Evaluation Kit*
FCC	*Federal Communications Commission*
FEC	*Far-End Crosstalk*
FPD	*Flat Panel Display*
FPD-LINK	*Flat Panel Display Link*
FPGA	*Field Programmable Gate Array*
Gbps	*Gigabits per second*
GTL	*Gunning Transceiver Logic*
HBM	*Human Body Model*
Hi-Z	*High Impedance*
I/O	*Input/Output*
IBIS	*Input/output Buffer Information Specification*
IC	*Integrated Circuit*
IDC	*Insulation Displacement Connector*
IEEE	*Institute of Electrical and Electronics Engineers*
ISI	*Inter-Symbol Interference*
Kbps	*Kilobits per second*
LAN	*Local Area Network*
LDI	*LVDS Display Interface*
LVDS	*Low-Voltage Differential Signaling*
LVTTL	*Low-Voltage Transister-to-Transister Logic*
Mbps	*Megabits per second*
MCH	*MicroTCA Carrier Hub*
MDR	*Mini Delta Ribbon*
MLC	*Multi-Layer Ceramic*
MLVDS	*Multipoint Low-Voltage Differential Signaling*
NEXT	*Near-End Crosstalk*
NRZ	*Non-Return to Zero*
PCB	*Printed Circuit Board*
PDF	*Probability Duty Function*
PE	*Pre-Emphasis*
PECL	*Positive-Emitter-Coupled Logic*
PHY	*Physical Layer Device*
PICMG	*PCI Industrial Computer Manufacturers Group*
PJ	*Periodic Jitter*
PLL	*Phase-Locked Loop*
PRBS	*Pseudo-Random Binary or Bit Sequence*
RJ	*Random Jitter*
RFI	*Radio Frequency Interference*
RS	*Recommended Standard*
RT	*Termination Resistor*
Rx	*Receiver*
SCI	*Scalable Coherent Interface*
SCSI	*Small Computer Systems Interface*
SDI	*Serial Digital Interface*
SerDes	*Serializer/Deserializer*
SMPTE	*Society of Motion Picture and Television Engineers*
SMT	*Surface Mount Technology*
SNR	*Signal-to-Noise Ratio*
SSC	*Spread Spectrum Clocking*
SSO	*Simultaneous Switching Output*
SUT	*System Under Test*
TDR	*Time Domain Reflectometry*
TEM	*Transverse Electro-Magnetic*
TFT	*Thin Film Transistor*
TIA	*Telecommunications Industry Association*
TIE	*Time Interval Equivalent*
TP	*Test Point*
TTL	*Transistor-to-Transistor Logic*
TWP	*Twisted Wire Pair*
Tx	*Transmitter*
UI	*Unit Intervals*
UTP	*Unshielded Twisted Pair*
VCM	*Common-mode Voltage*

10.7 Glossary of Common Datasheet Parameters

V_{IH} – High-level input voltage: TTL-input specification used for data and control pins

V_{IL} – Low-level input voltage: TTL-input specification used for data and control pins

V_{CL} – Input-clamp voltage: a specification for the clamp voltage given a current

I_{IN} – Input current: the amount of current drawn by each TTL input

V_{OH} – High-level output voltage: TTL-output specification used for data and control pins

V_{OL} – Low-level output voltage: TTL-output specification used for data and control pins

I_{OS} – Output short-circuit current: amount of current drawn when outputs are shorted to GND

I_{OZ} – TRI-STATE® output current: amount of current drawn when the outputs are in TRI-STATE; the outputs are either disabled by a control pin or the device is put in power-down mode

V_{TH} – Differential-threshold high voltage: any input signal above this threshold will have a logic HIGH on the output

V_{TL} – Differential-threshold low voltage: any signal below this threshold will have a logic low on the output

V_{OD} – Output differential voltage: the amplitude result of (DO+) – (DO-)

ΔV_{OD} – Output differential voltage unbalanced: the difference in amplitude between the positive and negative LVDS outputs

V_{OS} – Offset voltage: the common-mode voltage of the LVDS output

ΔV_{OS} – Offset voltage unbalanced: the difference in common-mode voltage between the positive and negative LVDS outputs

I_{OX} – Power-off output current: the amount of current drawn when V_{DD} = 0 and the outputs are either at 0V or another positive voltage

I_{CCD} – Serializer total supply current (includes load current): the total amount of current drawn by a serializer

I_{CCR} – Receiver total supply current (includes load current): the total amount of current drawn by a deserializer

I_{CCT} – Transceiver total supply current (includes load current): the amount of current drawn by both a serializer and a deserializer

I_{CCX} – Transceiver total supply current when powered down: the total current drawn when a transceiver is put into power-down mode

I_{CCXD} – Serializer total supply current when powered down: the total current drawn by a driver in power-down mode

I_{CCXR} – Receiver total supply current when powered down: the total current drawn by a receiver in power-down mode

t_{TCP} – Transmit clock period: a TTL-clock input specification for the serializer

t_{TCIH} – Transmit clock high time: specification for the portion of the clock period that must be high

t_{TCIL} – Transmit clock low time: specification for the portion of the clock period that must be low

t_{CLKT} – TCLK input transition time: rise/fall time requirement for the input clock measured at 10% and 90%

t_{JIT} – TCLK input jitter: the maximum amount of jitter that the input clock will tolerate

t_{LH} – Bus LVDS low-to-high transition time (measured from 20% to 80%): rise-time specification for the LVDS signal

t_{HL} – Bus LVDS high-to-low transition time (measured from 20% to 80%): fall-time specification for the LVDS signal

t_{DIS} – D_{IN} (0-x) Setup to TCLK: setup-time requirement between data and clock for a serializer

t_{DIH} – D_{IN} (0-x) Hold from TCLK: hold-time requirement between data and clock for a serializer

t_{HZD} – D_0 ± HIGH to TRI-STATE delay: the amount of time required for a serializer's LVDS outputs to change from HIGH to TRI-STATE

t_{LZD} – D_0 ± LOW to TRI-STATE delay: the amount of time required for a serializer's LVDS outputs to change from LOW to TRI-STATE

t_{ZHD} – D_0 ± TRI-STATE to HIGH delay: the amount of time required for a serializer's LVDS outputs to change from TRI-STATE to a HIGH state

t_{ZLD} – D_0 ± TRI-STATE to LOW delay: the amount of time required for a serializer's LVDS outputs to change from TRI-STATE to a LOW state

t_{SPW} – SYNC pulse width: the number of clock cycles the SYNC pin must be asserted HIGH before the device enters SYNC mode and SYNC patterns appear at the LVDS outputs

t_{PLD} – Serializer PLL lock time: the number of clock cycles the PLL requires to lock to the input clock before data can appear at the LVDS outputs

t_{SD} – Serializer delay: the amount of time required for data to travel through a serializer

t_{RJIT} – Random jitter: the amount of Gaussian jitter produced

t_{DJIT} – Deterministic jitter: the amount of non-Gaussian jitter produced

t_{RFCP} – REFCLK period: period requirement for the REFCLK input pin

t_{RFDC} – REFCLK duty cycle: duty cycle requirement for the REFCLK input pin

$t_{RFCP/TCP}$ – Ratio of REFCLK to TCLK: indicates the allowable difference between the TCLK and REFCLK periods

t_{RFFT} – REFCLK transition time: the rise-and fall-time requirement for the REFCLK pin

t_{RCP} – Recovered Clock (RCLK) period: the period of the clock recovered from the LVDS inputs

t_{RDC} – RCLK duty cycle: the duty cycle of the clock recovered from the LVDS inputs

t_{CLH} – CMOS/TTL low-to-high transition time: the rise time specification for TTL outputs

t_{CHL} – CMOS/TTL high-to-low transition time: the fall time specification for TTL outputs

t_{ROS} – R_{OUT} (0-x) setup data to RCLK: the amount of setup time provided between the RCLK edge (usually rising) and output data

t_{ROH} – R_{OUT} (0-x) hold data to RCLK: the amount of hold time provided between the RCLK edge (usually rising) and output data

t_{HZR} – HIGH to TRI-STATE delay: the amount of time for a deserializer's TTL outputs to change from HIGH to TRI-STATE

t_{LZR} – LOW to TRI-STATE delay: the amount of time for a deserializer's TTL outputs to change from LOW to TRI-STATE

t_{ZHR} – TRI-STATE to HIGH delay: the amount of time for a deserializer's TTL outputs to change from TRI-STATE to HIGH

t_{ZLR} – TRI-STATE to LOW delay: the amount of time for a deserializer's TTL outputs to change from TRI-STATE to LOW

t_{DD} – Deserializer delay: the amount of time for data to travel through a deserializer

t_{DSR1} – Deserializer PLL lock time from PWRDWN: the amount of time required for the deserializer's PLL to lock after exiting power-down mode

t_{DSR2} – Deserializer PLL lock time from SYNCPAT: the amount of time before the deserializer's PLL locks to the incoming SYNC pattern

t_{RNMI-R} – Ideal deserializer noise margin – Right: the amount of margin available for noise as measured from the ideal bit-stop position to the right edge of the sampling window

t_{RNMI-L} – Ideal deserializer noise margin – Left: the amount of margin available for noise as measured from the ideal bit-start position to the left edge of the sampling window

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national.com/appinfo/LVDS

Online Design Seminars

View over 50 design seminars by industry experts. Log onto **national.com/onlineseminar/#interface**

Technical References

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