

## 2:16 Low Additive Jitter LVDS Buffer

Check for Samples: [CDCLVD1216](#)

### FEATURES

- 2:16 Differential Buffer
- Low Additive Jitter: <300 fs RMS in 10 kHz to 20 MHz
- Low Output Skew of 55 ps (Max)
- Universal Inputs Accept LVDS, LVPECL, LVCMOS
- Selectable Clock Inputs Through Control Pin
- 16 LVDS Outputs, ANSI EIA/TIA-644A Standard Compatible
- Clock Frequency up to 800 MHz
- 2.375–2.625V Device Power Supply
- LVDS Reference Voltage,  $V_{AC\_REF}$ , Available for Capacitive Coupled Inputs
- Industrial Temperature Range  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Packaged in 7mm x 7mm 48-Pin QFN (RGZ)
- ESD Protection Exceeds 3 kV HBM, 1 kV CDM

### APPLICATIONS

- Telecommunications/Networking
- Medical Imaging
- Test and Measurement Equipment
- Wireless Communications
- General Purpose Clocking

### DESCRIPTION

The CDCLVD1216 clock buffer distributes one of two selectable clock inputs (IN0, IN1) to 16 pairs of differential LVDS clock outputs (OUT0, OUT15) with minimum skew for clock distribution. The CDCLVD1216 can accept two clock sources into an input multiplexer. The inputs can either be LVDS, LVPECL, or LVCMOS.

The CDCLVD1216 is specifically designed for driving  $50\ \Omega$  transmission lines. If driving the inputs in single ended mode, the appropriate bias voltage ( $V_{AC\_REF}$ ) should be applied to the unused negative input pin.

The IN\_SEL pin selects the input which is routed to the outputs. If this pin is left open it disables the outputs (static). The part supports a fail safe function. It incorporates an input hysteresis, which prevents random oscillation of the outputs in absence of an input signal.

The device operates in 2.5 V supply environment and is characterized from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  (ambient temperature). The CDCLVD1216 is packaged in small 48-pin, 7mm x 7mm QFN package.

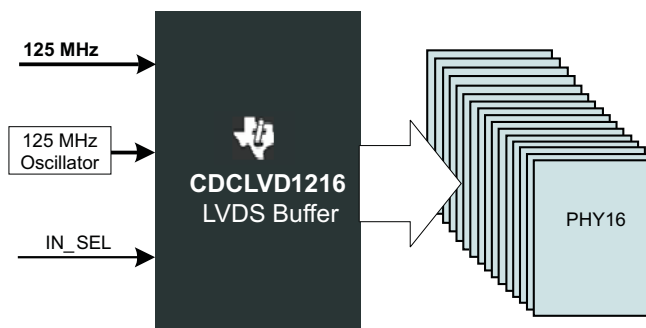


Figure 1. Application Example



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

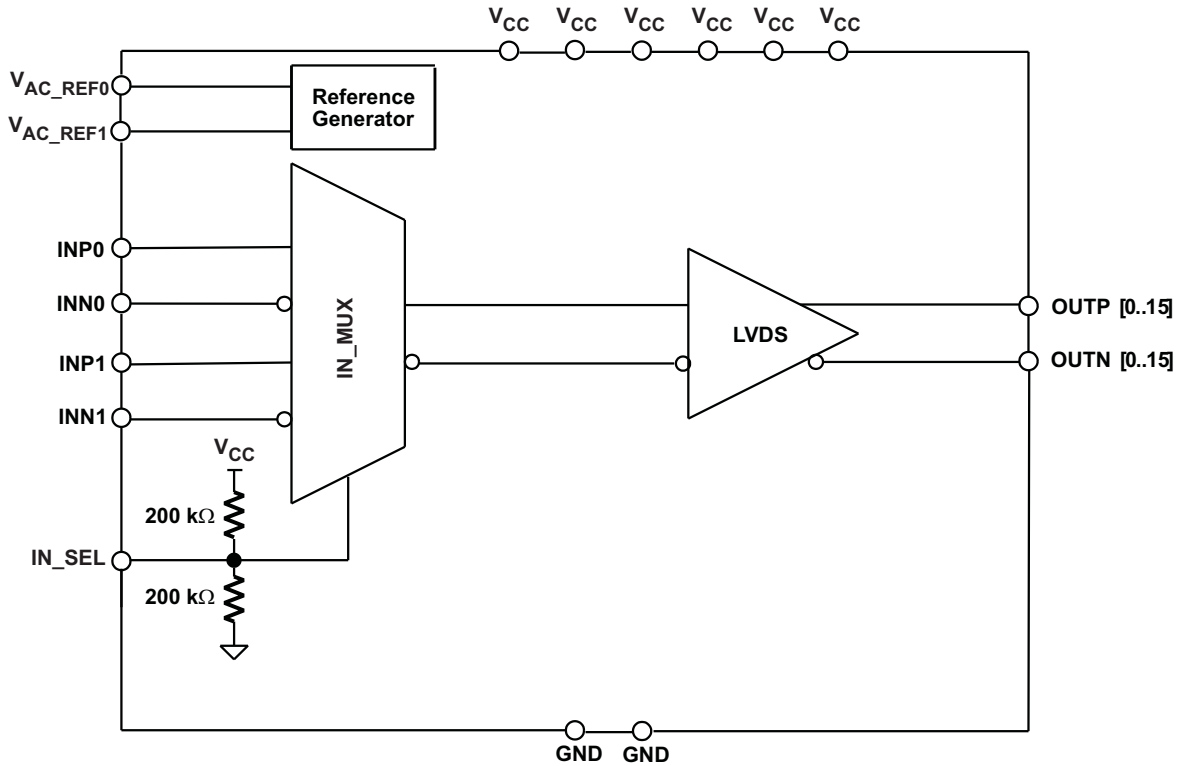
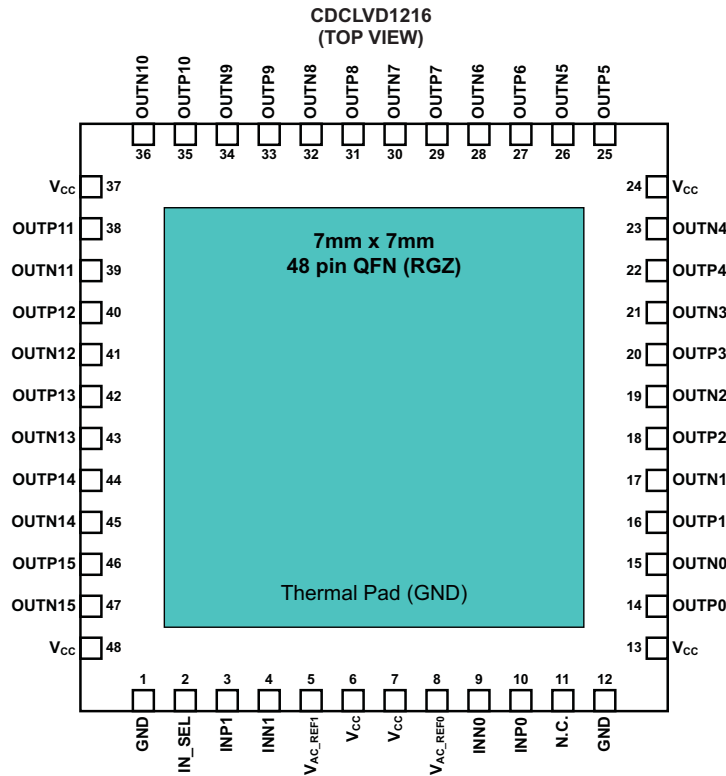


Figure 2. CDCLVD1216 Block Diagram



**PIN FUNCTIONS**

PIN		TYPE	DESCRIPTION
NAME	NO.		
V <sub>CC</sub>	6, 7, 13, 24, 37, 48	Power	2.5V supplies for the device
GND	1, 12	Ground	Device ground
INP0, INN0	10, 9	Input	Differential input pair or single ended input
INP1, INN1	3, 4	Input	Differential redundant input pair or single ended input
OUTP0, OUTN0	14, 15	Output	Differential LVDS output pair no. 0
OUTP1, OUTN1	16, 17	Output	Differential LVDS output pair no. 1
OUTP2, OUTN2	18, 19	Output	Differential LVDS output pair no. 2
OUTP3, OUTN3	20, 21	Output	Differential LVDS output pair no. 3
OUTP4, OUTN4	22, 23	Output	Differential LVDS output pair no. 4
OUTP5, OUTN5	25, 26	Output	Differential LVDS output pair no. 5
OUTP6, OUTN6	27, 28	Output	Differential LVDS output pair no. 6
OUTP7, OUTN7	29, 30	Output	Differential LVDS output pair no. 7
OUTP8, OUTN8	31, 32	Output	Differential LVDS output pair no. 8
OUTP9, OUTN9	33, 34	Output	Differential LVDS output pair no. 9
OUTP10, OUTN10	35, 36	Output	Differential LVDS output pair no. 10
OUTP11, OUTN11	38, 39	Output	Differential LVDS output pair no. 11
OUTP12, OUTN12	40, 41	Output	Differential LVDS output pair no. 12
OUTP13, OUTN13	42, 43	Output	Differential LVDS output pair no. 13
OUTP14, OUTN14	44, 45	Output	Differential LVDS output pair no. 14
OUTP15, OUTN15	46, 47	Output	Differential LVDS output pair no. 15
V <sub>AC_REF0</sub>	8	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1µF to GND on this pin.
V <sub>AC_REF1</sub>	5	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1µF to GND on this pin.
N.C.	11		No connect
IN_SEL	2	Input with an internal 200kΩ pull-up and pull-down	Input selection – selects input port; (See <a href="#">Table 1</a> )
Thermal Pad		Ground	Device ground. Thermal Pad must be soldered to ground. See thermal management recommendations.

**Table 1. Input Selection Table**

IN_SEL	ACTIVE CLOCK INPUT
0	INP0, INN0
1	INP1, INN1
Open	None <sup>(1)</sup>

(1) The input buffers are disabled and the outputs are static.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

	VALUE	UNIT
Supply voltage range, $V_{CC}$	-0.3 to 2.8	V
Input voltage range, $V_I$	-0.2 to ( $V_{CC} + 0.2$ )	V
Output voltage range, $V_O$	-0.2 to ( $V_{CC} + 0.2$ )	V
Driver short circuit current, $I_{OSD}$	See Note <sup>(2)</sup>	
Electrostatic discharge (Human Body Model, 1.5 k $\Omega$ , 100 pF)	>3000	V

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) The outputs can handle permanent short.

## RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
Device supply voltage, $V_{CC}$	2.375	2.5	2.625	V
Ambient temperature, $T_A$	-40		85	°C

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		CDCLVD1216	UNITS
		RGZ(48 PINS)	
$\theta_{JA}$	Junction-to-ambient thermal resistance	30.6	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	28.5	
$\theta_{JB}$	Junction-to-board thermal resistance	10.5	
$\Psi_{JT}$	Junction-to-top characterization parameter	0.4	
$\Psi_{JB}$	Junction-to-board characterization parameter	10.2	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	3.1	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## ELECTRICAL CHARACTERISTICS

At  $V_{CC} = 2.375V$  to  $2.625V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>IN_SEL CONTROL INPUT CHARACTERISTICS</b>						
$V_{dl3}$	3 State	Open		$0.5 \times V_{CC}$		V
$V_{dlH}$	Input high voltage		$0.7 \times V_{CC}$			V
$V_{dlL}$	Input low voltage				$0.2 \times V_{CC}$	V
$I_{dlH}$	Input high current	$V_{CC} = 2.625 V$ , $V_{IH} = 2.625 V$			30	$\mu A$
$I_{dlL}$	Input low current	$V_{CC} = 2.625 V$ , $V_{IL} = 0 V$			-30	$\mu A$
$R_{pull(IN\_SEL)}$	Input pull-up/ pull-down resistor			200		k $\Omega$
<b>2.5V LVCMOS (see Figure 7) INPUT CHARACTERISTICS</b>						
$f_{IN}$	Input frequency				200	MHz
$V_{th}$	Input threshold voltage	External threshold voltage applied to complementary input	1.1		1.5	V
$V_{IH}$	Input high voltage		$V_{th} + 0.1$		$V_{CC}$	V
$V_{IL}$	Input low voltage		0		$V_{th} - 0.1$	V
$I_{IH}$	Input high current	$V_{CC} = 2.625 V$ , $V_{IH} = 2.625 V$			10	$\mu A$
$I_{IL}$	Input low current	$V_{CC} = 2.625 V$ , $V_{IL} = 0 V$			-10	$\mu A$
$\Delta V/\Delta T$	Input edge rate	20%–80%	1.5			V/ns
$C_{IN}$	Input capacitance			2.5		pF

**ELECTRICAL CHARACTERISTICS (continued)**

 At  $V_{CC} = 2.375V$  to  $2.625V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DIFFERENTIAL INPUT CHARACTERISTICS</b>						
$f_{IN}$	Input frequency	Clock input			800	MHz
$V_{IN, DIFF}$	Differential input voltage peak-to-peak	$V_{ICM} = 1.25 V$	0.3		1.6	$V_{PP}$
$V_{ICM}$	Input common mode voltage range	$V_{IN, DIFF, PP} > 0.4 V$	1.0		$V_{CC} - 0.3$	V
$I_{IH}$	Input high current	$V_{CC} = 2.625 V$ , $V_{IH} = 2.625 V$			10	$\mu A$
$I_{IL}$	Input low current	$V_{CC} = 2.625$ , $V_{IL} = 0 V$			-10	$\mu A$
$\Delta V/\Delta T$	Input edge rate	20%–80%	0.75			V/ns
$C_{IN}$	Input capacitance			2.5		pF
<b>LVDS OUTPUT CHARACTERISTICS</b>						
$ V_{OD} $	Differential output voltage magnitude		250		450	mV
$\Delta V_{OD}$	Change in differential output voltage magnitude	$V_{IN, DIFF, PP} = 0.3V$ , $R_L = 100 \Omega$	-15		15	mV
$V_{OC(SS)}$	Steady-state common mode output voltage		1.1		1.375	V
$\Delta V_{OC(SS)}$	Steady-state common mode output voltage	$V_{IN, DIFF, PP} = 0.6V$ , $R_L = 100 \Omega$	-15		15	mV
$V_{ring}$	Output overshoot and undershoot	Percentage of output amplitude $V_{OD}$			10%	
$V_{OS}$	Output ac common mode	$V_{IN, DIFF, PP} = 0.6V$ , $R_L = 100 \Omega$		40	70	$mV_{PP}$
$I_{OS}$	Short-circuit output current	$V_{OD} = 0 V$			$\pm 24$	mA
$t_{PD}$	Propagation delay	$V_{IN, DIFF, PP} = 0.3 V$		1.5	2.5	ns
$t_{SK, PP}$	Part-to-part skew				600	ps
$t_{SK, O}$	Output skew				55	ps
$t_{SK, P}$	Pulse skew (with 50% duty cycle input)	Crossing-point-to-crossing-point distortion	-50		50	ps
$t_{RJIT}$	Random additive jitter (with 50% duty cycle input)	Edge speed 0.75 V/ns, 10 kHz – 20 MHz			0.3	ps, RMS
$t_R/t_F$	Output rise/fall time	20% to 80%, 100 $\Omega$ , 5 pF	50		300	ps
$I_{CCSTAT}$	Static supply current	Outputs unterminated, $f = 0$ Hz		17	28	mA
$I_{CC100}$	Supply current	All outputs, $R_L = 100 \Omega$ , $f = 100$ MHz		107	140	mA
$I_{CC800}$	Supply current	All outputs, $R_L = 100 \Omega$ , $f = 800$ MHz		147	180	mA
<b><math>V_{AC\_REF}</math> CHARACTERISTICS</b>						
$V_{AC\_REF}$	Reference output voltage	$V_{CC} = 2.5 V$ $I_{load} = 100 \mu A$	1.1	1.25	1.35	V

### Typical Additive Phase Noise Characteristics for 100 MHz Clock

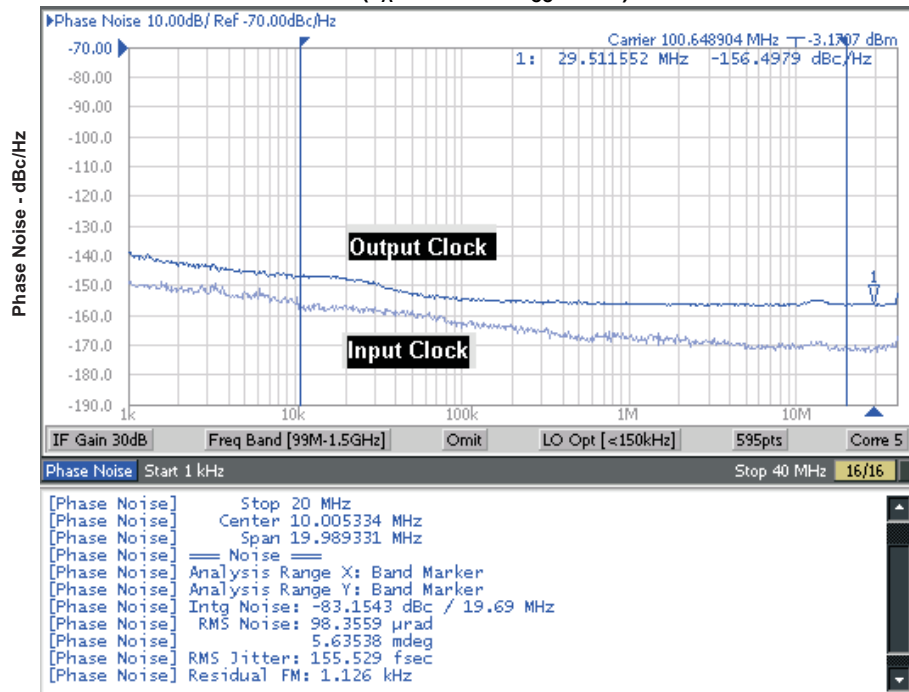
PARAMETER		MIN	TYP	MAX	UNIT
phn <sub>100</sub>	Phase noise at 100 Hz offset		-132.9		dBc/Hz
phn <sub>1k</sub>	Phase noise at 1 kHz offset		-138.8		dBc/Hz
phn <sub>10k</sub>	Phase noise at 10 kHz offset		-147.4		dBc/Hz
phn <sub>100k</sub>	Phase noise at 100 kHz offset		-153.6		dBc/Hz
phn <sub>1M</sub>	Phase noise at 1 MHz offset		-155.2		dBc/Hz
phn <sub>10M</sub>	Phase noise at 10 MHz offset		-156.2		dBc/Hz
phn <sub>20M</sub>	Phase noise at 20 MHz offset		-156.6		dBc/Hz
t <sub>RJIT</sub>	Random additive jitter from 10 kHz to 20 MHz		171		fs, RMS

### Typical Additive Phase Noise Characteristics for 737.27 MHz Clock

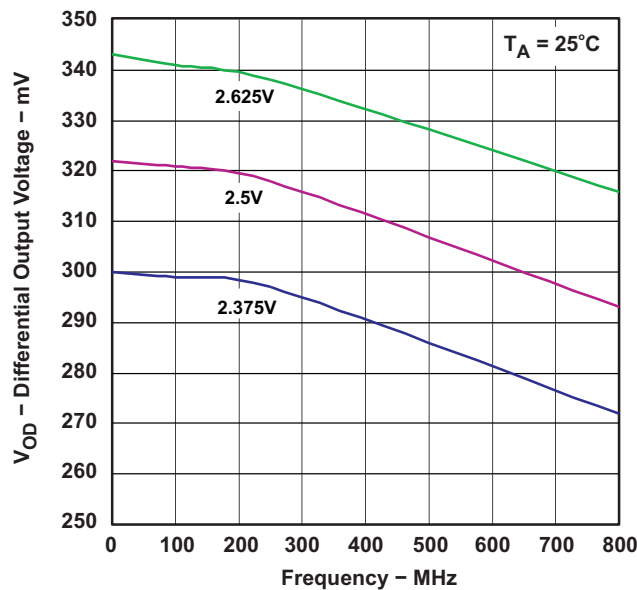
PARAMETER		MIN	TYP	MAX	UNIT
phn <sub>100</sub>	Phase noise at 100 Hz offset		-80.2		dBc/Hz
phn <sub>1k</sub>	Phase noise at 1 kHz offset		-114.3		dBc/Hz
phn <sub>10k</sub>	Phase noise at 10 kHz offset		-138		dBc/Hz
phn <sub>100k</sub>	Phase noise at 100 kHz offset		-143.9		dBc/Hz
phn <sub>1M</sub>	Phase noise at 1 MHz offset		-145.2		dBc/Hz
phn <sub>10M</sub>	Phase noise at 10 MHz offset		-146.5		dBc/Hz
phn <sub>20M</sub>	Phase noise at 20 MHz offset		-146.6		dBc/Hz
t <sub>RJIT</sub>	Random additive jitter from 10 kHz to 20 MHz		65		fs, RMS

**TYPICAL CHARACTERISTICS**

**INPUT- AND OUTPUT-CLOCK PHASE NOISES  
VS  
FREQUENCY FROM the CARRIER  
( $T_A = 25^\circ\text{C}$  and  $V_{CC} = 2.5\text{V}$ )**



Input clock RMS jitter is 32 fs from 10 kHz to 20 MHz and additive RMS jitter is 152 fs  
**Figure 3. 100 MHz Input and Output Phase Noise Plot**



**Figure 4. Differential Output Voltage vs Frequency**

TYPICAL CHARACTERISTICS (continued)

TEST CONFIGURATIONS

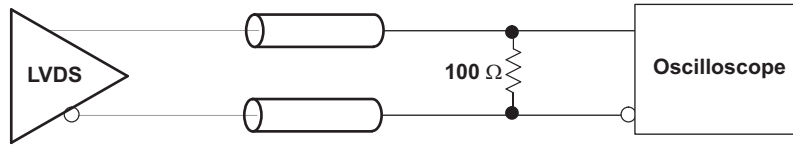


Figure 5. LVDS Output DC Configuration During Device Test

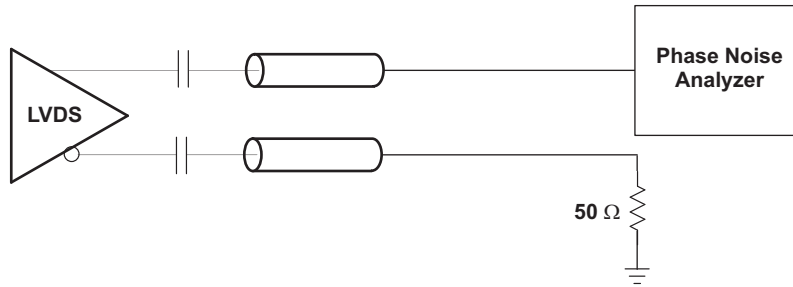


Figure 6. LVDS Output AC Configuration During Device Test

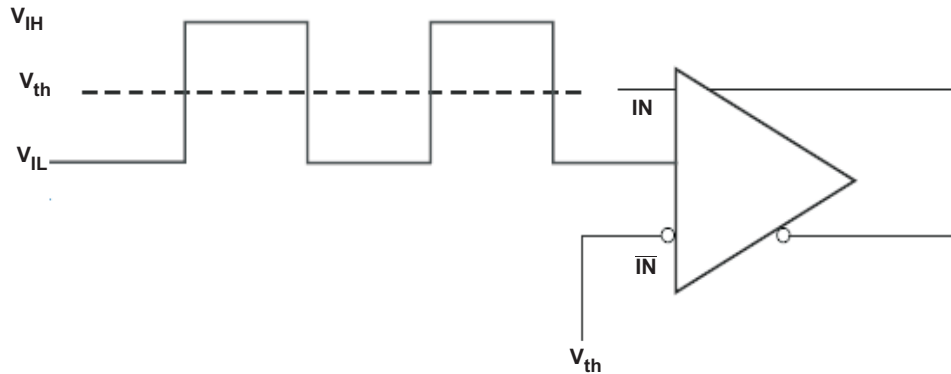


Figure 7. DC Coupled LVCMOS Input During Device Test

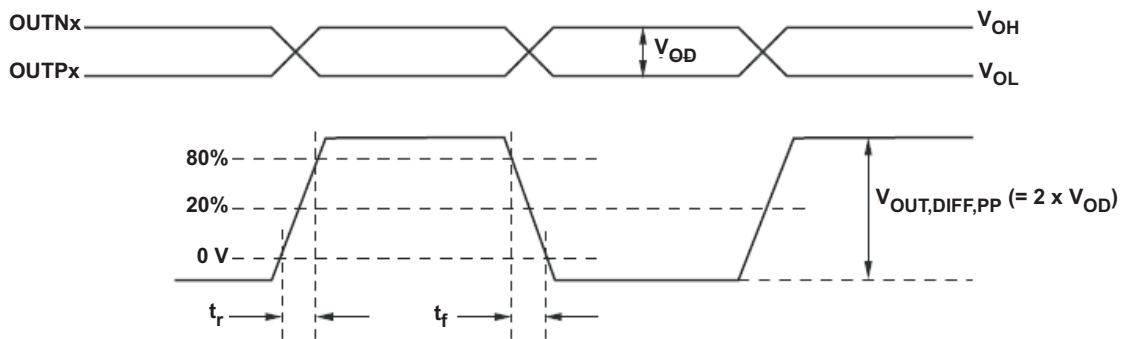
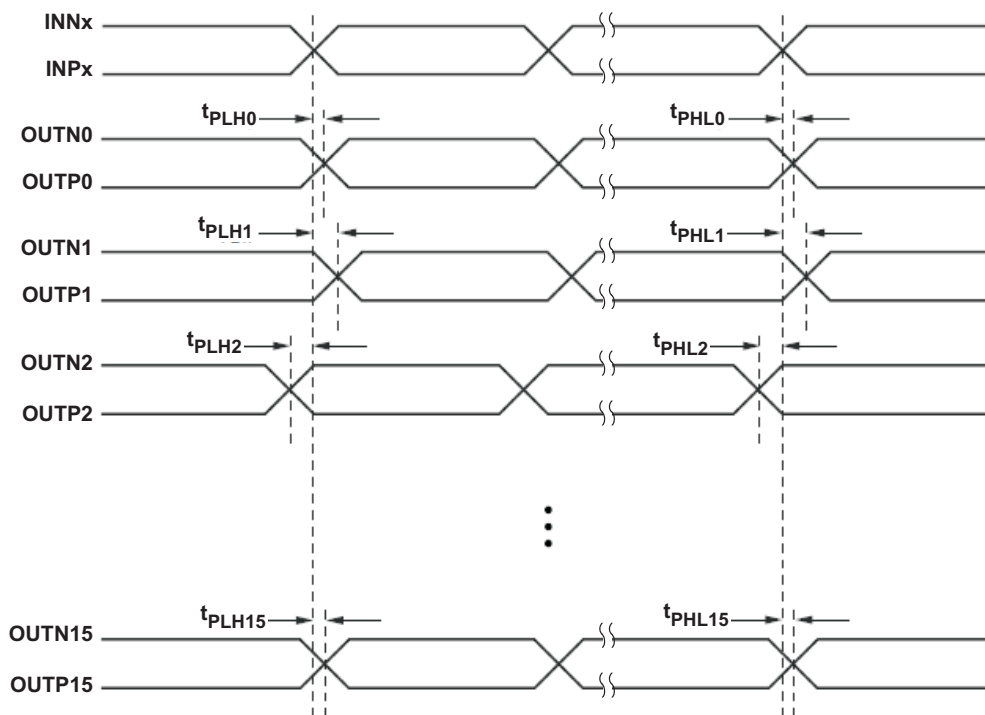


Figure 8. Output Voltage and Rise/Fall Time

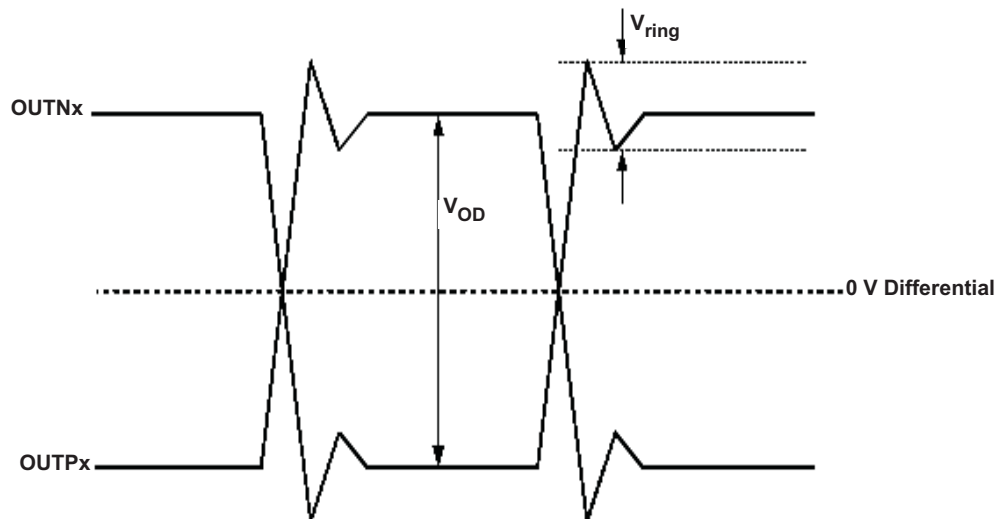


**TYPICAL CHARACTERISTICS (continued)**



- A. Output skew is calculated as the greater of the following: As of the difference between the fastest and the slowest  $t_{PLHn}$  or the difference between the fastest and the slowest  $t_{PHLn}$  ( $n = 0, 1, 2, \dots, 15$ )
- B. Part to part skew is calculated as the greater of the following: As the difference between the fastest and the slowest  $t_{PLHn}$  or the difference between the fastest and the slowest  $t_{PHLn}$  across multiple devices ( $n = 0, 1, 2, \dots, 15$ )

**Figure 9. Output Skew and Part-to-Part Skew**



**Figure 10. Output Overshoot and Undershoot**

### TYPICAL CHARACTERISTICS (continued)

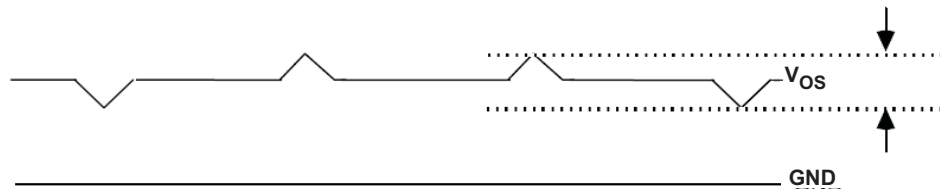


Figure 11. Output AC Common Mode

## APPLICATION INFORMATION

### THERMAL MANAGEMENT

For reliability and performance reasons, the die temperature should be limited to a maximum of +125°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. Check the mechanical data at the end of the data sheet for land and via pattern examples.

### POWER SUPPLY FILTERING

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is critical to the application.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed close to the power-supply pins and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1  $\mu\text{F}$ ) bypass capacitors as there are supply pins in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with low dc resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

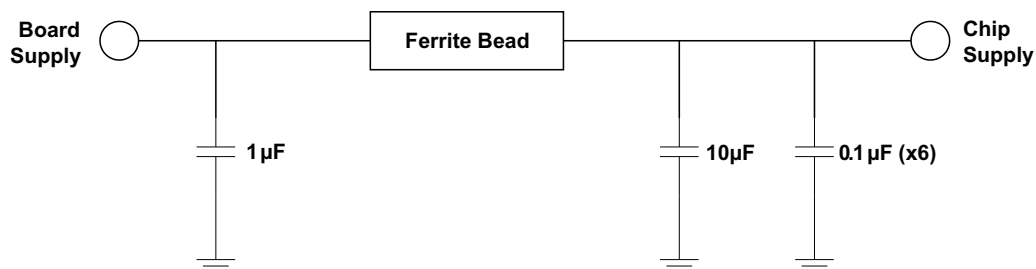


Figure 12. Power Supply Filtering

## LVDS OUTPUT TERMINATION

The proper LVDS termination for signal integrity over two 50  $\Omega$  lines is 100  $\Omega$  between the outputs on the receiver end. Either dc-coupled termination or ac-coupled termination can be used for LVDS outputs. It is recommended to place termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common mode voltage of the CDCLVD1216, ac-coupling should be used. If the LVDS receiver has internal 100  $\Omega$  termination, external termination must be omitted.

Unused outputs can be left open without connecting any trace to the output pins.

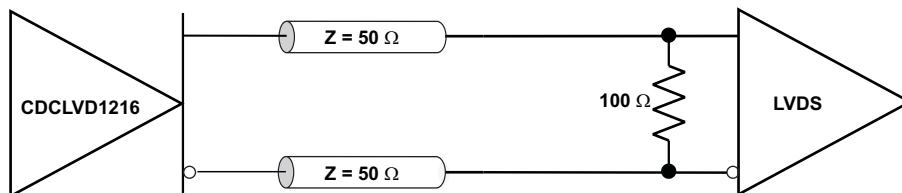


Figure 13. LVDS Output DC Termination

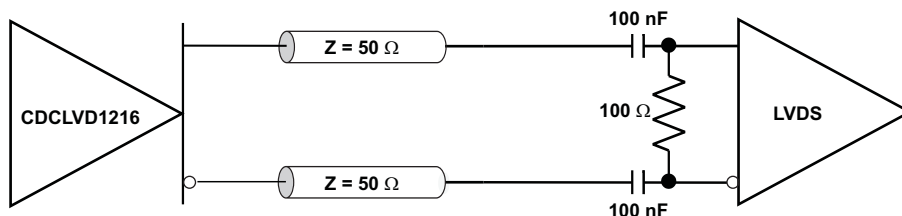
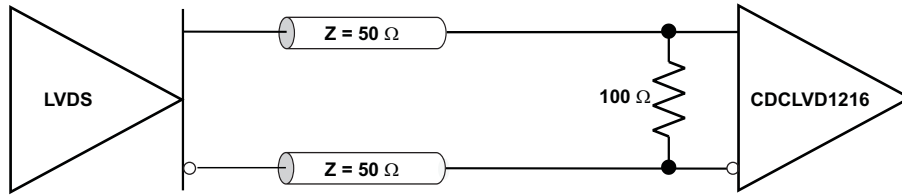


Figure 14. LVDS Output AC Termination with Receiver Internally Biased

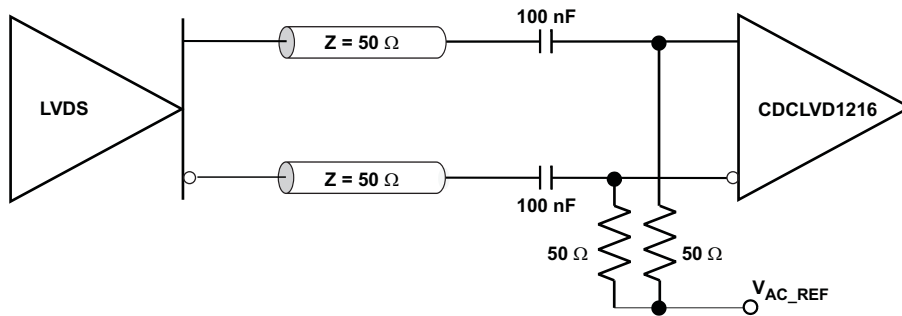
**INPUT TERMINATION**

The CDCLVD1216 inputs can be interfaced with LVDS, LVPECL, or LVCMOS drivers.

LVDS Driver can be connected to CDCLVD1216 inputs with dc or ac coupling as shown [Figure 15](#) and [Figure 16](#) respectively.

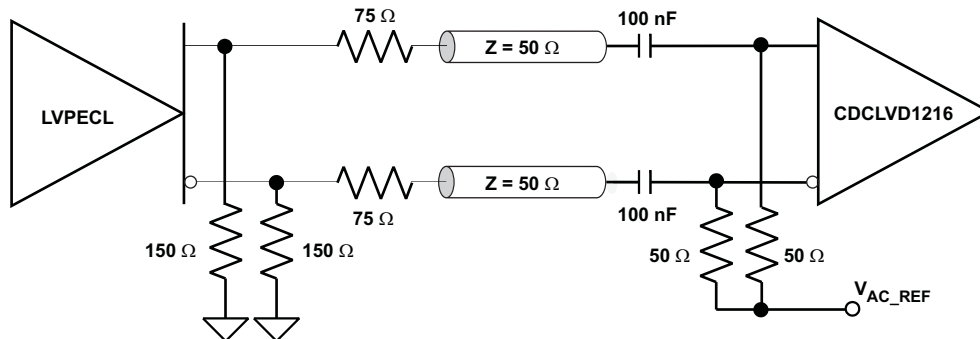


**Figure 15. LVDS Clock Driver Connected to CDCLVD1216 Input (DC coupled)**



**Figure 16. LVDS Clock Driver Connected to CDCLVD1216 Input (AC coupled)**

[Figure 17](#) shows how to connect LVPECL inputs to the CDCLVD1216. The series resistors are required to reduce the LVPECL signal swing if the signal swing is  $>1.6 V_{PP}$ .



**Figure 17. LVPECL Clock Driver Connected to CDCLVD1216 Input**

Figure 18 illustrates how to couple a 2.5 V LVCMOS clock input to the CDCLVD1216 directly. The series resistance ( $R_S$ ) should be placed close to the LVCMOS driver if needed. 3.3 V LVCMOS clock input swing needs to be limited to  $V_{IH} \leq V_{CC}$ .

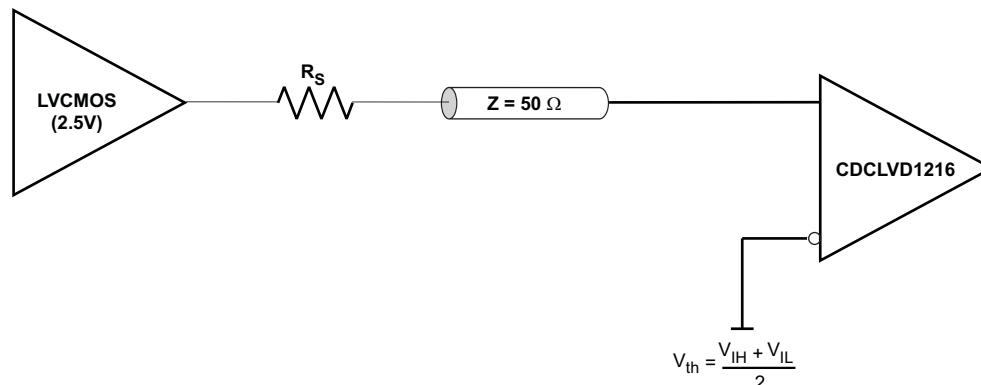


Figure 18. 2.5V LVCMOS Clock Driver Connected to CDCLVD1216 Input

For unused inputs, it is recommended to ground both input pins (INP, INN) using 1 kΩ resistors.

### REVISION HISTORY

Changes from Original (October 2010) to Revision A	Page
• Changed Feature - Low Output Skew of 45 ps (Max) To: Low Output Skew of 55 ps (Max) .....	1
• Changed $t_{sk, o}$ Output Skew From: 45 ps (Max) To: 55 ps (Max) .....	5
• Deleted the Recommended PCB Layout illustration .....	10
Changes from Revision A (November 2010) to Revision B	Page
• Changed the device status From: Product Preview To: Production .....	1

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCLVD1216RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCLVD 1216	<a href="#">Samples</a>
CDCLVD1216RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCLVD 1216	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVD1216RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CDCLVD1216RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



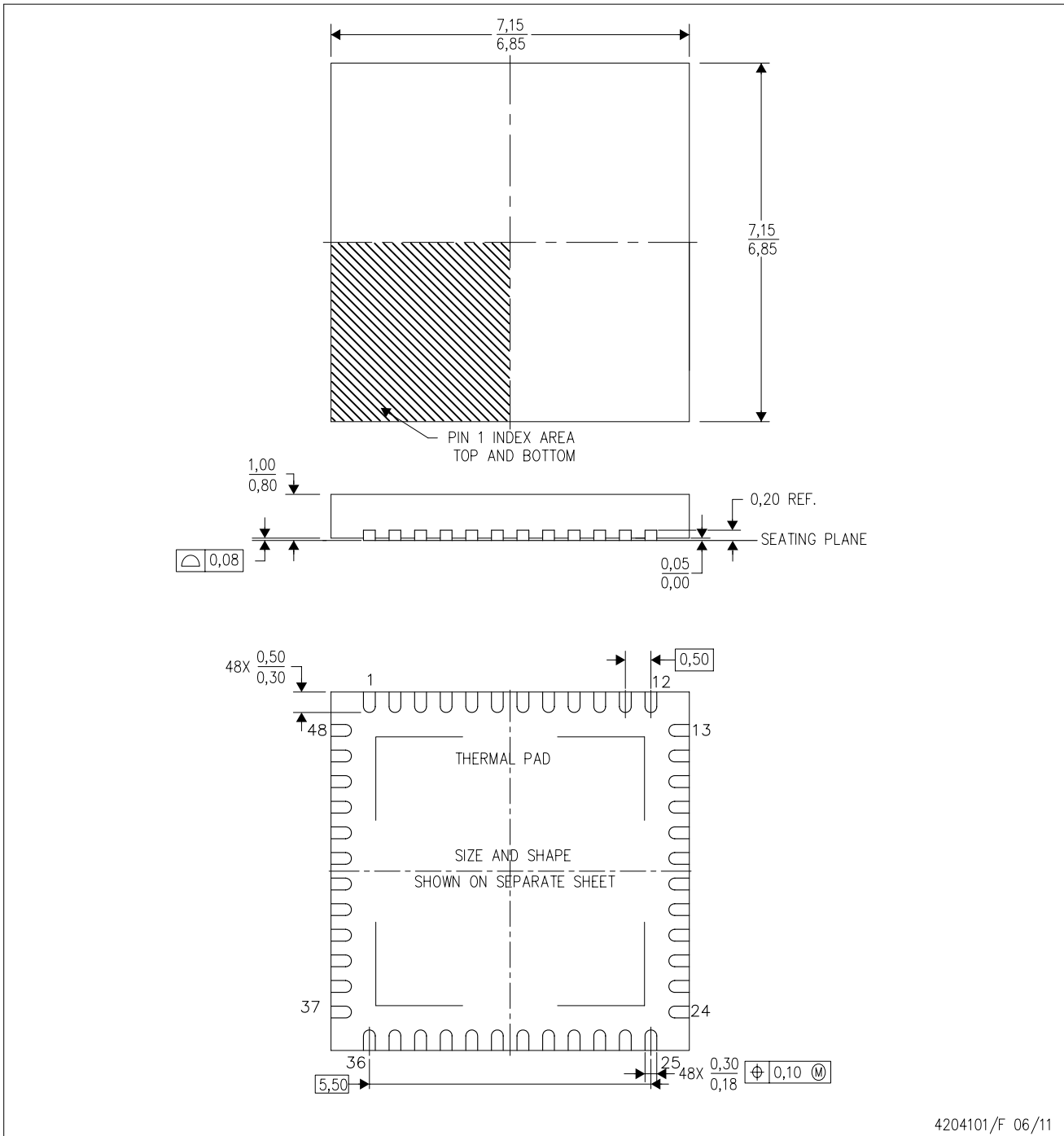
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVD1216RGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
CDCLVD1216RGZT	VQFN	RGZ	48	250	213.0	191.0	55.0



RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

# THERMAL PAD MECHANICAL DATA

RGZ (S-PVQFN-N48)

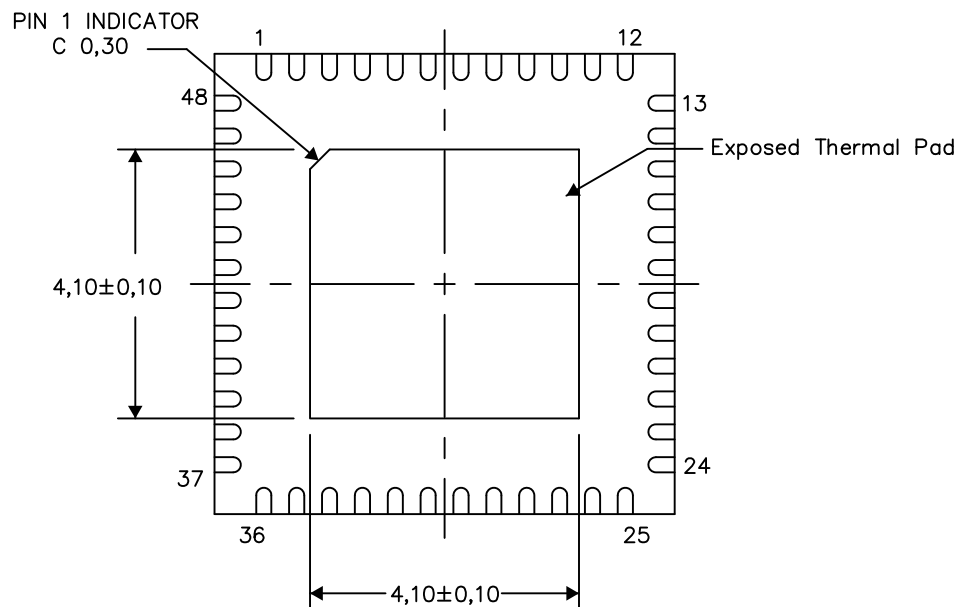
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

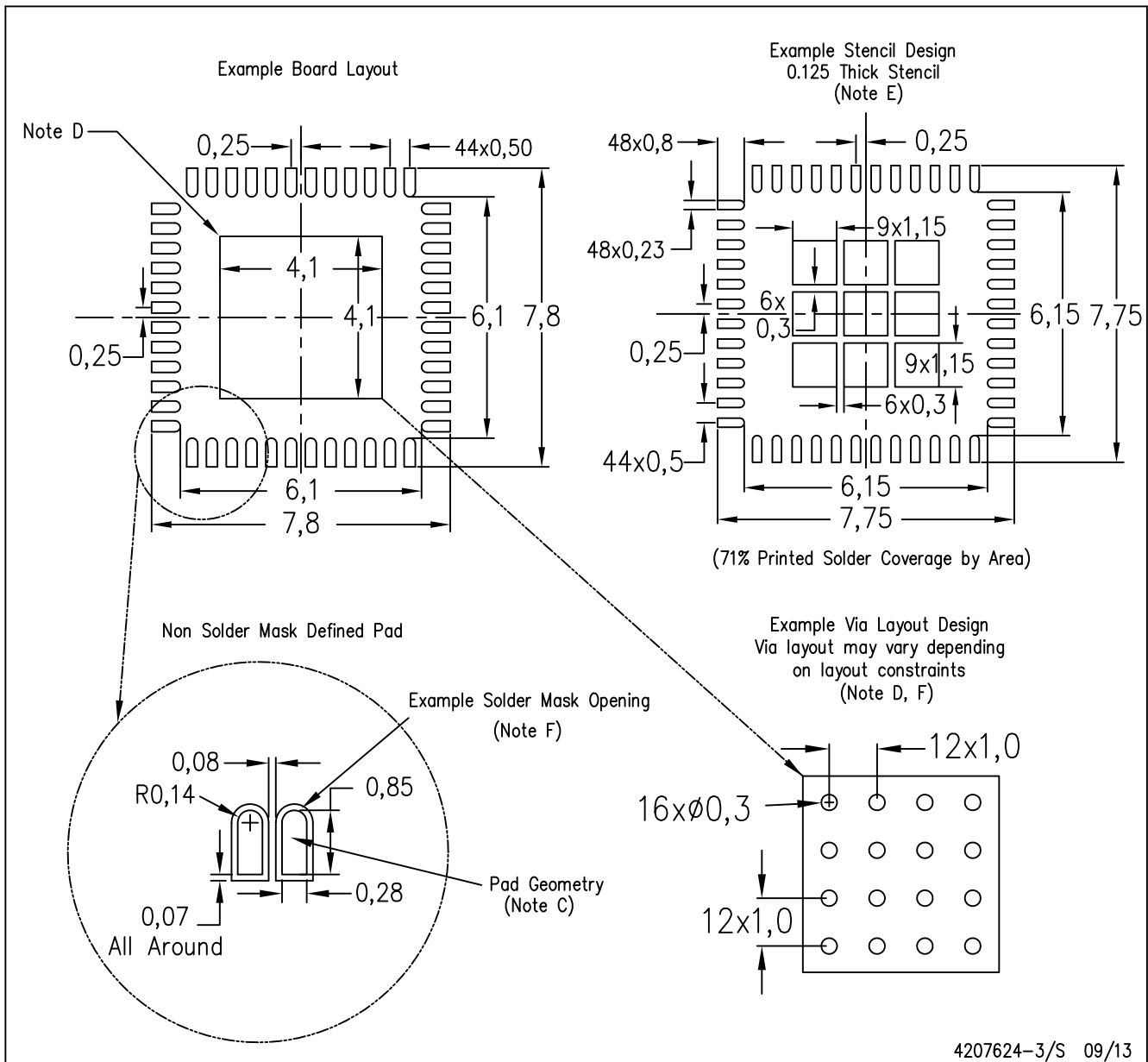
Exposed Thermal Pad Dimensions

4206354-3/X 01/14

NOTE: All linear dimensions are in millimeters

RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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