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DOCUMENT DESCRIPTION

Routing Checklist for the LAN8820, 56-pin QFN Package

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Routing Checklist for LAN8820

Information Particular for the 56-pin QFN Package

LAN8820 QFN Phy Interface:

1. The traces connecting the transmit/receive pair (TR0P, pin 44) & (TR0N, pin 43) to the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.

2. The traces connecting the transmit/receive pair (TR1P, pin 47) & (TR1N, pin 46) to the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.

3. The traces connecting the transmit/receive pair (TR2P, pin 52) & (TR2N, pin 51) to the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.

4. The traces connecting the transmit/receive pair (TR3P, pin 55) & (TR3N, pin 54) to the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.

5. For differential traces running from the LAN controller to the magnetics, SMSC recommends routing all eight traces on the component side of the PCB with a contiguous digital ground plane on the next layer. This will minimize the use of vias and avoid impedance mismatches by switching PCB layers.

6. Refer to Figure No. 1 for differential pair routing details.

7. Both traces of any one differential pair must be matched in length.

8. The delta in length between the four pairs should be less than 0.6 inches (600 mils).

9. The clearance between the four differential pairs should be at least 5 times the spacing between the TRxP and TRxN traces.

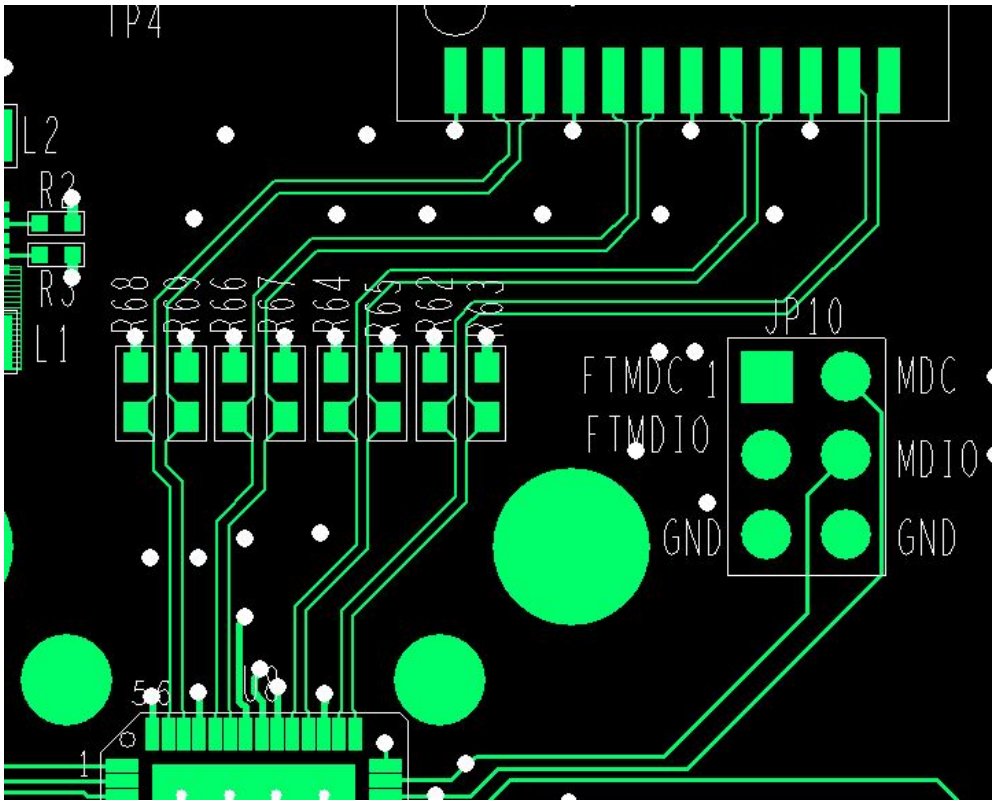

Figure No. 1

LAN8820 QFN Magnetics:

1. The traces connecting the transmit/receive signals from the magnetics to pins 1 & 2 on the RJ45 connector must be run as differential pairs. The differential impedance should be 100 ohms.

2. The traces connecting the transmit/receive signals from the magnetics to pins 3 & 6 on the RJ45 connector must be run as differential pairs. The differential impedance should be 100 ohms.

3. The traces connecting the transmit/receive signals from the magnetics to pins 4 & 5 on the RJ45 connector must be run as differential pairs. The differential impedance should be 100 ohms.

4. The traces connecting the transmit/receive signals from the magnetics to pins 7 & 8 on the RJ45 connector must be run as differential pairs. The differential impedance should be 100 ohms.

5. For three of the differential pair traces running from the magnetics to the RJ45 connector, SMSC recommends routing these traces on the component side of the PCB with all power planes (including chassis ground) cleared out from under these traces. This will minimize the use of vias and minimize any unwanted noise from coupling into the differential pairs. The plane clear out boundary is usually halfway through the magnetics.

6. For the fourth differential pair traces running from the magnetics to the RJ45 connector, SMSC recommends routing these traces on the bottom side of the PCB with all power planes (including chassis ground) cleared out from under these traces. This will minimize the use of vias and minimize any unwanted noise from coupling into the differential pairs. The plane clear out boundary is usually halfway through the magnetics.

7. Both traces of any one differential pair must be matched in length.

8. The delta in length between the four pairs should be less than 0.6 inches (600 mils).

9. The clearance between the four differential pairs should be at least 5 times the spacing between the TRxP and TRxN traces.

10. Refer to Figures No. 2 & 3 for differential pair routing details.

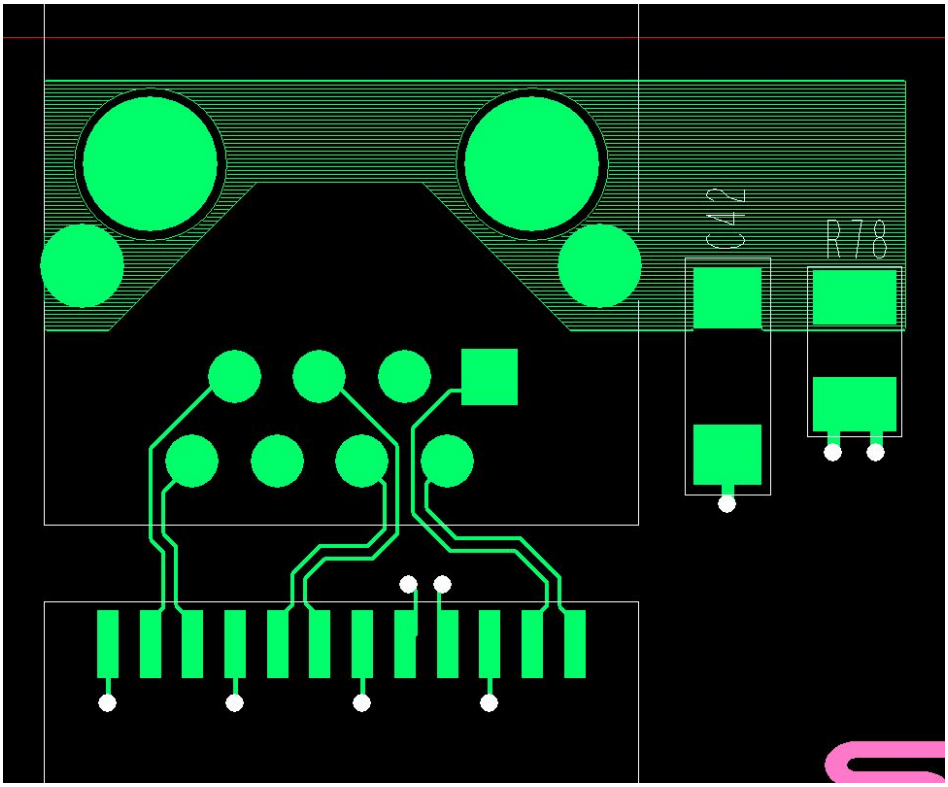

Figure No. 2

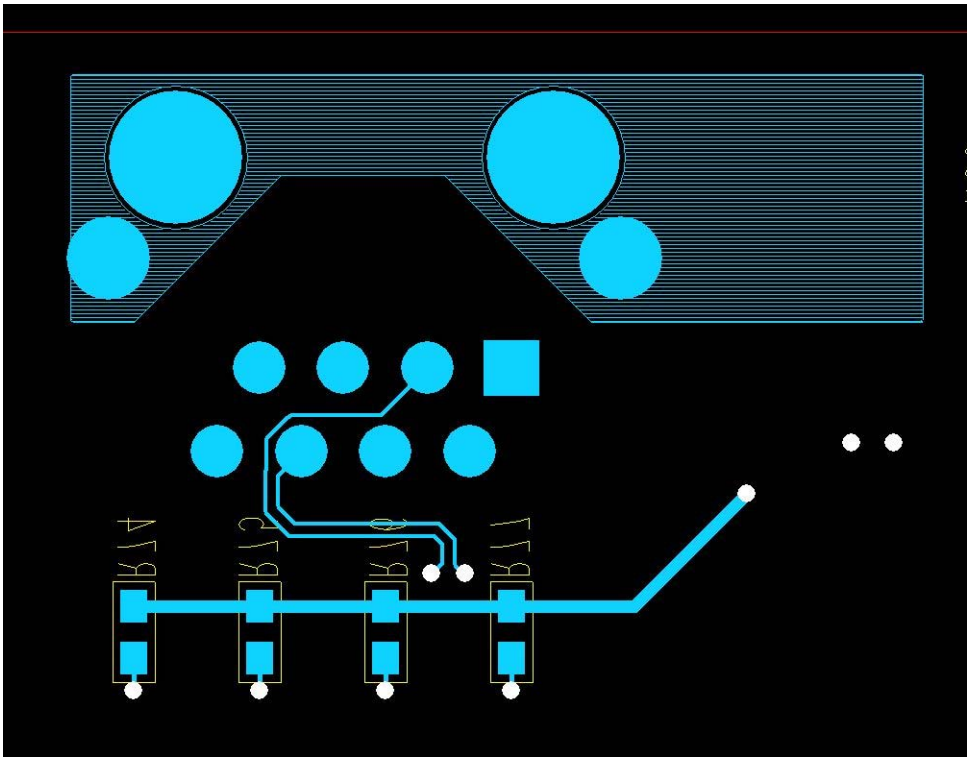

Figure No. 3

RJ45 Connector:

1. Try to keep all other signals out of the Ethernet front end (RJ45 through the magnetics to the LAN chip). Any noise from other traces may couple into the Ethernet section and cause EMC problems.

2. Also recommended, is the construction of a separate chassis ground that can be easily connected to digital ground at one point. This plane provides the lowest impedance path to earth ground.

VDD25IO Power Supply Connections:

1. Route the (4) VDD25IO pins of the LAN8820 QFN directly into a solid, +2.5V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

2. In addition, route the (4) VDD25IO decoupling capacitors for the LAN8820 QFN power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+2.5V & digital ground plane) for each cap.

+1.2V Power Supply Connections:

1. Route the (6) VDD12CORE pins of the LAN8820 QFN directly into a solid, +1.2V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

2. In addition, route the (6) VDD12CORE decoupling capacitors for the LAN8820 QFN power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+1.2V & digital ground plane) for each cap.

3. Route the (4) VDD12A pins of the LAN8820 QFN directly into a solid, +1.2V power plane (created with a ferrite bead). The pin-to-plane trace should be as short as possible and as wide as possible.

4. In addition, route the (4) VDD12A decoupling capacitors for the LAN8820 QFN power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+1.2V & digital ground plane) for each cap.

5. The bulk capacitance for the VDD12A power plane can reside anywhere on the plane.

6. Route the VDD12BIAS pin of the LAN8820 QFN directly into a solid, +1.2V mini-power plane (created with a ferrite bead). The pin-to-plane trace should be as short as possible and as wide as possible.

7. In addition, route the VDD12BIAS decoupling capacitor for the LAN8820 QFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+1.2V & digital ground plane) for the cap.

8. The bulk capacitance for the VDD12BIAS power plane can reside anywhere on the plane.

9. Route the VDD12PLL pin of the LAN8820 QFN directly into a solid, +1.2V mini-power plane (created with a ferrite bead). The pin-to-plane trace should be as short as possible and as wide as possible.

10. In addition, route the VDD12PLL decoupling capacitor for the LAN8820 QFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each power plane (+1.2V & digital ground plane) for the cap.

11. The bulk capacitance for the VDD12PLL power plane can reside anywhere on the plane.

Ground Connections:

1. The single digital ground pin (pin 57, EDP) on the LAN8820 QFN should be connected directly into a solid, contiguous, internal ground plane. The EDP pad on the component side of the PCB should be connected to the internal digital ground plane with 16 power vias in a 4x4 grid.

2. We recommend that all Ground pins be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

Crystal Connections:

1. The routing for the crystal or clock circuitry should be kept as small as possible and as short as possible.

2. A small ground flood routed under the crystal package on the component layer of PCB may improve the emissions signature. Stitch the flood with multiple vias into the digital ground plane directly below it.

ETHRBIAS Resistor:

1. The ETHRBIAS resistor (pin 42) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures. Do not run any traces under the ETHRBIAS resistor.

Required External Pull-ups/Pull-downs:

1. There are no critical routing instructions for the Required External Pull-up/ Pull-down connections.

RGMII Interface:

1. The RGMII interface on the LAN8820 can be designed using 50-ohm to 68-ohm traces.

2. Similar groups of the RGMII interface should be routed together on the PCB. Transmit channel signals should be routed together and separate from Receive channel signals.

3. RX_CLK and TX_CLK signals should be given sufficient spacing from all other RGMII signals.

4. All RGMII signals should be matched in length with a tolerance of +/- 0.4 inches (400 mils).

5. RGMII signals considered critical should be routed on the top layer next to a contiguous, digital ground plane. Slower RGMII signals can be routed on the bottom layer of the PCB.

6. As with any high-speed digital design, inter-space and intra-space guidelines between MII signals should help to improve crosstalk and signal integrity issues.

7. The use of vias should be kept to a minimum on RGMII interface and switching layers on the PCB is not recommended.

CONFIG[3..0] Pins:

1. There are no critical routing instructions for the CONFIG[3..0] pins of the Phy.

LED Pins:

1. There are no critical routing instructions for the LED pins of the Phy.

Dedicated Configuration Strap Pins:

1. There are no critical routing instructions for the Dedicated Configuration Strap pins of the Phy.

Miscellaneous:

1. SMSC recommends utilizing at least a four-layer design for boards for the LAN8820 QFN device. The design engineer should be aware, however, as tighter EMC standards are applied to his product and as faster signal rates are utilized by his design, the product design may benefit by utilizing up to eight layers for the PCB construction.

2. As with any high-speed design, the use of series resistors and AC terminations is very application dependant. Buffer impedances should be anticipated and series resistors added to ensure that the board impedance matches the driver. Any critical clock lines should be evaluated for the need for AC terminations. Prototype validation will confirm the optimum value for any series and/or AC terminations.

3. Bulk capacitors for each power plane should be routed immediately into power planes with traces as short as possible and as wide as possible.

4. Following these guidelines and other general design rules in PCB construction should ensure a clean operating system.

5. Trace impedance depends upon many variables (PCB construction, trace width, trace spacing, etc.). The electrical engineer needs to work with the PCB designer to determine all these variables.