

### Introduction

The purpose of this application note is to provide specific design and layout guidelines to printed circuit board and software designers utilizing the VSC8204 quad 10/100/1000BASE-T physical layer device.

### Power Supply Organization and Decoupling

The VSC8204 requires a 3.3v and a 1.5v power supply source for operation using GMII, MII or TBI digital interfaces. By default, RGMII and RTBI modes operate using 3.3v I/O power supply. An optional 2.5v power supply can be used as well for RGMII and RTBI modes, as specified by the RGMII/RTBI standard. Refer to MII register 23 in the VSC8204 datasheet for information on setting up RGMII and RTBI modes.

### PCB Power Plane Organization

It is recommended that the PCB power plane(s) in a system be divided into four separate regions:

**Table 1: Power Supply Plane Regions**

Plane Region	Description	Voltage	Current <sup>a</sup>	Associated VSC8204 Power Pins
V+IO	Input/output buffer supply	3.3v 2.5v (RGMII only)	100mA 76mA	VDDIO
V+A33	Filtered analog 3.3v supply	3.3v	362mA	VDDL, VDDREC, VDDPLL33, VREFP
V+A15	Filtered analog 1.5v supply	1.5v	196mA	VDD15_n, VDDPLL15
V+DIG	High-current digital core supply	1.5v	1584mA	VDDDIG

a. These numbers are based on typical performance at 25°C with all PHYs operating simultaneously in full-duplex 1000BASE-T mode. Further details, including worst-case estimates, can be found in the VSC8204 datasheet in the “Current and Power Consumption” section.

### Power Supply Filtering and Decoupling

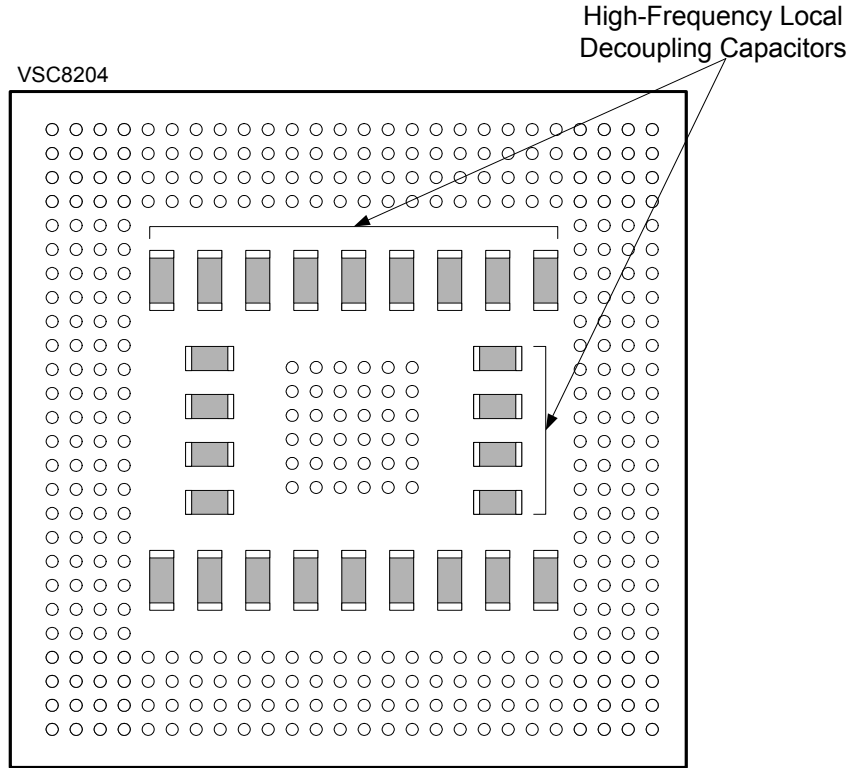
For best performance, each power supply region should contain capacitors for both bulk decoupling and for high-frequency local decoupling. This is summarized in the following table:

**Table 2: Bulk Decoupling**

Power Supply Plane Region	Bulk Decoupling Required	Local Decoupling Required <sup>a</sup>
V+IO	22uF	Seven 0.1uF capacitors
V+A33	22uF	Five 0.1uF capacitors
V+A15	22uF	One 0.1uF capacitor
V+DIG (with regulator FET option- see Section “Thermal Performance”)	2.2uF	Seven 0.1uF capacitors
V+DIG (without regulator FET option)	22uF	Seven 0.1uF capacitors

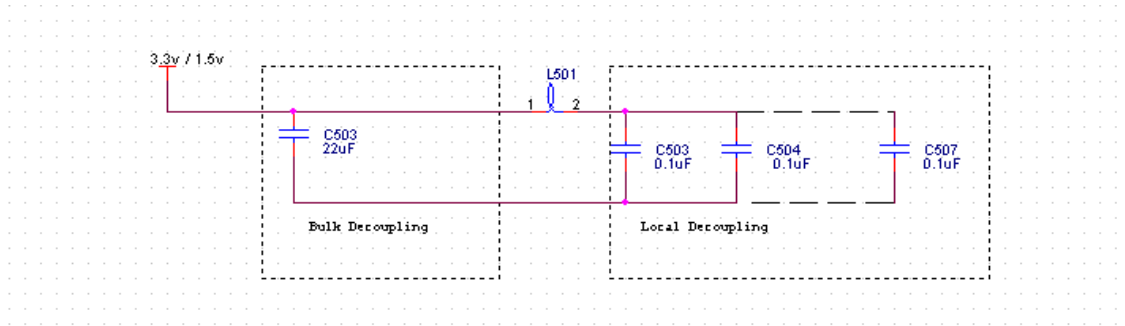
a. These numbers are based on typical performance of pre-production silicon at 25°C with all PHYs operating simultaneously in full-duplex 1000BASE-T mode.

Local decoupling capacitors should be placed as close to the VSC8204 as possible. The best location for local decoupling capacitors is on the bottom of the board, directly under the VSC8204 (see Figure 1: "Local High-Frequency Decoupling Capacitor Layout (View from bottom of PCB)", below).



**Figure 1: Local High-Frequency Decoupling Capacitor Layout (View from bottom of PCB)**

In addition, a ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.



**Figure 2: Decoupling Schematic**

The beads should be chosen to have the following characteristics:

- Current rating of at least 150% of the maximum current of the power supply
- Impedance of 80 to 100Ω at 100MHz

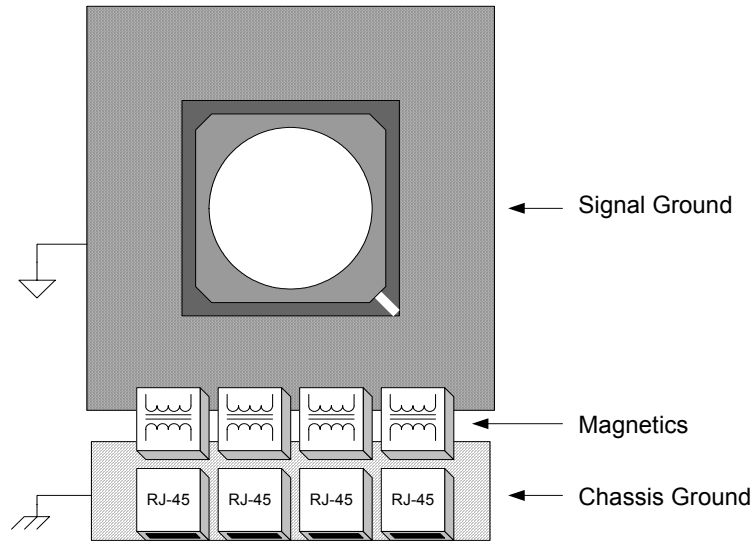
Recommended beads are:

- Panasonic EXCELSA39 or similar
- Steward HI1206N101R-00 or similar

Since all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. For this reason, it is recommended that system designers provide an option to replace the ferrite beads with zero-ohm resistors, once thorough evaluation of system performance is completed.

**PCB Chassis Ground Region**

To isolate the board from ESD events and to provide a common-mode noise ground path, a separate chassis ground region should be allocated. This should provide an electrical connection to the external chassis and the shield ground for RJ-45 connectors. In addition, the “Bob Smith” termination impedance should be connected between this ground and the cable-side center-taps of the magnetics modules. (see Figure 3: “Ground Plane Layout” and Figure 4: “Chassis Ground and Magnetics”, below).



**Figure 3: Ground Plane Layout**

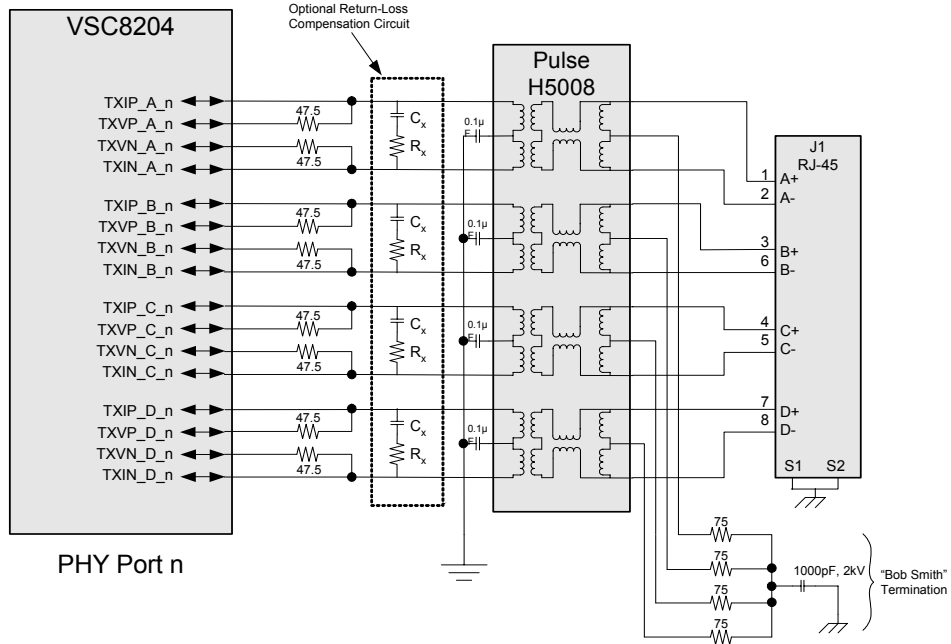


Figure 4: Chassis Ground and Magnetics

## Design for Signal Integrity

With the high-speed nature of the VSC8204 data signals, careful attention must be paid to PCB layout and design to maintain adequate signal integrity. To simplify board design, the VSC8204 has been designed with SimpliPIN™ outputs on certain pins, which automatically calibrate their output resistance to 50-Ω, eliminating the need for series termination resistors.

### MAC Transmit and Receive Interface Pins

These pins have been designed with extremely fast rise and fall times to allow for 125MHz operation. To adequately accommodate these signals on a PCB, it is recommended that the traces be designed as either microstrip or stripline transmission lines with a characteristic impedance of 50Ω. It is also important that an unbroken ground plane exist above and/or below these signals.

For the VSC8204 MAC receive interface, each pin is self-calibrating to an output resistance of 50Ω. Thus, external series termination resistors are unnecessary as long as the characteristic impedance of the PCB traces are also 50Ω (see Figure 5: "MAC Tx/Rx Series Termination", below)

For the VSC8204 MAC transmit interface, careful attention must be paid to the output resistance of the pins on the MAC or switch device. If that resistance is less than 50Ω, additional series termination resistors are required. These resistors should be placed as close as possible to the MAC or switch device.

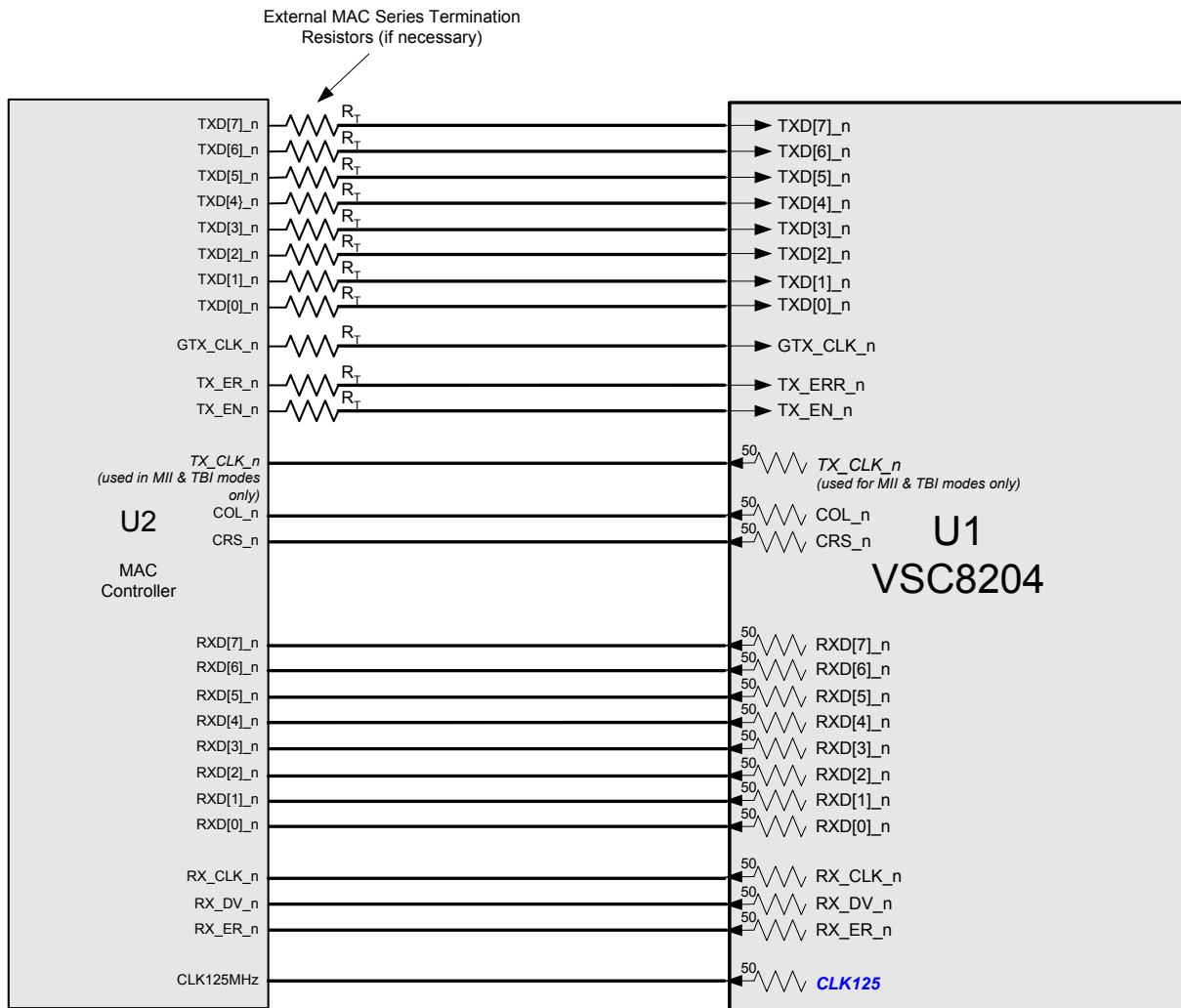


Figure 5: MAC Tx/Rx Series Termination

**Twisted-Pair Interface Pins**

These pins are the interface to the external CAT-5 cable and are organized in four differential pairs for each port. These are labeled "TXIP\_x\_n" and "TXIN\_x\_n", where 'x' is the particular pair within a single cable and 'n' is the port number. When routing these pairs on a PCB, the characteristics must match one of the following:

- Route each trace single-ended with a characteristic impedance of 50Ω referenced to ground.
- OR--
- Route each pair of positive and negative traces differentially, with a 100Ω differential characteristic impedance.

**47.5Ω Line-side Resistors**

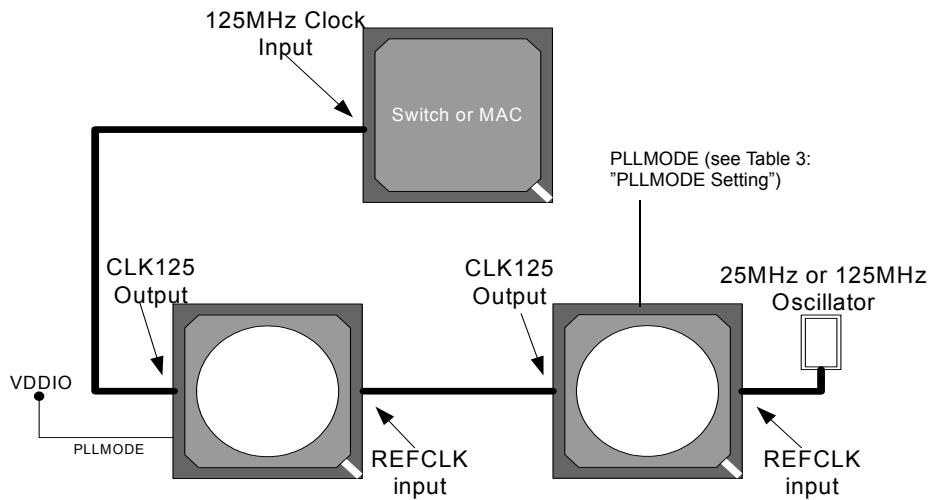
Eight resistors of value 47.5Ω are needed for proper line-side operation. It is important that these resistors be placed as close to the PHY as possible for best performance. Tolerance for these resistors should be 1% or better.

**125MHz Clock Output**

By default, the VSC8204 provides a low-jitter, 125MHz output clock for driving other devices in a system. As with the MAC transmit interface pins above, the output resistance of this pin is self-calibrating to 50Ω, and should be routed on the PCB using a microstrip or stripline transmission line trace.

**Note: The 125MHz output clock is NOT enabled if the VSC8204 is held in reset (RESET# pin held low).**

This clock output can be used in a daisy-chain fashion with other VSC8204 devices to provide a clock source to all devices in a system with the need for only a single crystal oscillator (see Figure 6: "Clock Distribution", below).



**Figure 6: Clock Distribution**

Careful attention must be paid to the PLLMODE signal for each device when using a daisy-chain clock source. For the first device in the chain, which is connected to the oscillator, the value of PLLMODE must be set to correspond to Table 3, below:

**Table 3: PLLMODE Setting**

PLLMODE Value	REFCLK Frequency
1	125MHz
0	25MHz
NC	25MHz (PLLMODE includes an on-chip pulldown, which results in a default value of 0)

For each addition VSC8204 device in the chain, set PLLMODE to 1 by tying the signal to VDDIO. This will enable each device to function using the 125MHz clock output of the previous device(s) in the chain.

Note that the CLK125 output is enabled by default. It can be disabled by writing a '0' to MII register 18, bit 0.

**An Important Note Regarding LED\_CLK, LED\_DATA and JTAG TDO Pins**

The LED\_CLK, LED\_DATA and JTAG TDO pins for the VSC8204 were designed with the same output driver technology as the MAC transmit and 125MHz clock outputs above, which provide an extremely fast rise and fall time with integrated series termination resistors (see Figure 7: "Miscellaneous Series Termination", below). Even though the overall clock speed is much slower, these signals must be treated as high-speed signals to avoid reflections caused by the extremely fast transitions. This issue can be addressed in one of two ways:

- Route each signal using a microstrip or stripline transmission line trace with a characteristic impedance of 50Ω.
- OR--
- Ensure that the lengths of the PCB traces are less than 0.75 inches.

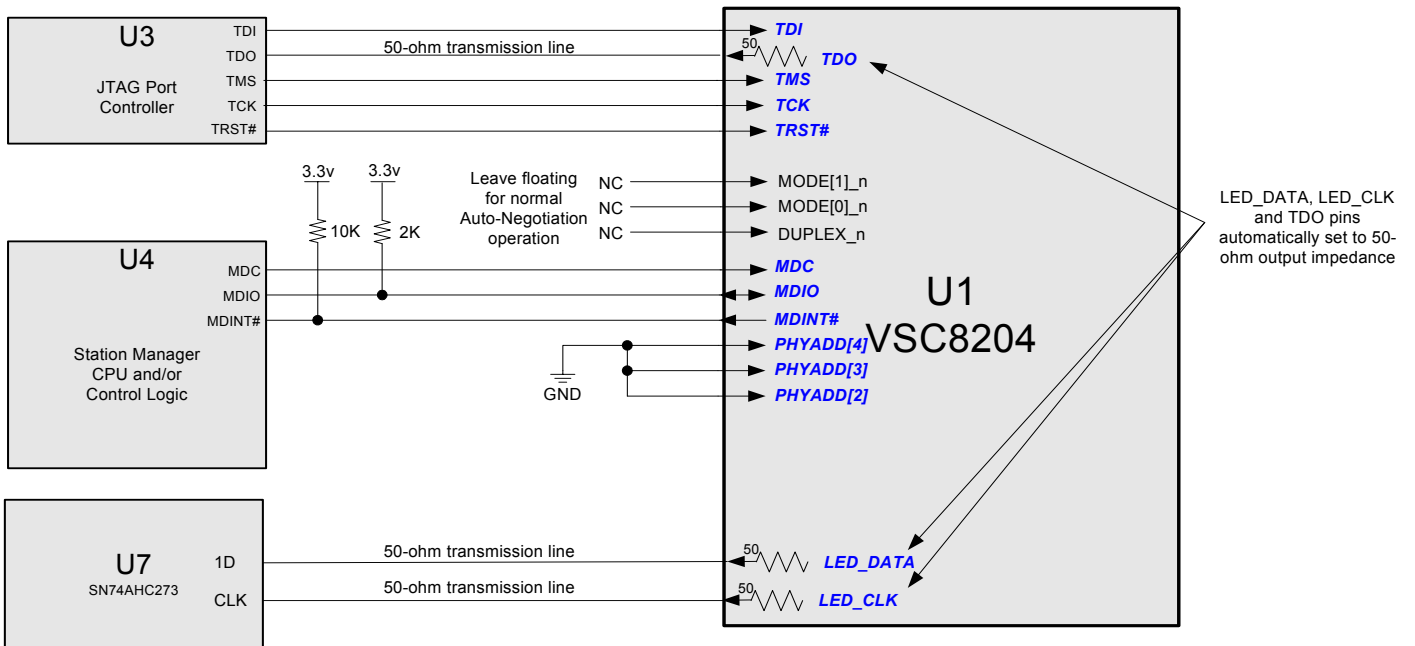


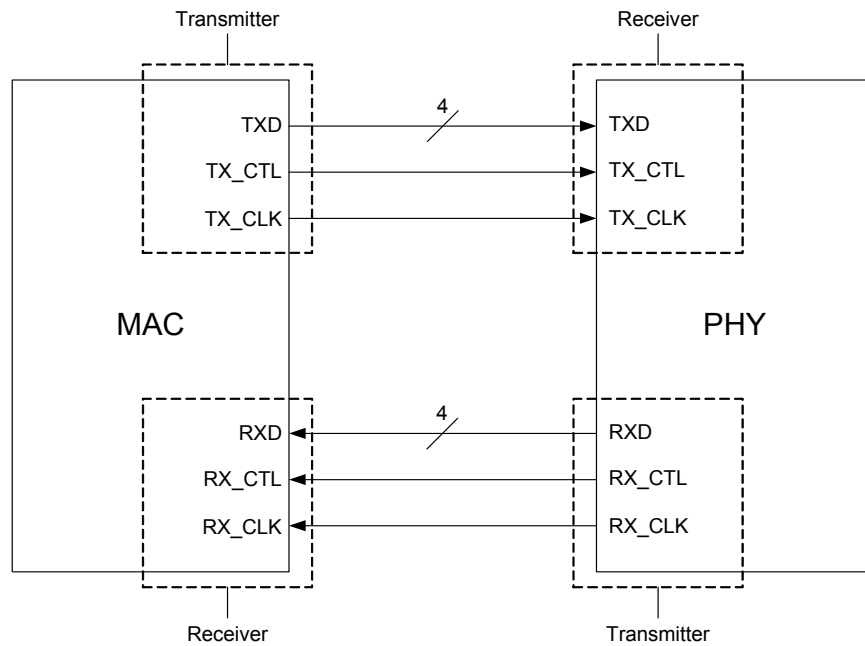
Figure 7: Miscellaneous Series Termination

### RGMI Interface Guidelines

The Reduced Gigabit Media Independent Interface (RGMI) is a variation upon the Gigabit Media Independent Interface (GMII) and Media Independent Interface (MII) outlined in IEEE802.3ab. This section refers to RGMI v2.0, which is the most recent version at the time of writing.

#### Clock Delays

When considering the interface between MAC and PHY, the relationship between transmitter and receiver is often confused. Please refer to the following diagram:

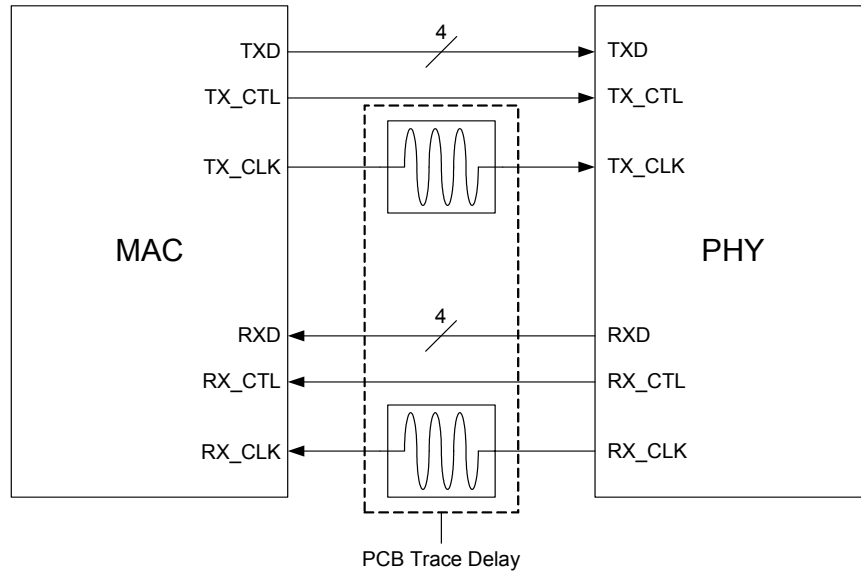


Note that for all traces beginning with "TX", the PHY is the receiver; while for all traces beginning with "RX", the MAC is the receiver.

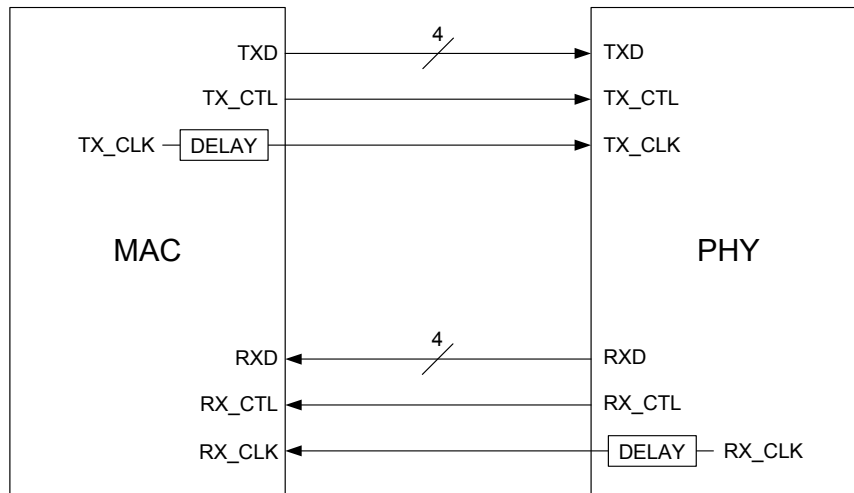


In order for the input registers (receivers) of the MAC and PHY to see a stable data signal during both rising and falling clock edges, several methods exist for the introduction of a clock delay:

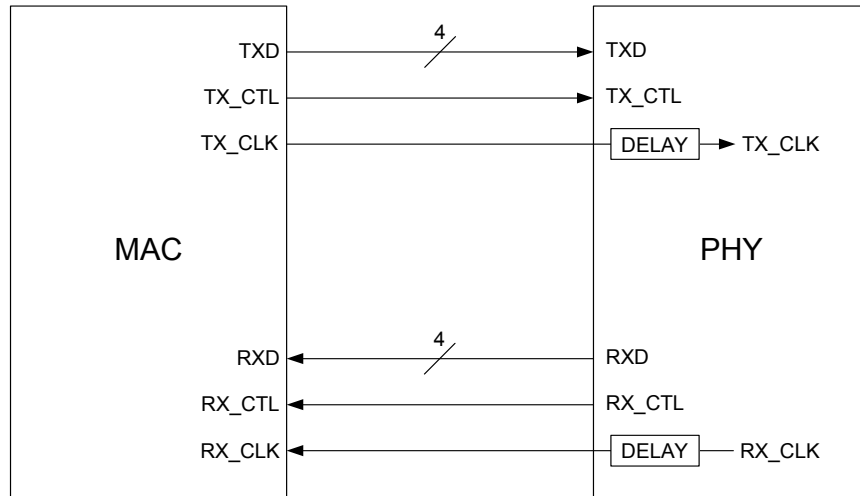
1. A delay of 1.5 to 2ns can be added to the TX\_CLK and RX\_CLK signals by routing them through a long PCB "trombone" trace delay.



2. An output clock skew can be integrated into the clock signal output of each transmitter. Specifically, this calls for the MAC to provide a clock skew on the TX\_CLK, while the PHY must provide a clock skew on the RX\_CLK. Devices supporting this type of configuration are defined as "RGMII-ID" in the RGMII standard.



3. A clock skew can be integrated into the PHY for both RX\_CLK and TX\_CLK. Strictly speaking, this method is not compliant with the RGMII standard. However, this allows a MAC which does not support the RGMII-ID configuration to be connected to a PHY without the use of PCB trace delays.



**Note:** The VSC8204 device supports methods 1 and 3 above, but does not support an integrated delay on only the TX\_CLK line as specified in method 2.

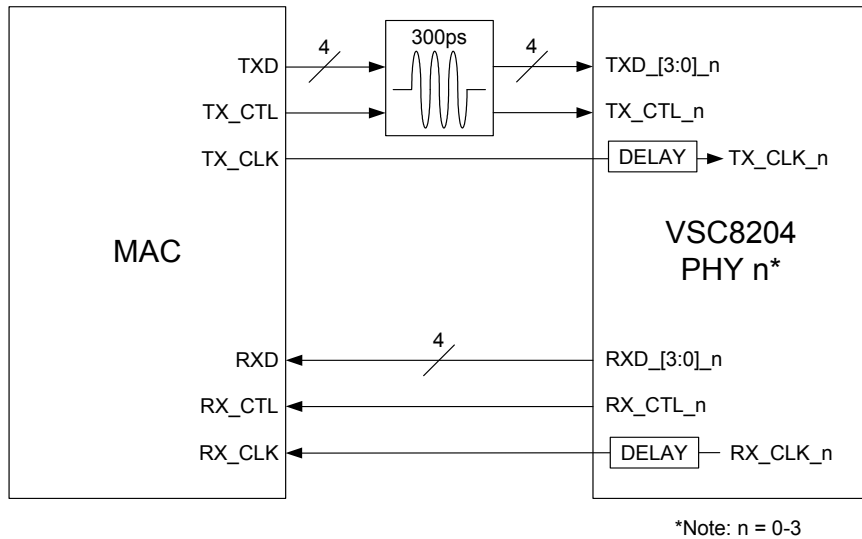
**Using Integrated Clock Skew to Implement RGMII with VSC8204**

The VSC8204 contains an internal delay element connected to each TX\_CLK and RX\_CLK pin, which can provide the necessary clock delays for the RGMII interface without the need for PCB trace delays. These elements are enabled by writing a 1 to MII register 23, bit 8. Note that the delay for TX\_CLK and RX\_CLK cannot be individually enabled or disabled - they are either both enabled or both disabled. For this reason, the VSC8204 cannot be considered an "RGMII-ID" compatible device.

For the RX\_CLK signal, the integrated clock skew provides a delay of 2ns relative to RXD and RX\_CTL. With this skew enabled, the RX traces should to be routed from the PHY to MAC without the introduction of additional skew. For the TX traces, however, an important consideration must be made. In the errata for VSC8204, it is stated that "when internal skew timing compensation is enabled (MII register 23, bit 8), the compensation on the TX\_CLK signal inside the device does not provide the correct delay of 2ns. Additional jitter is also added to the TX\_CLK signal inside the device." For these reasons, input timing for the TX signals in RGMII on the VSC8204 does not appear as expected.

To correct for this errata, a PCB trace delay of 300ps (±150ps) should be added to all TXD and TX\_CTL traces. Note that even though these delays must be added to each of these traces, the total PCB trace requirement is significantly less than what is required if the integrated clock skew is disabled.

The PCB system requirements for RGMII with the integrated clock skew enabled are shown in the following figure for VSC8204.



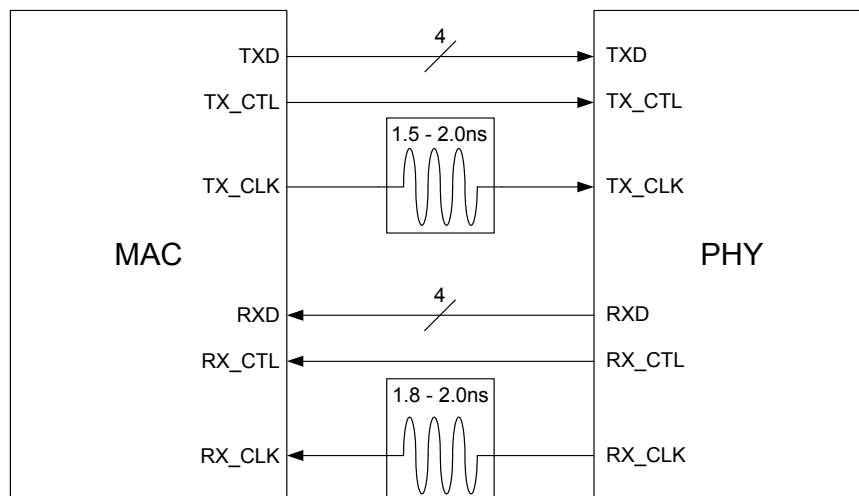
**Using PCB Trace Delays to Implement RGMII with VSC8204**

If it is desired to use PCB trace delays to implement the clock skew between the MAC and VSC8204, it is necessary to write a 0 to MII register 23, bit 8.

For the RX traces, an important consideration must be made. In the errata for the VSC8204, it is stated that "When internal skew timing compensation is disabled, the minimum and maximum data-to-clock output skews (TskewT) on RXD and RX\_CLK are greater than the specified -500ps and 500ps". To correct for this errata, the minimum allowable trace delay for RX\_CLK on all PHY ports is 1.8ns, vs. 1.5ns as specified in the RGMII standard.

For the TX traces, the input timing at the PHY conforms to the RGMII standard. For this reason, the TX\_CLK trace delay can range from 1.5ns to 2.0ns in the PCB.

The TX and RX PCB trace delay requirements are shown in the following figure for VSC8204.

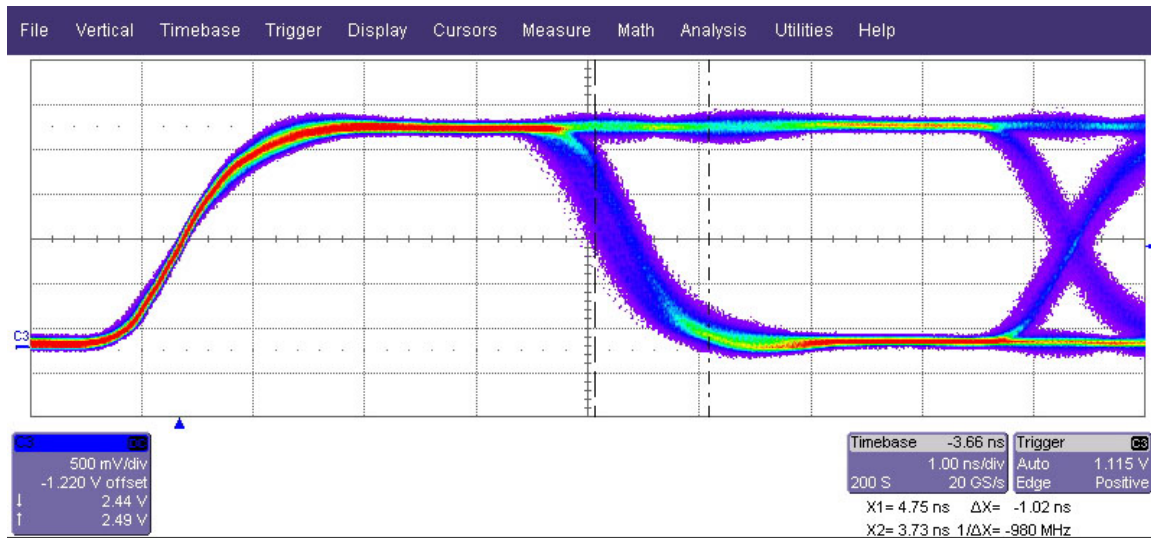


**Which Delay Technique Should Be Used?**

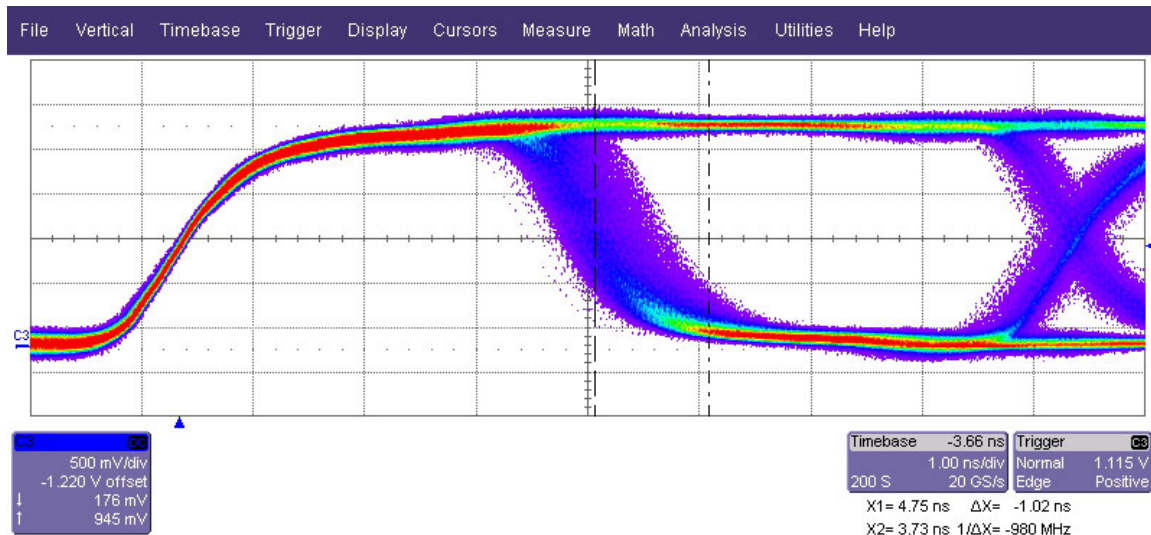
The VSC8204 allows the choice of using the RGMII internal integrated clock skew or of providing the clock skew in the design of the PCB traces. Using the PCB traces to delay to clock has the disadvantage of requiring extra board area for the clock delay lines. Even though, to correct for the errata, delay lines are also required when using the internal integrated clock skew of the VSC8204, this approach still requires less total circuit board area. For this reason, most designers will choose to use the internal integrated clock skew.

**Controlling Crosstalk in RGMII Traces**

Due to their double-data-rate nature, crosstalk can cause a much greater degradation in the signal integrity of RGMII signals versus single-data-rate signals of the same clock frequency. With each clock and data edge transitioning simultaneously, the effects of signal integrity can often appear as an increase in jitter. This is illustrated in the following two figures:

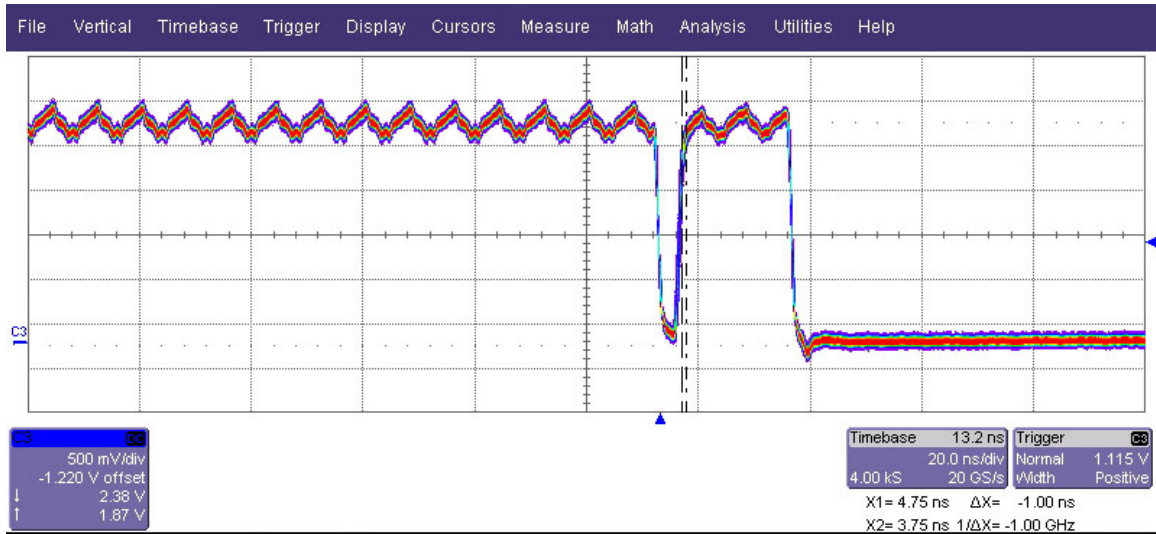


**Figure 8: Jitter in Short (~1.5 inch) RGMII Data Trace**



**Figure 9: Jitter in Long (~6 inch) RGMII Data Trace**

Notice the increased jitter apparent in the 6-inch trace versus the 1.5-inch trace above. The effects of crosstalk can also be seen as causing a ripple in the static voltage level of adjacent traces. The trace in the following figure is 6-inches in length, with data traces routed in parallel on either sides causing crosstalk as they change logic levels:



**Figure 10: Crosstalk from Parallel Data Traces**

PCB layouts for these type of signals commonly maintain a separation between traces equal to the width of a single trace. Although this is satisfactory for most single data rate signals, this arrangement has been shown to result in abnormally high crosstalk. For this reason, the following guidelines should be followed in order to reduce crosstalk in RGMII systems:

- For traces less than 1 inch in length, spacing between traces must be 5 mils or greater
- For traces greater than 1 inch in length, but less than 6 inches in length, spacing must be 10 mils or greater
- For traces greater than 6 inches in length, spacing must be 15 mils or greater. In addition, a guard trace must be placed between each signal trace. These guard traces must be connected to ground through several vias placed along the guard trace.

## Serial Management Interface

The VSC8204 contains a standard Serial Management Interface (SMI) as defined by IEEE standards. This interface consists of the following signals:

**Table 4: Serial Management Interface (SMI)**

Signal Name	Type	Description
MDC	Input	<b>Management Data Clock.</b> A 0 to 20MHz reference input used to clock serial MDIO data into and out of the VSC8204. The expected nominal frequency is 2.5MHz, as specified by the IEEE standard. This clock is typically asynchronous with respect to any PHY port's transmit or receive clock.
MDIO	Open-Drain	<b>Management Data I/O.</b> MDIO configuration and status data is exchanged on this pin bi-directionally between the PHY and the Station Manager, synchronously to the rising edge of MDC.
MDINT#	Open-Drain	<b>Management Interrupt Output.</b> This open drain, active low output signal indicates a change in any of the four PHY's link operating conditions for which a Station Manager must interrogate to determine further information. This pin should be pulled up to VDDIO at the Station Manager or controller through an external 10kΩ pullup resistor.
PHYADD[4:2]	Input <sup>a</sup>	<b>PHY Address Bus Input.</b> These inputs are the three uppermost bits of the 5-bit IEEE-specified PHY address. The states of these three pins are latched during power-up, or a hardware or software reset. The lower two bits, [1:0], of the 5-bit PHY address are hardwired to each of the four PHY ports within the device.

- a. In normal operating mode, these 3 pins are used as inputs only. However, for manufacturing test purposes, these pins are used as digital output pins.

It is important to note that both MDIO and MDINT# signals are configured as open-drain, and thus require an external pullup resistor. Only a single pullup resistor on each signal is needed for the system, regardless of the number of devices. For MDINT#, a single 10kΩ system pullup resistor is sufficient.

Unlike MDINT#, the value of pullup resistor needed for MDIO must be chosen to match the characteristics of the system. Of critical importance is the rise time needed to charge the total capacitive load on MDIO up to a logic '1' through the pullup resistor. This time constant is defined simply as:

$$\tau = R_{pu} C_{total}$$

Therefore, as more devices are added to the bus, the rise time increases due to the increased bus capacitance. In order to lower the rise time, a smaller resistor value must be used. However, if too small of a value is used, devices will be unable to transition the bus to a logic '0'. This occurs when the current sinking capability of the pins in a logic '0' state is exceeded. For the VSC8204, the MDIO input capacitance is 5pF, and the maximum current sinking capacity is 10mA.

Typical values are given below:

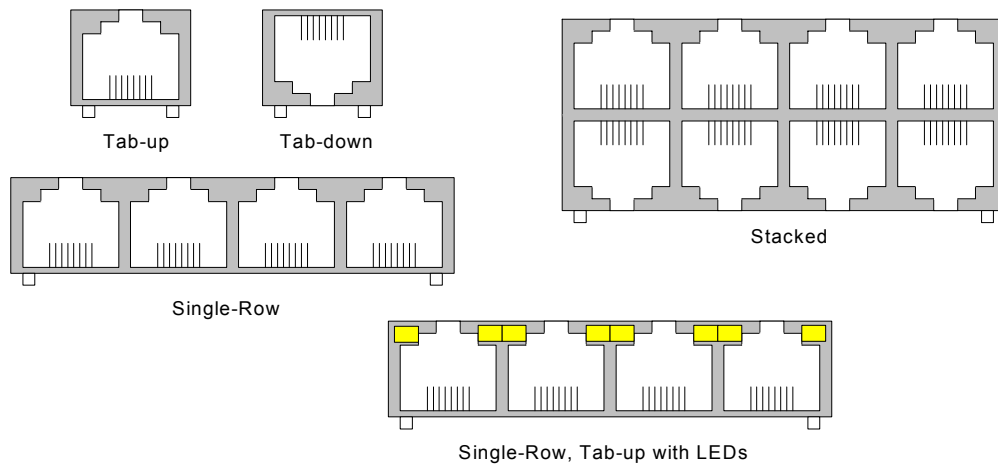
- For MDC frequencies of 2.5MHz and below, a 2kΩ pullup resistor should suffice for most applications. This assumes the input capacitance of each device is between 5-10pF and that each device can sink 1.65mA of current in the MDIO pin.
- For faster MDC frequencies (>2.5MHz), a smaller pullup is necessary. The smallest recommended pullup resistor for use with the VSC8204 is 470Ω.

## RJ-45 Connectors and Magnetic Modules

### RJ-45 Connector Recommendations

For system designers, several options exist for the choice of RJ-45 connectors. These are summarized as follows:

- Two tab orientations are available: up or down
- For multi-port connectors, two orientations are available: stacked and single-row.
- LEDs can also be integrated into the connectors.



**Figure 11: RJ-45 Example Configurations**

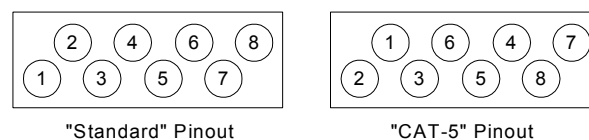
Most manufacturers can mix or match any combination of features. For example, LEDs can be added to any connector, or single-row multi-port configurations can be tab-up or tab-down. The exception is the stacked connector, which contains both tab-up and tab-down orientations.

An additional consideration is the pinout of tab-up versus tab-down connectors. Due to the orientation, the pinouts of these two are reversed. While the VSC8204 will work equally well using either orientation, signal routing will be simpler with the tab-down pinout. For the stacked variety, both orientations exist in one package, so both pinouts typically exist in one package. Some manufacturers have provided an option for “vertical” pin orientation, which allows for ease in PCB routing.

### CAT-5 vs. CAT-3 Connectors

When utilizing 1000BASE-T or 100BASE-T, it is important that “CAT-5” RJ-45 connectors be used as opposed to “CAT-3”. This refers to the amount of crosstalk between the wire pairs within the connector.

In addition to the electrical characteristics, some manufacturers have two options for the connector pinout. These are typically labelled as “standard” and “CAT-5”. This is not to be confused with the electrical specification for the connector. Thus, two versions of a CAT-5 RJ-45 connector are available: one with a “standard” pinout and one with a “CAT-5” pinout:



## Specific RJ-45 Recommendations

Virtually any RJ-45 connector that meets CAT-5 electrical specifications will work with the VSC8204. Two such manufacturers are:

**AMP (a division of Tyco International, Ltd.)**

Tel: 717-564-0100  
<http://www.amp.com/>

**Transpower Technologies, Inc.**

Tel: 775-852-0140  
<http://www.trans-power.com/>

Some example parts from these manufacturers are:

**Table 5: Sample Part Numbers for RJ-45 Connectors**

Part Number	Manufacturer	Description
558341-1	AMP	Single-port, unshielded, without LEDs, tab-down, "CAT-5" pinout.
558503-1	AMP	Four-port, shielded, without LEDs, tab-down, "CAT-5" pinout.
569264-1	AMP	Sixteen-port, shielded, without LEDs, stacked, "standard" pinout.
RJG4-7G02	Transpower <sup>a</sup>	Four-port, shielded, with LEDs and magnetics, tab-up. Pinout is unique to Transpower.
RJS16-8G02	Transpower <sup>a</sup>	Sixteen-port, shielded, with LEDs and magnetics, stacked, "vertical" pinout.

a. These modules do not require a separate magnetic module.

## Magnetic Modules

For best performance, proper magnetic modules must be used with the VSC8204. It is important that the configuration match that of Figure 4: "Chassis Ground and Magnetics" of this document. In addition, some companies integrate the magnetic modules into the RJ-45 connector.

**Note on Return-Loss Compensation Circuit:** Testing has indicated that some magnetic modules may not pass the IEEE specification for return loss. In these cases, a series resistor-capacitor circuit should be added across the primary of each transformer for each port. (see Figure 4: "Chassis Ground and Magnetics") The presence of this circuit serves only to allow the system to pass IEEE return loss measurements and does not affect the performance of the PHY in any other way. The exact values required for the resistors and capacitors vary according to each manufacturer and can be found in Table 6: "Recommended Magnetic Modules".

Below is a list of compatible magnetic modules:

**Pulse Engineering, Inc.**

Tel: 858 674-8100  
<http://www.pulseeng.com/>

**Bel Fuse, Inc.**

Tel: 201-432-0463  
<http://www.belfuse.com/>

**Halo Electronics, Inc.**

Tel: 650-568-5800  
<http://www.haloelectronics.com/>

**Transpower Technologies, Inc.**

Tel: 775-852-0140  
<http://www.trans-power.com/>

**Table 6: Recommended Magnetic Modules**

Part Number	Manufacturer	Description	Return loss compensation
H5008	Pulse	Single-port, surface mount	Rx=147Ω, Cx=10pF
S558-5999-P3	Bel	Single-port, surface mount	
TG1G-S002NZ	Halo	Single-port, surface mount	
GB2G04	Transpower	Single-port, surface mount	



## Reset Sequence

The following events occur in order when the VSC8204 is brought out of reset. This is triggered by a low-to-high transition of the RESET# pin.

1. Values for MODE, DUPLEX, PLLMODE and PHYADD pins are latched asynchronously immediately out of reset.
2. On the first rising edge of REFCLK after reset, the SMI (Serial Management Interface) becomes active.
3. Approximately 11 milliseconds after reset, the reference voltages and currents stabilize.
4. Once a stable reference is available, the PLL requires 50 microseconds to lock.
5. With a locked PLL, the analog-to-digital converter is calibrated, which requires 2.05 milliseconds.
6. Once the ADC is calibrated, the CLK125 output is activated

Once the PLL has locked, the internal chip clocks begin to run. At this point, the operation of the VSC8204 is dependent on the value of PWDN:

- If PWDN is high, the individual PHY blocks will not be enabled. The SMI is still operational.
- If PWDN is low, all sections of the device are enabled.

**Important note:** Since the values of MODE, DUPLEX, PLLMODE and PHYADD pins are latched on the rising edge of the RESET# pin, it is required that the power supply is stable before the rising edge of RESET#. Therefore, if RESET# is tied directly to a logic high on the PCB, the VSC8204 will behave unpredictably. If a design requires the RESET# pin to remain high at all times, a small RC circuit can be added to this line to provide the necessary delay.

Also, note that the SMI is enabled prior to the other blocks within the device. For applications which utilize this interface, this sequence provides a short period of time in which to configure the VSC8204 before the device is fully operational. This is useful for setting up MII registers that control items such as LEDs and MAC interface, which must be setup prior to device operation.

## Thermal Performance

Though the low power consumption of the VSC8204 eliminates the need for external heatsinks or fans in most designs, certain guidelines must be followed for adequate heat dissipation. For proper operation of the VSC8204, a silicon junction temperature ( $T_j$ ) equal to or below 125°C must be maintained for commercial temperature ranges. Within the constraints of the commercial temperature range, the limits for junction-to-ambient thermal resistance are as follows:

$$\Theta_{ja(Commercial)} \leq \frac{T_j - T_a}{P_d} \leq \frac{125^\circ C - 70^\circ C}{4W} \leq 13.75^\circ C/W$$

where  $\Theta_{ja}$  = Junction to ambient thermal resistance,  $T_j$  = Junction temperature,  $T_a$  = Ambient temperature and  $P_d$  = Power dissipation.

For the purpose of maintaining adequate junction temperature, 36 balls in the center of the BGA package have been allocated for thermal relief. Each of these is connected electrically to VSSDIG, allowing the use of PCB ground planes to transfer heat away from the BGA package. When utilized properly, these thermal balls provide the necessary junction-to-ambient thermal resistance ( $\Theta_{ja}$ ), assuming an airflow of approximately 1m/s.

For proper cooling, a PCB via must be placed between the thermal BGA ball pads in a checkerboard pattern (see Figure 12: "Thermal Via Layout", below). Each of these "thermal vias" should then be routed to the BGA ball pads near it with a wide trace or solid copper fill to increase the conductive area on the surface of the PCB. In order to dissipate heat below the BGA package, the PCB thermal vias must connect to a minimum of two solid ground planes within the board. It is recommended that each ground plane have a minimum thickness of two ounces (see Figure 13: "Thermal Ground Plane Connections", below).

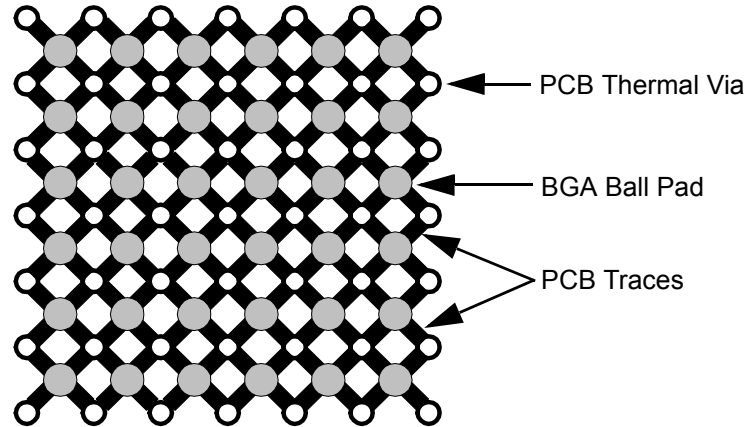


Figure 12: Thermal Via Layout

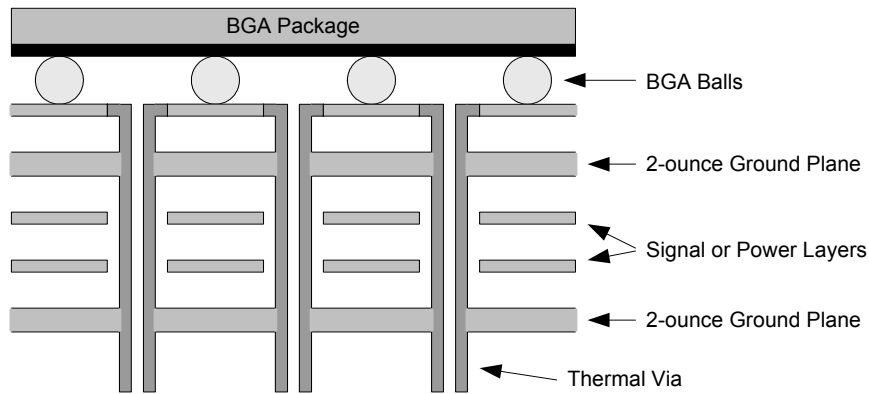


Figure 13: Thermal Ground Plane Connections

When connecting these thermal vias to ground planes, it is advisable not to use thermal-relief connection traces, as these are designed to prevent the flow of heat through the PCB. Instead, the thermal via should have a solid connection to the traces and planes on each layer (see Figure 14: "PCB Vias", below).

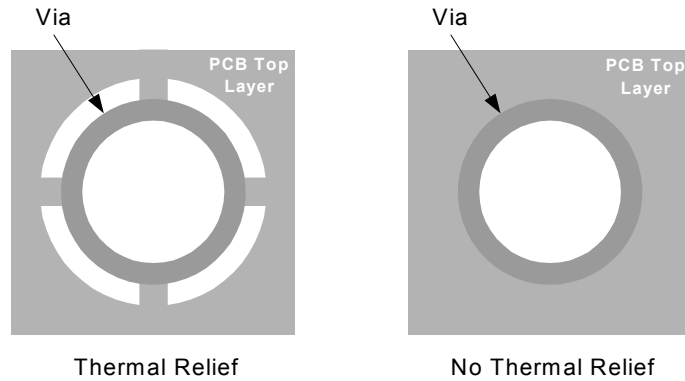


Figure 14: PCB Vias

### Voltage Reference Pins Circuit

For proper operation, the VSC8204 must generate an on-chip reference voltage of 1.65 volts with a tolerance of +/- 5% at the REF\_FILT pin. For this, the following components are required for each VSC8204 in the system:

- 2.26kΩ reference resistor, 1% tolerance, 1/16 watt.
- Two 1uF capacitors, with 10% tolerance or better. NPO, X7R or X5R ceramic materials are all acceptable.

### PCB Layout of Voltage Reference Pins Circuit

For best performance, special considerations for the ground connection of the voltage reference circuit are necessary to prevent bus drops which would cause inaccuracy in the reference voltage. This applies to the following elements:

- Ground connection of the 2.26kΩ reference resistor
- Ground connection of the two 1uF capacitors
- VREFN signal

These ground connections should each be connected to a shared PCB signal trace, rather than being connected individually to a common ground plane. This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitors and resistor should be placed as close as possible to the VSC8204. (see Figure 15: "Voltage Reference Schematic", below)

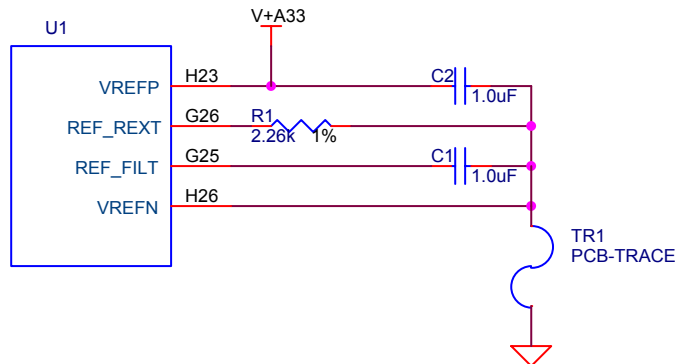


Figure 15: Voltage Reference Schematic

**Document History & Notices**

Revision Number	Date	Description
1.6	04 Oct 04	Changed CIS8204 to VSC8204 globally. Integrated the information from the CIS8204 RGMII Interface Appnote into this document.

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