Application Note 133

Interfacing Fast Ethernet Transceivers to MAC Processors

KS8721 / KS8001 Products

Introduction

The ubiquitous Fast Ethernet Transceiver is found in nearly all applications requiring network connectivity. These applications include consumer products, such as PC printers and wireless access points; test equipments, such as digital storage oscilloscopes and logic analyzers; industrial applications, such as surveillance cameras and process control/ monitoring devices; gaming devices; media converters; and just about anywhere an Ethernet port connection is needed for data communication, device configuration, or diagnostic purposes.

Micrel Fast Ethernet Transceivers interface and interoperate seamlessly with microprocessors and micro-controllers with integrated Fast Ethernet MAC (Media Access Control) units. These include successful designs with Intel's IXP4XX Family of Network Processors and Freescale's PowerQUICC™ Family of Network & Communications Processors and ColdFire ® Embedded Controllers.

This application note shows how to interface the Micrel KS8721 and KS8001 Families of Fast Ethernet Transceivers to MAC processors and controllers with integrated Fast Ethernet MAC units. A brief introduction of the MII / RMII / SMII data bus interfaces and the MIIM management bus components is provided along with pertinent hardware pin description and configuration information for Micrel's KS8721 and KS8001 products. Examples of PHY-MAC interfaces follow to illustrate how these three modes of MII operation and the management options are implemented in typical PHY-MAC applications.

PHY-MAC Interface

The PHY-MAC interface is comprised of two signal groups: a data bus interface and a management interface option that includes strap-in pins to configure the PHY address and an interrupt signal to alert the MAC processor of status change at the physical layer.

Data Bus Interface

Micrel's KS8721 and KS8001 Fast Ethernet Transceivers support Media Independent Interface (MII) and Reduced Media Independent Interface (RMII) for data transfer with external MAC processors. Additionally, the KS8001 products support the single data bit, Serial Media Independent Interface (SMII).

Fast Ethernet MAC processors are commonly integrated with Fast Ethernet MACs that support either MII or RMII. SMII is rarely found on Fast Ethernet MAC processors, and is mostly used for interfacing with MAC designs that use FPGAs, where I/O pin availability is limited.

MII Interface

The Media Independent Interface (MII) is specified in clause 22 of the IEEE 802.3 standard. MII consists of a nibble wide data bus and a management bus (MIIM). MIIM is discussed later in this application note.

Micrel's KS8721 and KS8001 products are configured by default, using internal pin strap-in setting(s), to MII mode after power-up. See 'Strapping Options' table of respective device's datasheet.

The MII interface contains distinct groups of signals for data transmission and data reception. Additionally, on the transmit side, TXEN indicates when data is sent by the MAC and TXER indicates if errors have occurred during transmission. Similarly, the receive side uses RXDV to convey when the data is valid, and RXER to signal if physical layer errors are detected. For half duplex operation, COL indicates if collisions have occurred during transmission, and CRS signals the presence of data transmission and/or data reception.

The following table describes the signals used by the MII data bus.

MII Signal Name	MII Signal Description	Direction (with respect to the PHY)	Direction (with respect to the MAC)	KS8721 / KS8001 MII Signal Name (direction, pin number)
RX_CLK	Receive Clock	Output	Input	RXC (output, 10)
RX_DV	Receive Data Valid	Output	Input	RXDV (output, 9)
RXD3	Receive Data Bit 3	Output	Input	RXD3 (output, 3)
RXD2	Receive Data Bit 2	Output	Input	RXD2 (output, 4)
RXD1	Receive Data Bit 1	Output	Input	RXD1 (output, 5)
RXD0	Receive Data Bit 0	Output	Input	RXD0 (output, 6)
RX_ER	Receive Error	Output	Input	RXER (output, 11)
TX_CLK	Transmit Clock	Output	Input	TXC (output, 15)
TX_EN	Transmit Enable	Input	Output	TXEN (input, 16)
TXD3	Transmit Data Bit 3	Input	Output	TXD3 (input, 20)
TXD2	Transmit Data Bit 2	Input	Output	TXD2 (input, 19)
TXD1	Transmit Data Bit 1	Input	Output	TXD1 (input, 18)
TXD0	Transmit Data Bit 0	Input	Output	TXD0 (input, 17)
TX_ER	Transmit Coding Error	Input	Output	TXER (input, 14) **[Tie TXER pin to ground if MAC does not transmit error]**
COL	Collision Detected	Output	Input	COL (output, 21)
CRS	Carrier Sense	Output	Input	CRS (output, 22)

RMII Interface

The Reduced Media Independent Interface (RMII) is defined by the RMII Specification version 1.2 and provides a lower pin count Media Independent Interface (MII), where the width of transmit and receive data buses are reduced from a nibble (4-bits) down to a di-bit (2-bits).

RMII mode is supported by Micrel's KS8721 and KS8001 products and is enabled after power-up with the following hardware settings:

- Connect a 50 MHz clock source to the REFCLK input (pin 15). This 50 MHz clock is also used by the MAC side and is provided by either the system board or MAC processor.
- Tie XI (pin 46) high and put XO (pin 45) as a no connect. The 25 MHz crystal/oscillator is not used in RMII mode.
- Tie strap-in selection RMII_SELECT (pin 21) high to enable RMII mode.

The RMII interface, like the MII interface, uses distinct groups of signals for data transmission and data reception. For RMII, the 50 MHz reference clock replaces the 25 MHz transmit and receive clocks in MII, and allows the width of the transmit and receive data buses to be cut in half. Furthermore, carrier sense and receive data valid is combined as one signal, CRS_DV. And collision detection is now regenerated on the MAC side by ANDing TX_EN and carrier sense that is recovered from the CRS_DV signal.

The following table describes the signals used by the RMII interface.

RMII Signal Name	RMII Signal Description	Direction (with respect to the PHY)	Direction (with respect to the MAC)	KS8721 / KS8001 RMII Signal Name (direction, pin number)
REF_CLK	50 MHz clock reference for receive, transmit and control interface	Input	Input (System Clock) or Output	REFCLK (input, 15)
CRS_DV	Carrier Sense/ Receive Data Valid	Output	Input	CRSDV (output, 9)
RXD1	Receive Data Bit 1	Output	Input	RXD1 (output, 5)
RXD0	Receive Data Bit 0	Output	Input	RXD0 (output, 6)
RX_ER	Receive Error	Output	Input **[Not required, MAC option]**	RXER (output, 11)
TX_EN	Transmit Enable	Input	Output	TXEN (input, 16)
TXD1	Transmit Data Bit 1	Input	Output	TXD1 (input, 18)
TXD0	Transmit Data Bit 0	Input	Output	TXD0 (input, 17)

SMII Interface

The Serial Media Independent Interface (SMII) provides the lowest pin count Media Independent Interface (MII). For SMII, the PHY-MAC interface comprises of a total of four pins.

SMII mode is supported by Micrel's KS8001 products and is enabled after power-up with the following hardware settings:

- Connect a 125 MHz clock source to the CLOCK input (pin 15). This 125 MHz clock is also used by the MAC side and is provided by the system board.
- Tie XI (pin 46) high and put XO (pin 45) as a no connect. The 25 MHz crystal/oscillator is not used in SMII mode.
- Tie strap-in selection SMII_SELECT (pin 10) high to enable SMII mode.

The SMII interface uses a 125 MHz reference clock. A 12.5 MHz SYNC signal is generated by the MAC side from the 125 MHz clock. Single data-bits are used to convey data and control information for transmit and receive directions. More details on the SMII interface is provided in the KS8001 Datasheet.

The following table describes the signals used by the SMII interface.

SMII Signal Name	SMII Signal Description	Direction (with respect to the PHY)	Direction (with respect to the MAC)	KS8001 SMII Signal Name (direction, pin number)
CLOCK	125 MHz clock reference for receive / transmit data and control	Input (System Clock)	Input (System Clock)	CLOCK (input, 15)
SYNC	12.5 MHz Synchronization Signal	Input	Output	SYNC (input, 18)
RX	Receive Data and Control	Output	Input	RX (output, 6)
TX	Transmit Data and Control	Input	Output	TX (input, 17)

Management Bus Interface

Micrel's KS8721 and KS8001 Fast Ethernet Transceivers have the option to be managed by a MAC processor or micro-controller. The supported management components include a MIIM interface, configurable PHY addresses, and an interrupt signal. All of which are available in MII, RMII and SMII modes.

MIIM Interface

The Media Independent Interface Management (MIIM) bus is defined in clause 22 of the IEEE 802.3 specification. It allows an external MAC processor or micro-controller to monitor the status and manage the states of the PHY transceiver, and is comprised of the following:

- A physical connection that includes a bi-directional data line (MDIO) and the clock line (MDC) that is sourced from the MAC side
- Access to standard MIIM PHY registers and customized PHY registers
- A management protocol that abides to the following frame format

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	AAAAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	AAAAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

Some MAC processors have built-in MIIM hardware modules and dedicated hardware pins to interface directly with PHY transceivers' MIIM bus. For those MAC processors or micro-controllers without the MIIM bus interface, GPIO (General Purpose Input/Output) pins can be used to emulate the MIIM bus interface.

Micrel's KS8721 and KS8001 products have very loose timing on the MIIM bus. The MDC clock input can operate at any clock speed up to a maximum of 5 MHz. This help to facilitate the use of GPIO pins for PHY register management.

PHY Address Configuration

The PHY address is used by the MAC processor or micro-controller to select the PHY transceiver it wants to manage. This allows for two or more PHY transceivers to share a common MIIM bus interface.

Micrel's KS8721 and KS8001 products have PHY addresses that can be configurable to any value from 1 to 31 (0x01 to 0x1f). The PHY address is formed by concatenating strap-in pins (6:3, 25) to produce PHYAD[4:0]. This 5-bit address is latched at power-up and hardware reset, and has a default value of 0x01 that can be overridden by placing external pull-ups and pull-downs on the respective strap-in pins.

Note, strap-in pins (6:3, 25) are also used in MII, RMII and SMII modes as receive data output pins. It is critical that the MAC side does not drive these strap-in pins and override their settings during power-up and hardware reset.

Interrupt Pin

Micrel's KS8721 and KS8001 products output an interrupt signal, INT# (pin 25), to alert the processor that there has been a status change at the physical layer. An interrupt signal helps to save valuable processing time, eliminating the need for the processor to poll for status change. Upon receiving an interrupt, the processor should read PHY register 0x1B for the latest interrupt status. The interrupt status is automatically cleared after register 0x1B is read. This same register is also used to enable and disable the types of events that will trigger an interrupt. Refer to respective device's datasheet for details.

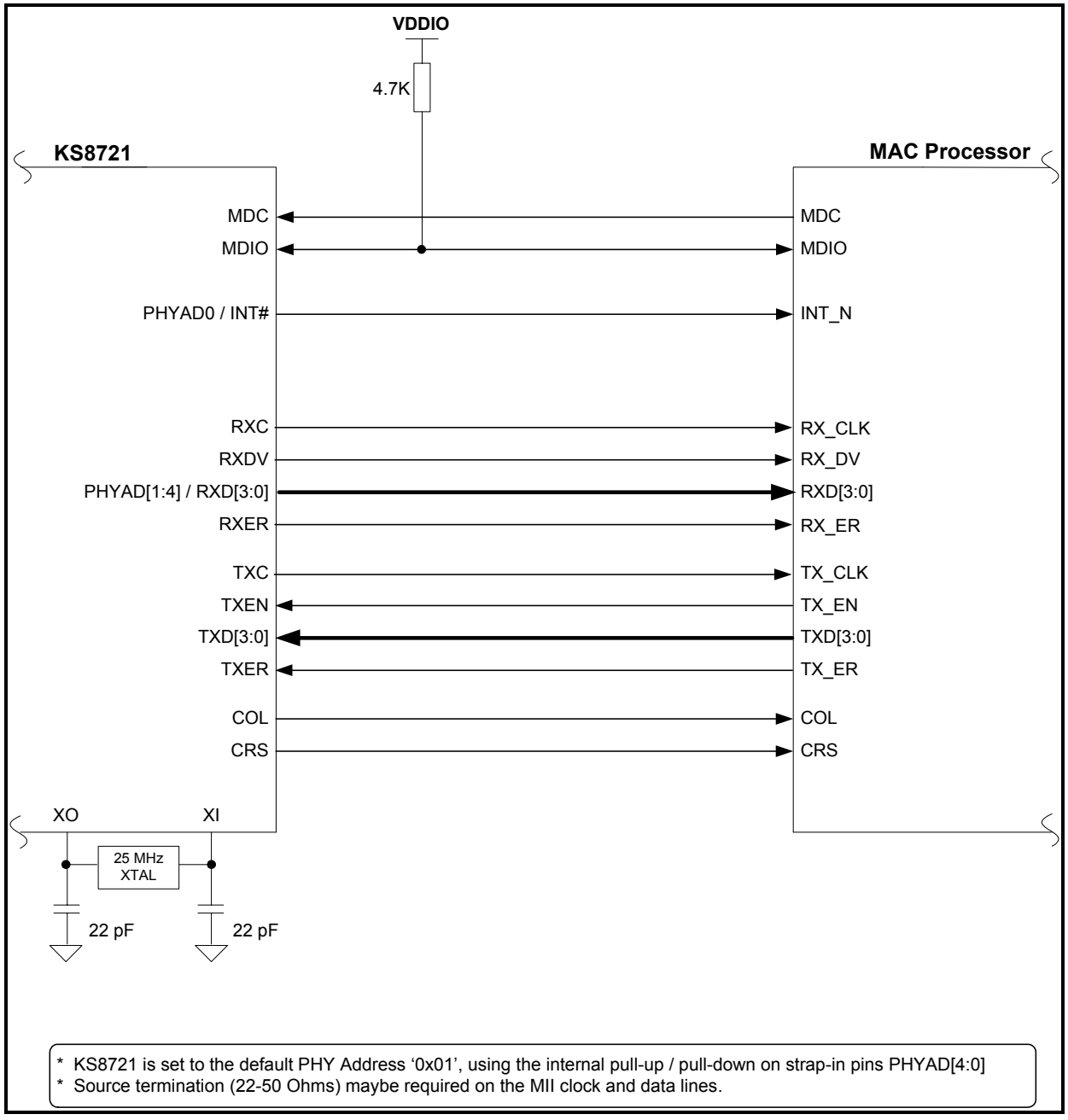
By default, the interrupt pin is active low. It can be programmed to be active high by writing a '1' to bit [9] of PHY register 0x1F.

The following table depicts the hardware pins used by Micrel's KS8721 and KS8001 products for MIIM bus management.

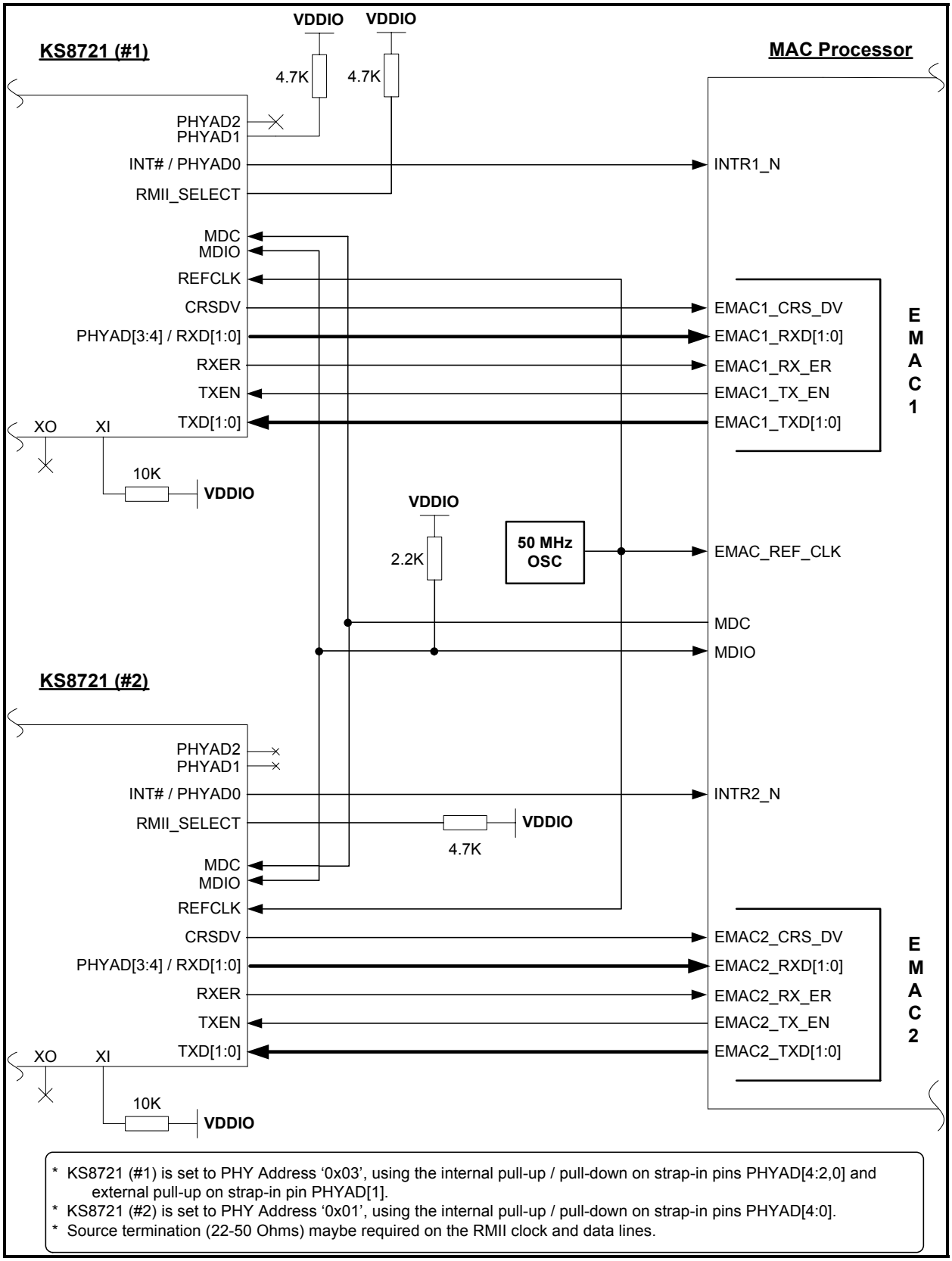
	Pin Number	Pin Type	Pin Name	Pin Description
PHY Address				
PHYAD4	6	Ipd / O	RXD0/ RXD[0]/ RX/ PHYAD4	MII mode: Receive Data Bit 0 RMII mode: Receive Data Bit 0 SMII mode (KS8001 only): Receive Data and Control Configuration mode: The pull-up / pull-down value is latched as PHYAD4 during power-up and reset.
PHYAD3	5	Ipd / O	RXD1/ RXD[1]/ PHYAD3	MII mode: Receive Data Bit 1 RMII mode: Receive Data Bit 1 Configuration mode: The pull-up / pull-down value is latched as PHYAD3 during power-up and reset.
PHYAD2	4	Ipd / O	RXD2/ PHYAD2	MII mode: Receive Data Bit 2 Configuration mode: The pull-up / pull-down value is latched as PHYAD2 during power-up and reset.
PHYAD1	3	Ipd / O	RXD3/ PHYAD1	MII mode: Receive Data Bit 2 Configuration mode: The pull-up / pull-down value is latched as PHYAD1 during power-up and reset.
PHYAD0	25	Ipu / O	INT#/ PHYAD0	Interrupt Pin Output (active low) Configuration mode: The pull-up / pull-down value is latched as PHYAD0 during power-up and reset.
MIIM Interface				
MDC	2	I	MDC	MII Management Clock Input (This pin is synchronous to the MDIO signal.)
MDIO	1	I / O	MDIO	MII Management Data Input / Output (If use, this pin requires a 4.7K external pull-up to VDDIO.)
Interrupt Pin				
INT#	25	Ipu / O	INT#/ PHYAD0	Interrupt Pin Output (active low) Configuration mode: The pull-up / pull-down value is latched as PHYAD0 during power-up and reset.

Examples

MII Example - Micrel KS8721 PHY interfacing with a MAC processor via MII interface

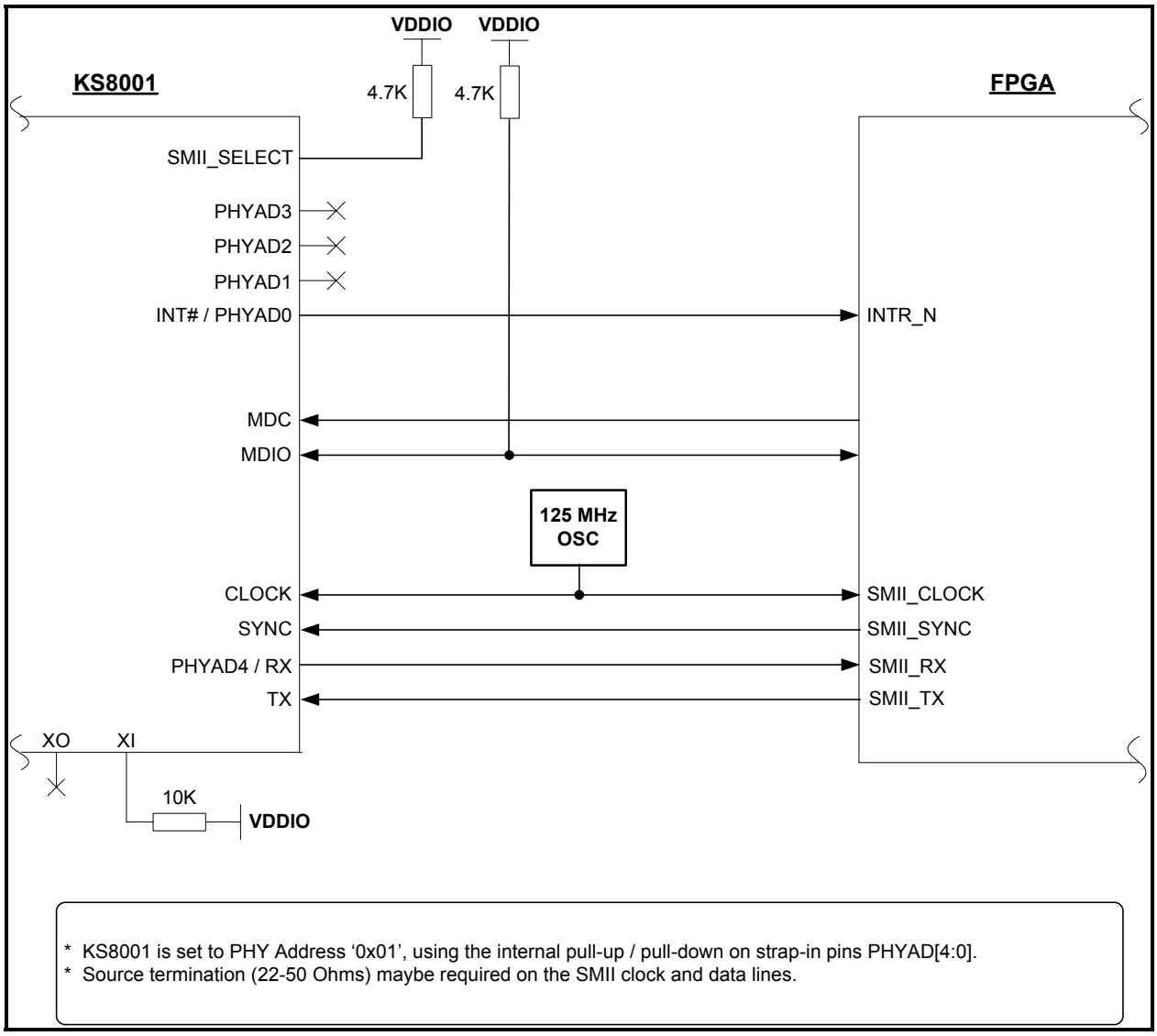


RMII Example - Two Micrel KS8721 PHYs interfacing with a MAC processor via dual RMII interfaces



* KS8721 (#1) is set to PHY Address '0x03', using the internal pull-up / pull-down on strap-in pins PHYAD[4:2,0] and external pull-up on strap-in pin PHYAD[1].
* KS8721 (#2) is set to PHY Address '0x01', using the internal pull-up / pull-down on strap-in pins PHYAD[4:0].
* Source termination (22-50 Ohms) maybe required on the RMII clock and data lines.

SMII Example - Micrel KS8001 PHY interfacing with a FPGA chip via SMII interface



Conclusion

Micrel Fast Ethernet Transceivers provide network connectivity to any device or product that incorporates a Fast Ethernet MAC processor or controller. Whether the network support is for data communication, web page device configuration for embedded systems, or diagnostic and management purposes, Micrel Fast Ethernet Transceivers are easy to implement in a new or existing design. The integration process can be summed up in the following steps:

- Use this application note to select from the MII, RMII and SMII data bus interfaces and MIIM management options available, and assist with the PHY-MAC interface connection with the MAC processor or controller.
- Follow the selected Micrel Fast Ethernet Transceiver's reference schematic for the analog front end connections.
- Modify software for MIIM management. If MIIM management is not used, no software development is required.

Micrel offers a diverse portfolio of Fast Ethernet Transceivers in various combination of package size, supply voltage and features in both commercial and industrial temperature range. Visit Micrel's website at http://www.micrel.com or contact your local Micrel FAE or Sales Representative for product availability.

MICREL, INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http:/www.micrel.com

The information furnished by Micrel in this data sheet is believed to be accurate and reliable. However, no responsibility is assumed by Micrel for its use. Micrel reserves the right to change circuitry and specifications at any time without notification to the customer.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is a Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2005 Micrel, Incorporated.