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Update

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Technical Update – Comparison of Ceramic and Tantalum Capacitors[i]

BASIC DIFFERENCES

Ceramic capacitors have a multitude of dielectric types available and each of these types is characterized by their sensitivities to temperature, but not to voltage or time. This paper compares the X7R, X6S, or X5R dielectric types of ceramic capacitors with tantalum capacitors. Ceramic capacitors constructed with these dielectrics offer moderate dielectric constants with moderate temperature and voltage sensitivities. They overlap with tantalum capacitors in capacitance/voltage range offerings. In many cases, the solder pad geometry allows swapping of ceramic 0603, 0805, 1206 or 1210 chip sizes with "J," "R," "A," or "B" case tantalums, respectively.

Among the more rudimentary differences between ceramic and tantalum capacitor types are factors of polarity, temperature, DC bias effect, AC signal level effects, and frequency response with the parasitic contributions within each.[ii]

There are significant differences in construction between multilayer ceramic (MLC) and tantalum capacitors. The ceramic MLC chip is a ceramic block with end metallizations applied to the opposing end termination faces (T1 & T2). This creates wrap-around metal pads on the adjacent faces, and these pads are soldered directly to the printed wire board (PWB) along the bottom of the chip. The active element of the tantalum capacitor is a metal-dominated structure that is encased in plastic, with leadframes extending out from the plastic to allow a leadframe wrap-under (T1 & T2), which creates metal pads along the bottom of the package to facilitate the soldering to the PWB. Plastic encapsulation and protruding metal leadframes act to protect the active tantalum capacitor elements during mounting to the PWB, and from environmental exposure during operation. However, the plastic encapsulation limits the maximum temperature of soldering due to thermal degradation and mismatch of coefficient of thermal expansion (CTE) between the plastic and the active capacitor element. The additional leadframe required with this package leads to higher inductive parasitics for tantalum capacitors as compared to ceramic capacitors.

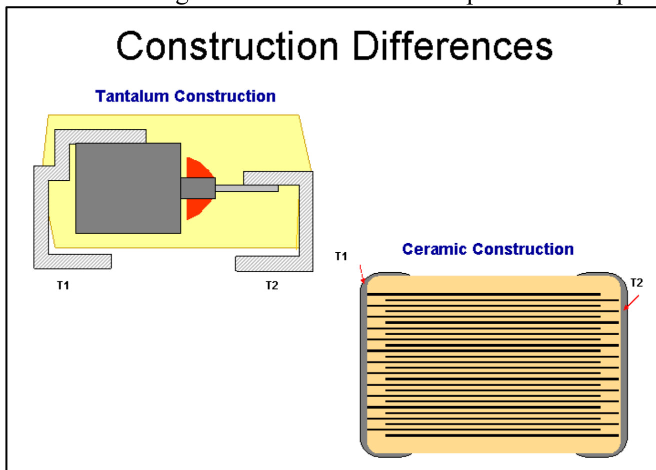

Figure 1. Tantalum and ceramic chip structures.

From the perspective of mechanical properties, the packaging differences that electrically favored the ceramic now favor the tantalum after the chip is soldered to the PWB. Because the ceramic is rigidly fixed to the PWB with the solder attachment, any mechanical stresses created in the PWB (flex, stretch, shock, and vibration) are now transferred directly to the ceramic body. These ceramic materials have enormous compressive capability, but have little tensile capability. The shear forces generated can lead to cracking of the ceramic structure, which leads to capacitor failures (short circuits). The leadframe of the tantalum chip allows mechanical isolation of the tantalum structure within the plastic encapsulate from the PWB.

Shared Elements

Ceramic	Tantalum
1. Temperature Coeff. of Capacitance	
2. Fail-short	
3. Parasitics (ESR/ESL)	
4. Power Derating	
5. Concerns with Lead-Free	
6. Volumetric efficiency	

Table 1. Shared elements between these two types.

NEARLY-SHARED ELEMENTS

In comparing these types of capacitors, it would be instructive to compare common elements as well as the distinctive elements of each. Table 1 contains a list of shared elements for these capacitors, which have nearly common performance characteristics. Shared performance characteristics include similar temperature coefficients, fail-short, power restrictions, voltage restrictions, parasitics of equivalent series resistance (ESR) and equivalent series inductance (ESL),

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power derating, and concerns with lead-free solder applications.

1. Temperature Coefficient of Capacitance (TCC)

The allowable change in capacitance for two of the ceramic dielectrics and for tantalum within their temperature ranges are all within a ±15% window. The X7R and X5R maintain this capability from -55°C through 125°C and 85°C, respectively. The X6S dielectric ceramic maintains capacitance within a ±22% window from -55°C through 105°C. These changes are all with respect to the near room ambient or 25°C reference.

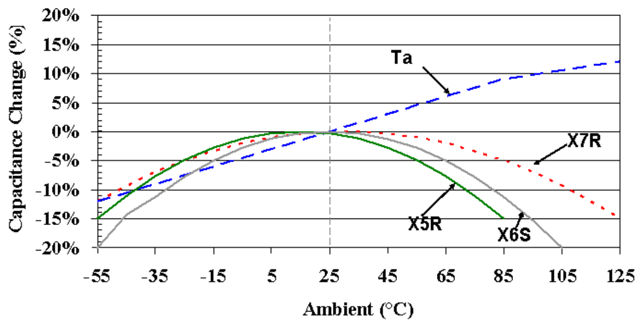

Figure 2. Capacitance change versus temperature.

Figure 2 shows the typical capacitance versus temperature responses of the three subject dielectrics and the tantalum's capacitance with temperature. The changes are all very similar in the low temperatures, but tantalum shows the only positive characteristics in the upper temperatures. For filtering applications, they are very similar, as deviations within ±20% will have little impact on circuit. For power supplies that are always in the temperature range above 25°C, the higher capacitance from the tantalum could result in lowered impedance and improved performance. Viewing these same considerations for decoupling of hot microprocessors or decoupling applications, the higher capacitance at elevated temperatures makes the tantalum response more desirable.

For both of these types of capacitors, the ESR typically has a negative temperature coefficient of resistance (TCR) – as temperature increases, the ESR decreases. Though this is a common feature, the new tantalum-polymer devices have a reduced effect negative TCR, with the high temperature ESR being very close to that of the 25°C ESR.

2. Fail-short

As with most capacitor types, the main failure mode of these capacitors is a dielectric failure resulting in a potential "short-circuit." There may be prejudice to the effect that the tantalum failures are more critical, but most of this bias is created by historical difference in applications. It is only with recent developments in expanded capacitance capability for surface-mount ceramic chips that exposure to high-power filter circuitry has been enabled for the MLCC device. Tantalum capacitors have a propensity to ignition failures (MnO_2 cathode system), but this will be covered in a later section.

Once the device is in a high-power, low-impedance circuit, concerns for excessive DC currents that can create a thermal hot spot must be addressed with some regulation circuitry or fuse. The difficulty of using many devices in parallel (normally required for high power) is that the normal circuit operational current exceeds the burn activation of any single element. A single fuse rated above the operational current will never detect the failure. Adding fuses in series with each element is too costly and degrades the performance of a capacitor by adding ESR and ESL. There are tantalum surface-mount devices that contain an internal fuse to enable the protection with minimal increase in ESR and negligible increase in ESL. There have been no commercially acceptable 'fused' ceramic capacitors, to date.

3. Parasitic ESR and ESL

Both of these capacitors contain parasitic ESR and ESL. The initial package geometries, being very similar in size and utilizing the same solder pad geometries, have very similar ESL values between 2 and 1 nH. In the case of the MLC (multilayer ceramic) however, there are opportunities for changing the aspect ratio of length and width to create much lower ESL values. This is highlighted by the 0612 chip having less than half the ESL of a 1206 chip (600 pH). This is demonstrated further with the multiterminal, interdigitated ceramic chip offerings that move the ESL well below 100 pH.

The tantalum ESL has recently been reduced using face-down terminations, minimizing the loop area and bringing down the ESL to less than 200 pH.

The ESR of MLC capacitors is typically lower than that of similar value tantalum. The ratio of this parasitic is typically 1:100. Using conductive polymers in place of the traditional MnO_2 cathode system has allowed this ratio to be diminished to less then 1:10 and, in some cases, approaching unity. More information will be revealed on these parasitics later on.

4. Power derating

Arbitrarily assigned power ratings for tantalum and MLC are based on an acceptable temperature rise. Typically, this rise is given as 20°C rise over ambient. Using the thermal resistivity of the device, the power rating in watts is then established. As the ambient temperature approaches the maximum temperature rating of the device, the allowable rise must be reduced, approaching zero at the extreme. The rise is arbitrary, but the maximum temperature is an absolute with a measurement tolerance of +2°C, -0°C applied. Regardless of the rise selected, the internal temperature (ambient plus rise) cannot surpass the maximum by more than the maximum tolerance of 2°C.

5. Concerns with lead-free solder processes

The move to lead-free solder processes results in higher temperatures and longer heat durations. Ceramics are mini-

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mally affected by peak temperatures, but temperature transitions must be carefully controlled. Ceramic is a poor thermal conductor and fast transitions can create thermal gradients within the part, resulting in differential forces which may lead to thermal cracks.

Plastic encapsulated tantalum capacitors are affected not only by the peak temperature, but also by the duration above the glass transition point in the thermal profiles. The plastic surrounding the metal structure expands faster than the metal. At the glass transition point, the plastic takes on an even higher CTE, and the rate of mismatch becomes greater. The expansion while heating creates little impact, but contraction during the cooling creates potentials for large unbalanced forces acting on the pellet structure, especially if the package has to fit back together after separating. These forces can create isolated stress points to initiate new defect sites. These may also stress areas with faults that were above the stress levels of the rated voltage, to the point where they now become susceptible to stress levels below rated voltage. Clearing these faults is possible with a "proofing" method, but once the device is mounted in the circuit, the other circuit elements could prevent this method from being effective.[iii]

6. Volumetric efficiency

Ten years ago, the volumetric efficiency ratio of tantalum to ceramic was close to 100:1 when comparing capacitors of the same size. Today that ratio has dropped to nearly 2:1 with the 'B' case 470-uF tantalum chip compared to the 220-uF 1210 ceramic chip.

Volume utilization is more efficient in the larger tantalum chip sizes because so much volume is wasted with packaging walls, the riser wire and the leadframe attachments in the smaller chips. Changing the design of these smaller packages to a "facedown" termination design increases the volumetric efficiency by nearly 100%. Along with this increase in efficiency, a reduction in ESL is realized.

The new facedown termination designs for tantalum capacitors specifically targeting lower ESL, can more than double the volumetric capability. This approach will become more prevalent as manufacturing volumes increase.

Ceramic capacitors have made enormous strides in increased capacitance capability by utilizing thinner dielectric layers (increasing the capacitance per layer) and, with additional layers, more can fit into a given height. This layer count increase at an acceptable cost was achievable only with BME (base metal electrodes of nickel or copper) systems replacing the previous precious-metal-based systems (platinum, palladium, silver, or mixtures of these). Layer counts approaching 1000 are achievable, and though the material costs have been greatly reduced with the BME transition, the time to build these high layer counts has increased tremendously.

The next large gain for ceramic capacitors may require abandoning the current thick film MLC process and converting to a thin film process. Costs associated with achieving the high layer counts via thin-film technology make this technique cost prohibitive at this time.

Unique Elements

Tantalum
1. Polar
2. Ignition Failures
3. Temperature/Application derating
4. RC-Ladder
5. Higher leakage

Table 2. Unique elements for tantalum capacitors.

TANTALUM DIFFERNCES HIGHLIGHTED

There are some very distinguishable differences between ceramic and tantalum capacitors, due to differences in materials, dielectric creation, method of manufacturing, and design. A listing of these differences is highlighted in Table 2. The discussion will focus first on the characteristics unique to tantalum capacitors.

1. Tantalum – a Polar Capacitor

Though both ceramic and tantalum capacitors are electrostatic capacitors (charge accumulation and field enhancement takes place with no chemical transition), the tantalum is in a class of electrolytic capacitors. This does not define a wet electrolyte as existing in the capacitor, but defines the formation of the dielectric by means of a wet electrolyte, through electro-chemical action on the valve metal (Ta).

The dielectric is an oxide of the base metal. In this case, Ta_2O_5 is the desired oxide created from the tantalum metal. Because there is a DC field applied to grow the oxide, the applied field of this capacitor must be polarized in the same manner as the formation voltage. Referring back to Figure 1, T1 is the cathode connection for the tantalum capacitor, and T2 is the anode connection.

Voltage applied to this device in application must always create a positive voltage at the anode, and negative at the cathode. Reverse voltage application of any level was initially declared as damaging to this component, to the point where capacitance measurements (an AC signal) were to be combined with a 2VDC bias to assure no reverse pulses were applied to the capacitor. We no longer use a DC bias in measuring these devices and we now believe that even in the reverse mode, a specific voltage level must first be achieved before the degradation of the device begins (approximately 15% of rated at 25°C).[iv] Exceeding this voltage degrades the dielectric and eventually the capacitor will fail.

2. Tantalum – Ignition Failures

This failure mode is most likely the one element that has brought more concern about tantalum applications than any other has. It is a true exothermic reaction, in which more energy is produced at the fault site than is delivered to that site. With the cathode material as MnO_2, this compound brings a

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high level of oxygen into the assembly. When a fault occurs and the tantalum metal becomes hot, the release of oxygen from this material allows a rapid oxidation of the tantalum to occur, with energy generated and released as heat.[v]

There is an attempt to eliminate this failure mechanism in the industry. By utilizing a conductive polymer in place of the MnO_2 cathode system, the oxygen is dramatically reduced to the point where ignition does not occur. Failures still result in short-circuits and high enough current can create thermal hot spots and smoke. Internal fusing of these devices is being proposed to eliminate smoke.

Switching the tantalum to niobium or niobium oxide and continuing the use of MnO_2 does not eliminate the potential for ignition. If these devices fail in a high-current environment (>10 amperes) there is still a potential for the very noticeable ignition failure.

3. Temperature/Application Voltage Derating

As previously stated, the temperature range of the tantalum capacitor is -55°C to 125°C. The voltage rating of the part is the same as the nameplate voltage up through 85°C, but from this temperature up to 125°C, there is a linear depletion of the voltage rating from 100%v at 85°C to 67% at 125°C. This derating method was instituted as the result of extensive, accelerated life testing, and it is applied exclusively to tantalum capacitors.

Additionally, hidden in many manufacturers' catalogs is a recommended application derating of the tantalum capacitor to 50% of the voltage rating (remember that the voltage rating is also diminished at temperatures above 85°C). This factor is a result of the stresses created on the device because of the mismatched CTEs and the solder profile for reflow solder attachment. The 100% electrical testing of the components prior to packaging does not assure that the devices will pass the same regimen after the solder attachment. By reducing the voltage applied afterwards, there is little likelihood of creating faults below this level.

This recommendation is slightly reduced for the polymer cathode and the niobium-oxide devices. With the polymer replacing the MnO_2, a soft elastic material replaces a hard brittle material. We have noticed an appreciable reduction in power-on failures, as we believe that the internal structure is less likely to transmit stresses with the polymer.[4] For the tantalum-polymer devices rated at or below 10 VDC, the recommended derating is 10% (use at 90% of rated), and for higher voltages, the derating is 20% (use at 80% of rated). For the niobium-oxide, the dielectric is formed to a significantly thicker range than the comparable tantalum dielectric. This allows a safer design, and fewer chances for creating failures close to the rated voltage of the device.

4. RC-Ladder Effects

The structure of the tantalum capacitor involves a pellet structure of porous tantalum metal, whereby the contact to the capacitor elements at the center of the pellet are through the penetrating cathode materials. This creates a distribution of resistances in that there is low resistance to capacitive elements near the pellet surface, and high resistance to those elements in the center (the RC-Ladder). As such, with increasing frequency, and an unequal resistance to the distributed capacitor elements, a loss of capacitance is associated with increasing frequency.

There are devices that attempt to circumvent this effect in that the depth to the center is reduced (multiple anodes and "fluted" anodes). By changing from the MnO_2 to the conductive polymer, the resistance in the paths is reduced, allowing the capacitance roll-off to be moved to a higher frequency range.

5. Higher leakage

The core of the tantalum capacitor has an enormous volumetric efficiency. Using this core in smaller case sizes reduces the efficiency, as the core becomes a smaller percentage of the volume of the plastic. Consider the tantalum 'B' case chip of nearly the same size as the ceramic 1210 chip. Only about 15% of the volume is taken up by the capacitive element. Yet looking at capacitance capability that is three times that of the ceramic, and considering that the dielectric constant is $1/100^{th}$ that of the ceramic, the difference in these two devices is overcome with thinner dielectric and higher surface area. Both of these increases will create higher leakages. Typical leakage for a 100 uF, 6.3 VDC rated tantalum-MnO_2 is 6.0 uA, compared to 60 uA for the tantalum-polymer. This difference is related to the healing activated by the cathode element and, as it turns out, the higher resistive element (the MnO_2) is more efficient at removing leakage sites within the pellet structure.[4] A ceramic capacitor of the same capacitance and voltage would have an equivalent leakage of 6.0 nA.

CERAMIC DIFFERENCES HIGHLIGHTED

Table 3 lists the unique attributes of ceramic chip capacitors. Among these, aging and piezoelectric effects may not be as well known as the voltage coefficients and flex cracks.

Unique Elements

Ceramic
1. Aging
2. Voltage Coeff.
3. Piezoelectric noise
4. Flex Cracks

Table 3. Unique elements for ceramic capacitors.

1. Aging

The crystalline structure of the Ba_2TiO_3-based ceramic changes dimensionally with time. After firing, the majority of the structures are in a cubic symmetrical arrangement and, with time, there is an evolution to tetragonal with a degree of

strain. With this transition, there is a loss of capacitance. For every tenfold time change, there is a consistent percentage of capacitance loss, which appears as a percentage per decade-hours. Typically, for these three dielectrics, the change will be between 1.5% and 3.5% per decade-hours for the moderate dielectrics (X7R, X5R), and from 4% to 10% per decade-hours for the high-K dielectrics (Y5V, Z5U).

This decay in capacitance can be recovered by heating the capacitor up past its Curie point (approximately 135°C or higher). By doing so, the crystalline structure reverts to the post-firing structure, and the capacitance is recovered. This increase in some cases has caused customers to send back devices that measure high and out of tolerance, but are measured too soon after soldering. This "out of tolerance" appearance will soon disappear with time (24 hours is usually long enough).

Ceramic capacitors should not be used in timing circuits as this capacitance change can upset even a moderate tolerance period. This change in capacitance may not be significant enough to prohibit use in delay circuits used to sequence timed activation at power-on.

2. Voltage coefficient

We might look at the dielectric constant in capacitors as a figure defining a relative ability to enhance the electric field that exists between the two plate charges. With dielectric constants as high as 3,000 (for these specific dielectrics), there is a great dependence on the dielectric for the capacitance capability of these devices. These constants are susceptible to temperature, as we have seen earlier, and to field magnitude or voltage strain. As such, the capacitance may appear to change with changing magnitudes of the AC voltage applied.

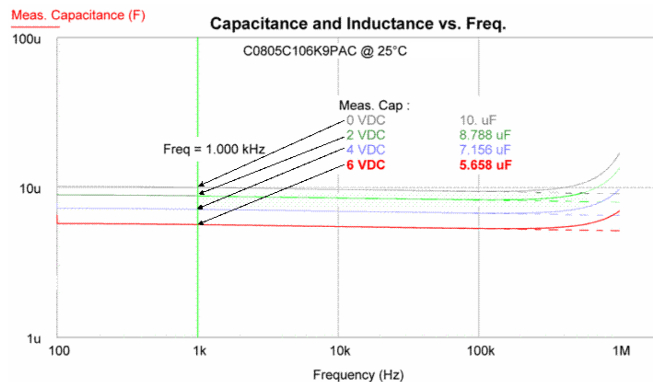

Figure 3. Capacitance vs. VDC vs. Frequency.

Consider the high-capacitance, lower-voltage offerings that are created today with hundreds of near 1-micron layers. To the benefit of the manufacturer, the capacitance verification is made at 120 Hz and at 0.5 VRMS. If the application is above 1 MHz and the signal magnitude is closer to 10 mV, then the apparent capacitance here is considerably less, because the field strength within the dielectric is so much lower.[vi]

Capacitance can also be depleted by applying a DC bias voltage. Figure 3 represents the capacitance versus frequency for an 0805 X5R ceramic capacitor rated at 6.3 VDC, with applied DC bias of 0, 2, 4, and 6VDC. The capacitance at 1 kHz is shown to decay from 10 uF to 8.8 uF at 2 VDC, 7.2 uF at 4 VDC, and 5.7 uF at 6 VDC.

These effects were rarely noticed with the thicker dielectrics available five and ten years ago, but are readily apparent with today's thinner dielectrics. Expanding the capacitance capability with thinner dielectrics will increase this voltage sensitivity.

3. Piezoelectric noise

The ceramic material is crystal based and has a potential for piezoelectric properties, though this applies only to Class II and Class III ceramics. The three dielectrics discussed in this article are within the Class II classification, and the piezoelectric effect either generates a mechanical displacement with electrical energy or generates electrical energy with mechanical displacement. In the case of the capacitor mechanically fixed to the board, any mechanical stresses created in the part by the board can generate unwanted electrical noise. This is especially important in high-gain amplifiers.

This property is most noticeable in the range of 30 Hz through 30 kHz, where these dielectrics appear to be most responsive. This range excludes these devices from being used in audio circuitry where the signal levels are high enough to trigger this effect. These capacitors are successfully used in front-end stages where the signal levels are small enough so they cannot create the mechanical displacement. In the back-end stages with higher signal levels, this displacement can create undesirable harmonic distortion.

In high-frequency applications, the body does not have enough time to displace itself mechanically, and these effects are greatly diminished. Care should be exercised when using a high-frequency supply with these capacitors on the output when the output is being pulsed in that audio frequency range where this property can be exercised. There have been cases reported where these capacitors have been responsible for emitting an audio tone because a cyclic test creates pulses in the audio range.

4. Flex cracks

Again, because the chip is mechanically tied to the PWB, the stresses from the board are transmitted directly into the chip. The most reported cause for failure of ceramic chips today is flex cracking.

The larger the capacitor chip, the greater propensity for cracking. The larger capacitor chips afford the largest capacitance. Replacing previous capacitor technologies usually requires the largest ceramic capacitance available. This creates a self-feeding cycle of failure.

There are modifications of the ceramic chip that increases its capabilities for withstanding the board flexure. These include but are not limited to fail-open, end-margin designs; fail-open, tear-away, polymer-layered terminations; and leadframes attached to the chips.

Lead-free solders that are more brittle or less malleable then the previous eutectic solders will make this failure mode more evident. The failures for a given board flexure will increase.

SUMMARY

Replacing one capacitor technology with another must be in consideration of fit, performance, availability, and cost. Of these four, cost will be the primary driver. There are capacitors of both types that are nearly identical in size and capacitance. Matches in capacitance, ESR, and ESL may have to be considered, and trade-offs among these might have to be made.

Performance requirements need to be met, as well as having available or multiple sources for whichever selection is chosen, but cost will ultimately be the main deciding factor. The cost element is too unpredictable to be included in this report, as conditions can change at any time. Table 4 is a summary of the comparisons discussed in this report.

	Ceramic	Tantalum
Similar	TCC Size Fail Short Lead-free concerns	
Advantage	1. ESL 2. Leakage 3. ESR	1. Voltage Stable 2. Mechanical
Disadvantage	1. VCC (AC & DC) 2. Piezoelectric 3. Flex Crack	1. Polar 2. Ignition 3. RC-Ladder 4. Temp. Derating

Table 4. Summary of comparisons (cost excluded).

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