–48-V ATCA Module Hot Swap Using the TPS2393

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ABSTRACT

The advanced telecommunication computing architecture (ATCA) PICMG 3.0 open standard has specific requirements for delivering dual –48-V power feeds to individual boards which may consume up to 200 W each. This application note describes a method for complying with the module hotswap requirements of the ATCA specification.

1   ATCA Power Requirements

ATCA contains many requirements which are typical of a modern, hotswapped power system. It also contains some requirements which are particular to ATCA. Among the most challenging are the transient ride-through specifications which mandate that boards continue operation through a 5-ms short on both inputs. Boards must also continue operation through a 10-μs, 100-V transient at the input. The requirements which this paper addresses are shown in Table 1.

Table 1. Selected ATCA Module Power Requirements

PARAMETER	MIN	MAX	UNITS	ATCA PARA	NOTES
Power distribution networks	2	2	–	4.1	2 Isolated feeds
Power plants	1	2	–	4.1	1 or 2 power plants
V operational	–43	–72	V	4.1.2.2	
$V_{IN(max)}$	0	–75	V	4.1.2.2	
UVLO (V_{IN} mag decreasing)	–32	–36	V	4.1.2.2	The device must be less than 10 mA if V_{IN} below UVLO for more than 2 s
$T_{ON(delay)}$ UVLO (V_{IN} mag increasing)	0	5	s	4.1.2.2	Time from $|V_{IN}| > 43$ V until board on
Power dissipation		200	W	4.1.3	
I_{INRUSH} 0 to 0.9 ms		5	I_T / I_M	4.1.4.1	I_T = instantaneous current
I_{INRUSH} 0.9 to 3.0 ms		Log decay from 5 to 2	I_T / I_M	4.1.4.1	I_M = I_{MAX} rating from manufacturer
I_{INRUSH} over 3 ms		1	I_T / I_M	4.1.4.1	
$T_{100\text{-}V(transient)}$	10		μs	4.1.4.3	
$T_{75\text{-}V(transient)}$	10		ms	4.1.4.3	
$T_{0\text{-}V(transient)}$	5		ms	4.1.4.3	

The most common technique for connecting the two power feeds is diode ORing, as shown in Figure 1. Diode ORing is simple, small, inexpensive, and prevents current flow between the two feeds as required by the ATCA spec. When also used on the high side (–48VA RTN, –48VB_RTN) current flow is prevented between the two returns, as required by ATCA. Although ORing diodes are used in the solution presented in this paper it should be noted that they are lossy and lack controllability when compared to FET based solutions. Diode losses increase proportional to load current so this issue becomes more significant as board power gets higher. Using FETs instead of diodes is possible but beyond the scope of this discussion.

Figure 1 shows a TPS2393 based hot swap solution configured for ATCA. Component selection details are well covered in the TPS2393 datasheet and only those aspects particular to ATCA are discussed here. Those parameters and their associated components are shown in Table 2.
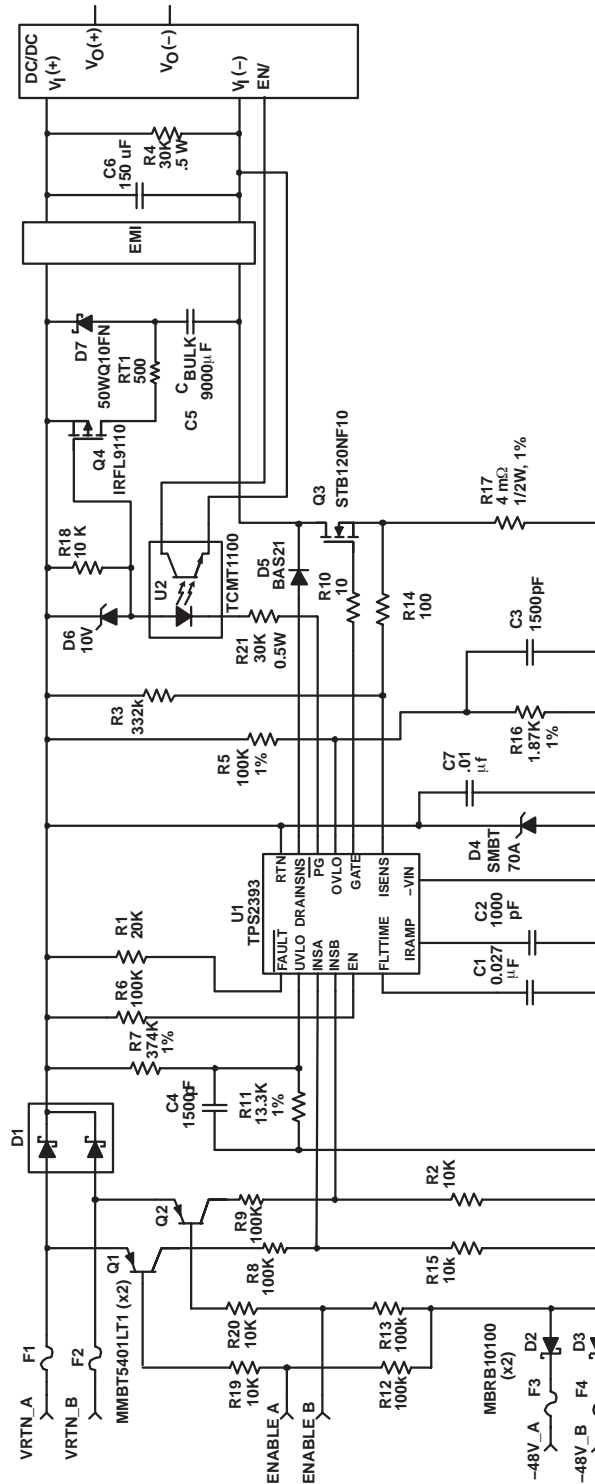

Figure 1. TPS2393 ATCA Hot Swap Control

2   Component Selection

2.1   Overvoltage (OV) Resistors

The two primary consideration when selecting OV level are;

1. Maximum input voltage allowed at the input to the downstream power converters, and

2. The ACTA requirement that converters operate with up to 72-V magnitude at the input. Some converter suppliers with an eye to the ATCA market allow 75 V continuous operational and up to 80 V continuous non-operational.

R8 is the first resistor to be selected since it determines the OV hysteresis and is half of the resistor ladder which sets the OV threshold. To ensure shut off below –80 V, ensure operation to –72 V, and allow for component tolerances, a 1 V nominal OV hysteresis is chosen. The TPS2393 datasheet formula for R8 is applied as follows;

$$V_{HYS(ov)} = 1 \; V;$$

$$R8 = \frac{V_{HYS(uv)}}{10 \; \mu A} = \frac{1 \; V}{10 \; \mu A} = 100 \; k\Omega$$

With R8 selected at 100 kΩ it is now possible to select R9 and set the OV threshold. Circuit assumptions include the downstream power converters are functional to 75 V, able to withstand 80 V indefinitely, and the bulk capacitors are rated to 100 V. Also,the ORing diodes each have ~0.75 V drop under maximum load. To ensure that power is still on when the module input is –72 V the OV threshold must be set to at least;

$$V_{OV} = -\left|V_{MAX} + 2 \times V_{DIODE} + V_{HYST}\right| = -\left|72 + (2 \times 0.75) + 1\right| \; V = -74.5 \; V$$

Since the chosen dc-to-dc converter can handle 80 V the OV level is set to –75 V. Using the datasheet equation for R9;

$$R9 = \frac{V_{REF} \times R8}{V_{OV} - 1.4} = \frac{1.4 \times 100 \; k\Omega}{75 - 1.4} = 1902 \; \Omega$$

Closest standard value = 1870 Ω

Where;

* V_{OV} = 75 V

* V_{REF} = 1.4 V (per datasheet)

*   R8 = 100 kΩ (as previously selected)

Select a standard value 1870, 1% resistor which yields an OV threshold of – 76.2 V. With the OV resistors set the next step is the UV resistors.

2.2   Undervoltage (UV) Resistors

ATCA requires a shutoff between −32 V and −36 V. When input voltage magnitude falls below the shutoff level total board current draw must be less than 10 mA. Board operation must only be ensured to −43 V so it is not clear why this specification is a range instead of a fixed point (−32 V) below which current draw must be less than 10 mA. The PICMG 3.0 standard leaves a large undefined range between the −43 V *must operate* level and the −32 V *must be off and drawing less than 10 mA* level. This undefined range does allow the designer to accommodate common power supply, battery, and converter requirements.

This design performs UV monitoring across C_{BULK} instead of across V_{IN}. which prevents $\overline{FAULT}$ from asserting (and prevents $\overline{PG}$ from deasserting) during a 5-ms zero volt transient.

Many power converters operate with as little as −32-V input, and may have their own internal UV shutoff. Consequently, there is a temptation to set the board UV to 32-V magnitude and let the converters take care of all UV duties. Two factors make this a potentially undesirable choice.

The first issue is the input current required to power a 200-W load at −32 V. A 200-W load requires 4.1 A at −48 V. That same load requires 6.25 A at −32 V. Since I2R losses rise with the square of the current the potential for overstressing power elements on the board is quite real. All current carrying components would have to be sized for the 34% increase in nominal current.

A second reason to set UV well above 32-V magnitude is battery life. Some end users want all loads removed if battery voltage magnitude drops below 37 V because battery life drops significantly or, worst case, stops then and there. Understand as much as possible about the end system before setting the UV level.

This design example considers battery life issues so the UV lower threshold will be set at −37 V. When the ORing diode drops are factored in the UV threshold when measured at the board input is;

$$V_{UVLO} \text{ at board input } = -37 - \left(2 \times V_{DROP}\right) \sim -38.5 \text{ V}$$

The upper UV target magnitude needs to be below −43 V and there needs to be sufficient hysteresis to prevent the board from turning on and off due to line drops in the distribution network. Furthermore, it is desirable for the upper UV threshold magnitude to be lower than 43 V so C_{BULK} can start charging before the −43 V *must operate within 5 seconds* threshold is reached.

UV hysteresis should be maximized to reduce the chances of UV limit oscillations. This results in the TPS2393 hysteresis being −37 V / −40.75 V. The board thresholds is two diode drops higher for each parameter. That is, −38.5 V / 42.25 V.

R1 is the first resistor to be selected since it determines the UV hysteresis. Using the datasheet formula R1 is calculated for 3.75-V hysteresis as follows;

For $V_{HYS(uv)}$ = 3.75 V;

$$R1 = \frac{V_{HYS(uv)}}{10\,\mu A} = \frac{3.75\ V}{10\,\mu A} = 375\ k\Omega$$

Closest standard value = 374 kΩ

With R1 selected at 374 kΩ it is now possible to select R2 and set the UV threshold. –41-V UV threshold is calculated using the datasheet formula shown below.

$$R2 = \frac{V_{REF} \times R1}{V_{UV} - 1.4} = \frac{1.4 \times 374\ k\Omega}{40.75 - 1.4} = 13.306\ k\Omega$$

Closest standard value = 13.3 kΩ

Where;

- V_{UV} = 40.75 V

- V_{REF} = 1.4 V

- R1 = 374 kΩ

An R2 value of 13.3 kΩ results in a UV threshold of –40.76 V.

2.3 Bulk Capacitor (Hold-Up Capacitor)

ATCA requires boards to remain operational and *ride-through* a 5 ms, 0 V transient on the power inputs to the board. ATCA further states that this requirement applies with starting input voltage magnitudes as low as 43 V.

There are alternate, complex methods for storing the energy but only the brute strength bulk capacitor method is considered here. It is simple and reliable, but can take large amounts of board space. To calculate the total energy storage requirements it is necessary to determine the total time the module is without power. ATCA para 4.1.4.4 defines the magnitude falling at 50 V/ms and rising at 12.5 V/ms. The resulting time below 43 V is calculated as;

$$T_{DROPOUT} = \frac{43\ V}{50\ V}ms + 5ms + \frac{40.75\ V}{12.5\ V}ms = 0.86 + 5 + 3.26 = 9.12\ ms$$

And the stored energy requirement is;

$$energy = power \times time = 200\ W \times 9.12\ ms = 1.824\ joule$$

After factoring in the capacitor tolerance the energy available from the capacitor is;

$$E = \frac{C_{BULK} \times \left(V_1{}^2 - V_2{}^2 \right)}{2 \times (1 - Tolm) \times (1 - Tola)}$$

Where;

- C_{BULK} = bulk capacitor value

- E = energy used during 5-ms holdup = 1 Joule

- V_1 = V_{CBULK} at start of 5-ms transient = –43 V – (2 x 0.75) = – 41.5 V

- V_2 = V_{CBULK} at end of 5-ms transient = – 37 V

- Tolm = capacitor manufacturing tolerance = +/–0.2 = +/–20%

- Tola = capacitor aging tolerance = –0.2 = –20%

Manipulating the above yields the following equation for determination of C_{BULK}.

$$C_{BULK} = \frac{(2 \times E)}{\left[\left(V_1 \right)^2 - \left(V_2 \right)^2 \right] \times (1 - Tolm) \times (1 - Tola)}$$

$$C_{BULK} = \frac{(2 \times 1)}{-41.5^2 - (-37)^2 \times 0.8 \times 0.8} = 8846\ \mu F$$

The ATCA maximum component height of 21.33 mm forces the use of multiple capacitors to achieve the 8846 µF required. Nine 100-V, 1000-µF capacitors fits the bill.

2.4 Overcurrent Sense Resistor (R_{SENSE})

Setting the overcurrent limit requires selecting R_{SENSE} such that 40 mV appears across it at slightly above the maximum expected load current. To calculate maximum expected current (I_{MAX}) P_{MAX} is divided by $V_{IN(min)}$.

$$I_{MAX} = \frac{P_{MAX}}{V_{IN(min)}} = \frac{200\ W}{37\ V} = 5.4\ A$$

As a point of reference the nominal current I_{NOM} is calculated below.

$$I_{NOM} = \frac{P_{NOM}}{V_{NOM}} = \frac{200\ W}{48\ V} = 4.17\ A$$

It is desirable to err on the high side when setting the overcurrent limit to reduce nuisance faults. The over current threshold should not be set too high since it could overstress Q1.

To assure the worst case TPS2393 does not prematurely limit current the minimum value of $V_{REF(k)}$ is used. This yields;

$$R_{SENSE} = \frac{V_{REF(kmin)}}{I_{MAX}} = \frac{33\ mV}{5.37\ A} = 6.15\ m\Omega$$

Closest standard value = 6 mΩ

With R_{SENSE} set to 6 mΩ and $V_{REF(k)}$ equal to 40 +/−7 mV the OC threshold(s) are;

- $I_{OC(nom)}$ = 6.67 A

- $I_{OC(max)}$ = 7.83 A

- $I_{OC(min)}$ = 5.5 A

Since the maximum expected current is 5.4 A these values provide a reasonable margin.

2.5 Current Ramp Slope (C_{IRAMP})

Setting the current ramp slope is straightforward using the equation from the TPS2393 datasheet. Setting I_{RAMP} to a specific value allows control of the inductive voltage drop during inrush which is defined as;

$$V_{DROP(inrush)} = L\left(\frac{di}{dt}\right)$$

Where;

- L = combined inductance of the power distribution network

- di/dt = programmed current ramp slope A/s

It is assumed that the system will easily tolerate a di/dt of 2000 A/sec. C_{RAMP} is then calculated using the TPS2393 datasheet formula as follows;

$$C_{RAMP}\,\mu F = \frac{11}{100 \times R_{SENSE} \times \left(\frac{di}{dt}\right)MAX} = \frac{11}{100 \times 0.006 \times 2000} = 9160\ pF$$

Where;

- R_{SENSE} = 0.006 Ω

- $(di/dt)_{MAX}$ = 2000 A/s

The closest common value is 10,000 pF which gives a current slope of 1833 A/sec. Therefore. C_{RAMP} is selected to be 10,000 pF = 0.01 μF.

2.6 Power Limiting

In the unlikely (but allowed) event that a –72-V supply is used resistors have been added to implement power limiting. R3 and R14 both feed the ISENS pin of the TPS2393. As VIN magnitude increases the amount of current bled into ISENS through R3 increases. This, in turn, reduces the amount of current through R17 necessary to cause an overcurrent detection.

This may seem like much effort to protect a fet. However, it is wise to remember the dc curve on most SOA plots assumes TJ is 25°C. This is rarely the case when a fet is conducting many amps of current as it would while powering a 200-W load.

2.7 Fault Time

Fault time (T_{FAULT}) should be set long enough to ignore nuisance trips but short enough to keep Q3 well within advertised SOA under normal conditions. It is worth noting that the fault timer starts counting as soon as the TPS2393 goes into current limit. It does not wait until the OC limit has been reached but starts counting as soon as current is being limited to the level of the current ramp slope.

If fault time (T_{FAULT}) were set to allow the 9000-µF C_{BULK} to completely charge without a time out it would have to be set between 100 ms – 150 ms according to the formulae in the TPS2393 datasheet. Such a long fault time would leave Q3 extremely susceptible to damage from overcurrent events, such as shorts on the board. To allow a suitably short T_{FAULT} (1 ms – 5 ms in this case) C_{BULK} is not allowed to start charging until $\overline{PG}$ asserts and turns on Q4. Prior to the assertion of $\overline{PG}$ only the input capacitors on the power bricks will present a significant load to VIN. Brick input caps are typically specified from 100 µF – 200 µF for each brick. Once $\overline{PG}$ asserts, current into C_{BULK} is limited to a few tenths of an Amp by RT1. D7 allows C_{BULK} to discharge without being current limited by RT1.

When a fet has been selected for Q3 it is wise to evaluate it in the circuit under all expected conditions to determine it's *situational SOA*. After T_{FAULT} has been determined by calculation and experimentation the following equation yields C_{FAULT}.

$$C_{FAULT}(\mu F) = 14.4 \times T_{FAULT}, \ (in\ seconds)$$

3 Summary

An ATCA hotswap power control scheme has been defined and components selected using ATCA requirements and necessary system assumptions to steer the process. Methods and criteria for selection of undervoltage, overvoltage, fault, ramp, and overcurrent components have been demonstrated and applied.

Care must be taken when selecting components so that second and third order effects such as tolerances are not neglected. The ATCA standard applies to many equipment types and customer bases. Specific applications and customer requirements must be considered when designing the power system.

Table 3 itemizes many of the critical factors which should be considered during component selection.

Table 2. Hot Swap Parameters and Component Selection Considerations

Parameter	Symbol	Component(s)	Considerations/Limitations
Overvoltage	OV	R5, R16	Check max VIN of power converter being used ATCA requires operation for (-43 V $> V_{IN} > -72$ V) ATCA requires no damage to $V_{IN} = -75$ V
Undervoltage	UV	R7, R11	Must draw less than 10 mA if V_{IN} magnitude less than 32 V I^2R loss on board EMI, fuse, component current ratings
Overcurrent	OC	R17	C_{BULK} charging time External FET safe operating area (SOA)
Fault time	FLTTIME	C1	Check fuse blow time External FET Safe operating area (SOA)
C_{BULK}	C_{BULK}	C5	P_{LOAD}, V_{UV}, $V_{HYSTERESIS(uv)}$
Current ramp	IRAMP	C2	Max desirable dI/dt of power distribution network and ATCA current profile

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