Application Guidelines for Non-Isolated Converters
AN04-006: PWB Layout Considerations

Introduction

Non-Isolated POL dc-dc converters are switching buck regulators which require careful layout considerations when designing on to a printed wiring board (PWB). Many applications using these non-isolated dc-dc converters utilize high-density multi-layer circuit boards, and proper component placement and power/control routing is critical for trouble-free operation of the power modules. This application note provides generic guidelines for laying out the Austin Lynx and TLynx series of non-isolated dc-dc modules. Please consult Lineage Power Technical Representatives for guidelines in more specialized applications.

General Guidelines

Location of the Module

Dc-dc converters, because of their switching action, are a source of rapidly varying electrical and magnetic fields. The EMI spectrum from these modules can range from the switching frequency (typically around 300 kHz for the Austin Lynx series modules) to harmonics in the MHz range. To minimize effects on other components on the PWB, location of the dc-dc converter module should be carefully considered. Proper input and output filtering can reduce the noise levels at the terminals of the modules. Suggested layout of the traces used to connect the modules and locations of external components are provided later in this application note. These, along with good analog design layout practices are sufficient to achieve proper performance when using these modules.

Minimizing Loop Area

The input current of a buck converter is discontinuous, and while both the Austin Lynx and Tlynx series of modules have input filter capacitors incorporated in the module, the current into the module does have a significant ripple component, which leads to a voltage ripple being superimposed on the input source. This high frequency ripple voltage and current could be a potential source of noise. To avoid noise coupling, it is recommended that the loop area for both power and signal traces to the dc-dc module be minimized. In addition, input and output capacitor, located as close as possible to the module, are recommended for high frequency filtering. Figure 1 shows a typical application circuit of the Austin Lynx module, incorporating these recommendations. Input (C_{IN}) and output (C_{OUT}) are ceramic Low ESL and ESR capacitors. Such capacitors are available from companies such as Syfer, TDK and Murata. Capacitors used for minimizing the ripple component are termed as bulk capacitors with capacitance needed being in the order of tens or hundreds of microfarads. For reducing high-frequency switching noise at the input and output of the module, 0.1µF (0603) and 1.0µF (0603) small package ceramic capacitors should be placed at input and output of the module in the above order. For a more detailed discussion of input filtering for the Austin Lynx series, please refer to **Application Note AN04-002** titled ***"Application Guidelines for Non-Isolated Converters: Input Filtering Considerations".***

Figure 2 shows an example layout for a Austin Lynx Series module. This example details the key guidelines to be followed when designing the module on to your board. For simplicity, all three power traces (input, output and ground) are assumed to be on the top layer of the PWB – where the Austin Lynx module is placed. The first key guideline is to extend the ground plane to the area underneath the module. It is not recommended that this space be utilized for routing signal traces unless they are in inner layers underneath the ground plane. The V_{OUT} and ground planes are placed close together to minimize interconnect inductance on the output side. Output capacitors (C_{OUT}) are connected as close to the

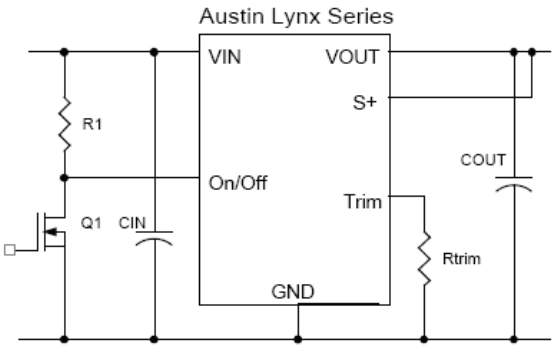

Fig. 1. Typical application circuit of an Austin Lynx series module.

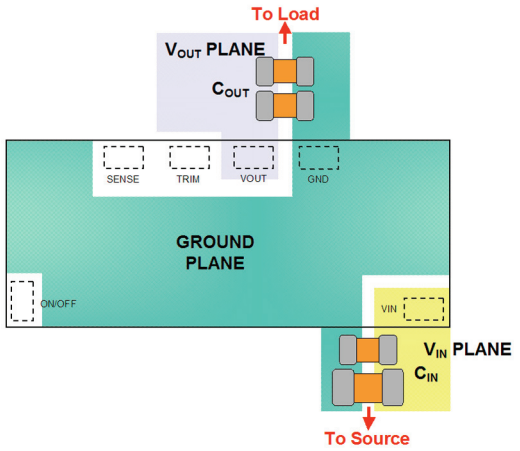

Fig. 2. Simplified layout for the Austin Lynx and SuperLynx series modules.

output/ground pins as possible to provide the most effective output filtering. Similarly on the input side, interconnect inductance is minimized by placing the V_{IN} and ground planes close together and the input capacitors are placed as close to the input/pins as possible.

Sizing Traces and Vias

Whenever possible, copper planes should be used for routing power traces (input, output and ground connections. In most applications, the application PWB will have multiple layers with the top and bottom layers being primarily used for routing signals. This leads to the inner layers being used for ground, input and output. With non-isolated modules, since the input voltage is often used to feed multiple modules, one layer can be assigned to it. The output can either be another layer or part of a layer. In applications where the layout is very tight, input and output may only be portions of inner layers. When inner layers are used with SMT modules, multiple vias are needed to carry the current from the top layer to the inner power planes. A rule of thumb is to have 3A/per via. The recommended via size is 22 mils (0.022" or 560µm) plated-through hole. For control pins, one via per pin is sufficient. Vias should be located in the direction of current flow (location of the load ICs – See recommended layouts for load and source arrows) for optimum performance. For signal traces, the recommended trace width for signal traces is 7 – 10 mils (180 - 250µm). For bulk capacitors, 1-2 vias per capacitor connection are recommended. Figure 3 shows a layout of the Austin Lynx module showing vias located near the output, input and ground pins for carrying current to the inner layers.

External Component Placement

Austin Lynx dc-dc module should be placed to minimized loop area and noise coupling. Signal traces should not be routed underneath the module, unless sandwiched between ground planes, to avoid noise coupling. Also, components should not be placed under the module to prevent any coupling. The ground plane can be placed under the module. For repair and removal of the SMT module from the PWB, 4.0 mm (0.16 inches) of clearance is recommended around the module outline. This clearance provides clearance and isolates adjacent components from exposure to heat during the removal process.

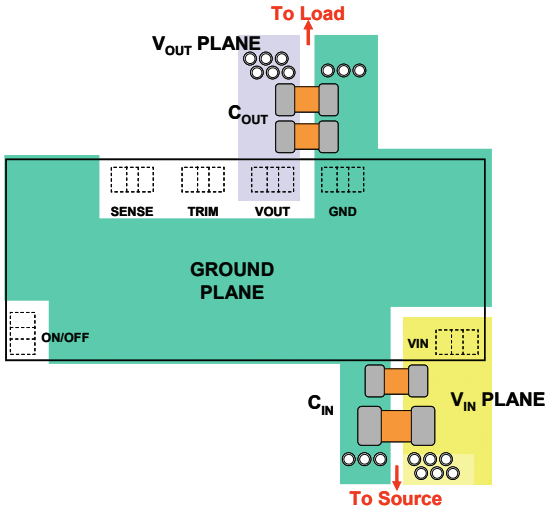

Fig. 3. Austin Lynx II and SuperLynx II SMT recommended layout showing placement of vias.

Dual Layout for Lynx and MicroLynx Series

In applications where there is uncertainty on the required load current levels, it may be useful to have a Lynx and MicroLynx module both laid out together. Such an arrangement allows for the lower-current MicroLynx to be used in the event that actual load currents move lower as the design progresses. Figure 4 shows such an example dual layout, where the Lynx module outline and pin locations are shown in black and the MicroLynx in blue.

Example Layouts for SIP Modules

Figures 5 shows an example layout for the Austin Lynx and SuperLynx series SIP modules, and Fig. 6 shows the example layout for the Austin MicroLynx series SIP modules. Both layouts follow the same guidelines of having the ground layer extend below the modules and placing input and output capacitors as close as possible to the input/ground and output/ground pins. Thermal reliefs should be used with holes associated with through-hole pins connected to large planes as per the guidelines in IPC 2222, section 9.1.2.

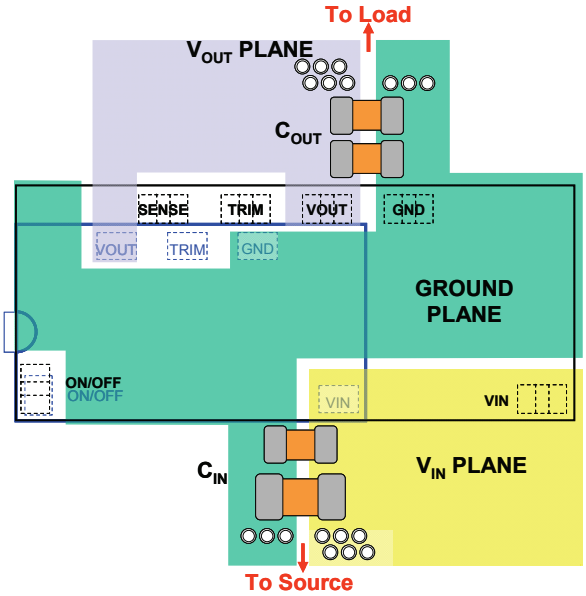

Fig. 4. Example showing dual layout of Austin Lynx and MicroLynx series modules.

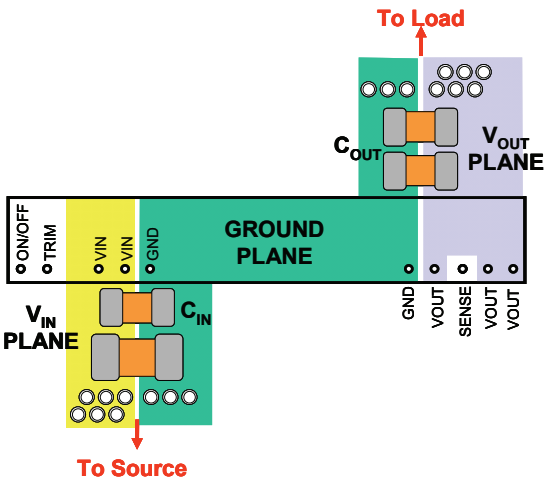

Fig. 5. Simplified layout for the Austin Lynx and SuperLynx series SIP modules.

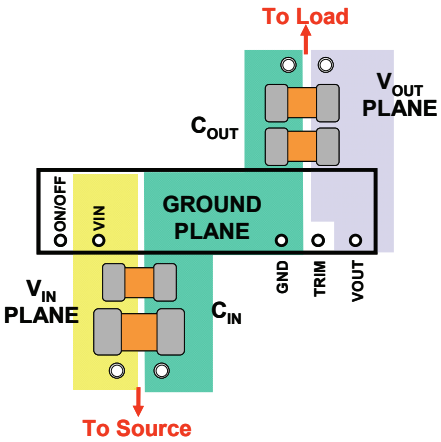

Fig. 6. Simplified layout for the Austin MicroLynx series SIP modules.

Example Layouts for The TLynx Series

The TLynx series of modules include the PicoTLynx, the MicroTLynx and the TLynx modules. The MicroTLynx has a similar pinout to the Austin MicroLynx, while the TLynx module pinout corresponds to the Austin Lynx modules. The PicoTLynx however is a smaller module with a new pinout.

Whenever possible, dual layouts of modules are recommended in order to accommodate a need for a higher power module if current demands are not fully known or support a lower power module if actual load requirements turn out to be lower than anticipated in the initial design. Figure 7 shows a dual layout of a PicoTLynx and MicroTLynx, while Fig. 8 shows a dual layout of a MicroTLynx and PicoTLynx. These figures also provide an example of actual layouts using these modules.

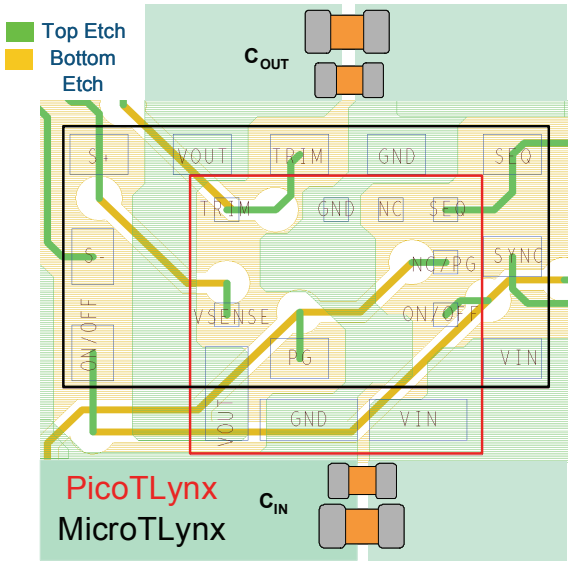

Fig. 7. Dual layout for the PicoTLynx and MicroTLynx modules.

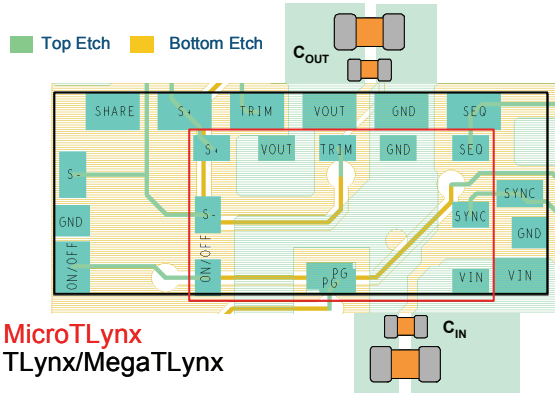

Fig. 8. Dual layout for the MicroTLynx and TLynx/MegaTLynx modules.

Summary

Several example layouts for the Austin Lynx and TLynx series of modules have been presented to illustrate the important principles involved in designing Lineage POLs into an application. In addition, guidelines for via sizing, number of vias and their placement have been provided. For specific questions in specialized applications, please consult your Lineage Power Technical Representatives for additional information.

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