Application Guidelines for Non-isolated Converters
AN13-001 Filtering and Layout Guidelines for Non-Isolated Converters

Introduction

On-board powering of IC loads requires careful attention to filtering and layout of the POLs that typically generate the various powering voltages. This application note guides the user through the various considerations involved and provides recommendations on how to achieve optimal performance.

Most POL DC-DC converters use the buck converter topology shown along with key circuit waveforms in Figure 1. The input current of such a converter is discontinuous. In addition, the transitions in the switching current can cause ringing voltages and currents due to the presence of parasitic inductances and capacitances, causing both conducted and radiated EMI.

Figure 2 shows the output and input voltage waveforms of an example POL when a load transient is applied. Both output and input voltage dip momentarily when the load current increases. The load current also has an influence on the ripple and noise voltages at the input and output as shown in Fig 2. Input ripple voltage is directly proportional to load current while output ripple voltage changes only slightly. Switching noise however increases with load current on both the input and output voltage waveforms. Switching ripple and noise generated within the POL has two components as shown in Figure 2.

1. Internal switching ripple which occurs at the switching frequency and its harmonics (250KHz to 20MHz).

2. Internal switching noise related to switching transition times of the power switches (20MHz to 1GHz+)
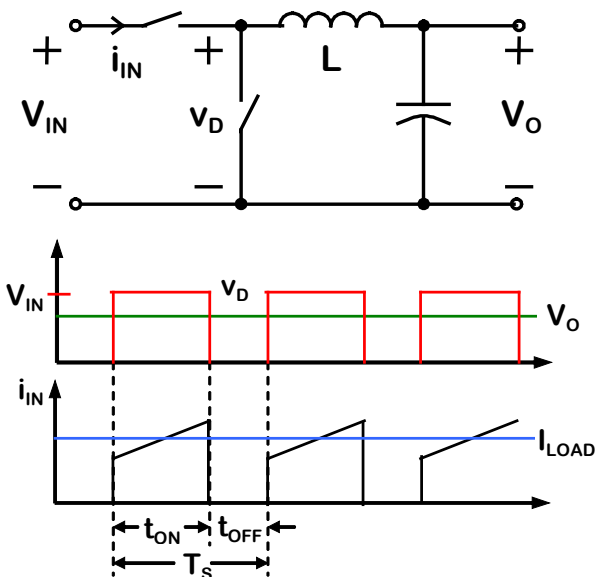

Figure 1. Simplified circuit diagram and waveforms of a buck converter.

Figure 3 shows the high-frequency nature of input switching noise with an expanded time scale. The generation of high frequency noise during switching transitions will be explained later in the section on High Frequency Noise Generation.

Measurement of these high frequency signals needs special attention regarding oscilloscope probe usage and oscilloscope settings, these considerations are explained in the next section.
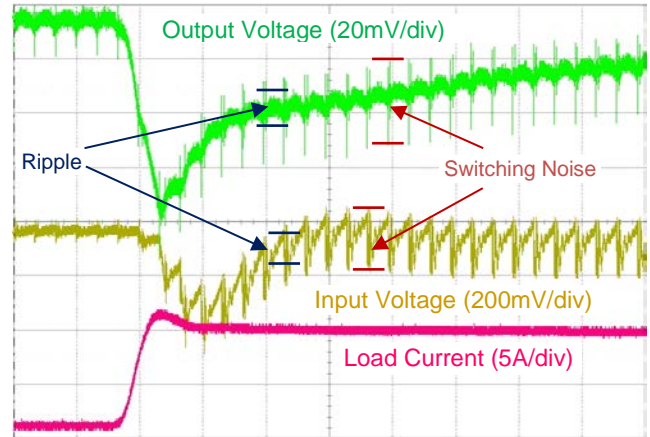

Figure 2. Input and output voltage waveforms on a PicoDLynx* module with a 10A load transient.
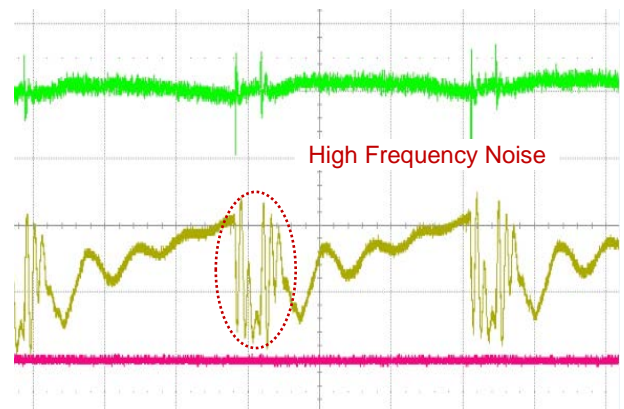

Figure 3. Expanded version of Figure 2 showing switching noise on the input voltage waveform.

Considerations for Measuring POL Input and Output Voltages

Probe Considerations

Nearly all oscilloscopes ship with 10X attenuation passive probes because this type of probe is the best choice for making measurements across a broad range of applications. A general purpose probe is usually rated from DC to 200 MHz and capable of measuring up to a few hundred volts. However, making low voltage measurements using a 10X probe can yield inaccurate results because of their inability to make measurements in the low millivolt range as can be typically encountered when measuring ripple and noise. When making such measurements, it is important to consider oscilloscope sensitivity, system noise, probe grounding and probe parameters such as attenuation, input impedance, offset and bandwidth.

When a probe is inserted into a circuit, it will have some effect on the circuit under test. The interaction of resistive, inductive and capacitive elements produces total probe impedance

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that varies with signal frequency. To minimize probe loading and noise pickup, the user should use the shortest ground leads possible to minimize the inductance and use a probe with low input capacitance. Passive probes with 1X and 10X attenuation are compared below.
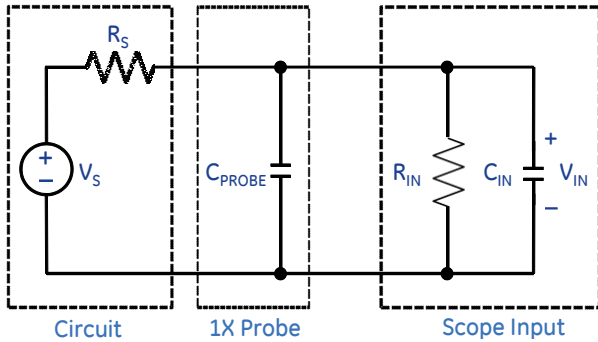

Figure 4. Equivalent circuit of a 1X passive probe.

At very low frequencies, capacitors act as an open circuit and the probe behaves as a low-pass filter. The equivalent circuits of 1X and 10X probes are shown in Figs. 4 and 5, respectively. The input capacitance of a 1X probe is much larger than a 10X probe. For example, a 1X probe has C_{PROBE} of 100pF, while a 10X probe has C_{PROBE} of 12pF. The 10X probe therefore reduces resistive loading and capacitive loading by a factor of approximately 10. The higher input capacitance of 1X probes leads to lower bandwidth than 10X probes. As an example, a switchable 1X/10X probe has only 6MHz bandwidth when on the 1X setting, but 200MHz when on the 10X setting. Bandwidth of the probe should typically match that of the scope to obtain accurate measurements. In addition, the general recommendation is for the probe bandwidth to be at least five times the largest frequency of the signal being measured.
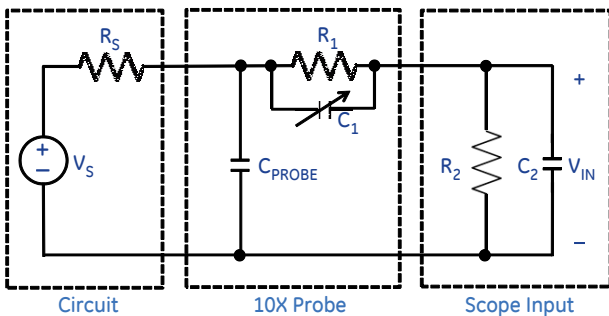

Figure 5. Equivalent circuit of a 10X passive probe.

It is sometimes necessary to use a 50-ohm coaxial cable to measure a voltage waveform without being affected by probe bandwidth. The equivalent circuit when using coaxial cables is shown in Figure 6. This method of probing is restricted to DC coupling and the bandwidth automatically matches that of the oscilloscope. However, due to limitations on the voltage that can be connected to oscilloscope inputs, this method can only be used with relatively low voltages.

The ground lead plays a crucial role in noise measurements. Longer ground leads result in higher ground lead inductance. Figure 7 shows that ground lead inductance forms a series resonant circuit with only R_{IN} for damping. Figures 8 and 9 provide example results that illustrate the effects of ground

lead inductance when making POL output voltage measurements. The example waveforms shown in Fig. 8 are from measuring output ripple in two different ways. The first is using a probe socket as shown in Fig. 9, while the second is using a probe with a six-inch ground lead. The long ground lead picks up spurious noise and also produces ringing with the probe input capacitance leading to measurements that can be quite inaccurate. Figure 10 shows the same measurement with even longer 12 inch ground leads. In this case, the noise amplitude almost doubles when compared to using 6 inch ground leads. Moreover, the excessive ground lead inductance limits the charging current to Cin and thus the rise time of the pulse leading to further signal distortions.
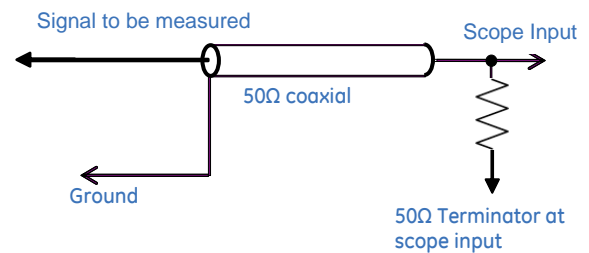

Figure 6. Diagram showing a resistive input passive probe using 50-ohm cable.
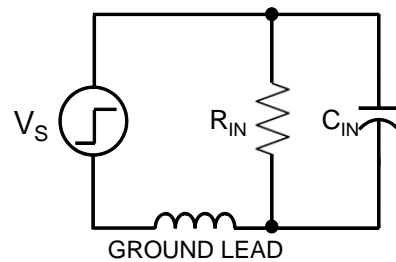

Figure 7. Probe ground lead forming a series resonant circuit with R_{IN} and C_{IN}.
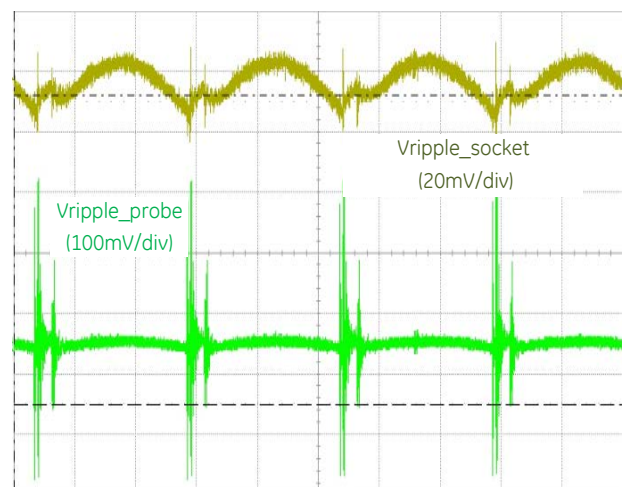

Figure 8. Measurement of output voltage ripple on an MDT040 evaluation board with socket (upper waveform) and using probe with 6 inch ground lead length (lower waveform). Conditions are Vin = 12V, Vout = 1V and Iout = 32A.

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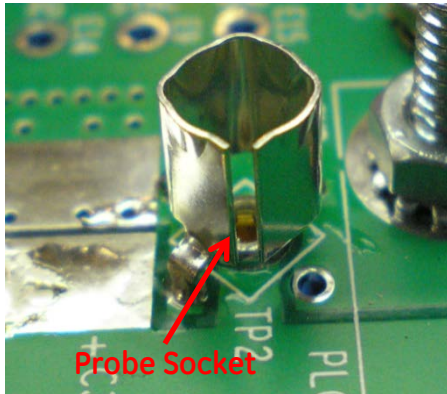## AN13-001 Filtering and Layout Guidelines for Non-Isolated Converters

Figure 9. Tektronix Probe socket (part number 131-4353-00) used to make measurements with negligible ground lead inductance.
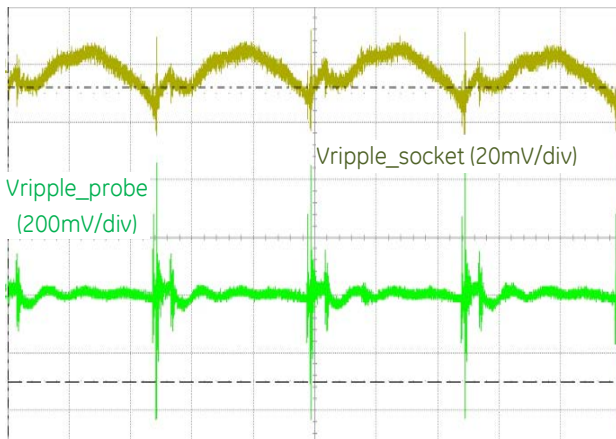

Figure 10. Measurement of output voltage ripple on an MDT040 evaluation board with socket (upper waveform) and using probe with 12 inch ground lead length (lower waveform). Conditions are Vin = 12V, Vout = 1V and Iout = 32A.

One measurement challenge is measuring a low voltage AC signal riding on top of a DC signal. When using a low attenuation passive probe to look at these kinds of AC signals, users should use the AC coupling feature on the oscilloscope to block the DC component and show only the AC signal. This method enables users to examine the AC portion of the signal in much more detail. It is also necessary to select a probe with sufficient bandwidth. The rule of thumb is to have the probe bandwidth be at least five times the bandwidth of the signal being measured. For signals that change quickly over time and have a fast slew rate (dv/dt), the measurement system must be capable of capturing these events. The specification that determines how effective the measurement system is over time is the rise time specification. The input ripple measurement waveforms for a PDT012 module at 12Vin, 1.2Vout and 12A load with different probe attenuation and bandwidth settings is illustrated in Figs. 11, 12, 13 and 14, respectively.

After this discussion of voltage measurement techniques, we move on to the next section describing the noise generation mechanisms and their effects within a POL.

High Frequency Noise Generation and its Effects

Noise generation due to Parasitics

As previously discussed, the discontinuous input current of a buck converter causes both ripple and noise. Ripple, which occurs at the switching frequency, is affected by both capacitance and ESR of the POL input capacitors. The AC ripple component is mostly sourced by the high frequency input capacitor due to its low impedance at high frequencies. Input ripple is created by the AC component of the input pulsating current as it flows through the ESR of the input capacitors. To observe this ripple on an oscilloscope while masking switching noise, the bandwidth of the oscilloscope can be reduced to 20MHz. Figure 15 shows the input and

Figure 11. Input ripple voltage measurement - full bandwidth, 10X probe, 47.4mV (pk-pk).

Figure 12. Input ripple voltage measurement - 20MHz bandwidth, 10X probe, 21.1mV (pk-pk).
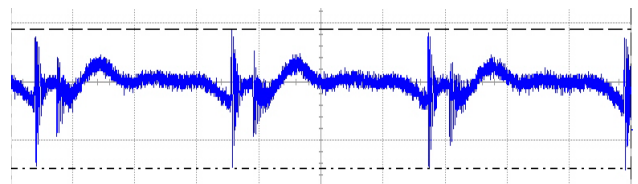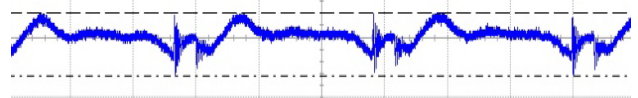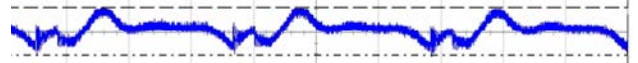

Figure 13. Input ripple voltage measurement - Full bandwidth, 1X probe, 17.9mV (pk-pk).
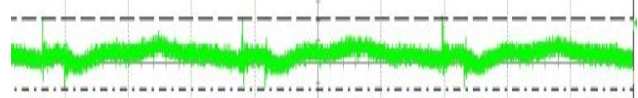

Figure 14. Input ripple voltage measurement - full bandwidth, 50 ohm probe, 70mV (pk-pk).
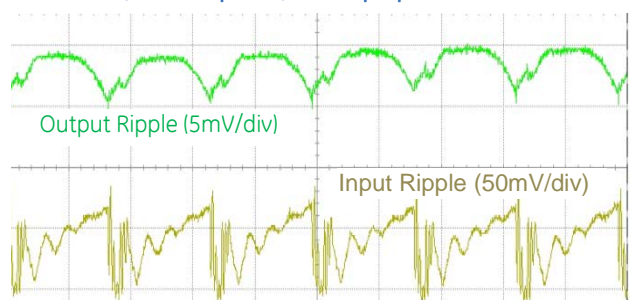

Figure 15. Input and output ripple waveforms with oscilloscope bandwidth at 20MHz on a PicoDLynx module.

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output ripple voltage waveforms taken with the oscilloscope set at 20MHz bandwidth.

To illustrate the details of how switching noise is generated, consider the simplified equivalent circuit of the buck converter shown in Figure 16. When the top switch is turned off, the capacitance of the top FET $C_{DS,TOP}$ is charged and the capacitance of the bottom MOSFET $C_{DS,BOT}$ gets discharged. The loop parasitic inductance L_{LOOP} alters turn-off transition by introducing a high frequency resonance with the series combination of capacitances in the loop. The high frequency oscillation continues until the bottom MOSFET is fully turned on. Similar resonances can alter the switching transition when the bottom switch is turned off and the top switch is turned ON. Thus noise due to these resonant transitions is generated twice during a switching cycle – first during the transition from the top switch being ON to the bottom switch turning ON, and next when the bottom switch is turned OFF and the top switch turns back ON. This noise generally occurs in the range of few tens of MHz to over 500MHz depending on parasitic inductances, and the MOSFETs and how they are driven.
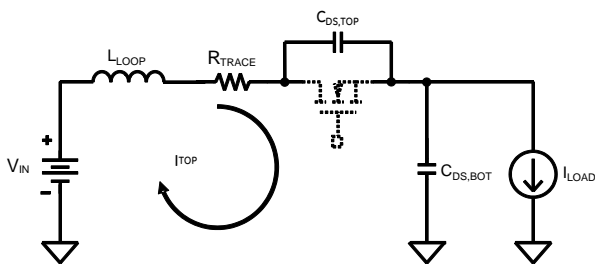

Figure 16. Simplified equivalent circuit of a buck converter when the top switch turns off and the bottom switch has not yet turned on.

Coupling of input noise to output

Switching noise at the input of a POL can also couple to the output. Figure 17 can be used to explain this phenomenon. Since the GND lead is common to both the input and output circuits, any interconnect inductance in the GND path can cause input ripple/noise to also partially show up on the output. Thus noise created from the switching action can propagate to other parts of the circuit if not properly filtered. In addition, improper layout of key components on and
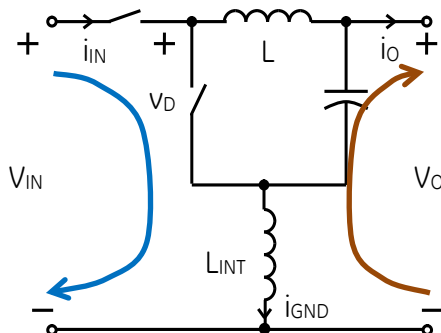

Figure 17. Schematic showing the effects of ground lead inductance on input and output noise.

around the POL can cause noise to be coupled or inadequately suppressed near the source.

Filter Capacitor Characteristics and Design Considerations

Capacitors are integral to input and output filtering, providing a stable voltage source, and minimizing voltage excursions during load transients. Most DC-DC converters use input and output filter capacitors to achieve good transient response and for noise decoupling. The non-ideal characteristics of the capacitor include parasitic resistance and inductance. The simple C-R-L equivalent circuit model of a capacitor is shown in Fig. 18.

Figure 18. Simple C-R-L model of a Capacitor.

Depending on the type of capacitor, C, R_C and L_C may vary with frequency. Therefore it is critical to know the impedance of the capacitor in the frequency range of interest. There are many different types of capacitors and understanding their individual characteristics is necessary to the design of practical and effective power supply filters. The capacitors used in filtering are broadly classified by their dielectric types, for e.g., ceramic, polymer, tantalum, aluminum and organic electrolytic. Table 1 provides a summary of the characteristics of different capacitors and recommended applications.

Figure 19 shows plots of the impedances of typical ceramic and polymer capacitors, and how combining those in parallel can result in lower impedance over a wider frequency range than any one single capacitor. The point where each impedance graph reaches its minimum is the Self Resonant
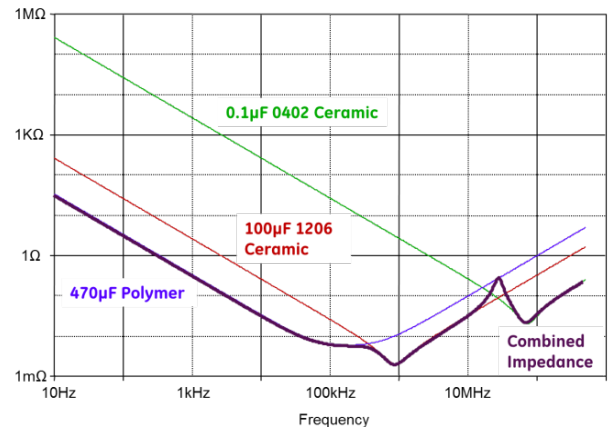

Figure 19. Impedance characteristics of an example parallel combination of capacitors.

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Table 1. Comparison of different types of capacitors.

	Ceramic (Multilayer)	Polymer (solid electrolyte)	Tantalum Electrolytic	Aluminium Electrolytic
Size	Small	Small	Medium	Medium to high
Capacitance	Medium	High	High	High
ESR & ESL	Very low	Low	Medium	High
Voltage Ratings	Low to high	Low	Low to medium	Low to high
Application	High frequency filtering and supporting fast transient response	Bulk capacitance for transient response and low frequency filter	Bulk capacitance for transient response and low frequency filter	Bulk capacitance for voltage stability and low frequency filter
Ripple Current rating	High	Medium	medium	Low
Temperature & Bias voltage Effects	ESR varies with temperature and capacitance varies with Bias	Capacitance varies slightly with temperature	Capacitance varies slightly with temperature	ESR rises at low temperature

Frequency (SRF) of the capacitor. At frequencies above the SRF point, the impedance of the capacitor will become inductive, making the capacitor ineffective. Choosing a capacitor in a smaller package with a smaller capacitance value normally increases the SRF of the capacitor due to increases in the ESL L_C. However, since a DC-DC converter typically requires additional capacitance on the input and output, it is common practice to add a smaller capacitor in parallel with the required larger capacitor. The smaller value/size ceramic capacitor attenuates the high-frequency noise, while the larger value/size ceramic capacitor primarily provides attenuation of the switching ripple. In addition, polymer capacitors which have capacitances in the hundreds of µF are used on the output to reduce the voltage excursions that occur during load transients. Higher voltage aluminum capacitors are also used to stabilize the input supply to the POL as well as reduce the effect of load transients on the POL on the input bus to the POL. The aluminum capacitors used on the inputs typically have higher ESRs which also helps with damping the input source impedance as seen by the POL.

Input Filter Design Considerations

Designing for Low Input Ripple and Noise

In general, the AC components on the input bus are suppressed using reactive filter components, such as capacitors and inductors. The input filter capacitors carry the AC component of the current. Most of the ripple current flows through the input ceramic capacitors already placed inside the module. However, a portion of the AC ripple current is also drawn from the input bus. It is therefore crucial not to exceed the RMS current rating of the external capacitors.

Low ESL and ESR ceramic capacitors are recommended for input decoupling of the high-frequency ripple and noise since they provide the maximum attenuation in a small package size. To attenuate high-frequency voltage spikes at the input of the module, 0.1 µF and/or 1.0 µF small-package ceramic capacitors should also be placed at the input of the module. The smallest (both in value and physical size) capacitors are placed closest to the module input pins. Adding 10 or 22µF ceramic capacitors at the input helps to attenuate the ripple.

Table 2 gives an example of the effect of using input capacitors to reduce input ripple and noise. As additional capacitors are added, the input voltage ripple + noise are substantially reduced. Note that just using a high frequency (HF) capacitor of value 0.047uF on the input reduces the ripple + noise amplitude by 6 ~ 7 times in comparison to not using any external capacitors.

Table 2: Input ripple of the 12A PicoDLynx module for Vin = 12V and minimum output Capacitor Cout = 22µF ceramic.

Output Voltage	Vout = 1.2V			Vout = 3.3V		
Load Current (A)	**0**	**6**	**12**	**0**	**6**	**12**
Input Capacitance	Measured Input Ripple + Noise (mVp-p)					
No external Capacitors	1800	8900	8500	900	8400	8300
High Frequency capacitor of 0.047uF/0402 size	232	1088	1536	471	1244	2120
High Frequency capacitor of 0.047uF/0402 size + 22uF ceramic capacitor	65	341	366	57	332	464
High Frequency Capacitor of 0.047uF/0402 size + 2x22uF ceramic capacitor	37	200	245	35	202	237

Stabilizing the Input Bus with Capacitors

The input bus voltage ripple should be reduced sufficiently to ensure proper operation of the loads and the overall power system. A reasonable target (unless special loads are also present on the input voltage bus) is a peak-to-peak voltage ripple of 2% of the bus voltage. The designer should also take into account the static output voltage regulation of the 12V bus converter. For example, the QBDW025A0B1 12V bus converter regulates its output to within ±2% which corresponds to

$$12V \times 2\% = 0.24V$$

Assuming a maximum peak-to-peak input ripple voltage of 2% voltage, and that the bus converter powers TLynx[*] series of input modules which have a minimum input voltage of 4.5V, the decoupling circuit should be designed in such a way that the maximum bus voltage deviation due to a load transient is limited to

$$12V - 0.24V - 0.24V - 4.5V = 7.02V$$

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to guarantee proper operation of the POL converters. This is such a large allowed voltage deviation that it is typically easy to meet.

For the 5V and 3.3V input bus voltage cases, the allowable ripple on the input bus is usually dictated by IC loads powered from the same input bus. Although requirements vary, maximum bus voltage peak-to-peak ripple limits are typically 100mV on 5V systems, and 50mV on 3.3V systems.

For typical POL modules, input ripple voltage increases with both output current and output voltage of the module. Figure 20 shows the variation of input ripple voltage with load at different output voltages for the 20A MicroDLynx* module, with 4 x 22μF ceramic capacitors at the input of the module. The input voltage ripple is seen to be generally larger for higher output voltages.
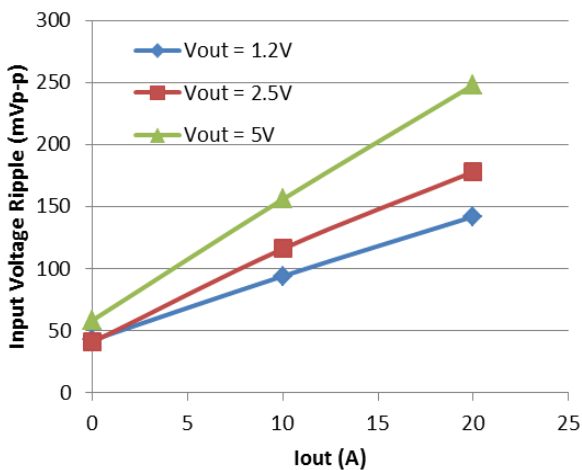

Figure 20. Input Ripple voltage vs load current for the 20A MicroDLynx* module at different output voltages showing a linear relationship between input ripple and load current (Vin = 12V, Vout = 1.2V, Cin = 4x22uF).

The input ripple voltage can be further reduced by increasing the amount of input capacitance. Figure 21 shows a set of curves for the 20A MicroDLynx module with 2x22μF and 3x22 μF ceramic capacitors across the module input, showing how ripple reduces with larger capacitance.

Decoupling the Input Bus for Extra-Low Ripple and Noise

In some applications, it may be necessary to reduce the input ripple of the POL converter to unusually low values. In such cases, the best cost and space saving approach for decoupling is to use a π–filter as shown in Figure 22. The inductor in the filter circuit increases the source impedance of the input bus. This in turn may cause input filter instability if the source impedance of the bus is not substantially lower than the input impedance of the POL converter. The value of the inductor should be chosen carefully such that it does not cause instability due to input-filter+converter interactions. It is recommended that the inductance be kept less than 0.5 μH.
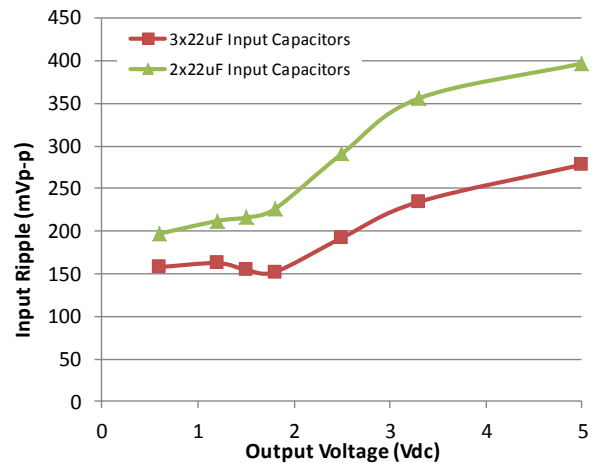

Figure 21. Input Ripple voltage vs output voltage for the 20A MicroDLynx module for two different input capacitor combinations.
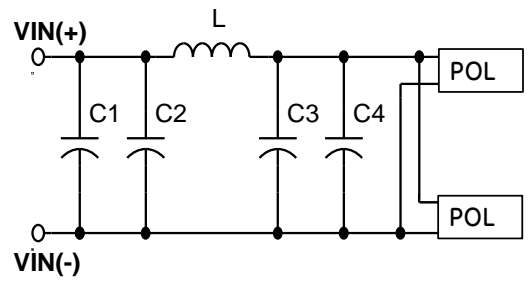

Figure 22. Circuit diagram showing a π-filter arrangement for input-bus decoupling.

Using Simulation for Input Filter Design

Circuit simulation can be used to predict the input ripple voltage and RMS currents flowing through individual capacitor branches. It is very important not to exceed the RMS current rating of the capacitors as it may cause component failures. Figure 23 shows a model of the POL converter with an input filter consisting of capacitors C6 and C7. In this particular example, an UDT020A0X3 module is shown. There are three 10 μF, 16V ceramic capacitors located inside the module, across the input pins. Under 12V input voltage bias, the capacitance of the ceramic capacitors declines as much as 20% from its nominal value. Therefore, in the PSpice model their value is adjusted downwards to 14.8μF. The effective series inductance (ESL) of the capacitor depends on the case size and for the 1210 capacitors used in UDT020A0X3, the ESL is 1 nH.

For simulating the input voltage ripple, the ESR at the switching frequency of POL converter should be used in the PSpice model. The ESR of the capacitor is critical in the accuracy of the simulation. Contact and trace resistance should also be included in the model if possible.

The current pulses drawn from the input bus by the buck converter are modeled using the current sources I1 and I2 which when combined create the trapezoidal input current waveform of a buck converter. The shape and amplitude of the current depends on the input voltage, programmed

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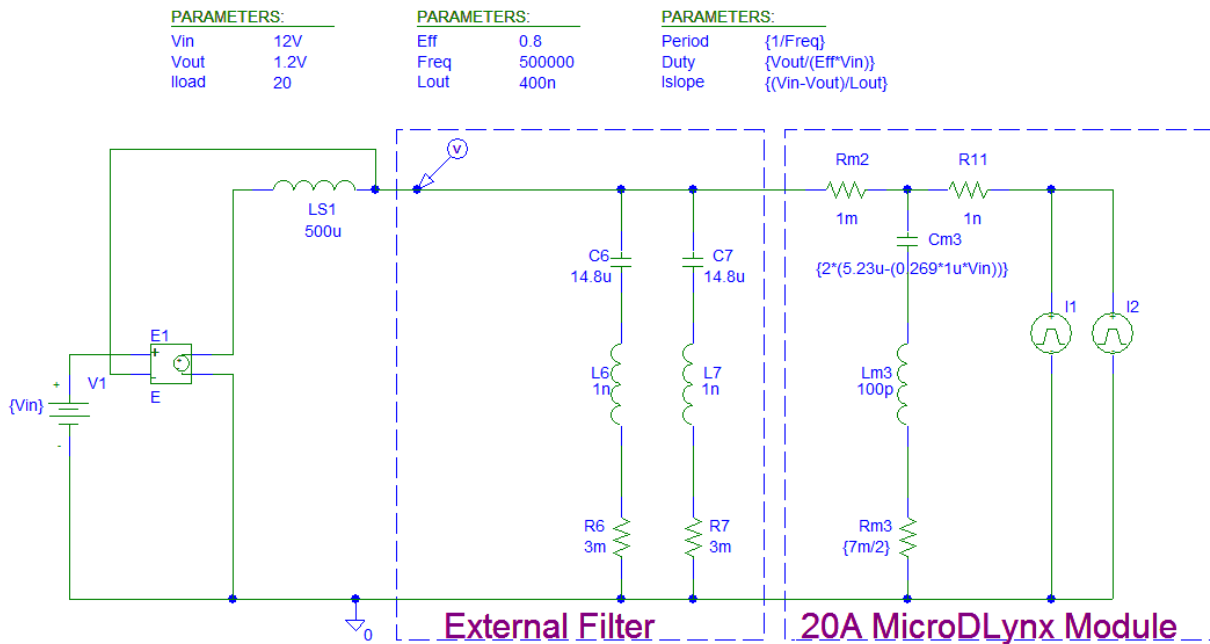| PARAMETERS:			PARAMETERS:			PARAMETERS:	
Vin	12V		Eff	0.8		Period	{1/Freq}
Vout	1.2V		Freq	500000		Duty	{Vout/(Eff*Vin)}
Iload	20		Lout	400n		Islope	{(Vin-Vout)/Lout}

Figure 23. PSpice simulation model of an example POL converter and input filter circuit.

output voltage, output inductor of the buck converter, output load current and the switching frequency.

The following example shows the power of simulation in designing input decoupling circuits. In Figure 21, the input ripple voltage for the 12V, 20A MicroDLynx module was plotted as a function of the output voltage at full load current of 20A, with two 22 μF ceramic capacitors at the input. The measured ripple voltage was 212mV p-p for 1.2V out. The oscilloscope picture showing the measured ripple voltage
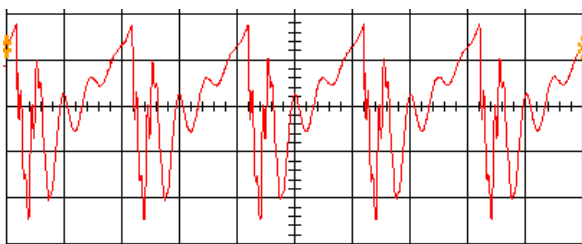

Figure 24. Measured input ripple voltage waveforms for the UDT020A0X3 module at an output voltage of 1.2V @ 20A, with two 22μF input capacitors (vertical scale: 50mV/div and time scale at 1μs/div).
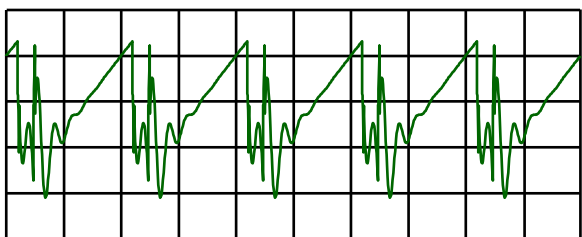

Figure 25. Simulated input ripple voltage waveforms for the UDT020A0X3 module at an output voltage of 1.2V @ 20A, with two 22μF input capacitors (vertical scale: 50mV/div and time scale 1μs/div).

waveform for this condition is shown in Figure 24. The results from simulation under the same operating conditions with the same decoupling circuit are shown in Figure 25 and indicate a peak-to-peak value of 170mV. The comparison of measured and simulated waveforms shows that reasonably accurate results can be obtained. Some adjustment of circuit simulation values may be needed if higher accuracy is desired. The ringing in the input ripple voltage waveform as seen in Figure 24, is affected by the ESL of the input ceramic capacitors and interconnect inductances, some of which are shown in the PSpice model of Figure 23.

One of the advantages of simulation is that it provides a way of calculating the RMS current flowing in each capacitor, a variable which is difficult to measure experimentally. The designer can thus easily check whether the maximum RMS current ratings of the capacitor are exceeded in a design.

Filtering the input bus of POL converters requires careful attention to component selection and PCB layout. Low ESR, surface mount multi-layer ceramic capacitors are the best choice for filtering high-frequency ripple voltage. Several graphs to aid the circuit designer in selecting input filter capacitors to use with POLs have been provided. If other capacitor technologies such as tantalum or aluminum electrolytics are utilized for load transient suppression on the input bus, they should always be used in parallel with ceramic capacitors. An excessive amount of current may cause failure of tantalum capacitors if they are used alone due to their high ESR. Finally, circuit simulation is shown to be an effective tool in predicting ripple voltage with the appropriate filter capacitors. Using simulation models, very effective filtering can be designed in a straightforward manner to meet most system requirements.

GE

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Output Filtering

Although a typical POL module contains an L-C filter on the output, most applications will require additional filtering for a variety of reasons. In applications that demand that output voltage deviation to load current transients be kept small, additional external capacitance must be added. The output voltage deviation is inversely proportional to the output capacitance and is also reduced by lower effective ESR from a number of output capacitors in parallel. Additional capacitance also leads to smaller output ripple. Low ESR polymer and ceramic capacitors are effective in improving the dynamic response of POL modules. For stable operation of the module, limit the capacitance to less than the maximum output capacitance as specified in the POL data sheet. Optimal performance of the module's transient response can be achieved by using the Tunable Loop™ feature available in GE POL modules.

The POL datasheet provides information on the output ripple measurements for various output voltages with output capacitance as the variable parameter. An example set of curves is shown in Fig. 26 for the MDT040 POL module, while Table 3 shows example data on the output ripple+noise reduction that can be achieved by using ceramic capacitors on the output. Using a high frequency low ESR and ESL capacitor close to the output terminals of the module reduces the total noise+ripple by 5 to 6 times as compared to a module without high frequency capacitors.
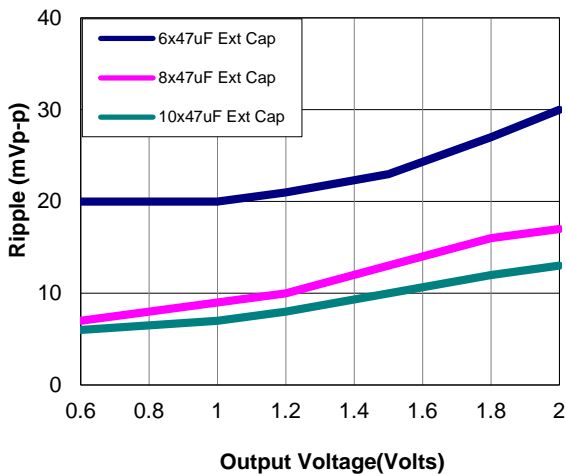

Figure 26. Output ripple voltage for various output voltages with external 6x47 µF, 8x47 µF or 10x47 µF ceramic capacitors at the output (40A load) for MegaDLynx* module. Input voltage is 12V. Scope Bandwidth limited to 20MHz.

Output Filtering for Very Low Ripple/Noise

In some demanding applications, output ripple and noise must be reduced to very low levels to avoid interference with sensitive load circuitry. External C-L-C filters as shown in Fig. 27 are effective in such situations. Care needs to be exercised when designing such filters to avoid stability issues. The first step in designing the external C-L-C filter is choosing an inductor. The current rating of the inductor has to be equal to

or larger than the maximum output current of the POL module to avoid the saturation. The next step is to choose the capacitors with dynamic response, size and voltage ratings as main determining factors. The resonant frequency of the external L_F-C_{F2} filter must be at least decade above the crossover frequency of the voltage control loop of the module to avoid interfering with the feedback loop.

Table 3: Output ripple measured for the 12A PicoDLynx module for Vin = 12V and various values of Output Capacitance

Output Voltage	Vout = 1.2V			Vout = 3.3V		
Load Current (A)	0	6	12	0	6	12
Output Capacitance	Measured Output Ripple + Noise (mVp-p)					
22uF Ceramic (minimum output capacitance required)	35	122	88	48	115	85
22uF Ceramic capacitor + High Frequency capacitor of 0.047uF/0402 size	28	29	30	47	48	49
High Frequency capacitor of 0.047uF/0402 size + 2x22uF ceramic capacitor	19	19	20	28	28	28

Proper care needs to be exercised when using external C-L-C filter or heavy capacitive loading used at the output. Connecting the remote sense pin of the module after the external C-L-C filter affects converter stability due to a double pole being introduced into the feedback loop. Therefore it is recommended to connect the remote sense pin before the external C-L-C filter as shown in Fig 27. Simulations can be must be used to verify the stability margins of the converter when external filtering is added to the output.
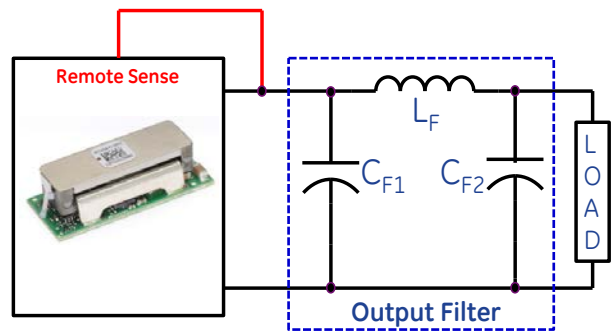

Figure 27. External C-L-C filter to reduce output ripple significantly.

Layout Guidelines

Location of the module

Location of the POL module should be carefully considered to minimize the effects of noise. POL modules are typically located as close as possible to the load. When multiple loads are powered from one module, it should be located closest to the most voltage sensitive load. If a trade-off between the length of the input and output traces needs to be made, the output trace should be made as small as possible. Suggested layout of the traces used to connect the modules and locations of external components are provided later in this application note. These considerations, along with good

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analog design layout practices are sufficient to achieve optimal performance when using these modules.

Minimizing loop area

To provide the most effective filtering and avoid noise coupling from a POL to other parts of the circuit, it is recommended that the loop area for both power and signal traces to the POL module be minimized. To minimize input noise, it is necessary to reduce the parasitic inductance of the input loop significantly, by reducing the loop area. Using a high frequency, low ESR and ESL bypass capacitor, close to the POL module input pins reduces the area of this loop significantly. Additional precautions to minimize loop area during board layout also help minimize the parasitic inductances.

Figure 28 shows a typical application circuit incorporating these recommendations. For reducing high-frequency switching noise at the input and output of the module, 0.047μF (0402), 0.1μF (0402), etc. small package ceramic capacitors should be placed at the input and output of the module. Capacitors used for minimizing the ripple component (CI2, CI3, CO2 & CO3) are termed as bulk capacitors with capacitance needed being in the order of tens or hundreds of μF.
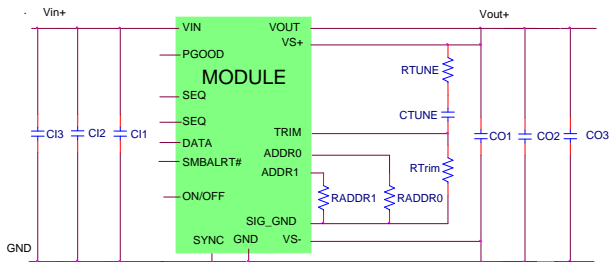

Figure 28. Typical Application Circuit of a DLynx series module.

Figure 29 shows an example layout for the PicoDLynx module. This example details the key guidelines to be followed when designing the module on to your board. For simplicity, all three power traces (input, output and ground) are assumed to be on the top layer of the PWB – where the PicoDLynx module is placed.

The guidelines are:

1. Extend the ground plane to the area underneath the module. It is not recommended that this space be utilized for routing signal traces unless they are in inner layers underneath the ground plane. Observe any keepout areas specified for the module.

2. The V_{OUT} and ground planes are placed close together to minimize interconnect inductance on the output side. Similarly on the input side, interconnect inductance is minimized by placing the V_{IN} and ground planes close together

3. Output capacitors (C_{OUT}) are connected as close to the output/ground pins as possible to provide the most effective output filtering. Similarly the input capacitors are placed as close to the input/pins as possible.
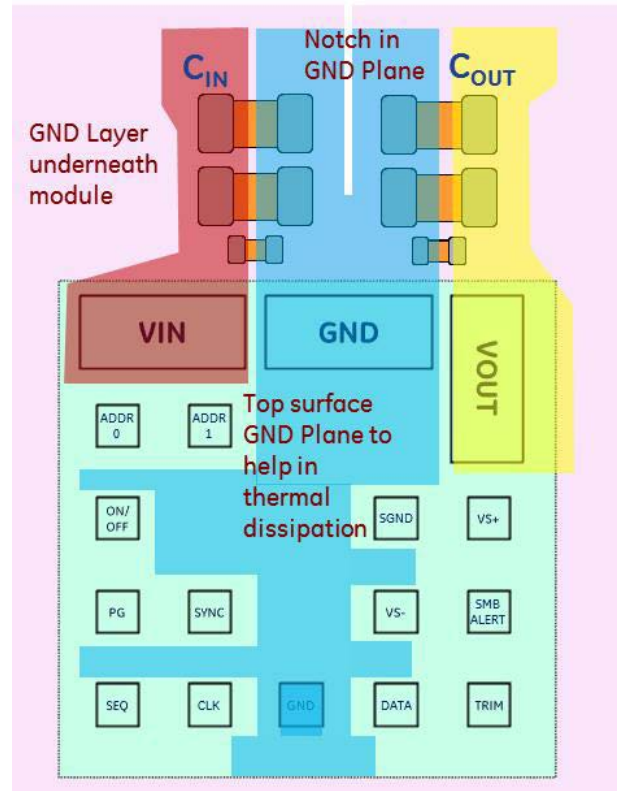

Figure 29. Simplified layout for the PicoDLynx series module.

4. Pinch traces slightly in the areas where filtering capacitors are placed to force current to flow near the capacitors.

5. Insert a notch in the GND Plane to separate GND currents flowing into the input and output pins. The length of the notch should be determined depending on current rating and cooling of modules. If the module is not force cooled, then the notch should not be too close to the Ground pin to allow for longer unbroken ground plane surface to conduct heat from the module ground pads. The same criteria should be applied for notch sizes among different current rating modules – the higher the module rating the further the separation of the notch from the ground pad.

6. The high frequency low ESR and ESL capacitors (usually 0.01μF or 0.0047μF capacitor in 0402 package should suffice) must be placed closest to the input and output terminals to provide the shortest loop for noise attenuation. The placement of these capacitors should take priority in terms of proximity to the module as compared to other higher value capacitors on both input and output terminals.

Location of Filtering Components

It is desirable to have the POL, filter capacitors and input and output traces all on the same layer. However, practical considerations may require the use of multiple vias to either connect to the input and/or output to a different board layer. There are 2 possible layouts with the use of vias.

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In the first and preferred layout arrangement both input and output capacitors are on the same layer as the module. Connections are then made vias to inner layers if needed. The high frequency capacitors are placed closest to the module before the vias are placed. A rule of thumb is to have 3A/per via. The recommended via size is 22 mils (0.022" or 560µm) plated-through hole. For control pins, one via per pin is sufficient. Vias should be located in the direction of current flow for optimum performance. For signal traces, the recommended trace width for signal traces is 7 – 10 mils (180 - 250µm). For bulk capacitors, 1-2 vias per capacitor connection are recommended. It is important that the vias be located past the input/output filter caps. Figure 30 shows a layout of the PicoDLynx module showing vias located one the output, input and ground traces for carrying current to the inner layers.
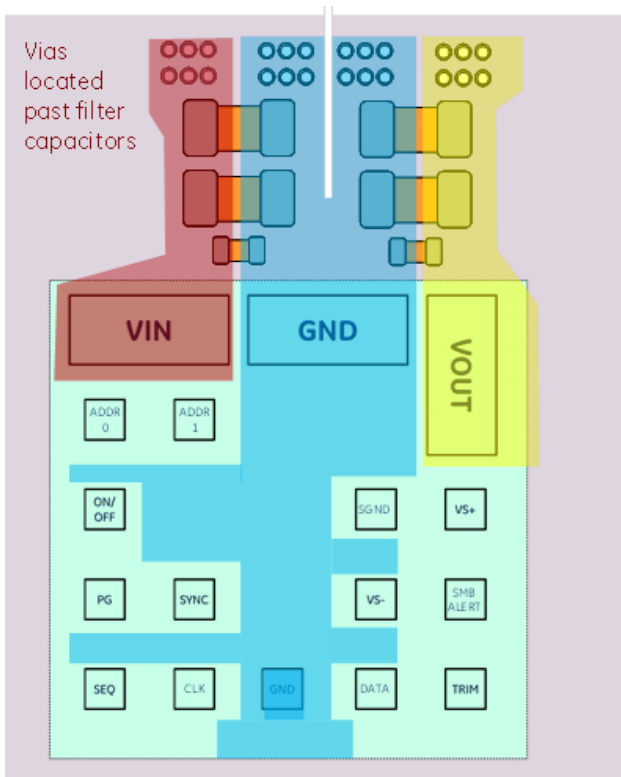

Figure 30. Layout for the PicoDLynx series module with vias for output and input power connections.

Layout Recommendations for High Density Layouts

The second and less acceptable arrangement, shown in Fig. 31, is where the bulk filter capacitors are located on the opposite layer from the module (module on top layer and filter capacitors on bottom layer and vice-versa). In this case it is important that the high frequency filtering capacitors still be located on the same layer as the module and only the bulk capacitors be located on the opposite layer. If the Voltage Sense+ (VS+) and Voltage Sense- (VS-) connection also need to be routed through vias to the opposite layer, they should connect through a 0 ohm resistor on the module layer. TRIM and SGND are sensitive, high-impedance analog terminals.

Keep traces connecting them separate from DATA, CLK and SMBALERT traces. Running the CLK, DATA and SMBALERT traces under the GND plane and in one of the inner layers would help to isolate the noise from sensitive traces like the one connecting TRIM and SGND. Like the high frequency capacitors, it is recommended that the trim resistor and tunable loop components be on the same layer (preferably on top) and close to the module. If the return path for the TRIM is being connected to a SGND, Vs- or GND do not connect that return path to any other trace on the board. This is relevant when multiple modules are being used either individually or in parallel. The return connections from the trim resistor for each module should terminate directly back to the module pin and not be tied to a common return/ground path.

Clearances around the Module

Signal traces should not be routed underneath the module, unless sandwiched between ground planes, to avoid noise coupling. Also, components should not be placed under the module to prevent any coupling. The ground plane can be placed under the module. For repair and removal of the SMT module from the PWB, 4.0 mm (0.16 inches) of clearance is recommended around the module outline. This clearance provides and isolates adjacent components from exposure to heat during the removal process.

Example Layouts for other DLynx* Series

The DLynx series of modules include the PicoDLynx, the MicroDLynx and the MegaDLynx modules. Figure 32 shows a suggested layout for the MicroDLynx module while Figure 33
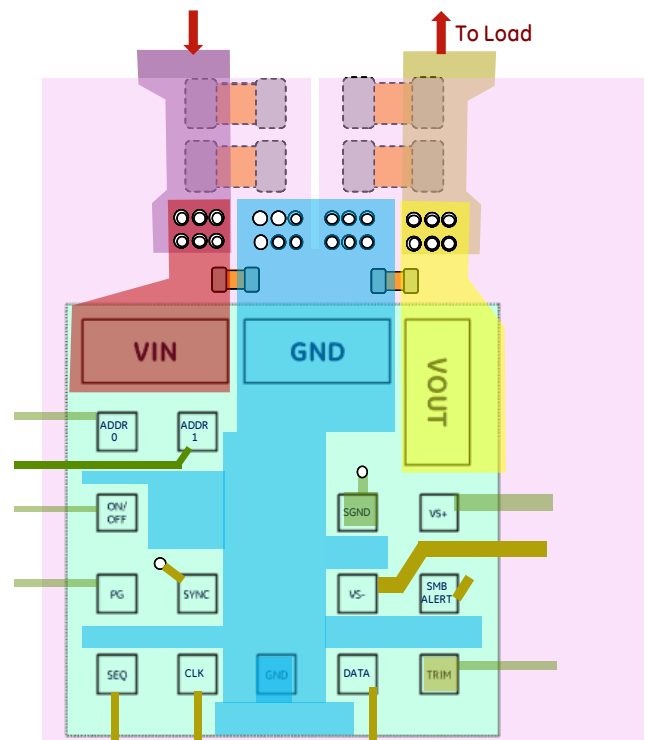

Figure 31. Layout for the PicoDLynx series module with vias for bulk caps, input-output power and suggested control connections.

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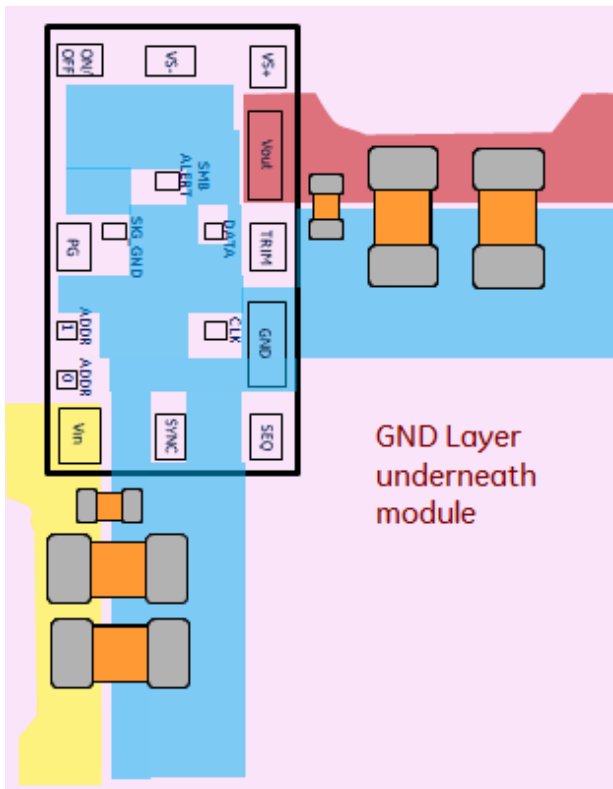## AN13-001 Filtering and Layout Guidelines for Non-Isolated Converters

Figure 32. Suggested Layout for the MicroDLynx series module.
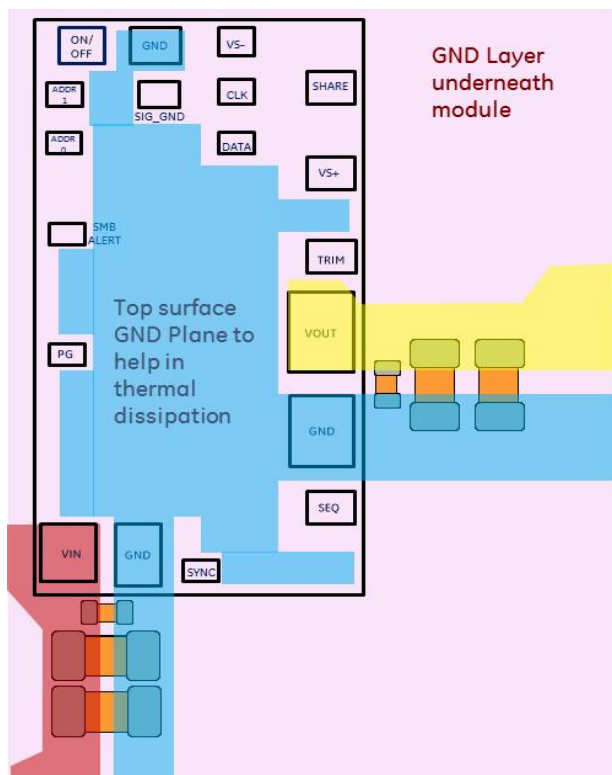

Figure 33. Suggested Layout for the MegaDLynx series module.

shows a layout for the MegaDLynx modules. The same broad considerations that were shown for the PicoDLynx module also apply for these.

Summary

POL Modules have switching frequencies in the range of few hundred kilohertz to Megahertz. The high switching frequencies, even though beneficial in reducing size and cost of the POL module, can cause problems by way of high frequency noise and EMI issues if not carefully designed. This application note explains the remedial measures that the designer can take during the board design phase by following the suggested layout guidelines and designing appropriate filtering components and circuits.

Filtering the input bus of POL converters requires careful attention to component selection and PCB layout, both of which have been discussed in detail here. Low ESR, surface mount multi-layer ceramic capacitors are the best choice for filtering high-frequency ripple voltage. Several graphs to aid the circuit designer in selecting the right input filter capacitors to use with POLs have been provided. If other capacitor technologies such as tantalum or aluminum electrolytics are utilized for load transient suppression on the input bus, they should always be used in parallel with ceramic capacitors.

Finally, circuit simulation is shown to be an effective tool in predicting ripple voltage and the RMS currents through the filter capacitors. Using simulation models, very effective filtering can be designed in a straightforward manner to meet most sets of requirements. Several example layouts for the DLynx series of modules have been presented to illustrate the important principles involved in designing GE POLs into an application. In addition, guidelines for via sizing, number of vias and their placement have been provided. For specific questions in specialized applications and also evaluation board layout, please consult your local GE Technical Representatives for additional information.

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Application Note

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