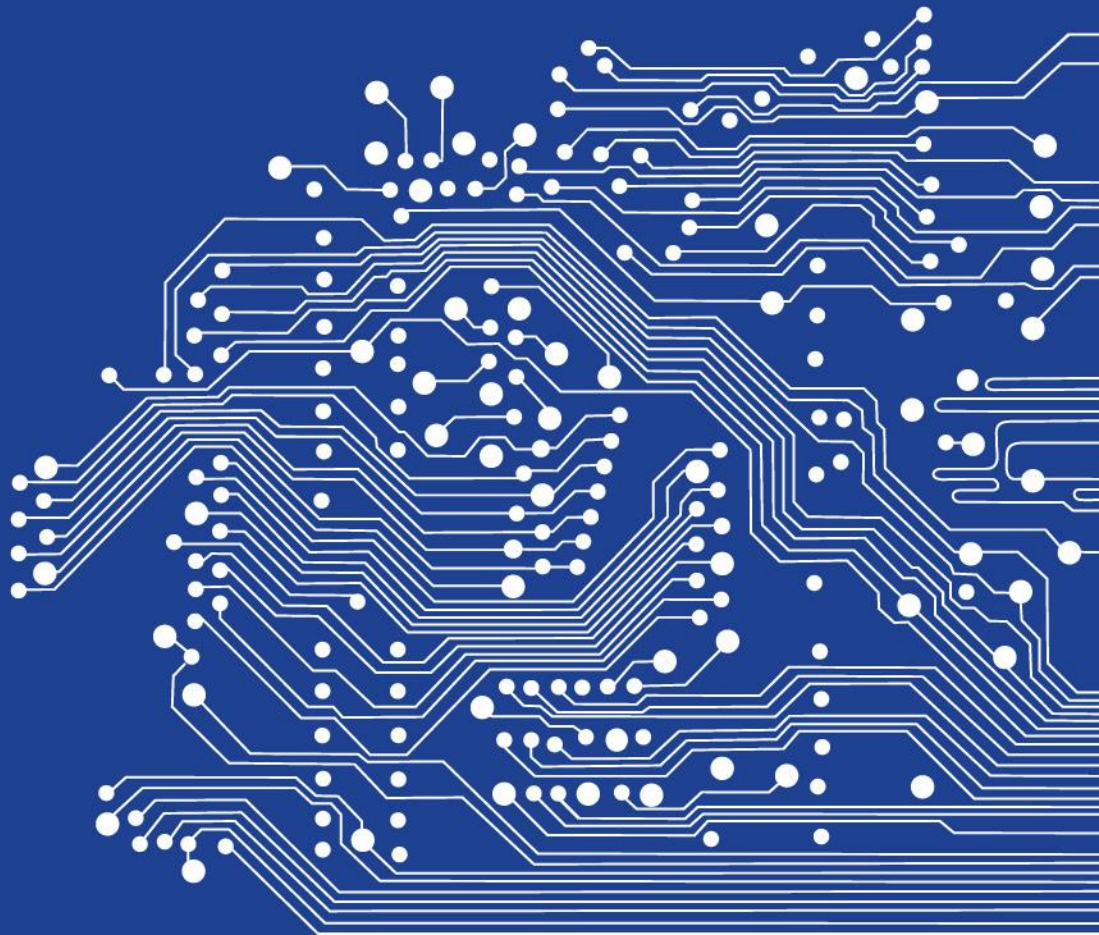
# DLynx Evaluation board with Top and Bottom Layer capability

Feb 2012



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# Introduction and Summary

- During the APTS006 modification project, GE Energy offered to develop an evaluation board that would be more representative of current board designs where modules are being placed on the top layer and filter capacitors on bottom layer and also demonstrate the layout guidelines provided in GE Application Notes.

- A new 4 layer evaluation board with the same form factor as previous generation boards was developed with a layout focused solely on the PICO DLynx modules. The same form factor allows this board to be used in kits currently using the dual footprint boards

- Using the new evaluation board a test plan was developed to measure the input and output High Frequency(HF) noise performance using the PDT012

# LAYOUT & PLACEMENT RECOMMENDATIONS:

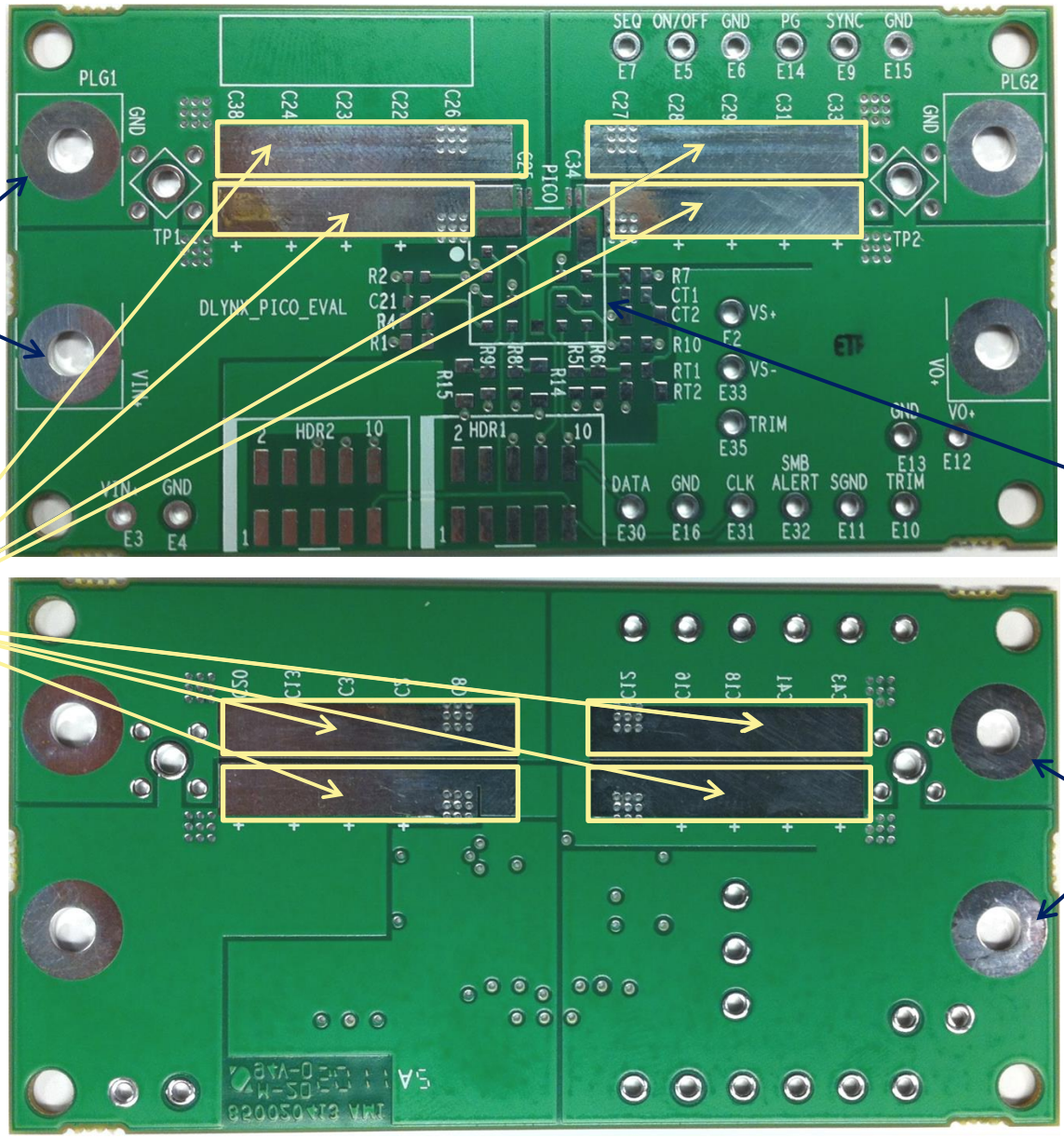
- DECOUPLING CAPS:
  1. Small ceramic ~0306 0.047 µF or 0.01 µF closest to module input.
  2. Input/output caps connected prior to planes.
  3. Smallest caps closest to the module input and output.

- LAYOUT & VIAS:
  1. Minimize loop area including vias.
  2. Extend ground plane underneath module.
  3. Copper planes should be used for routing power.
  4. Separate layers for input, output, input ground and output ground, if possible.
  5. Power & ground planes immediately adjacent.
  6. Input and input ground close to each other and module.
  7. Input ground and output ground layers should be separated elsewhere.
  8. 3A/per power via. 22 mils. Vias located in the direction of current flow.
  9. One via per control pin. Signal traces 7 – 10. 1-2 vias per bulk capacitors.
  10. Avoid signal traces under module unless sandwiched between ground.

# Detailed Recommendations & Explanations

- **DECOUPLING CAPS:**
  1. For input decoupling of the high-frequency ripple & noise: Low ESL & ESR ceramic capacitors (0.047 µF & 0.1 µF small-package ~0306) are recommended & should be placed at the module input and output. [AN04-002, AN04-006]
  2. Layout is important in dealing with high frequency switching ripple and noise. The figure above demonstrates that input/output caps should be connected prior to source or load planes. [AN04-002, AN04-006]
  3. The smallest (both in value and physical size) capacitors are placed closest to the module input. Ceramic capacitors should be placed as close as possible to the input of the POL module. [AN04-002, AN04-006]
- **LAYOUT & VIAS:**
  1. The loop area for both power and signal traces to the dc-dc module be minimized. Via distances are a significant consideration at MHz range & should not be used prior to filter caps. [AN04-006]
  2. Extend the ground plane to the area underneath the module. [AN04-006]
  3. Whenever possible, copper planes should be used for routing power traces (input, output and ground connections. [AN04-006]
  4. One layer can be assigned to input voltage feeding multiple modules. The output can either be another layer or part of a layer. In applications where the layout is very tight, input and output may only be portions of inner layers. [AN04-006]
  5. Input and output layers should have ground planes immediately adjacent (above or below). [GENERAL]
  6. Interconnect inductance is minimized by placing the input and ground planes close together and close to the module and the input capacitors are placed as close to the input pads as possible. [AN04-006]
  7. Input and output ground layers should be separated. [GENERAL]
  8. When inner layers are used with SMT modules, multiple vias are needed to carry the current from the top layer to the inner power planes. A rule of thumb is to have 3A/per via. The recommended via size is 22 mils (0.022" or 560µm) plated-through hole. Vias should be located in the direction of current flow. [AN04-006]
  9. For control pins, one via per pin is sufficient. For signal traces, the recommended trace width for signal traces is 7 – 10 mils (180 - 250µm). For bulk capacitors, 1-2 vias per capacitor connection are recommended. [AN04-006]
  10. Signal traces should not be routed underneath the module, unless sandwiched between ground planes, to avoid noise coupling. [AN04-006]

# New DLynx Evaluation Board – Top & Bottom Layers

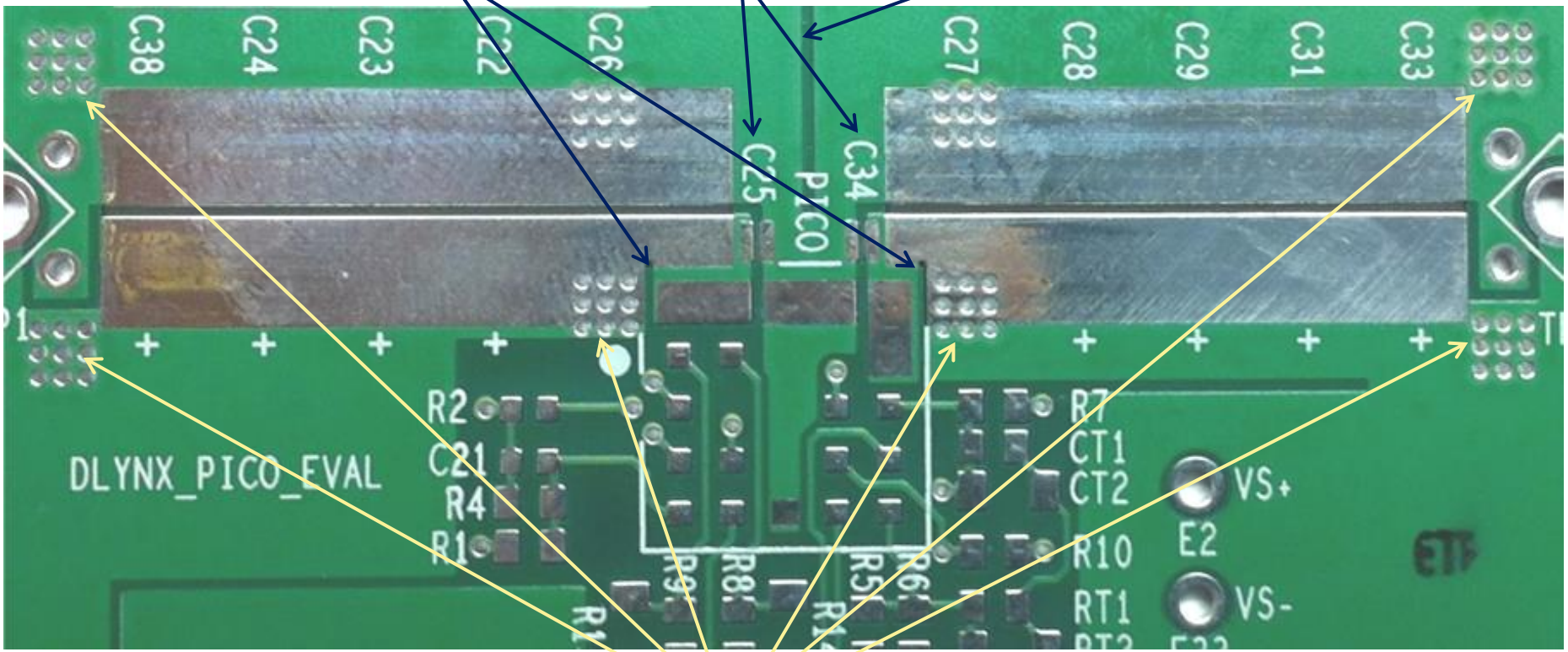


# New DLynx Board – Top & Bottom Layers

Notch in Vin, Vout layers to force currents to flow past capacitors

Low ESL decoupling capacitor pads (Input and Output)

Notch in Copper separating grounds for input and output



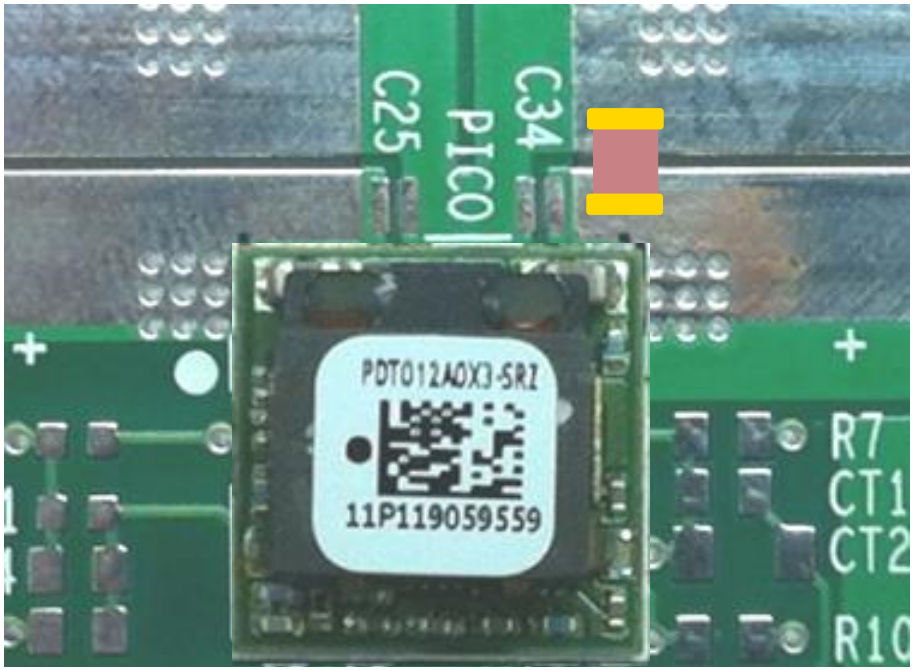

Vias to couple top and bottom layers

# Filtering Test Procedure

- Start with module + test board + 22µF output capacitor (minimum required output capacitance)
- Output/Input capacitors used are 0306 size low-ESL 0.047µF and 1210 size 22µF ceramic
- Input and output ripple measurements done using oscilloscope probes inserted in probe sockets
- All measurements made with maximum bandwidth available on scope (400MHz) and probe set at 10X (minimum probe capacitance)
- Sequence of tests with additional capacitance added on input/output and top/bottom of test board

# Test Results – Unfiltered Board (22µF on Vout)

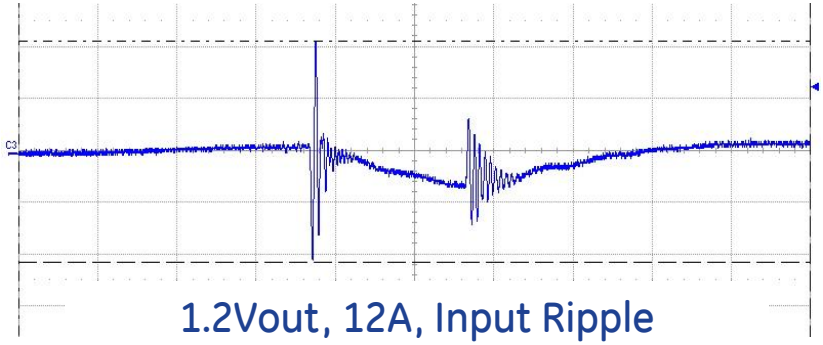
Only 22µF capacitor added on output (min. required)




| Input Caps | | Output Caps | |
|---|---|---|---|
| Top | Bottom | Top | Bottom |
| | | 22µF | |
| | | | |

| 1.2V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 1800 | 8900 | 8500 | 35 | 122 | 88 |

| 3.3V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 900 | 8400 | 8300 | 48 | 115 | 85 |



1.2Vout, 12A, Input Ripple
2V/div. & 100ns/div.

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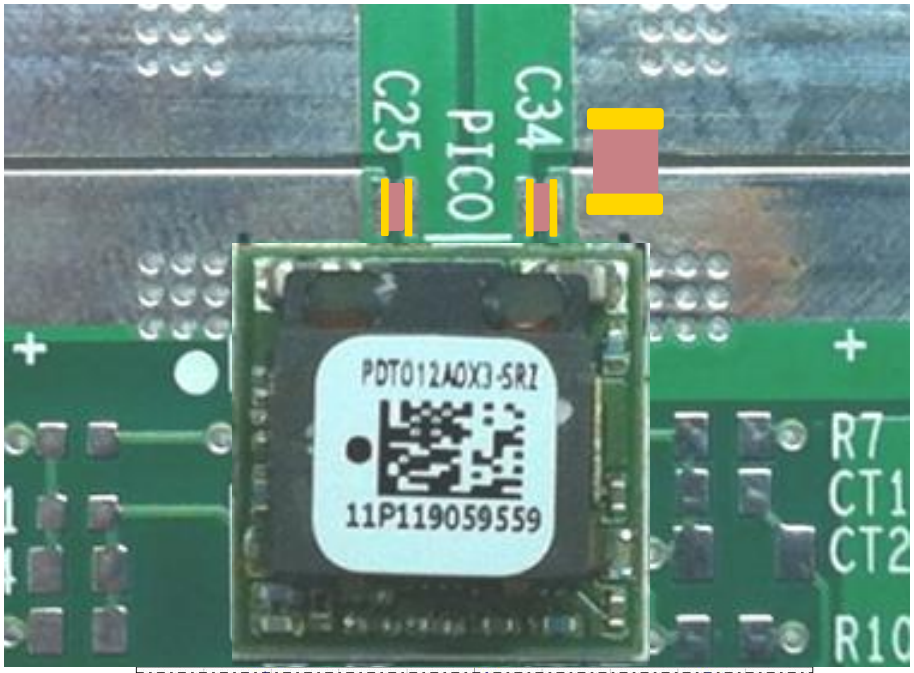
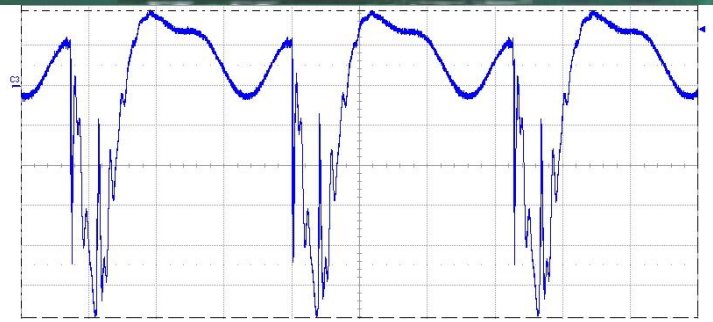
# Test Results – Filtered Board

22µF capacitor added on output (min. required) + hi-freq. input/output caps (top)



1.2Vout, 12A, Input Ripple
200mV/div. & 500ns/div.

| Input Caps | | Output Caps | |
|---|---|---|---|
| Top | Bottom | Top | Bottom |
| | | 22µF | |
| Hi-Freq. | | Hi-Freq. | |

| 1.2V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 232 | 1088 | 1536 | 28 | 29 | 30 |

| 3.3V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 471 | 1244 | 2120 | 47 | 48 | 49 |

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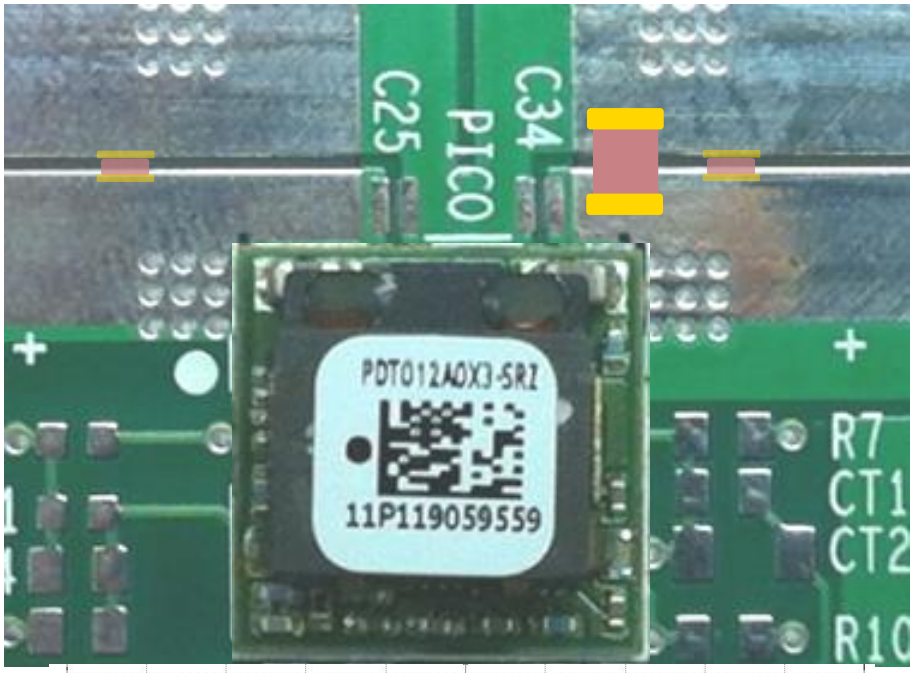
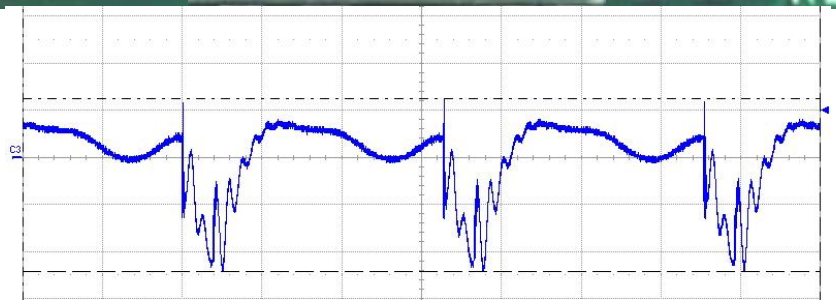
# Test Results – Filtered Board

22µF capacitor added on output (min. required) + hi-freq. input/output caps (bottom)



1.2Vout, 12A, Input Ripple
500mV/div. & 500ns/div.

| Input Caps | | Output Caps | |
|---|---|---|---|
| Top | Bottom | Top | Bottom |
| | | 22µF | |
| | Hi-Freq. | | Hi-Freq. |

| 1.2V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 245 | 1284 | 1840 | 25 | 30 | 30 |

| 3.3V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 454 | 1354 | 2140 | 47 | 48 | 49 |

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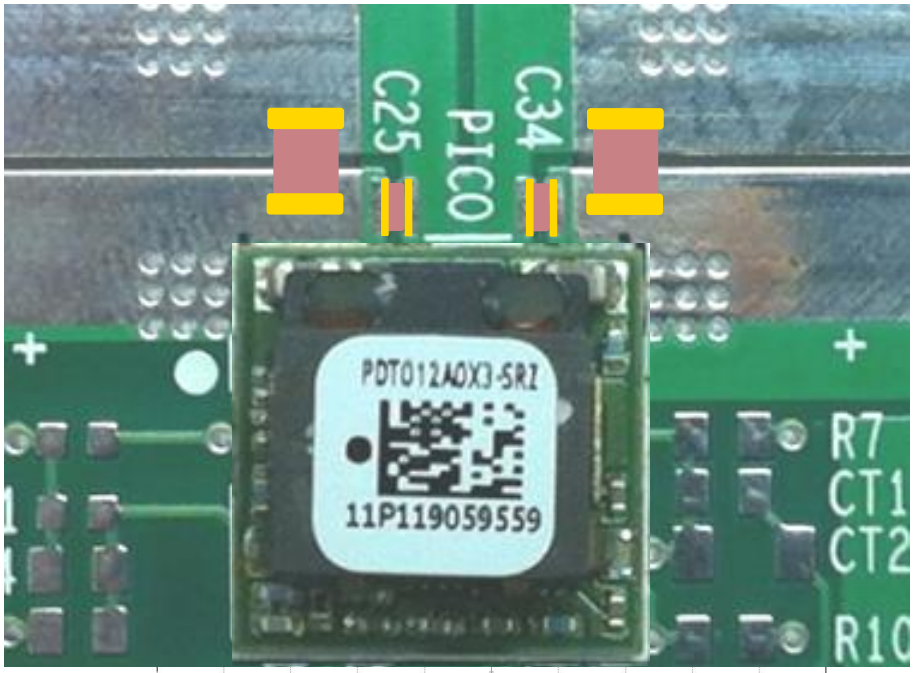
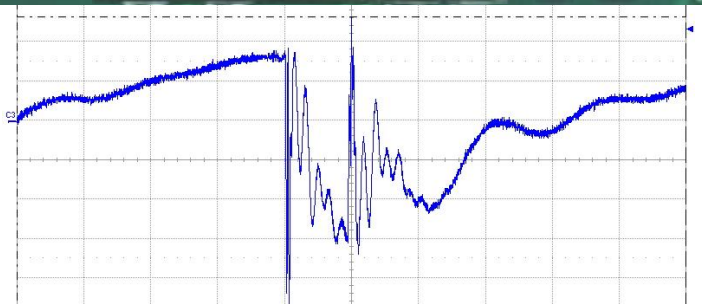
# Test Results – Filtered Board (cont.)

22µF capacitor added on output (top)+ hi-freq. input/output caps+22µF input cap (top)



1.2Vout, 12A, Input Ripple
50mV/div. & 200ns/div.

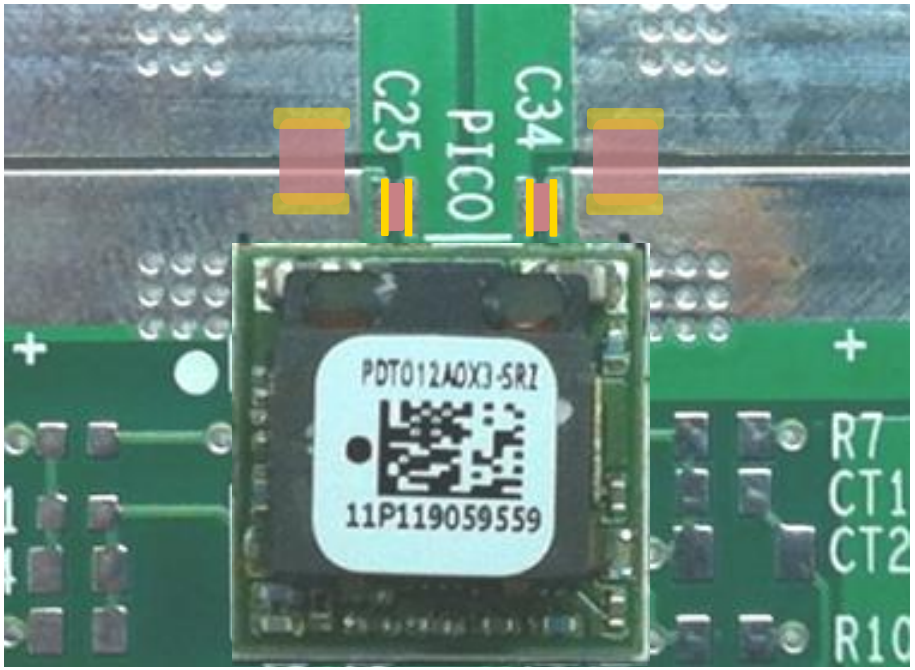
| Input Caps | | Output Caps | |
|---|---|---|---|
| Top | Bottom | Top | Bottom |
| 22µF | | 22µF | |
| Hi-Freq. | | Hi-Freq. | |

| 1.2V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 65 | 341 | 366 | 28 | 28 | 28 |

| 3.3V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 57 | 332 | 464 | 49 | 47 | 48 |

# Test Results – Filtered Board (cont.)

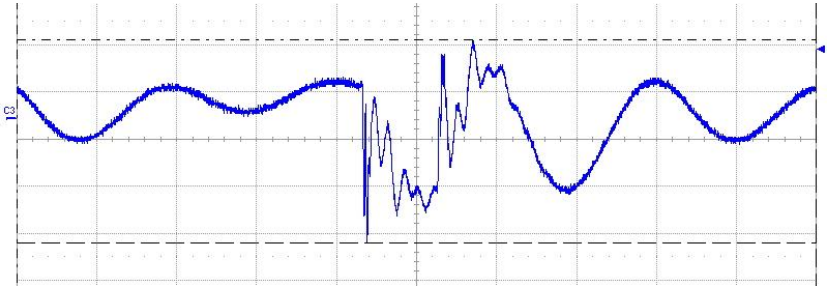
22µF capacitor added on output (bot)+ hi-freq. input/output caps+22µF input cap (bot)




| Input Caps | | Output Caps | |
|---|---|---|---|
| Top | Bottom | Top | Bottom |
| | 22µF | | 22µF |
| Hi-Freq. | | Hi-Freq. | |

| 1.2V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 52 | 290 | 429 | 27 | 29 | 31 |

| 3.3V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 71 | 277 | 339 | 49 | 48 | 49 |



1.2Vout, 12A, Input Ripple
100mV/div. & 200ns/div.

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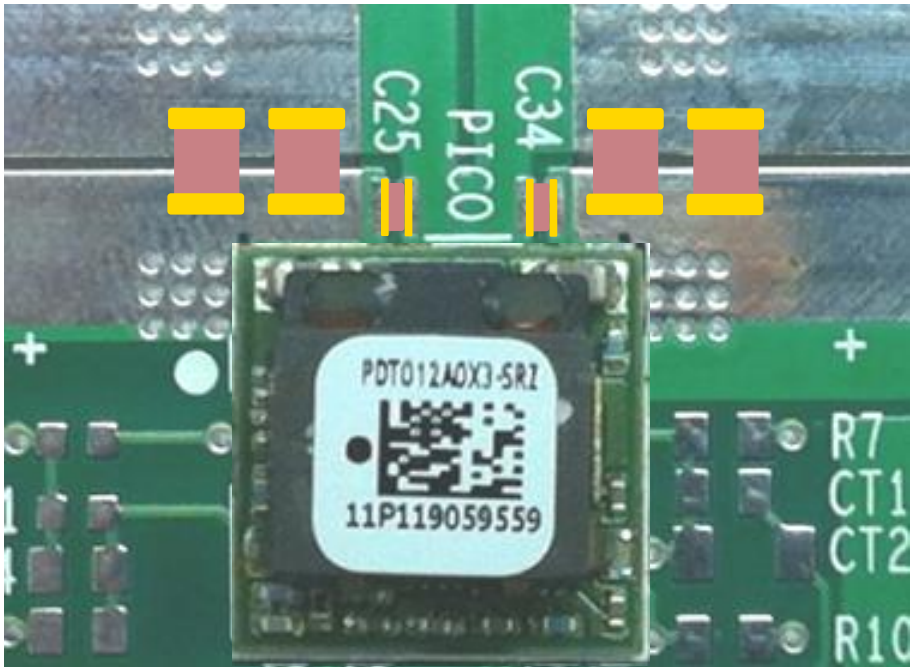
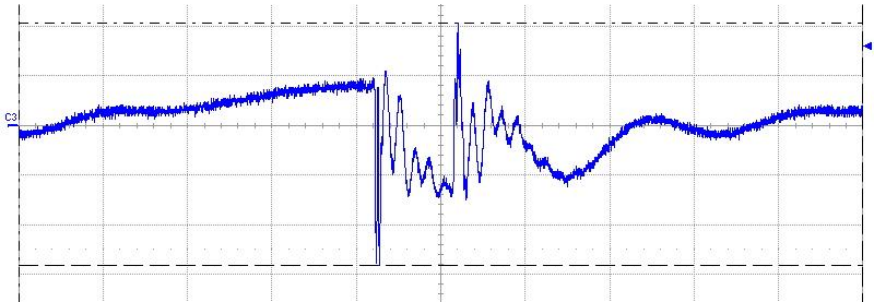
# Test Results – Filtered Board (cont.)

2x22µF capacitor added on output (top) + hi-freq. input/output caps+2x22µF input cap (top)



1.2Vout, 12A, Input Ripple
50mV/div. & 200ns/div.

| Input Caps | | Output Caps | |
|---|---|---|---|
| Top | Bottom | Top | Bottom |
| 2x22µF | | 2x22µF | |
| Hi-Freq. | | Hi-Freq. | |

| 1.2V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 37 | 200 | 245 | 19 | 19 | 20 |

| 3.3V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 35 | 202 | 237 | 28 | 28 | 28 |

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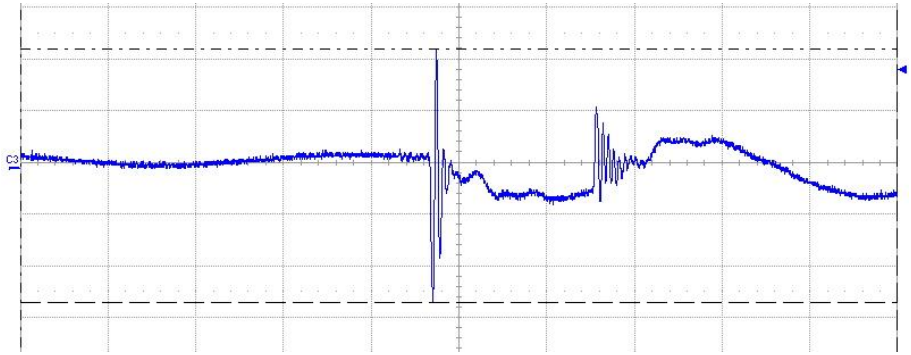
# Test Results – Filtered Board (cont.)

2x22µF capacitor added on output (bot) + hi-freq. input/output caps (bot) +2x22µF input cap (bot)


| Input Caps | | Output Caps | |
|---|---|---|---|
| Top | Bottom | Top | Bottom |
| | 2x22µF | | 2x22µF |
| | Hi-Freq. | | Hi-Freq. |

| 1.2V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 173 | 910 | 978 | 21 | 21 | 21 |

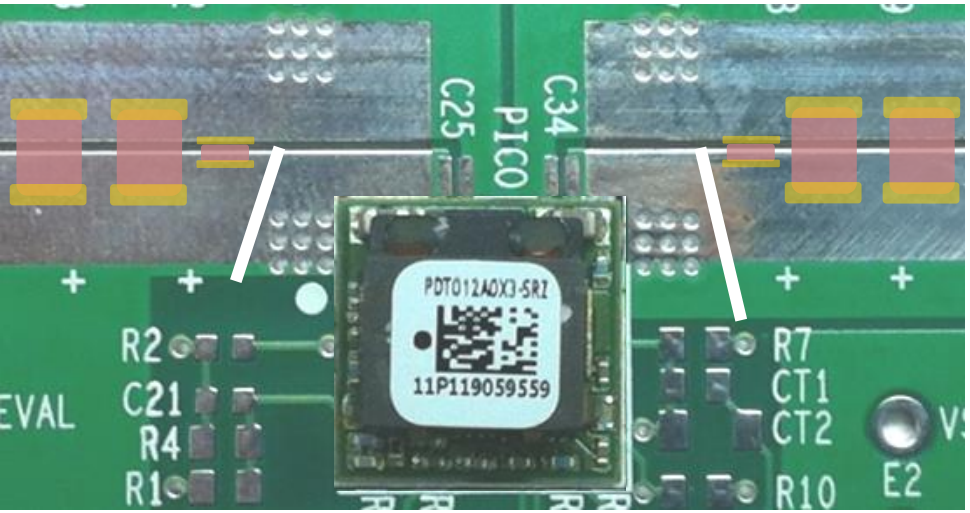
| 3.3V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 70 | 852 | 960 | 29 | 28 | 33 |

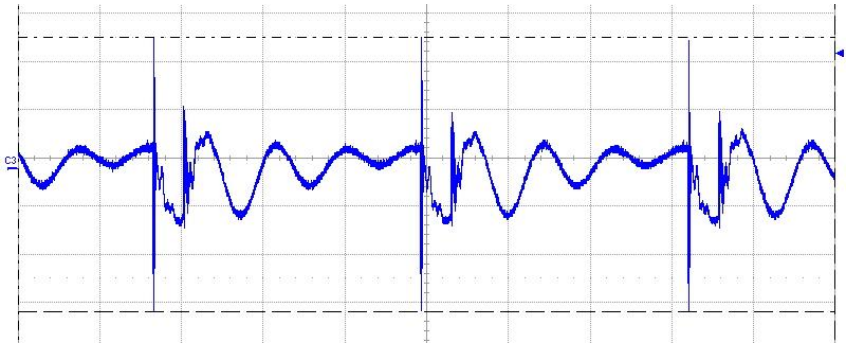


1.2Vout, 12A, Input Ripple
200mV/div. & 100ns/div.

# Test Results – Filtered Board (cont.)

2x22µF capacitor added on output (bot) + hi-freq. input/output caps+2x22µF input cap (bot) +cuts



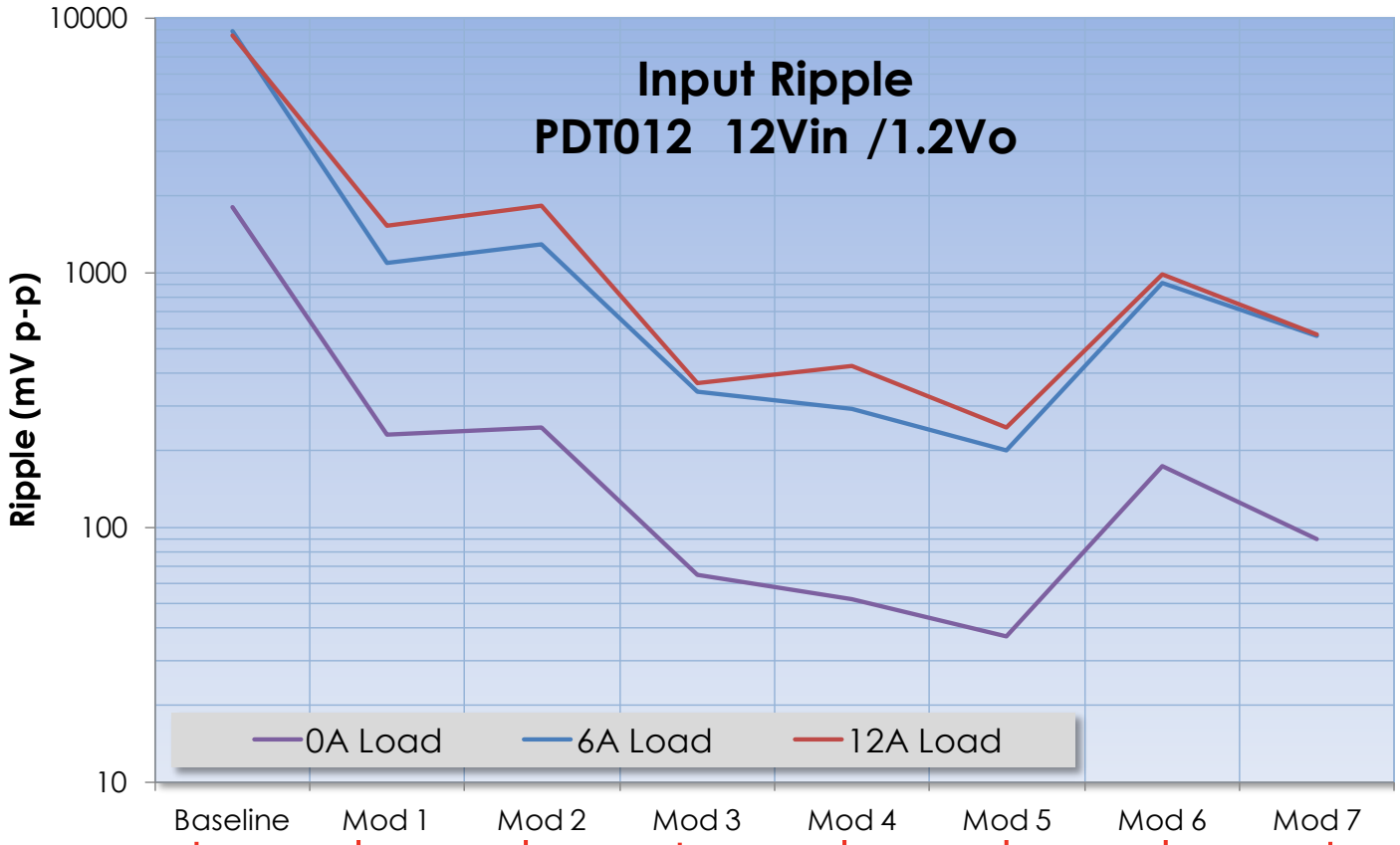
1.2Vout, 12A, Input Ripple
100mV/div. & 500ns/div.

| Input Caps | | Output Caps | |
|---|---|---|---|
| Top | Bottom | Top | Bottom |
| | 2x22µF | | 2x22µF |
| | Hi-Freq. | | Hi-Freq. |

| 1.2V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 90 | 565 | 570 | 18 | 21 | 22 |

| 3.3V | | | | | |
|---|---|---|---|---|---|
| Input Ripple (mV p-p) | | | Output Ripple (mV p-p) | | |
| 0A | 6A | 12A | 0A | 6A | 12A |
| 52 | 532 | 549 | 27 | 28 | 27 |

# Input Ripple Summary (1.2Vo)




22µF Output (top)

22µF Output (top) + HF caps (top)

22µF Output (top) + HF caps (bot)

22µF Output/Input (top) + HF caps (top)

22µF Output/Input (top) + HF caps (bot)

2x22µF Output/Input (top) + HF caps (top)

2x22µF Output/Input (bot) + HF caps (top)

2x22µF Output/Input (top) + HF caps (top) + top etch cuts

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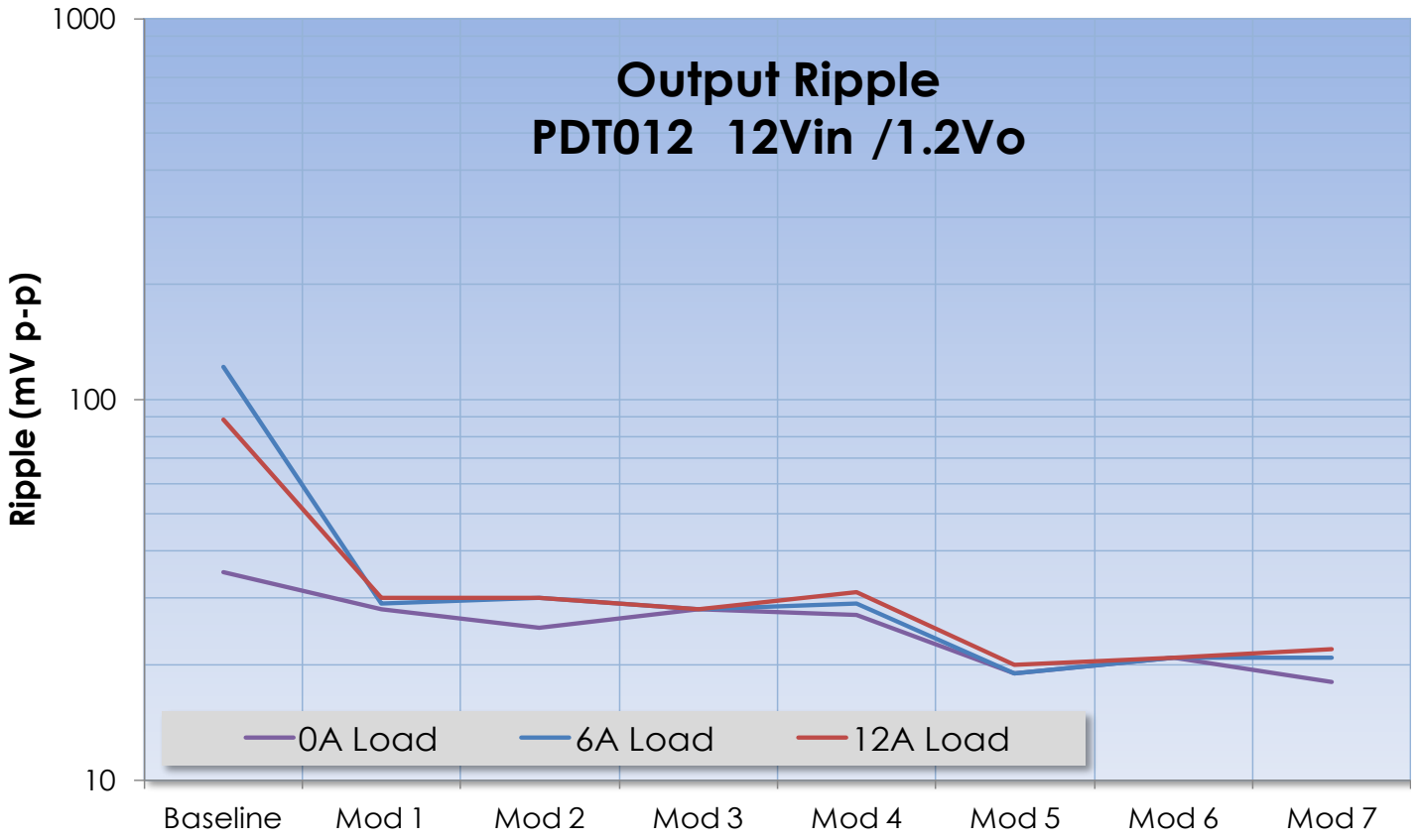
# Output Ripple Summary (1.2Vo)




22µF Output (top)

22µF Output (top) + HF caps (top)

22µF Output (top) + HF caps (bot)

22µF Output/Input (top) + HF caps (top)

22µF Output/Input (top) + HF caps (bot)

2x22µF Output/Input (top) + HF caps (top)

2x22µF Output/Input (bot) + HF caps (top)

2x22µF Output/Input (top) + HF caps (top) + top etch cuts

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# Conclusions and Summary

- During the APTS006 modification project, GE Energy offered to develop an evaluation board that would be more representative of current board designs where modules are being placed on the top layer and filter capacitors on bottom layer and also demonstrate the layout guidelines provided in GE Application Notes.

- A new 4 layer evaluation board with the same form factor as previous generation boards was developed with a layout focused solely on the PICO DLynx modules. The same form factor allows this board to be used in kits currently using the dual footprint boards

- Using the new evaluation board a test plan was developed to measure the input and output High Frequency(HF) noise performance using the PDT012

- As per the results of the measurements, it can be quantitatively demonstrated that HF noise can be substantially reduced by the recommended placement of decoupling and bulk capacitors on either layer and being powered from either layer.