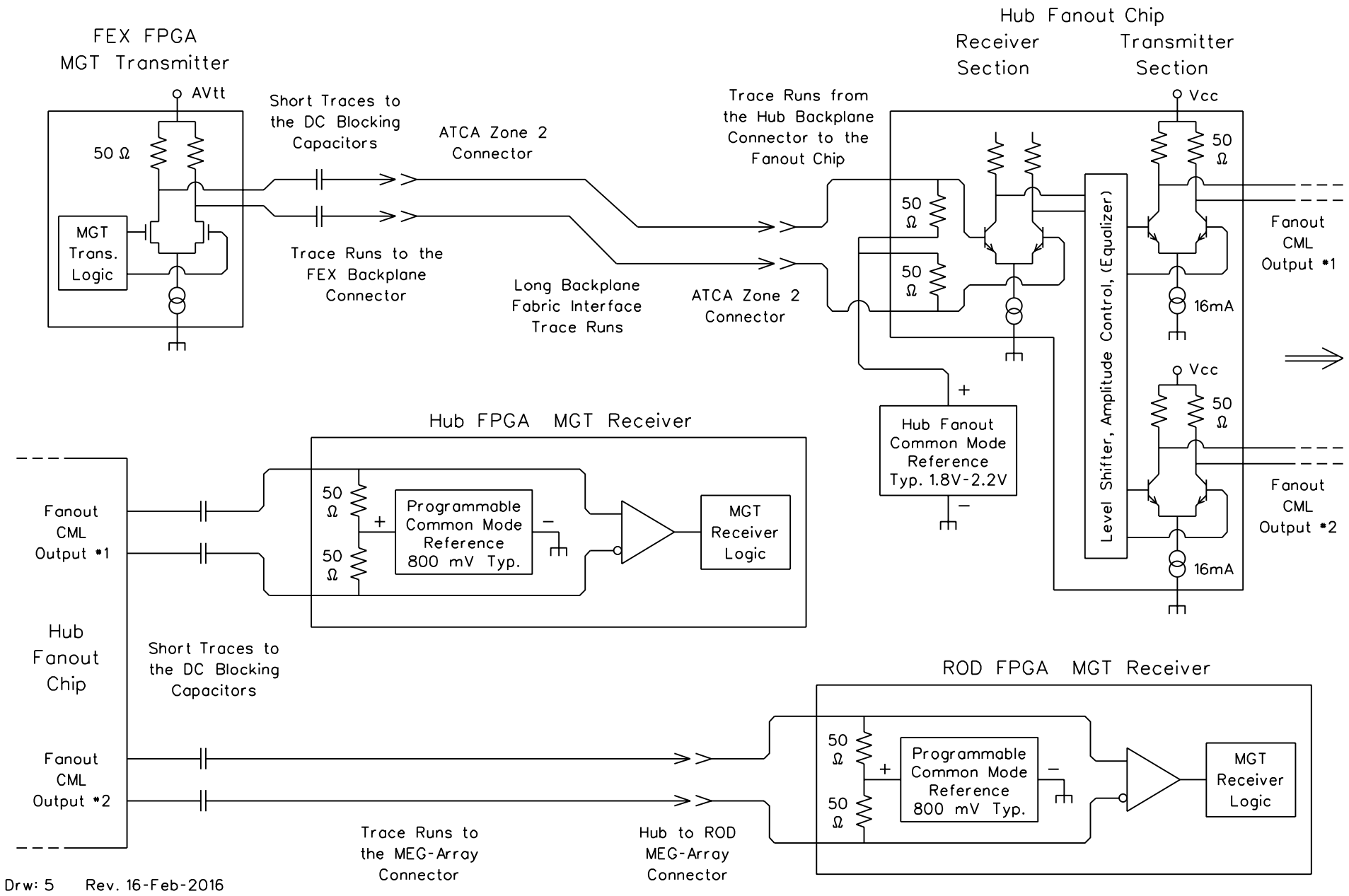
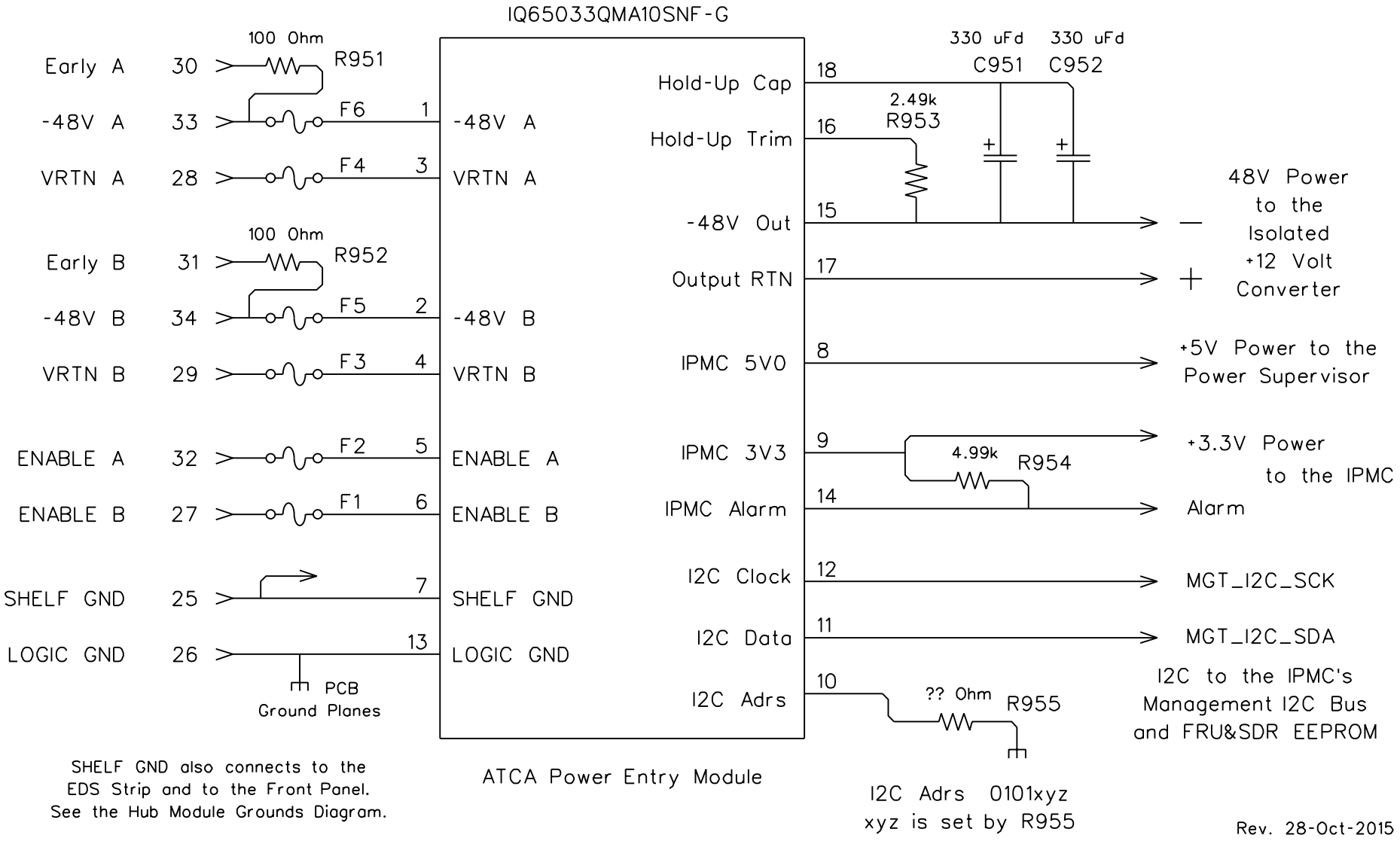
Data Path - FEX to Hub and then to ROD



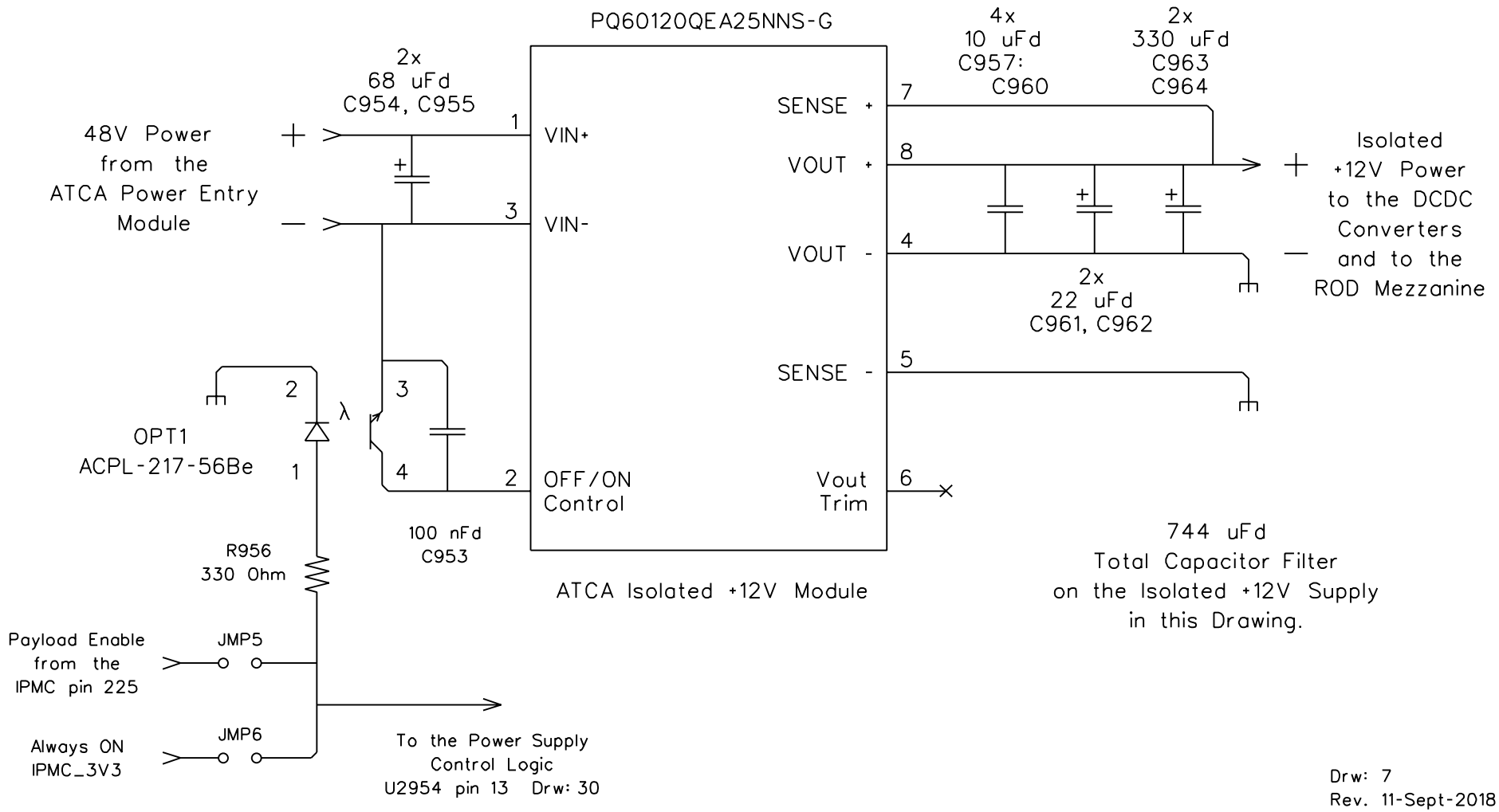
Drw: 5 Rev. 16-Feb-2016

Hub-Module ATCA Power Entry

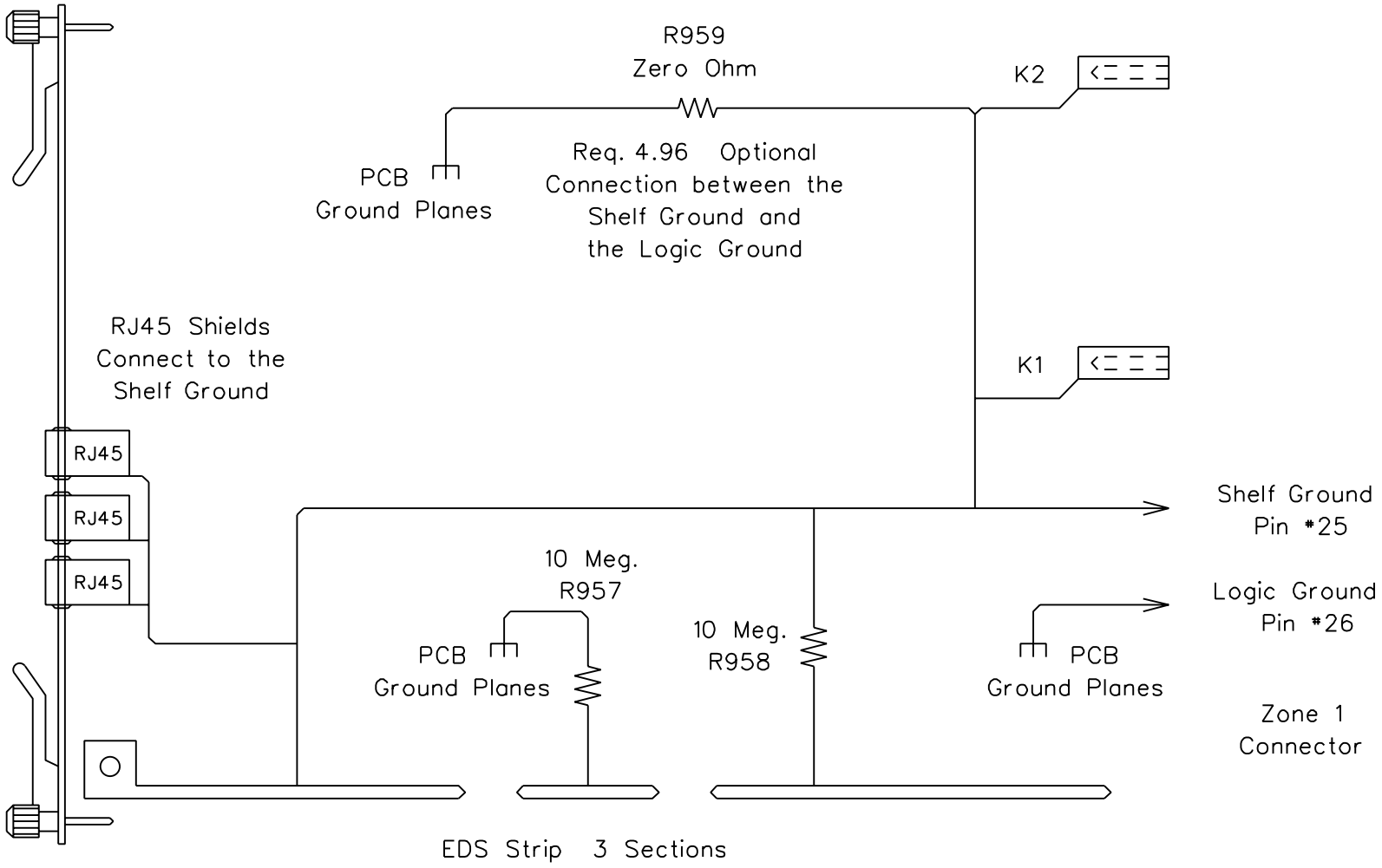


Rev. 28-Oct-2015

Hub-Module Isolated +12V Supply



Hub-Module Ground Connections

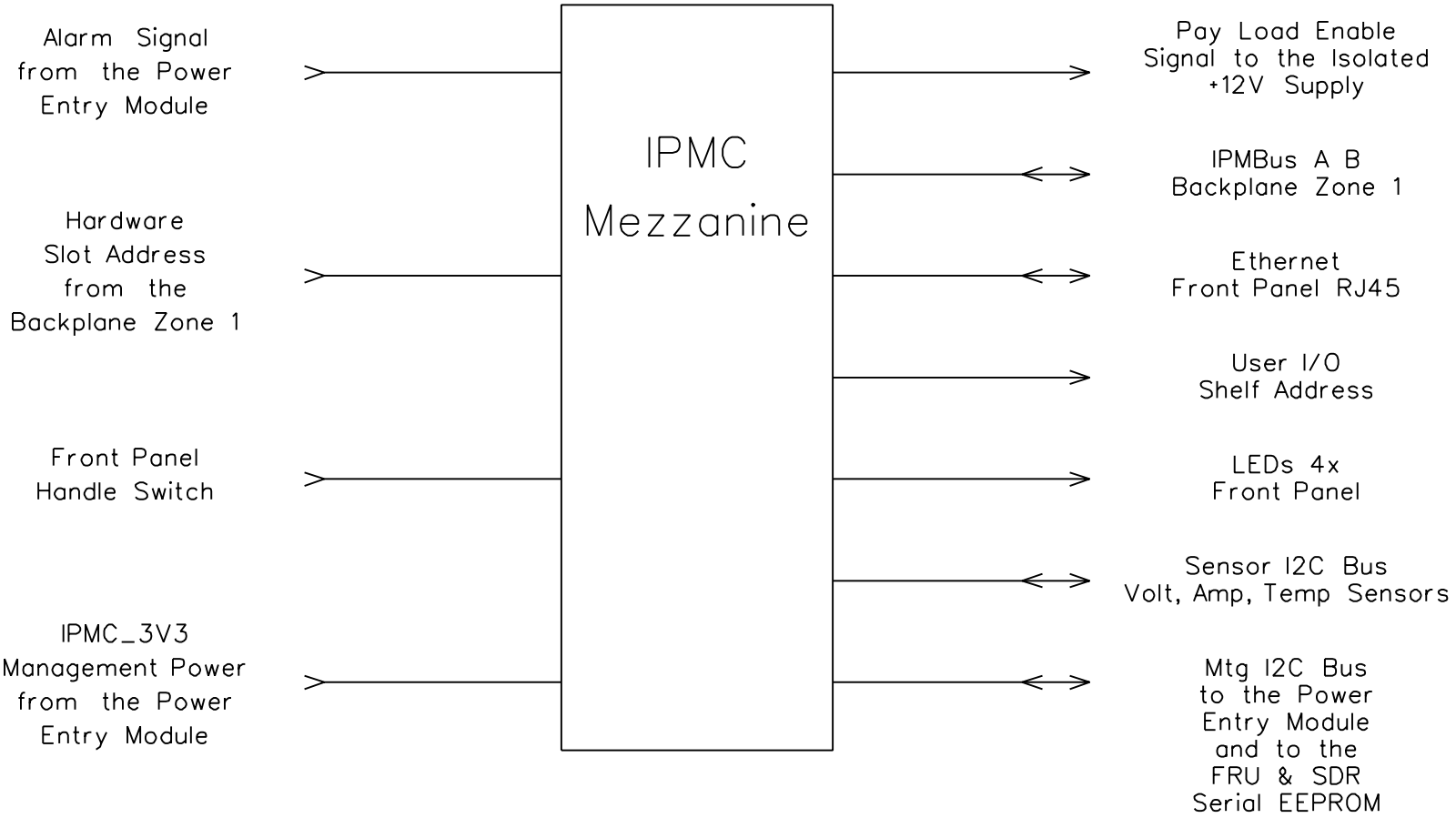


The Front Panel Connects to the Front Section of the EDS Strip and thus to the Shelf Ground

Not shown are the 400 connections from the Zone 2 Connector Ground Pins to the PCB Ground Planes.

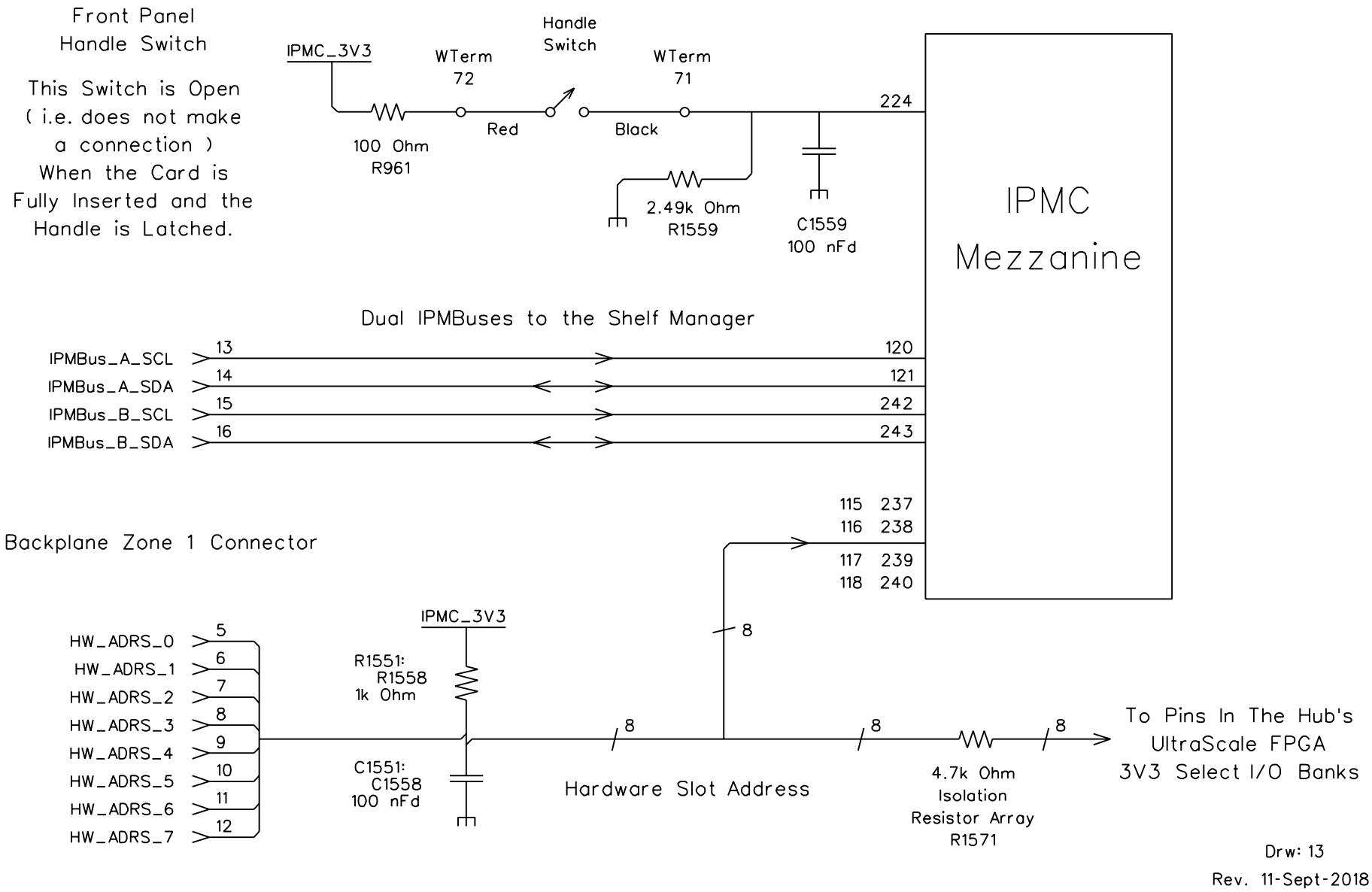
Drawing: 8
Rev. 4-May-2016

Hub-Module IPMC General



The IPMC's master and slave JTAG ports are not used in the Hub Module design.

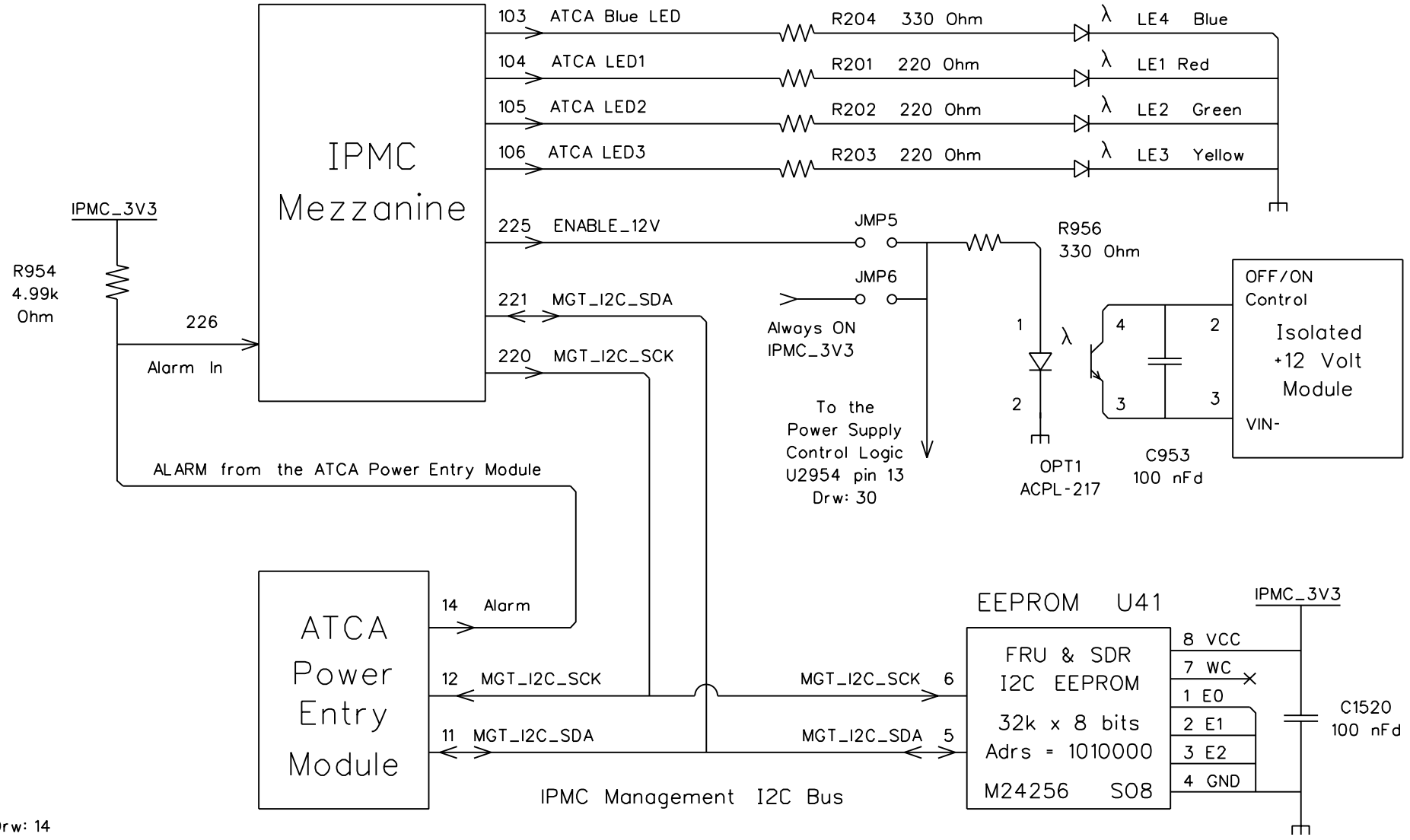
IPMC: HW-Adrs, Handle Switch, IPMBus



Drw: 13

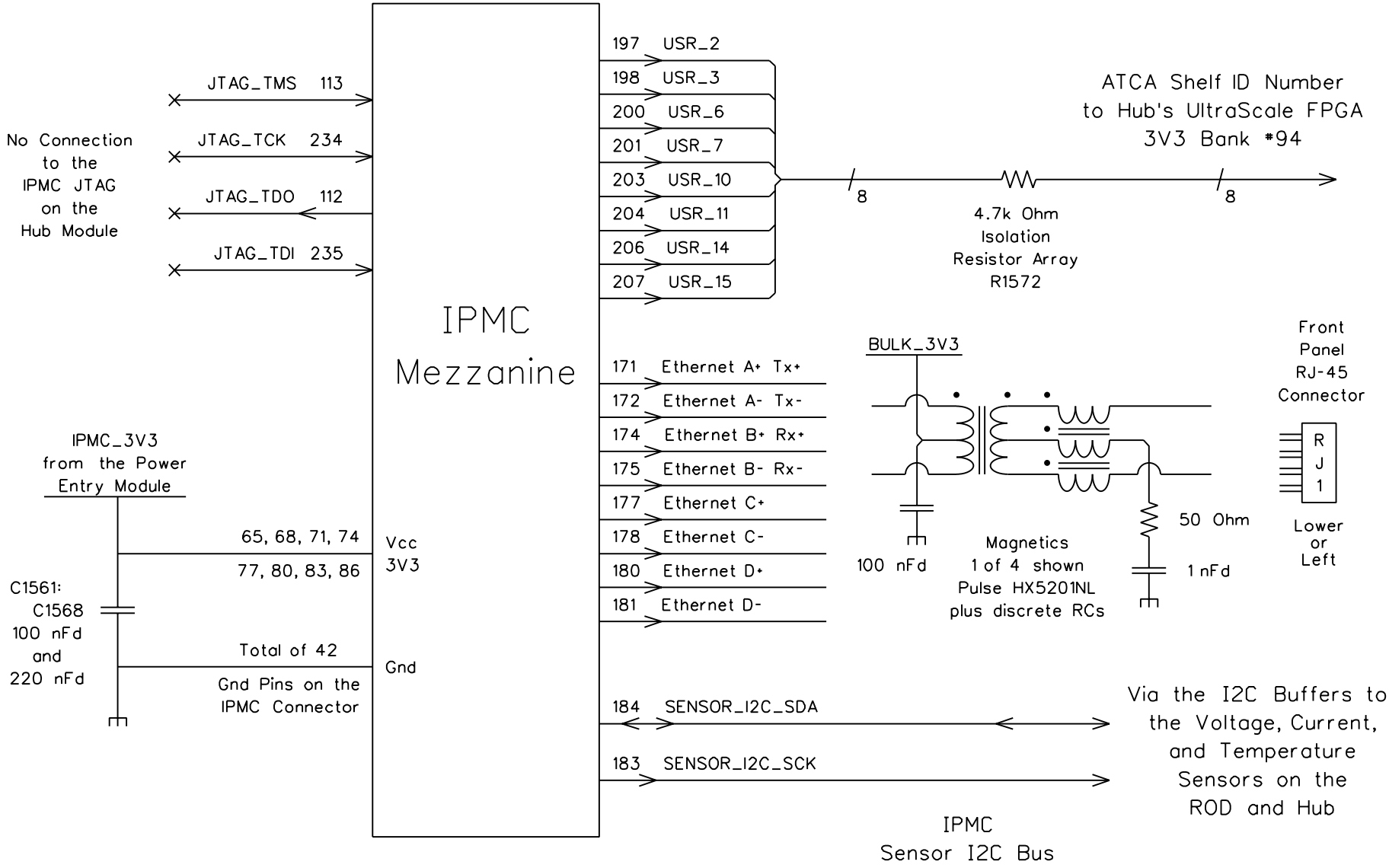
Rev. 11-Sept-2018

IPMC: Power Entry Alarm, Mgt. I2C, Payload Enable, LEDs



Drw: 14
Rev. 15-Jan-2020

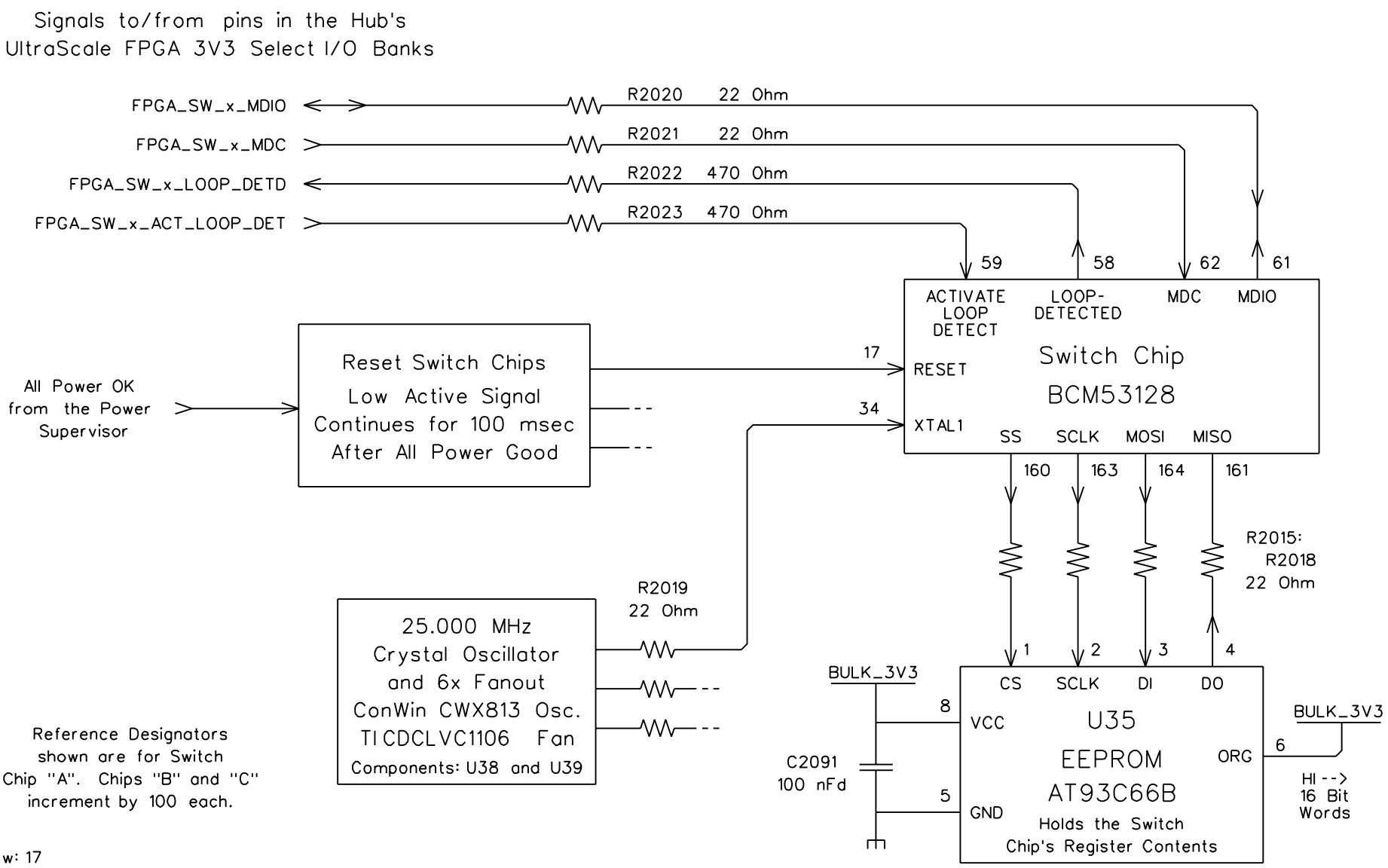
IPMC: Vcc-Gnd, Ethernet, User I/O, JTAG, Sensor I2C



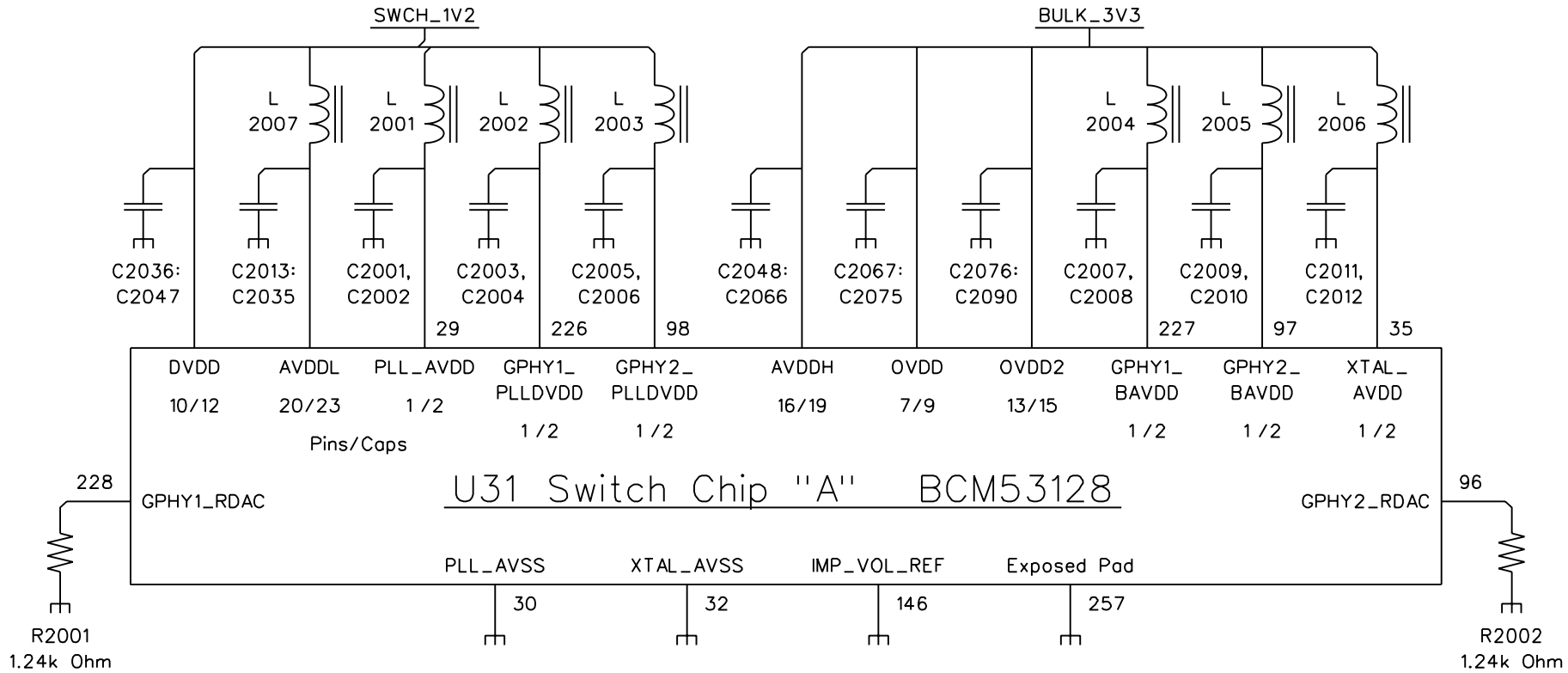
Rev. 12-Dec-2016

Drw: 16

Switch Chip - Support Circuits 1



Switch Chip - Support Circuits 2



DVDD Pins: 16, 27, 31, 40, 53, 135, 148, 162, 169, 183

AVDDL Pins: 71, 77, 83, 89, 95, 100, 106, 112, 118, 124, 200, 206, 212, 218, 224, 229, 235, 241, 247, 253

AVDDH Pins: 74, 80, 86, 92, 103, 109, 115, 121, 203, 209, 215, 221, 232, 238, 244, 250

OVDD Pins: 125, 129, 133, 138, 142, 145, 153

OVDD2 Pins: 3, 11, 19, 43, 44, 57, 63, 68, 165, 173, 180, 187, 193

Reference Designators are shown for U31 Switch Chip "A".
Reference Designators increment by 100 going to chips "B" and "C".

10 uFd Capacitors: C2001, C2003, C2005, C2007, C2009, C2011, C2013:C2015, C2036, C2037, C2048:C2050, C2067, C2068, C2076, C2077

1 uFd Capacitors: C2016:C2035, C2051:C2066

100 nFd Capacitors: C2002, C2004, C2006, C2008, C2010, C2012, C2038:C2047, C2069:C2075, C2078:C2090

Rev. 1-Dec-2015

Switch Chip - Support Circuits 3

U31 Switch Chip "A" BCM53128

56	IMP_PAUSE_CAP_TX	HI	
55	IMP_PAUSE_CAP_RX	HI	
54	IMP_LINK	LOW	
52	IMP_DUPLEX	HI	
51	IMP_SPD_SEL(0)	LOW	
50	IMP_SPD_SEL(1)	HI	
49	IMP_VOL_SEL(0)	LOW	
48	IMP_VOL_SEL(1)	LOW	
8	IMP_MODE(1)/GPIO6	HI	
7	IMP_MODE(0)/GPIO5	LOW	
47	EN_8051_TxRx	LOW	
26	EN_CLK25_OUT	LOW	
21	EN_CLK50_OUT	LOW	
15	CLK_FREQ1/GPIO1	LOW	
14	CLK_FREQ0/GPIO0	HI	
38	EN_EEE	HI	R2012

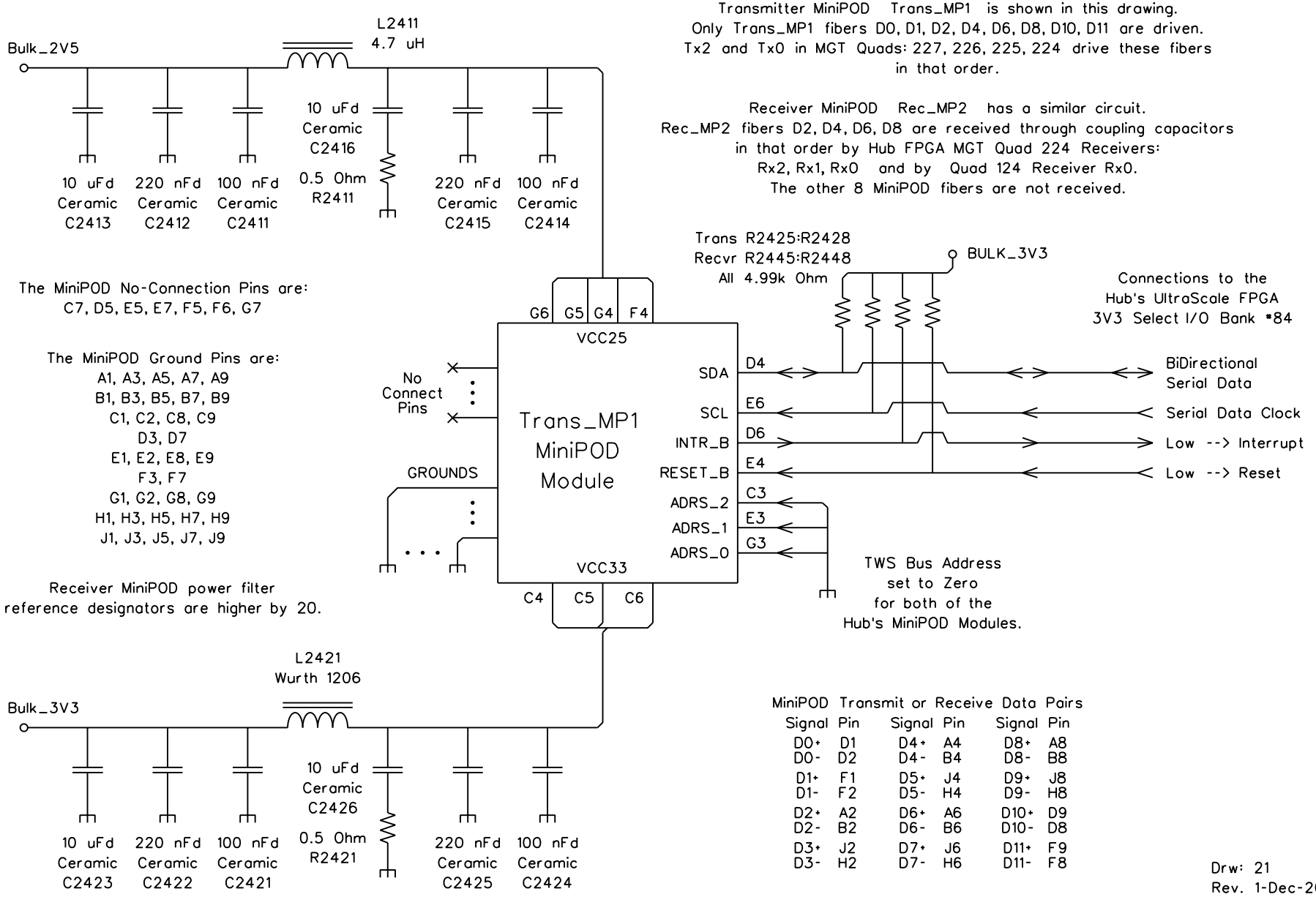
4	LED31/IMP_RXC_DELAY	HI	
2	LED30/IMP_TXC_DELAY	HI	
255	LED27/EN_HDX_FLOW	HI	
254	LED26/EN_FDX_FLOW	HI	
197	LED23/IMP_DUMP_FW_EN	LOW	
196	LED22/DIS_IMP	LOW	R2011
191	LED18/BC_SUPP_EN	LOW	
188	LED15/LOOP_IMP_SEL	LOW	
186	LED14/LOOP_DET_ENB	LOW	R2010
182	LED11/EPROM_TYPE1	LOW	R2009
181	LED10/EPROM_TYPE0	LOW	
172	LED3/EN_GREEN	LOW	R2008
36	TRST	HI	R2007
18	CPU_EEPROM_SEL	HI	R2006
13	LED_MODE(1)/GPIO4	LOW	R2005
12	LED_MODE(0)/GPIO3	HI	R2004
9	HW_FWDG_EN/GPIO7	LOW	R2003

Drw: 19

Jumper Reference Designators Increment by 100 for U32 and by 200 for U33.

Rev. 15-July-2016

Transmitter and Receiver MiniPOD Modules

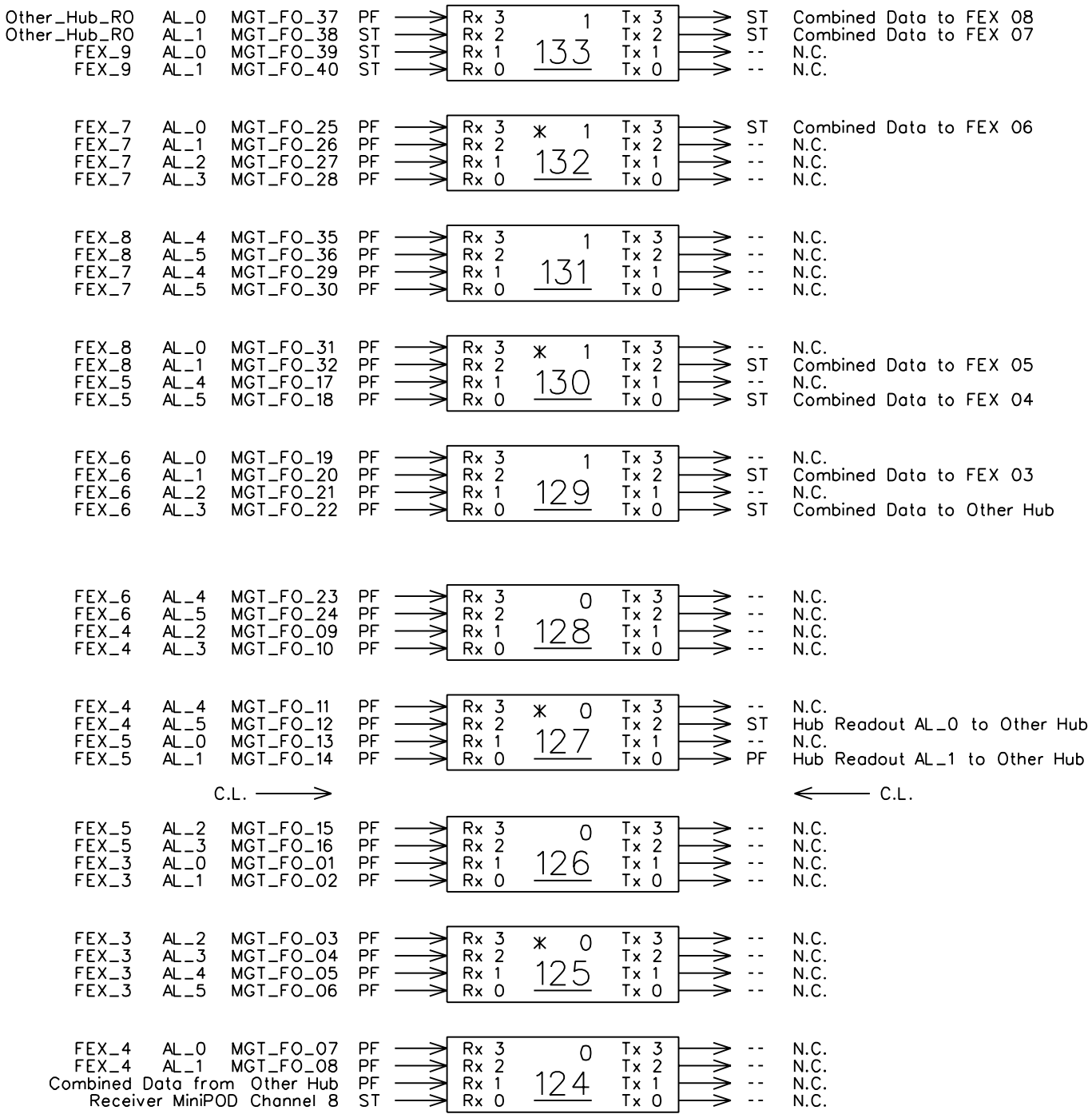


MiniPOD Transmit or Receive Data Pairs

Signal	Pin	Signal	Pin	Signal	Pin
D0+	D1	D4+	A4	D8+	A8
D0-	D2	D4-	B4	D8-	B8
D1+	F1	D5+	J4	D9+	J8
D1-	F2	D5-	H4	D9-	H8
D2+	A2	D6+	A6	D10+	D9
D2-	B2	D6-	B6	D10-	D8
D3+	J2	D7+	J6	D11+	F9
D3-	H2	D7-	H6	D11-	F8

Drw: 21
Rev. 1-Dec-2016

Hub - GTY Transceivers - QUADs 124:133



* → These Quads receive the LHC locked 320.6296 MHz reference clock.

MGT_FO_ → MGT Data Fanout Channel Number

ST → Straight Through

PF → Polarity Flip

AL → Aurora Lane Number

0,1 → UltraScale FPGA Super Logic Region

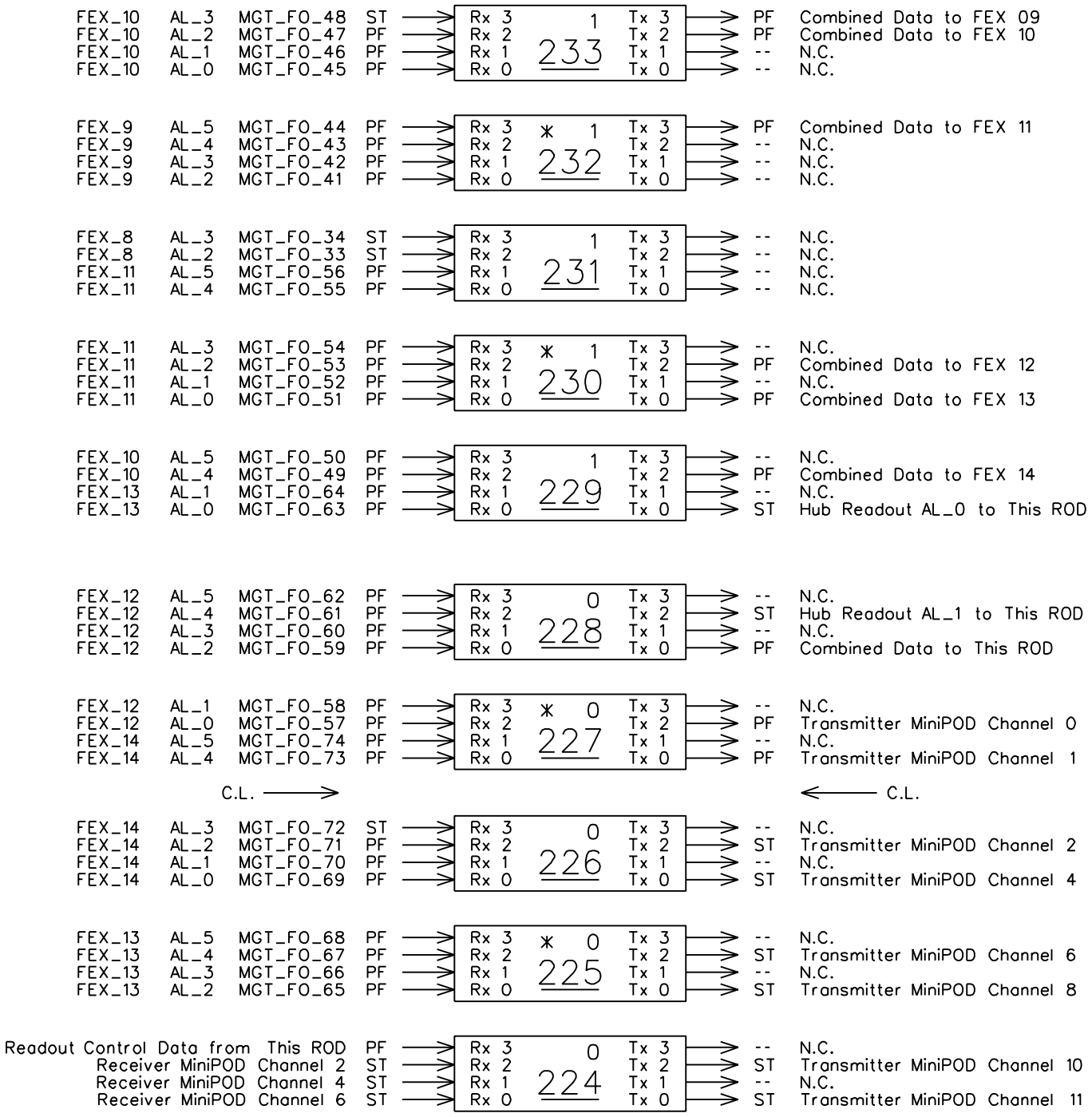
N.C. → No Connection

C.L. → Center Line of BGA

Drw: 22

Rev. 25-Feb-2019

Hub - GTH Transceivers - QUADs 224:233



* → These Quads receive the LHC locked 320.6296 MHz reference clock.

MGT_FO_ → MGT Data Fanout Channel Number

ST → Straight Through

PF → Polarity Flip

AL → Aurora Lane Number

0,1 → UltraScale FPGA Super Logic Region

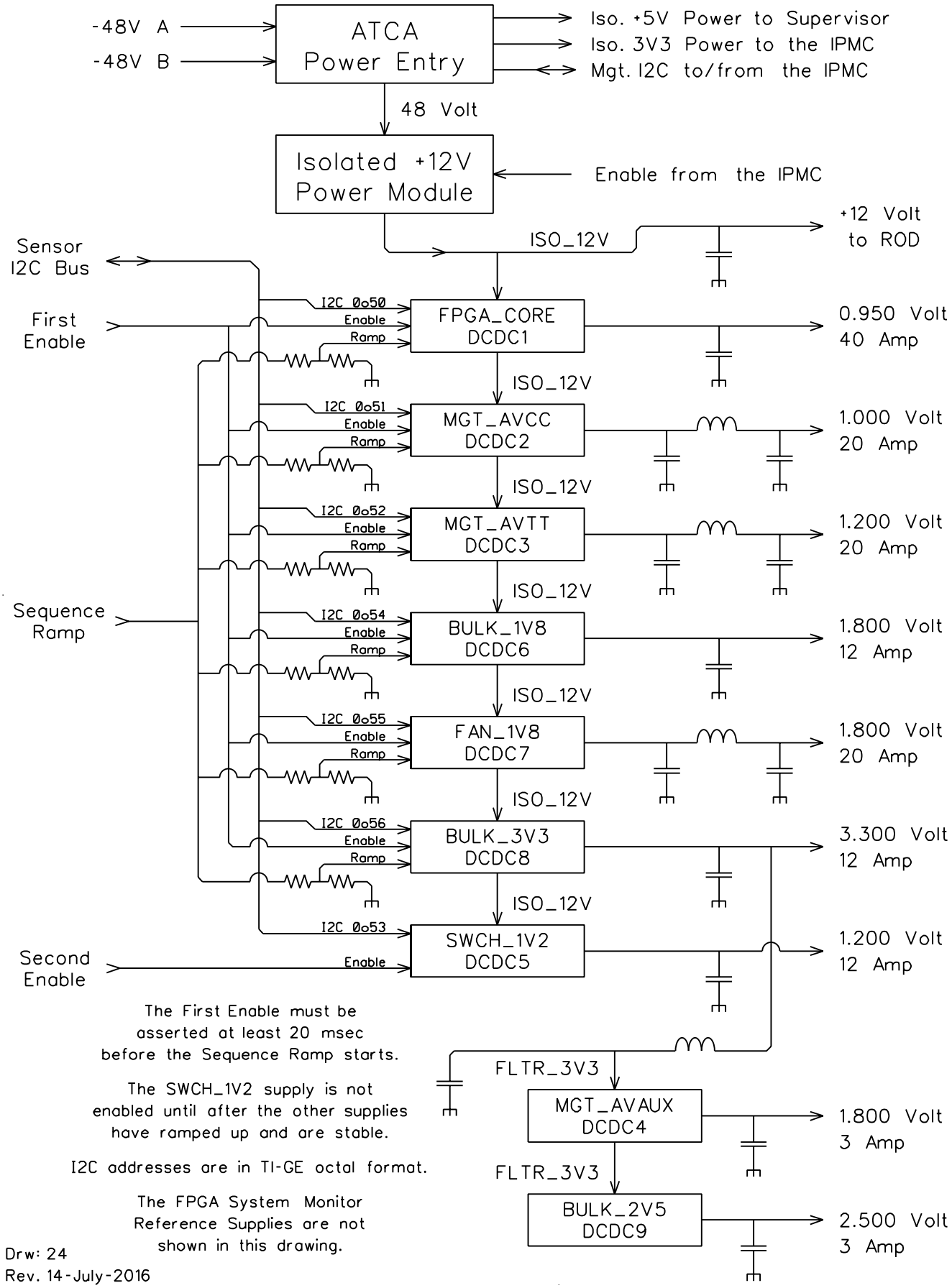
N.C. → No Connection

C.L. → Center Line of BGA

Drw: 23

Rev. 25-Feb-2019

Hub Module Power Supplies



The First Enable must be asserted at least 20 msec before the Sequence Ramp starts.

The SWCH_1V2 supply is not enabled until after the other supplies have ramped up and are stable.

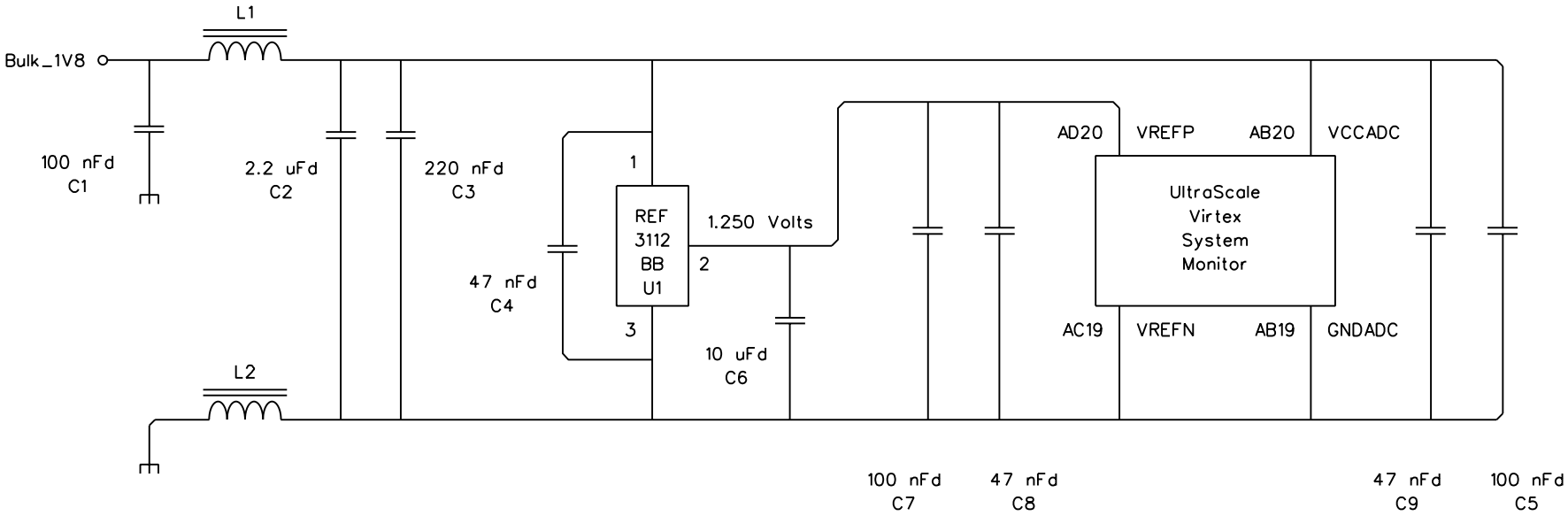
I2C addresses are in TI-GE octal format.

The FPGA System Monitor Reference Supplies are not shown in this drawing.

Drw: 24
Rev. 14-July-2016

HUB System Monitor Reference Supply

UltraScale Virtex FPGA System Monitor Reference

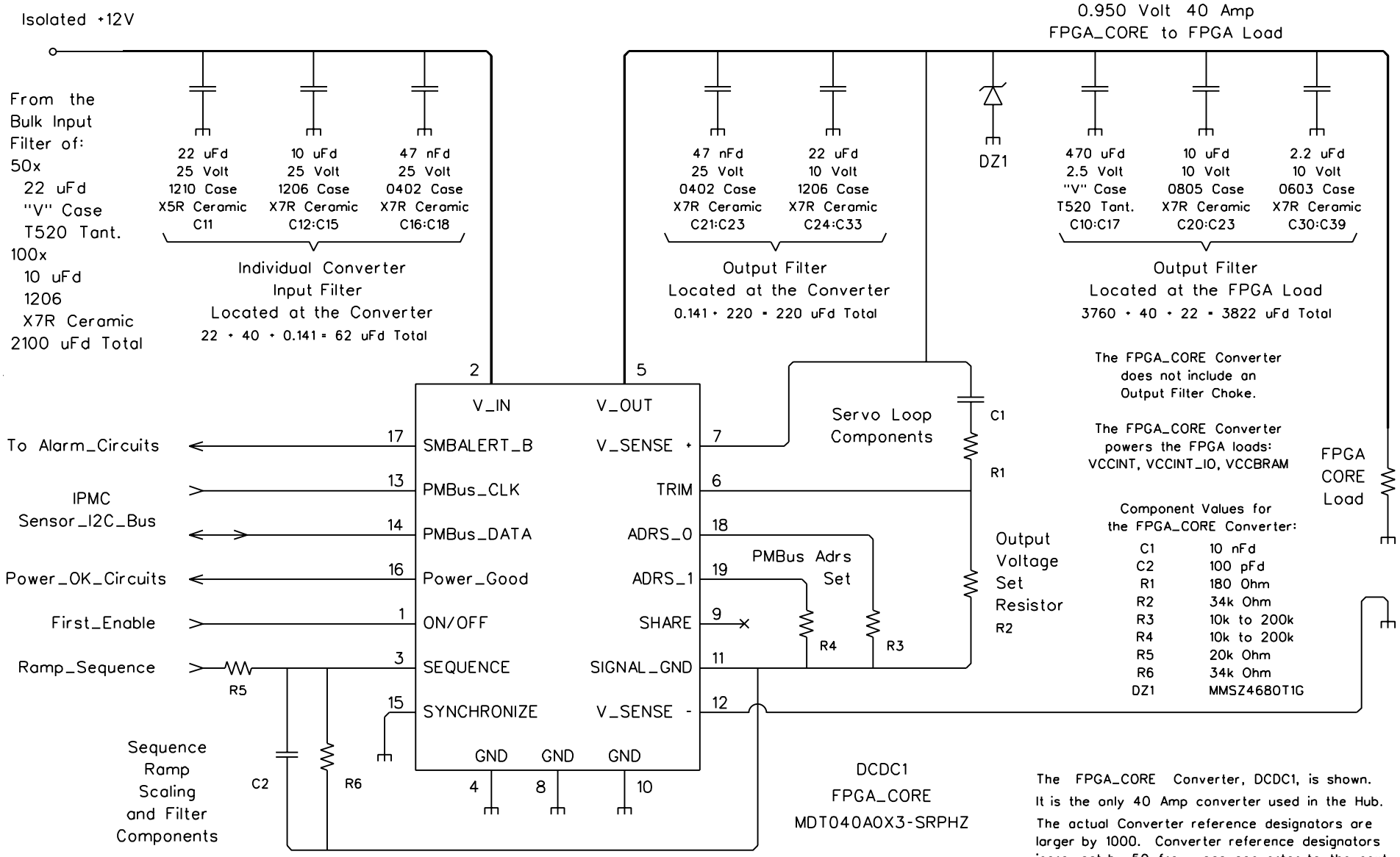


The inductors are Wurth 742792116, 1206, 60 mOhm.

See: SysMon UG580 Pg. 9 and 71, 72.

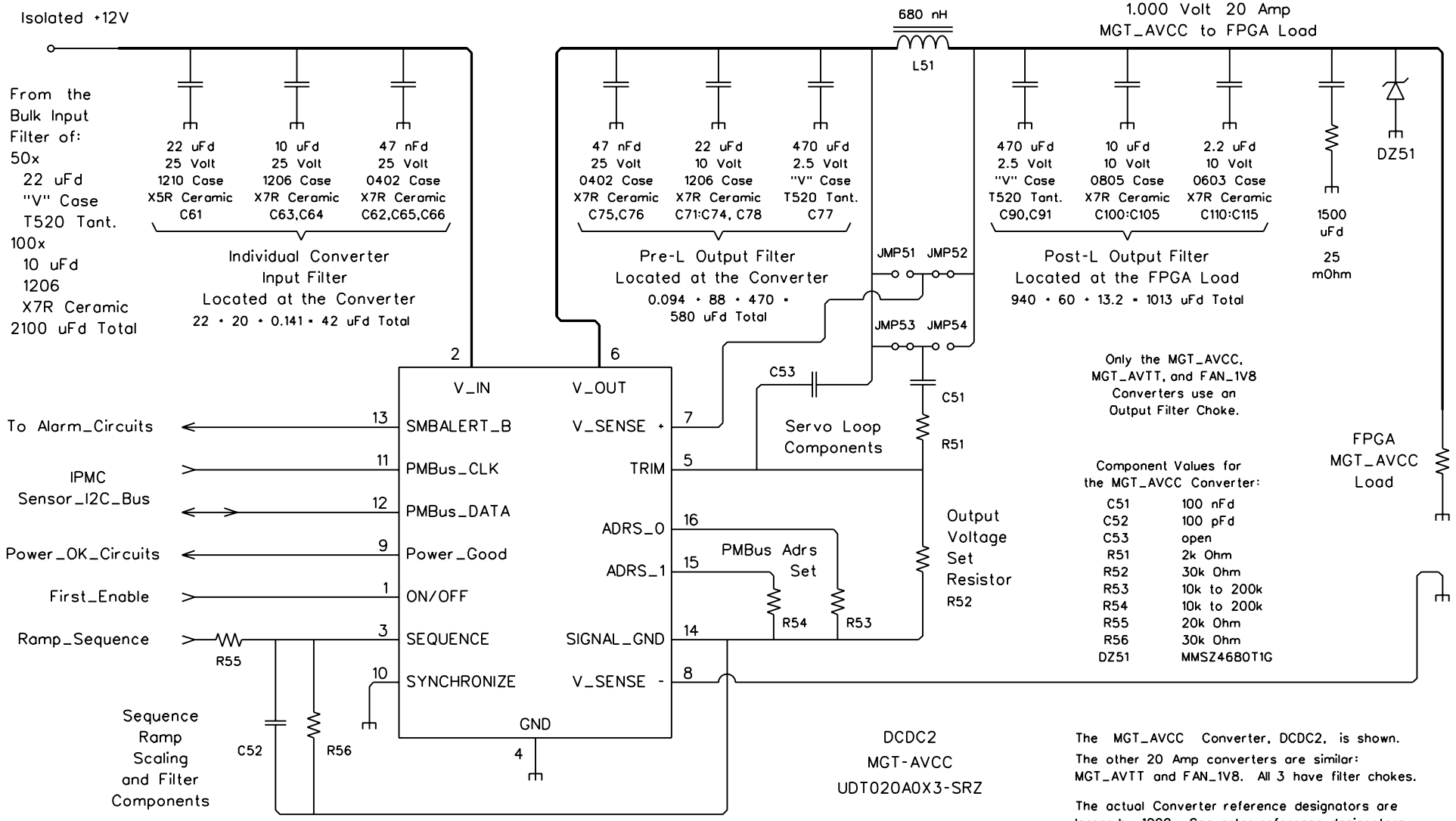
Actual reference designators are larger by 1850.

Hub Module 40 Amp DC-DC Converter Design



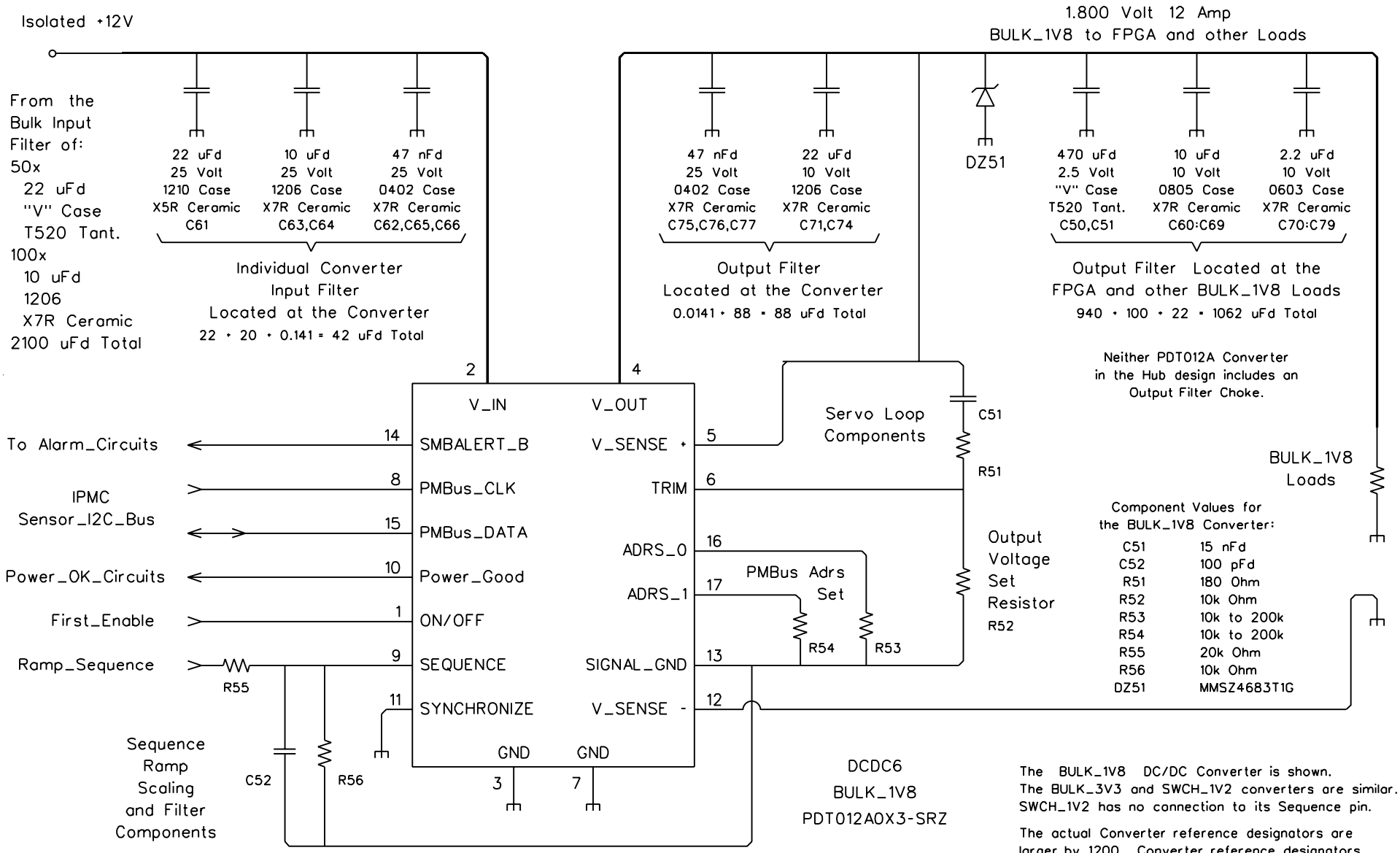
Drw: 26A
Rev. 22-Nov-2016

Hub Module 20 Amp DC-DC Converter with External Filter



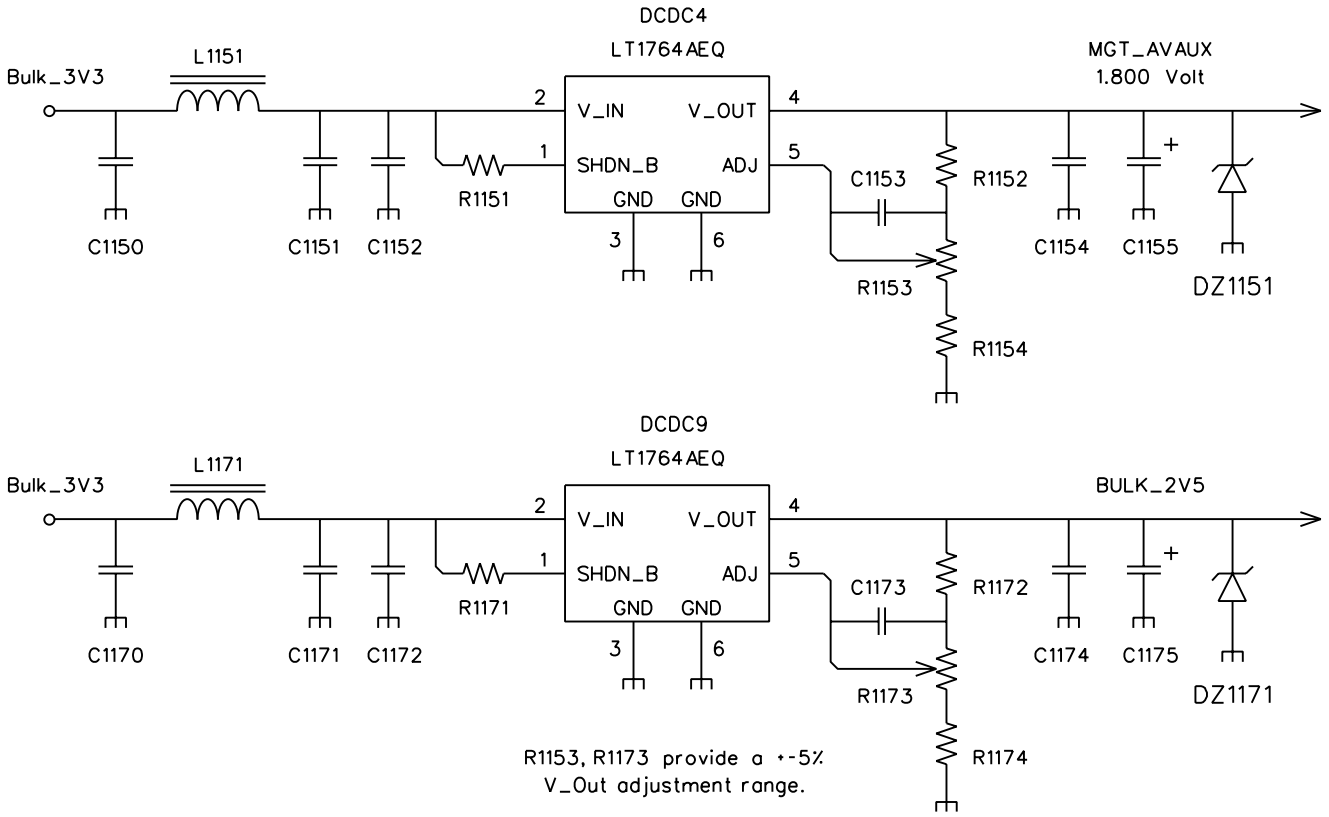
Drw: 26B
Rev. 21-May-2017

Hub Module 12 Amp DC-DC Converter Design



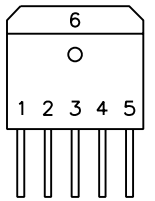
Drw: 26C
Rev. 22-Nov-2016

Hub Module Linear Regulators



LT1764AEQ*PBF
LT1764AEQ*TRPBF

Top View DD Package



1 Shut_Down_B
2 V_IN
3 Ground
4 V_OUT
5 Sense/Adjust
6 Ground

Internal reference 1.210 Volt
Dropout Voltage < 450 mV

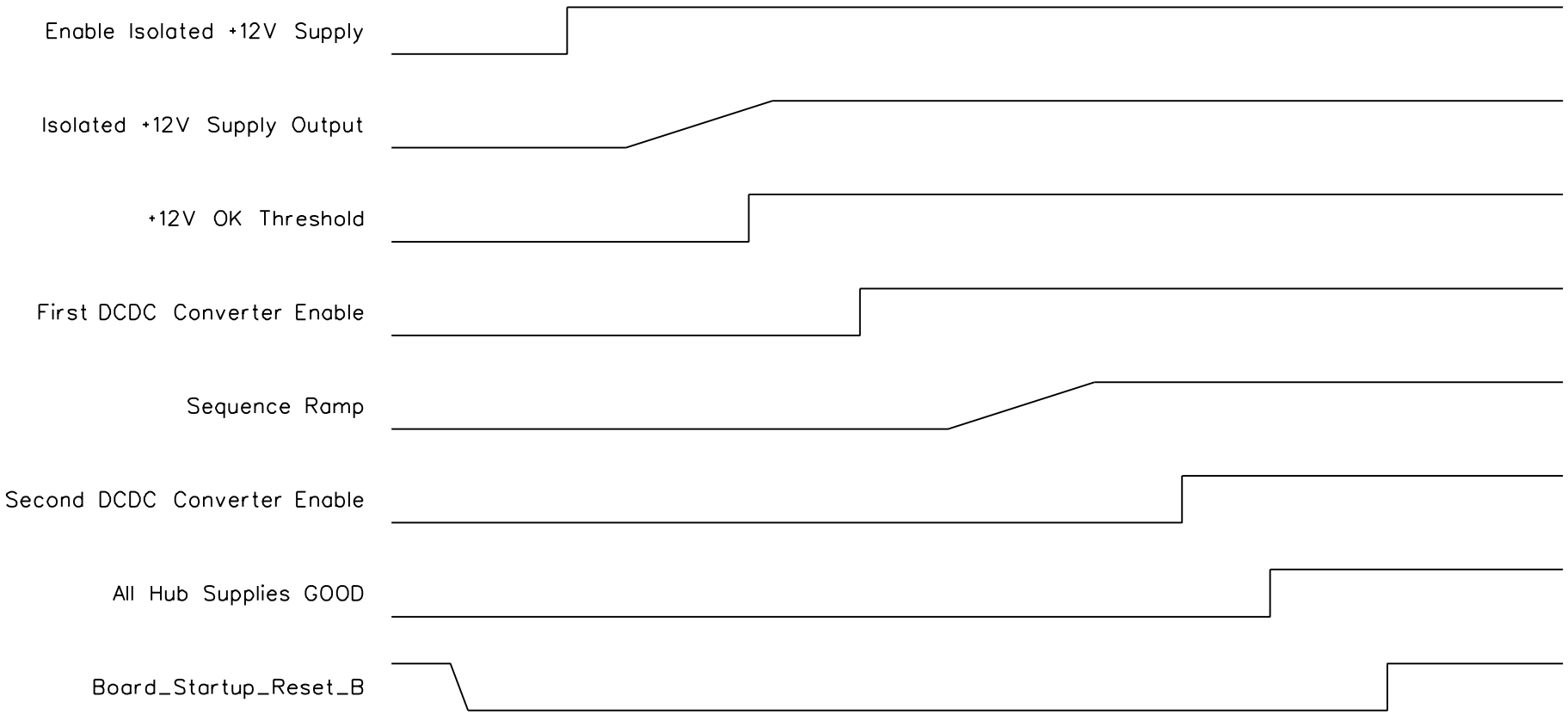
Expexted Loads

MGT_AVAUX 1.800 Volt	109 UltraScale GTH and GTY Connections 0.60 Amps est.
BULK_2V5 2.500 Volt	MiniPOD Trans + Rec 0.90 Amps max.
	Clock Fanout 0.30 Amps max.

Component Values

C1150, C1170	Cap_220_nFd_0603	R1151, R1171	Res_Zero_Ohm_0603	L1151	Wurth 742792116
C1151, C1171	Cap_220_nFd_0603	R1152	Res_464_Ohm_0603_TC	L1171	~2 uH, 2.5 Amp
C1152, C1172	Cap_10_uFd_10_V_0805	R1172	Res_1070_Ohm_0603_TC		
C1153, C1173	Cap_220_nFd_0603	R1153, R1173	Res_100_Ohm_3_Turn_Var	DZ1151	MMSZ4683T1G
C1154, C1174	Cap_10_uFd_10_V_0805	R1154, R1174	Res_1k_Ohm_0603_TC	DZ1171	MMSZ4683T1G
C1155, C1175	Cap_330_uFd_Tant_V				

Hub Power Supply Startup

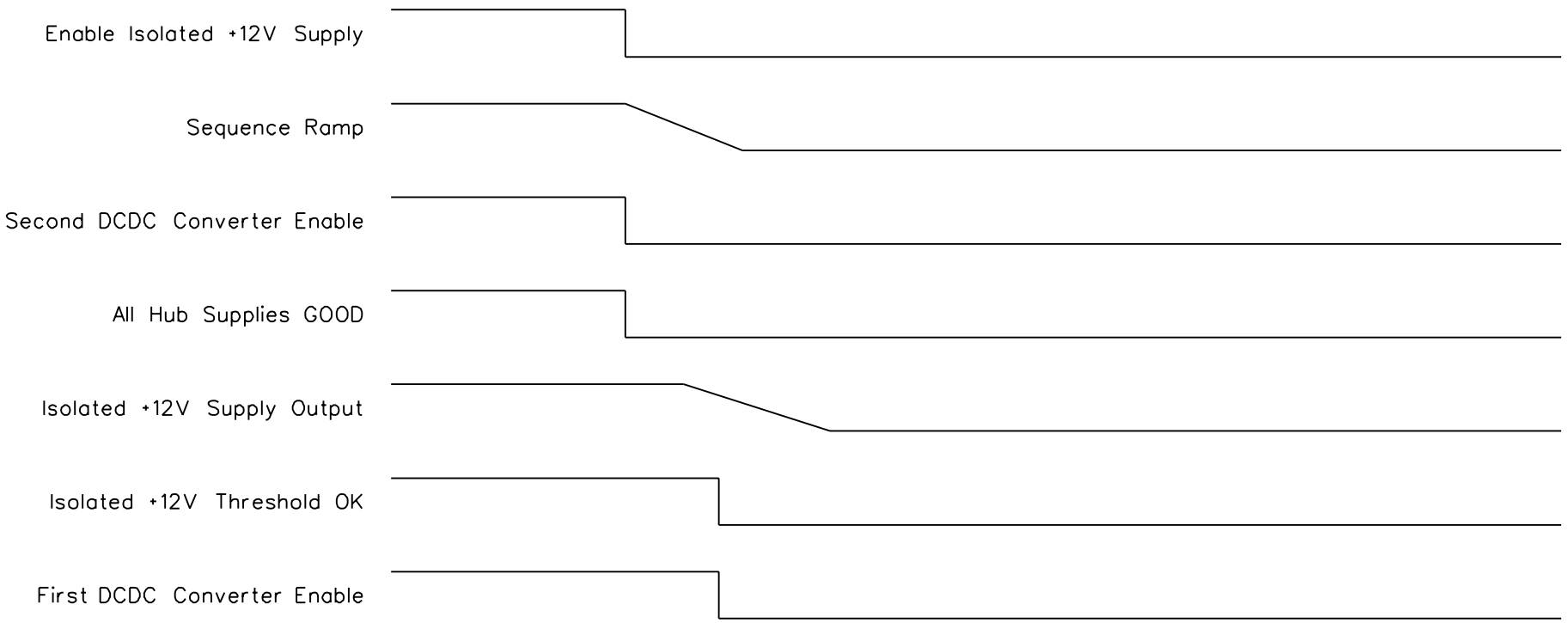


Requirements

Allow the Isolated +12V Supply to stabilize for 500 msec before asserting the First DCDC Converter Enable.
First DCDC Converter Enable must be asserted for 20 msec minimum before the Sequence Ramp starts.
The Sequence Ramp should bring up the FPGA supplies in about 5 to 9 msec.
Once the Sequence Ramp is complete must wait a minimum of 10 msec before asserting the Second DCDC Converter Enable.
The SWCH_1V2 supply must ramp up within 2 msec maximum.
All supplies must be up and stable for 100 msec minimum before the Startup Reset is dropped.

Drw: 28
Rev. 11-Feb-2016

Hub Power Supply Shutdown

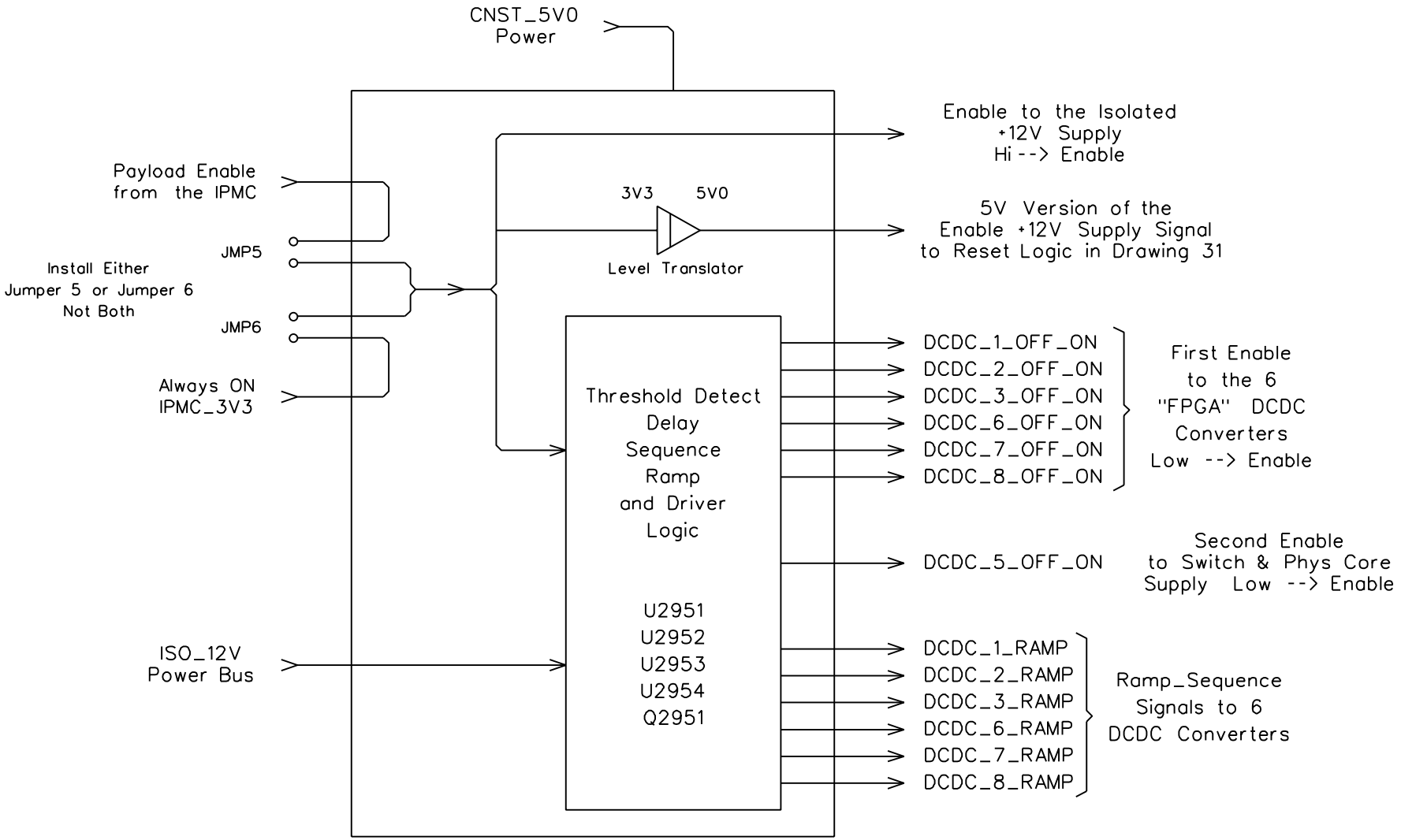


Sequence

When the Enable signal to the Isolated +12V Supply is dropped the Sequence Ramp will immediately begin to fall.
The supplies will ramp down in an organized manner for as long as the Isolated +12V remains above threshold.
Once the Isolated +12V bus falls below threshold then the First Enable signal to the 6 FPGA DCDC Converters is dropped.
The Second Enable (to the SWCH_1V2 converter) is dropped as soon as the Isolated +12V Enable is deasserted.

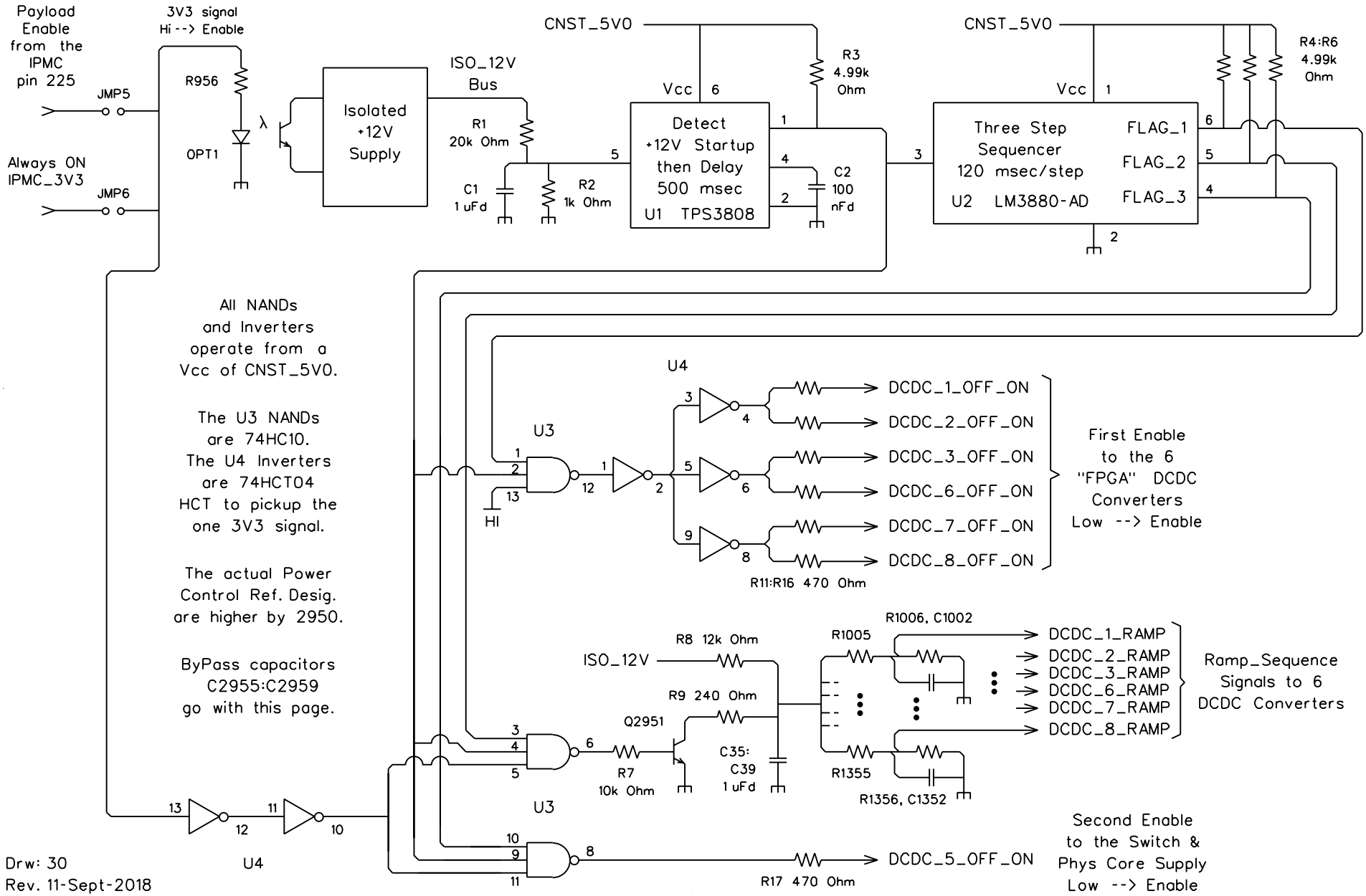
Drw: 29
Rev. 11-Feb-2016

Block Diagram of Power Control Drawing #30



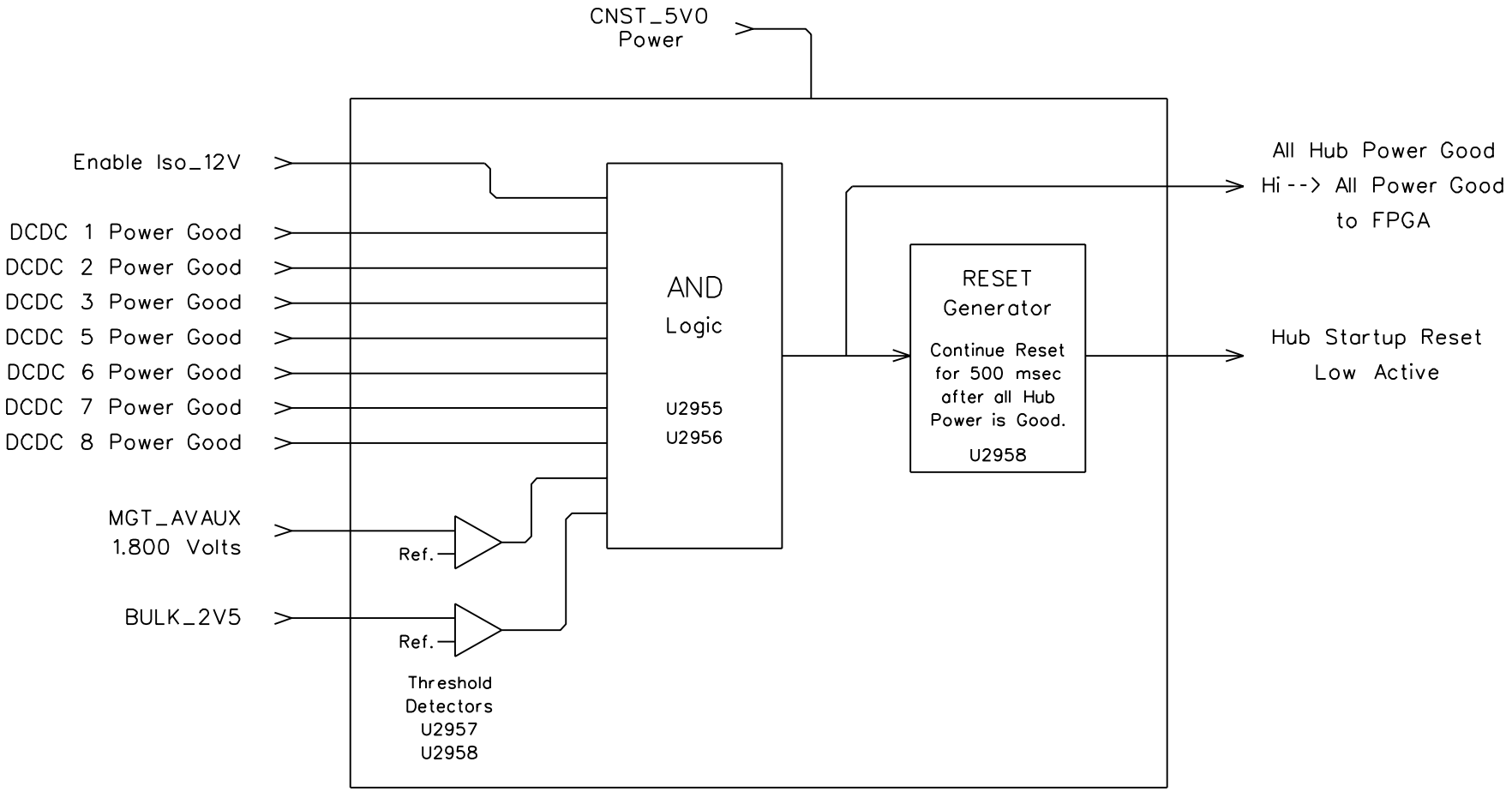
Drw: 30_Blk
Rev. 31-May-2016

Hub Power Supply Control



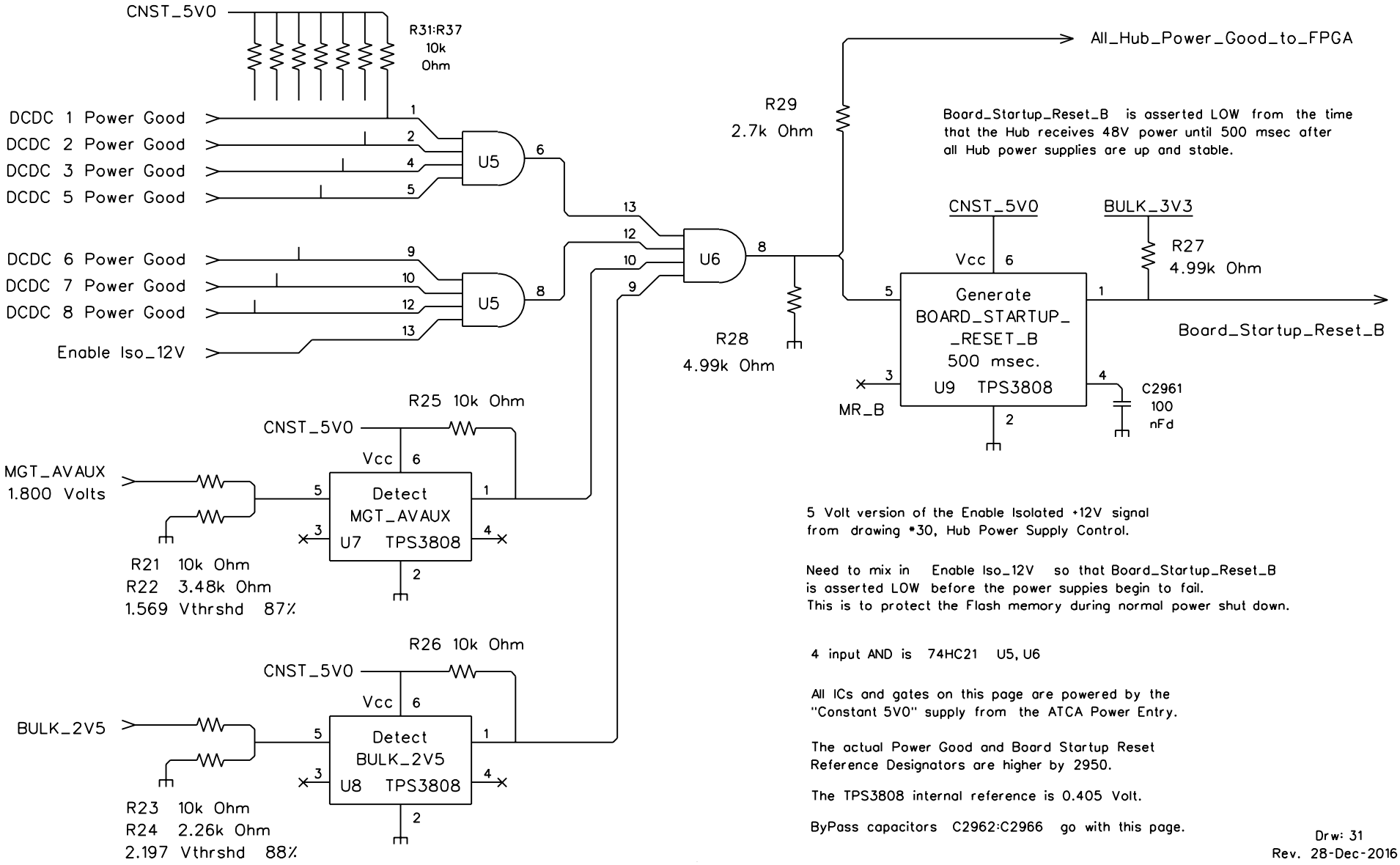
Drw: 30
Rev. 11-Sept-2018

Block Diagram Power Good & Reset Drawing #31



Drw: 31_Blk
Rev. 28-Dec-2016

Hub Power Good and Board Startup Reset



5 Volt version of the Enable Isolated +12V signal from drawing #30, Hub Power Supply Control.

Need to mix in Enable Iso_12V so that Board_Startup_Reset_B is asserted LOW before the power suppies begin to fail. This is to protect the Flash memory during normal power shut down.

4 input AND is 74HC21 U5, U6

All ICs and gates on this page are powered by the "Constant 5V0" supply from the ATCA Power Entry.

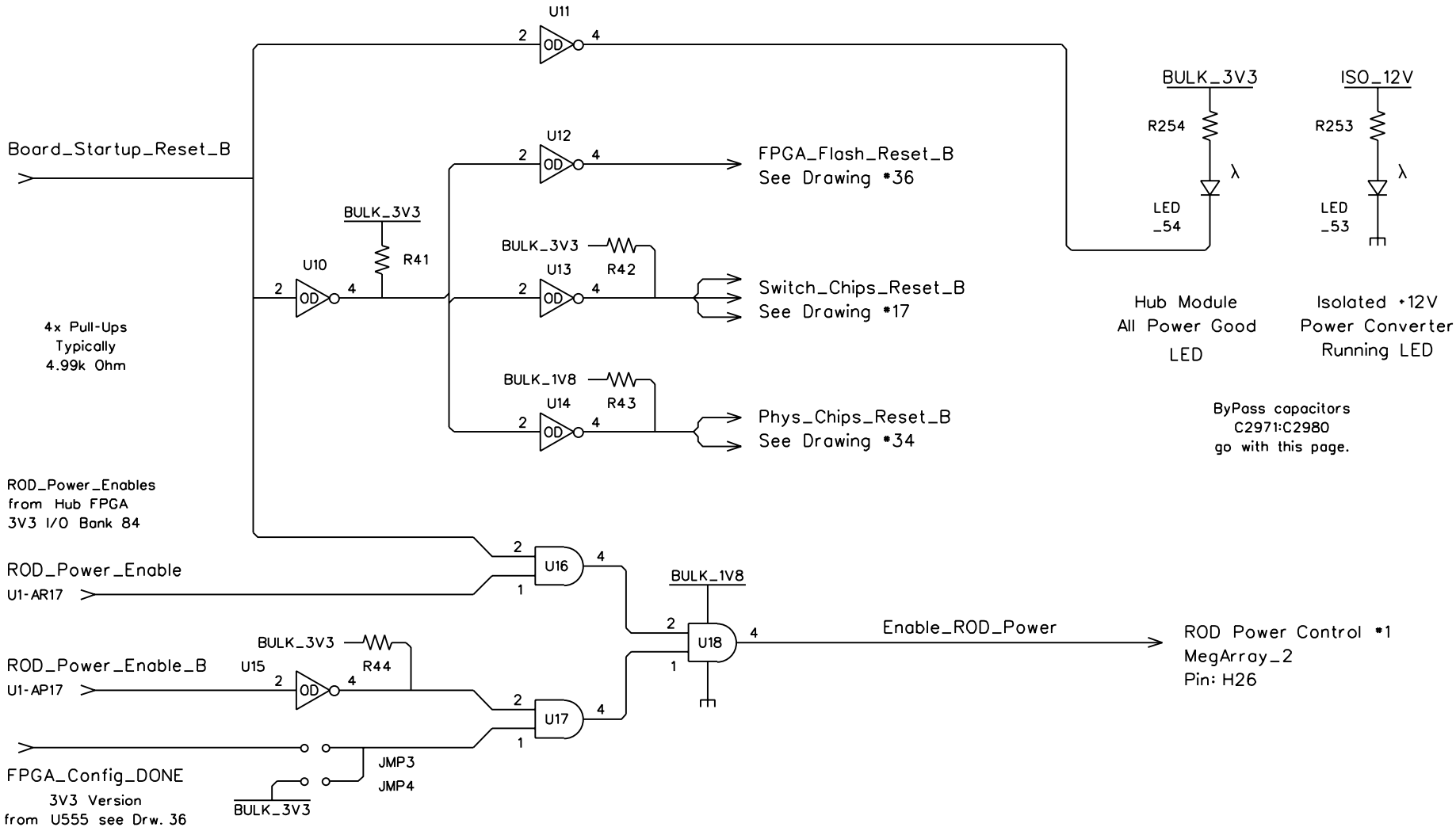
The actual Power Good and Board Startup Reset Reference Designators are higher by 2950.

The TPS3808 internal reference is 0.405 Volt.

ByPass capacitors C2962:C2966 go with this page.

Drw: 31
Rev. 28-Dec-2016

Board Reset Distribution - ROD Power Control



Consumers of the Board_Startup_Reset_B signal and Rules:

When all power is Good and Board_Startup_Reset_B has finished, then turn ON the front panel Power Good LED.

Allow FPGA to Configure, hold FPGA INIT Low with open-drian until ready to Configure, pull-up to 1V8.

Flash active Low Reset must be held Low for 300 usec min after all power good, 1V8 signal.

Switch chips active Low Reset, 80 msec min Low with 25 MHz clock running and power good, Max rise time 25 nsec, 3V3 signal.

Phys chip active Low Reset must be held Low for 10 msec min after all power good, 1V8 signal.

Enable_ROD_Power must drive 1V8 signal into a 1k Ohm load to Gnd on the ROD.

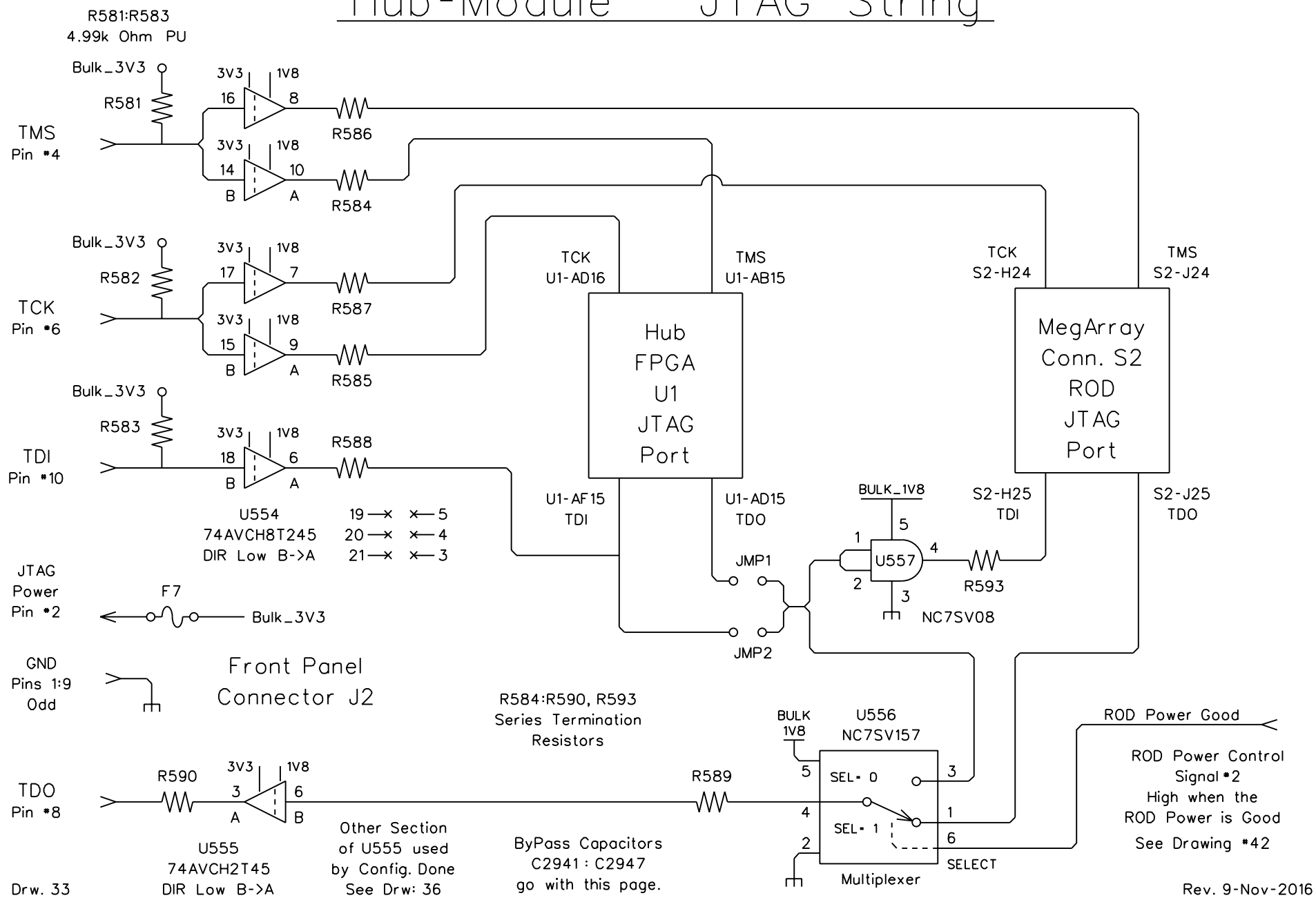
Open Drain Inverters are NC7SV05
2 input ANDs are NC7SV08

All ICs on this page are powered by BULK_3V3 except as indicated.

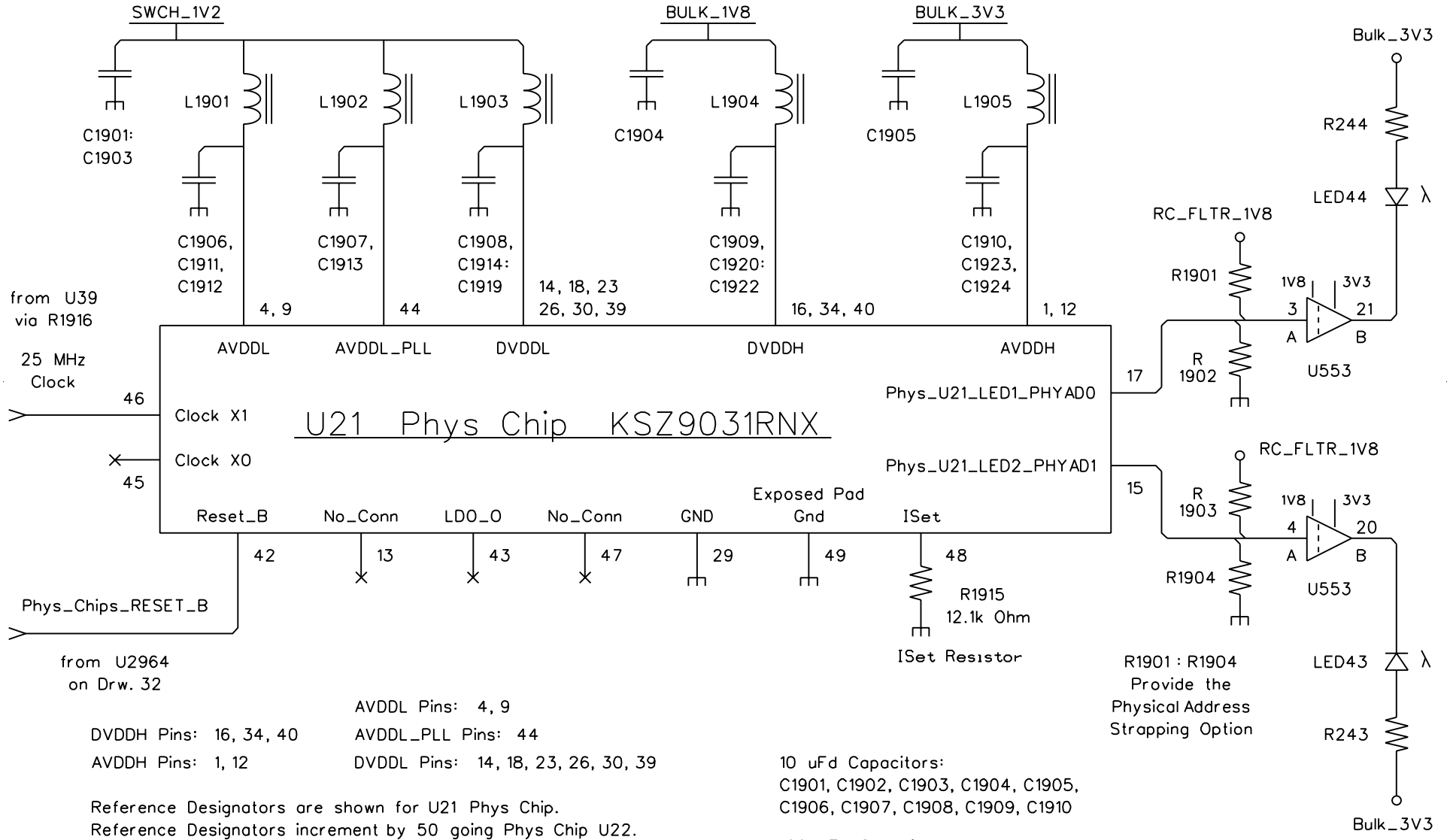
Except for the LED circuits, the actual Ref Desigs on this page are higher by 2950.

Drw: 32
Rev. 28-Nov-2016

Hub-Module JTAG String



Phys Chip - Power, Clock, Reset, and LED Circuits



R1901 : R1904 Provide the Physical Address Strapping Option

AVDDL Pins: 4, 9

DVDDH Pins: 16, 34, 40

AVDDL_PLL Pins: 44

AVDDH Pins: 1, 12

DVDDL Pins: 14, 18, 23, 26, 30, 39

Reference Designators are shown for U21 Phys Chip.
Reference Designators increment by 50 going Phys Chip U22.

L1903: Wurth_742792116 2 uH 60 mOhm 2.5 A

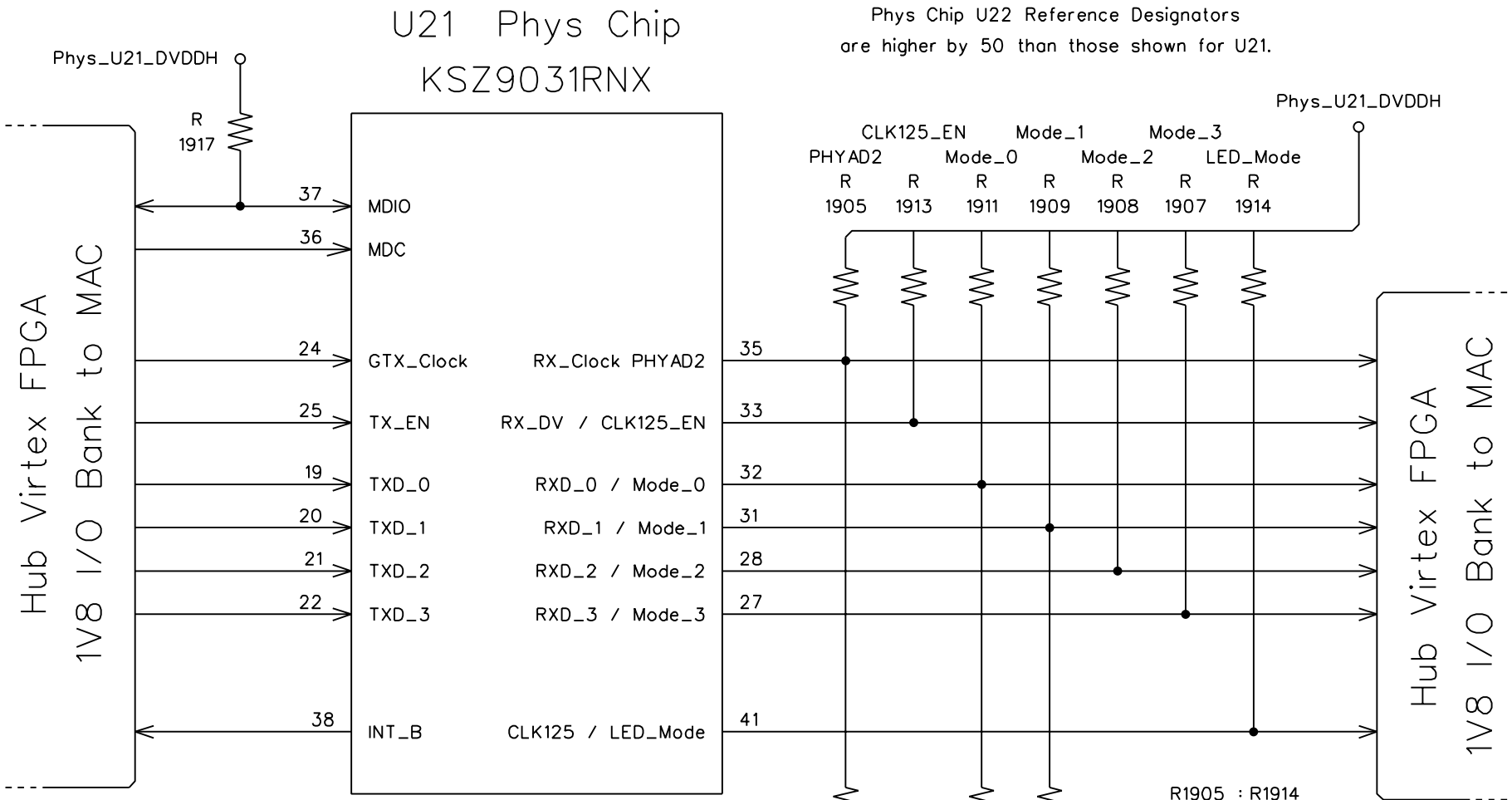
L1901, L1902, L1904, L1905: Wurth 782633601 2 uH 200 mOhm 1A

10 uFd Capacitors:
C1901, C1902, C1903, C1904, C1905, C1906, C1907, C1908, C1909, C1910

100 nFd Capacitors:
C1911, C1912, C1913, C1914, C1915, C1916, C1917, C1918, C1919, C1920, C1921, C1922, C1923, C1924

Drw: 34
Rev. 31-May-2016

Phys Chip - RGMII, MDC/DMIO, and Base-T Circuits

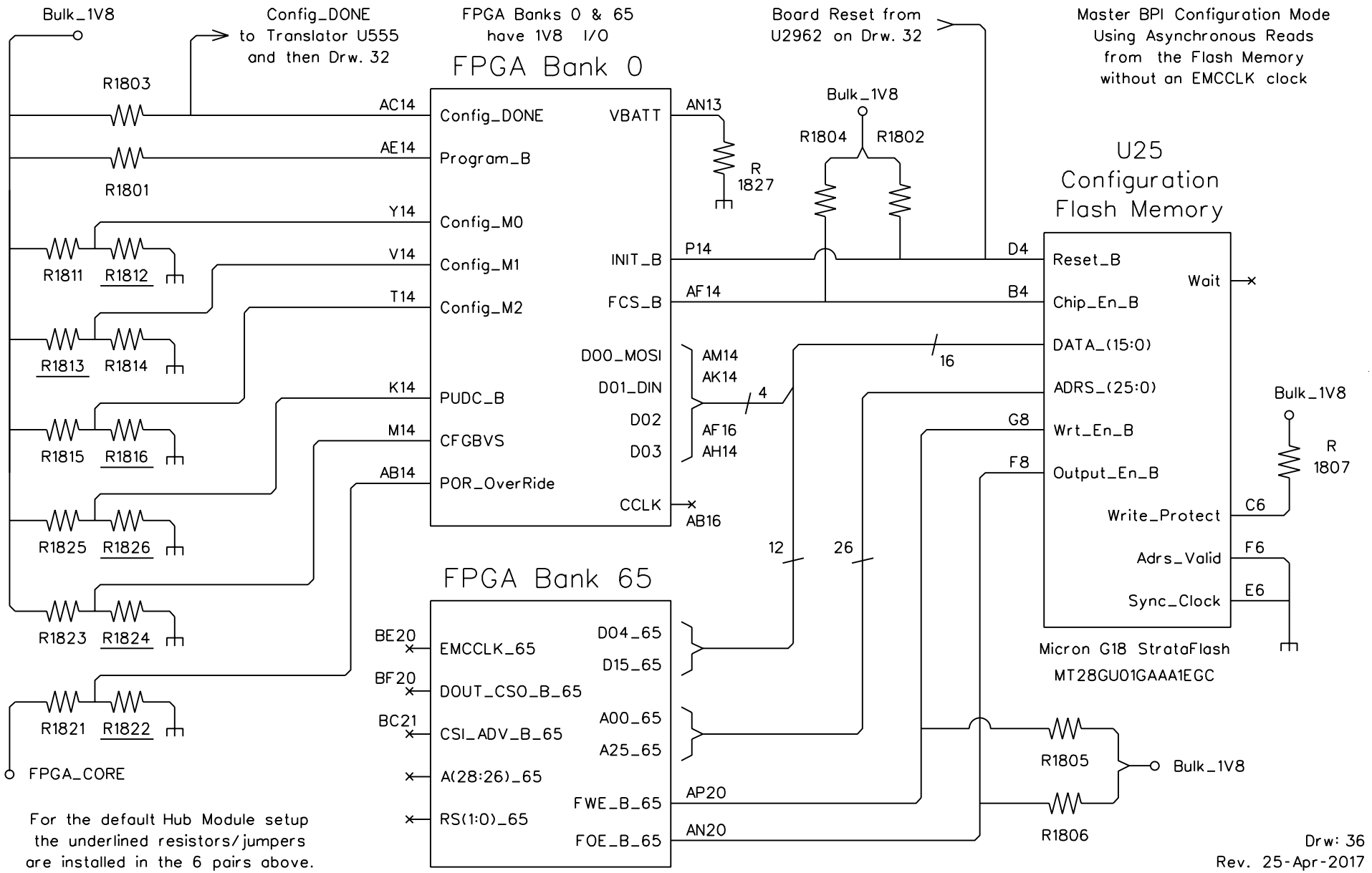


Phys Chip BASE-T Connections to the "Magnetics" or to Capacitor Coupling:

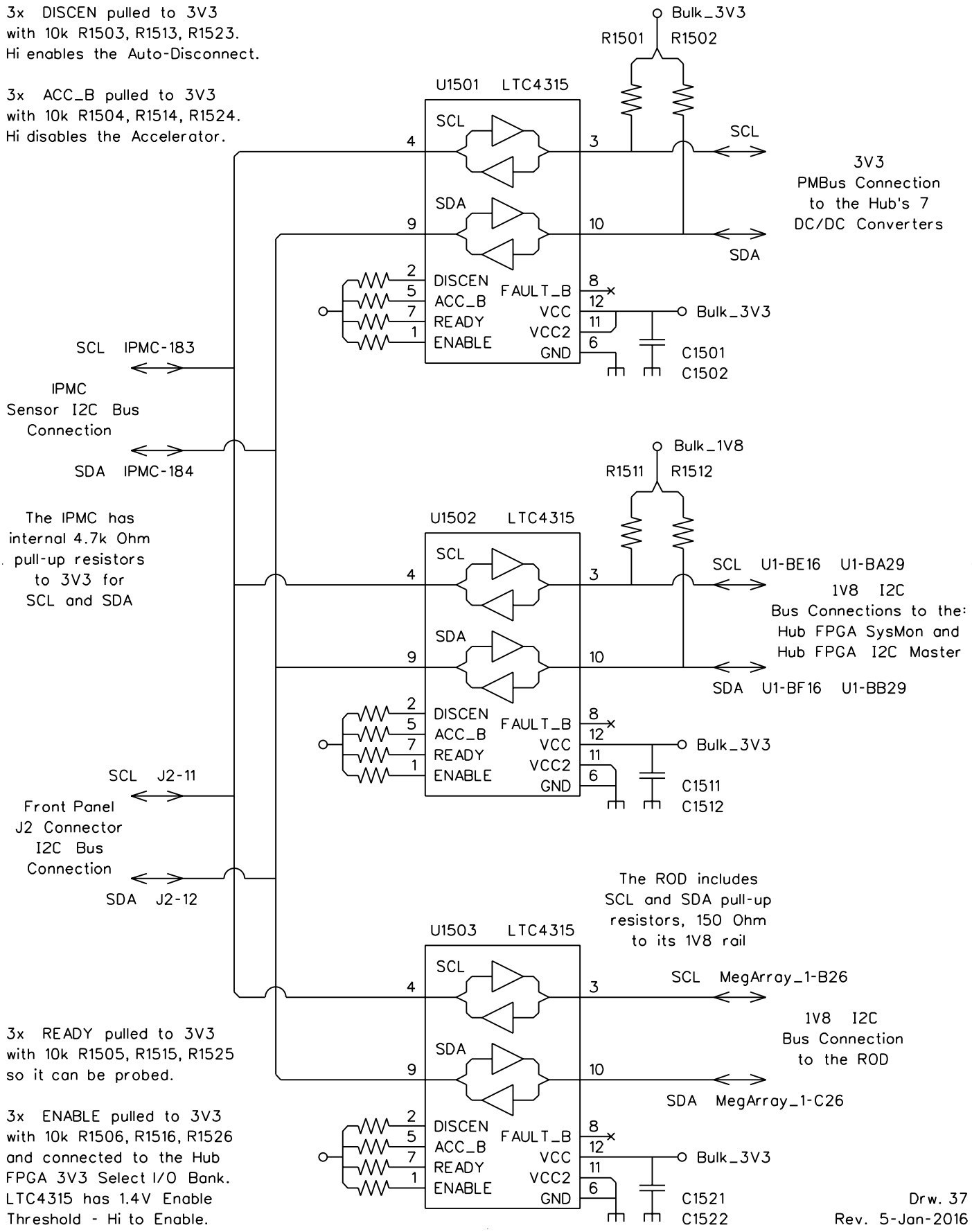
TxRxP_A pin 2	TxRxP_B pin 5	TxRxP_C pin 7	TxRxP_D pin 10
TxRxN_A pin 3	TxRxN_B pin 6	TxRxN_C pin 8	TxRxN_D pin 11

Drw: 35
Rev. 21-Apr-2016

Hub FPGA - Banks 0 & 65 - Configuration



Hub-Module IPMC Sensor I2C Bus

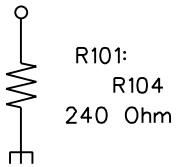


Hub FPGA DCI, VREF, MGT Calibration Resistors

Select I/O
Banks

DCI Calibration
Resistors

VRP Pins



Installed in Banks:
65, 66, 67, 68, 71

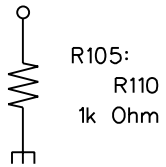
Banks: 70, 72 are
only used for static output
signals in the Hub design.

Banks: 84, 94
do not support DCI.

Select I/O
Banks

VREF Pull-Down
Resistors

VREF Pins



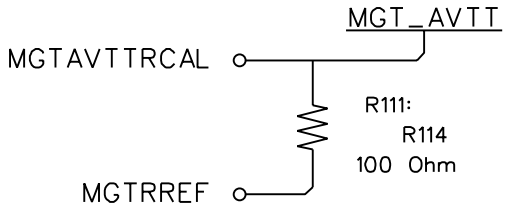
Installed in Banks:
65, 66, 67, 68, 71, 84, 94

Banks: 70, 72 are
only used for static output
signals in the Hub design.

MGT
Transceivers

MGT Termination
Calibration Resistors

MGTAVTTRCAL and
MGTRREF Pins

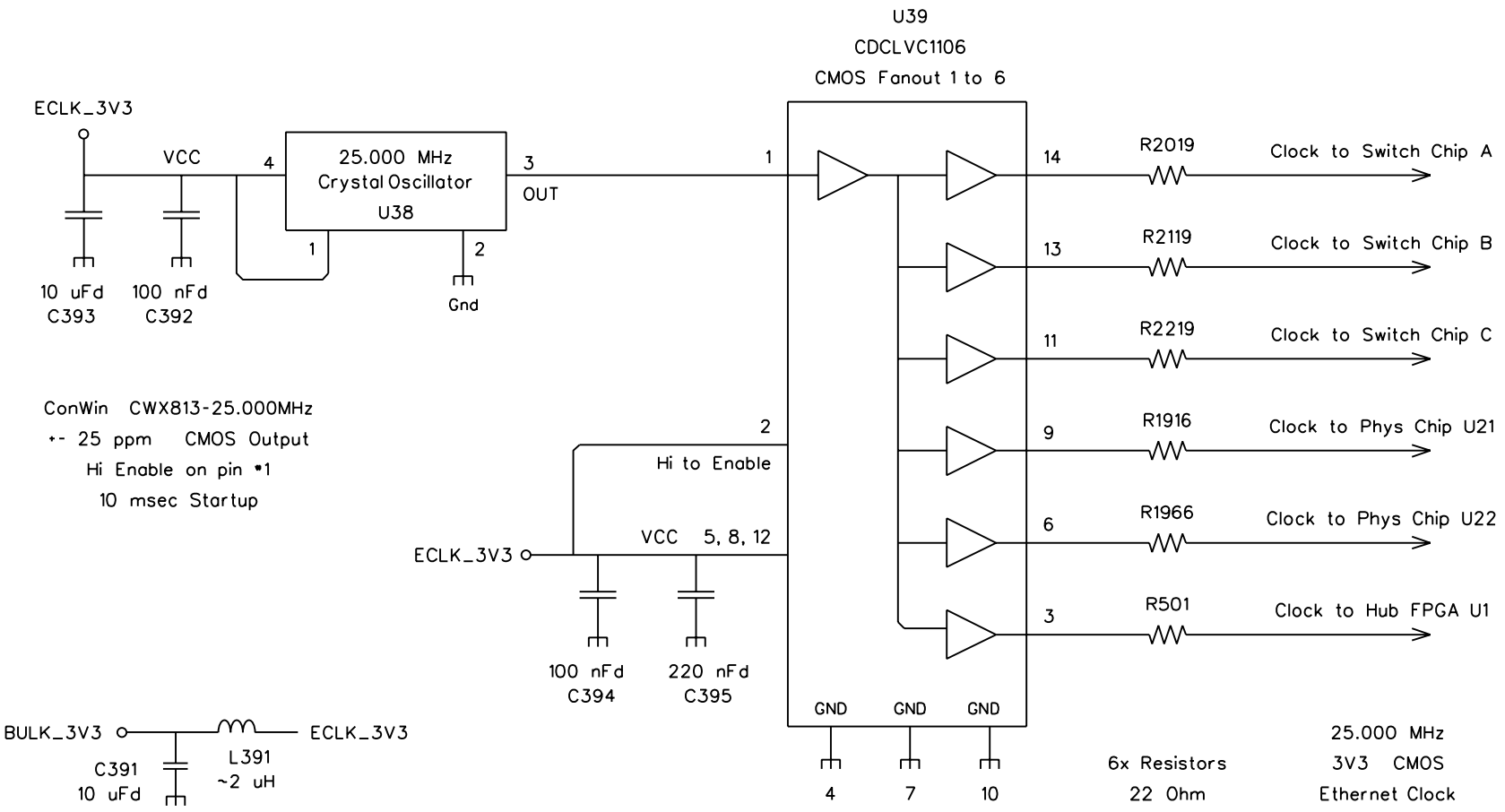


Installed in Quads:
125, 130, 226, 231

These service all 80 MGT Transceivers

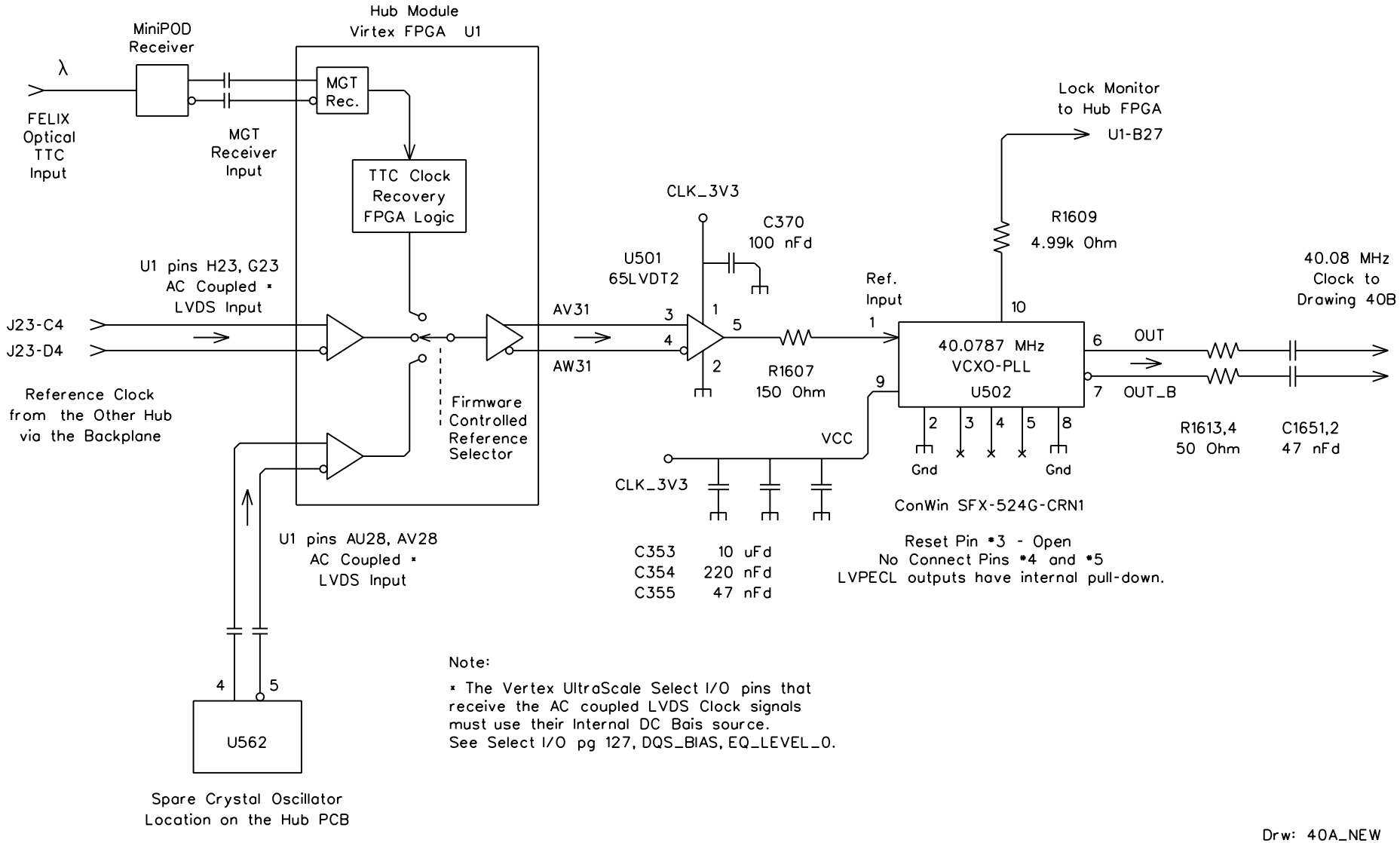
Drw. 38
Rev. 13-Nov-2016

Hub Module - 25 MHz Ethernet Clock



Drw: 39
Rev. 30-Dec-2015

Hub 40.08 MHz LHC Clock Generation

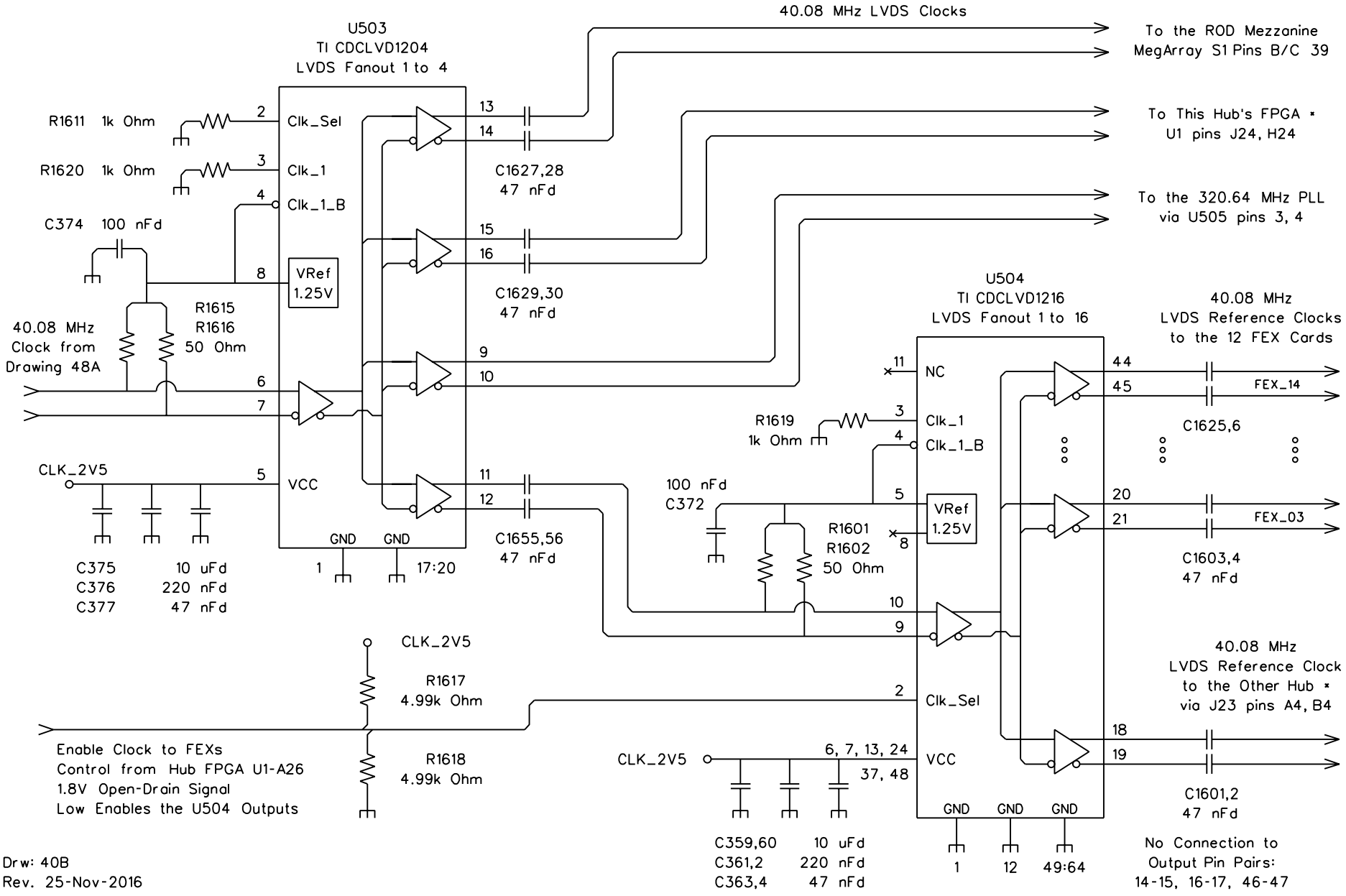


Note:

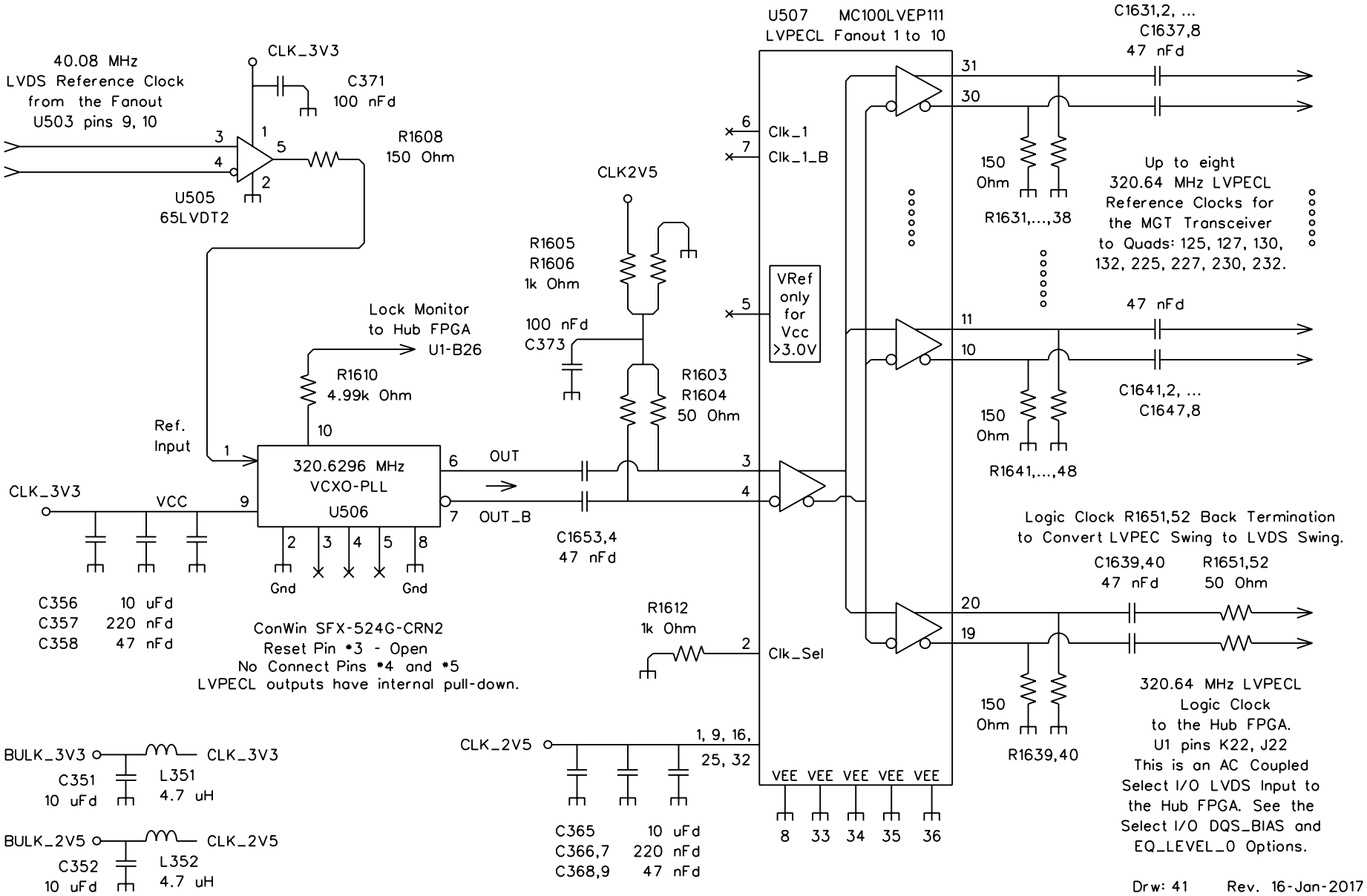
* The Vertex UltraScale Select I/O pins that receive the AC coupled LVDS Clock signals must use their Internal DC Bais source. See Select I/O pg 127, DQS_BIAS, EQ_LEVEL_0.

Drw: 40A_NEW
Rev. 5-June-2017

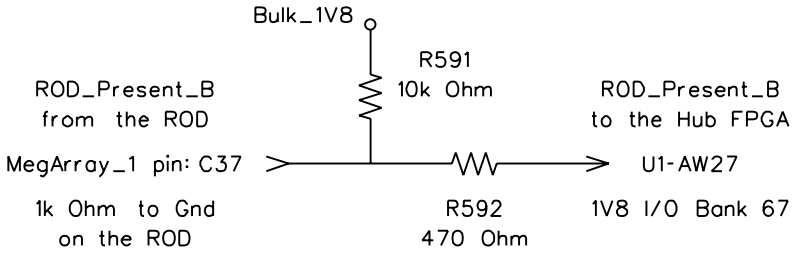
Hub 40.08 MHz LHC Clock Distribution

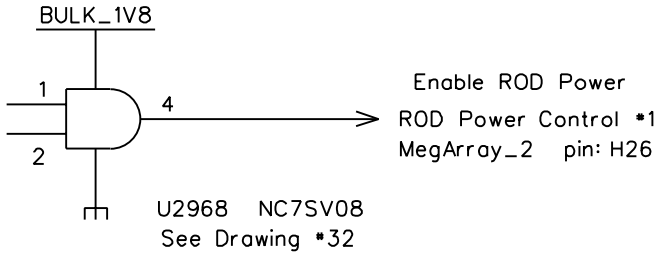


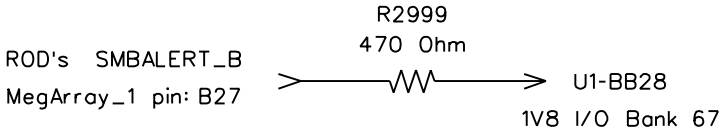
Hub Module 320.64 MHz LHC Clock

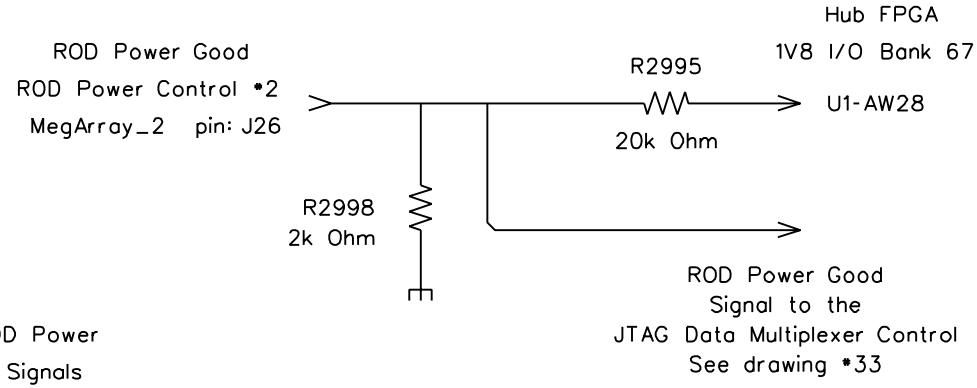


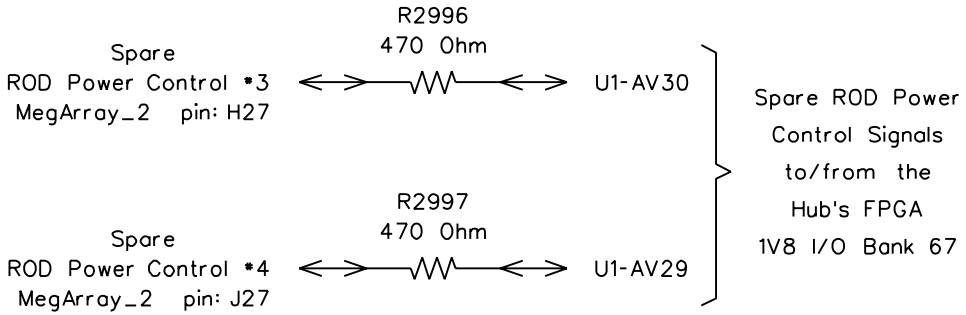
ROD Present - ROD's SMBAlert - 4 ROD Power Control Signals







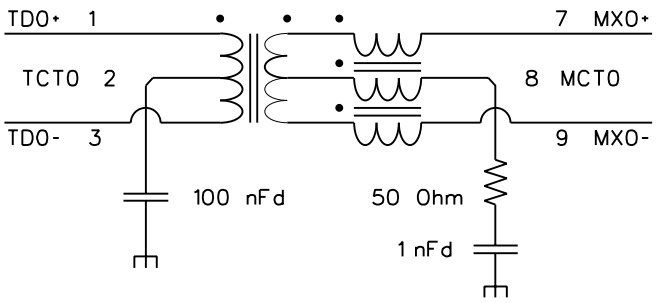


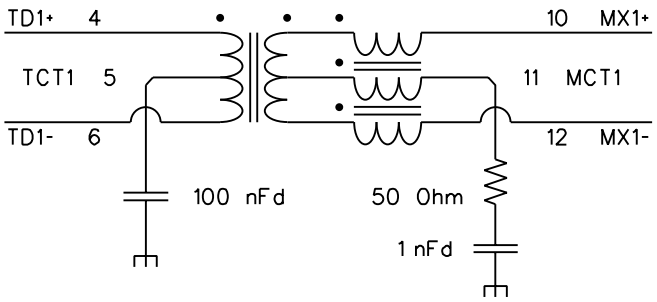


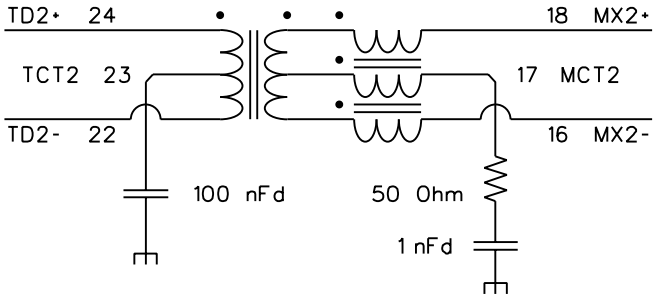
Drw: 42
Rev. 15-June-2017

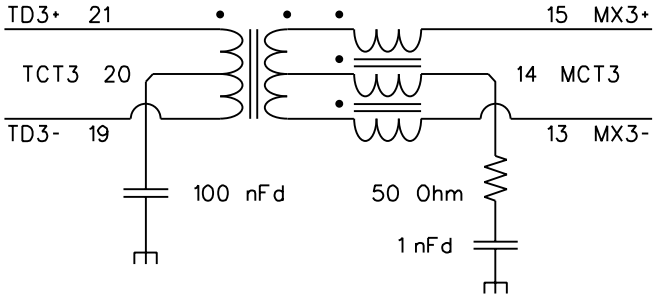
Ethernet Magnetics

Switch or Phys RJ-45 or Backplane









Magnetics
Pulse HX5201NL

Front Panel RJ-45
AMP 1888653-4
Pin Assignments

Circuit	Pin
0+, DA+	1
0-, DA-	2
1+, DB+	3
1-, DB-	6
2+, DC+	4
2-, DC-	5
3+, DD+	7
3-, DD-	8

The Condo RJ-45 geometry has pin numbers that are correct for both sections (i.e. tabs up and down).

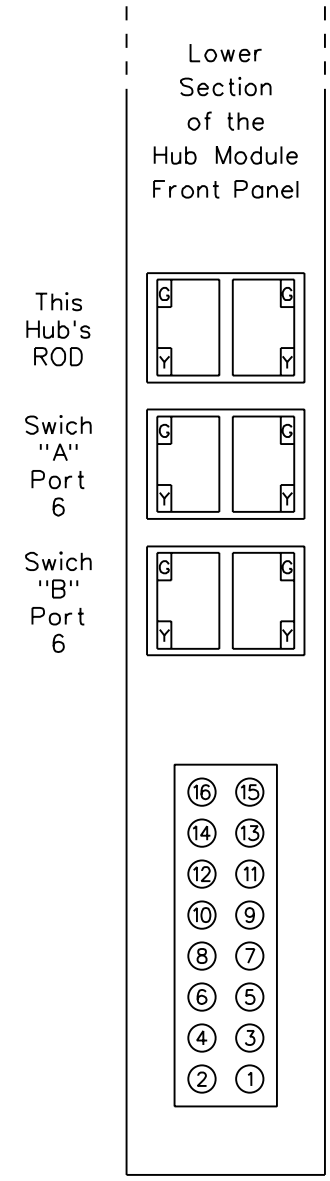
ATCA Backplane
Hub Slot Base Interface
Pin Assignments

Circuit	Pin
0+, DA+	A
0-, DA-	B
1+, DB+	C
1-, DB-	D
2+, DC+	E
2-, DC-	F
3+, DD+	G
3-, DD-	H

For a given Ethernet 4 pair connection routing may swap sections within one set of magnetics.

In a given section of magnetics routing may swap the Dir and Cmp pins just as long as this swap is made at both the input and output of that section.

Hub Module Front Panel Connectors and Cables



Condo RJ45 Connector

This Hub's IPMC — RJ1

Swich "C" Port 6 — RJ2

Swich "B" Port 7 — RJ3

J2 Access Connector

Access Signals, Sensor I2C Bus, and JTAG

Front Panel Access Signals — Twisted-Pair Cable

Hub J2 Connector Pins					Access Signal BNC Connectors
Access_1	15	→	Access_1		
Gnd.	13	→	Gnd.		
Access_2	16	→	Access_2		
Gnd.	14	→	Gnd.		

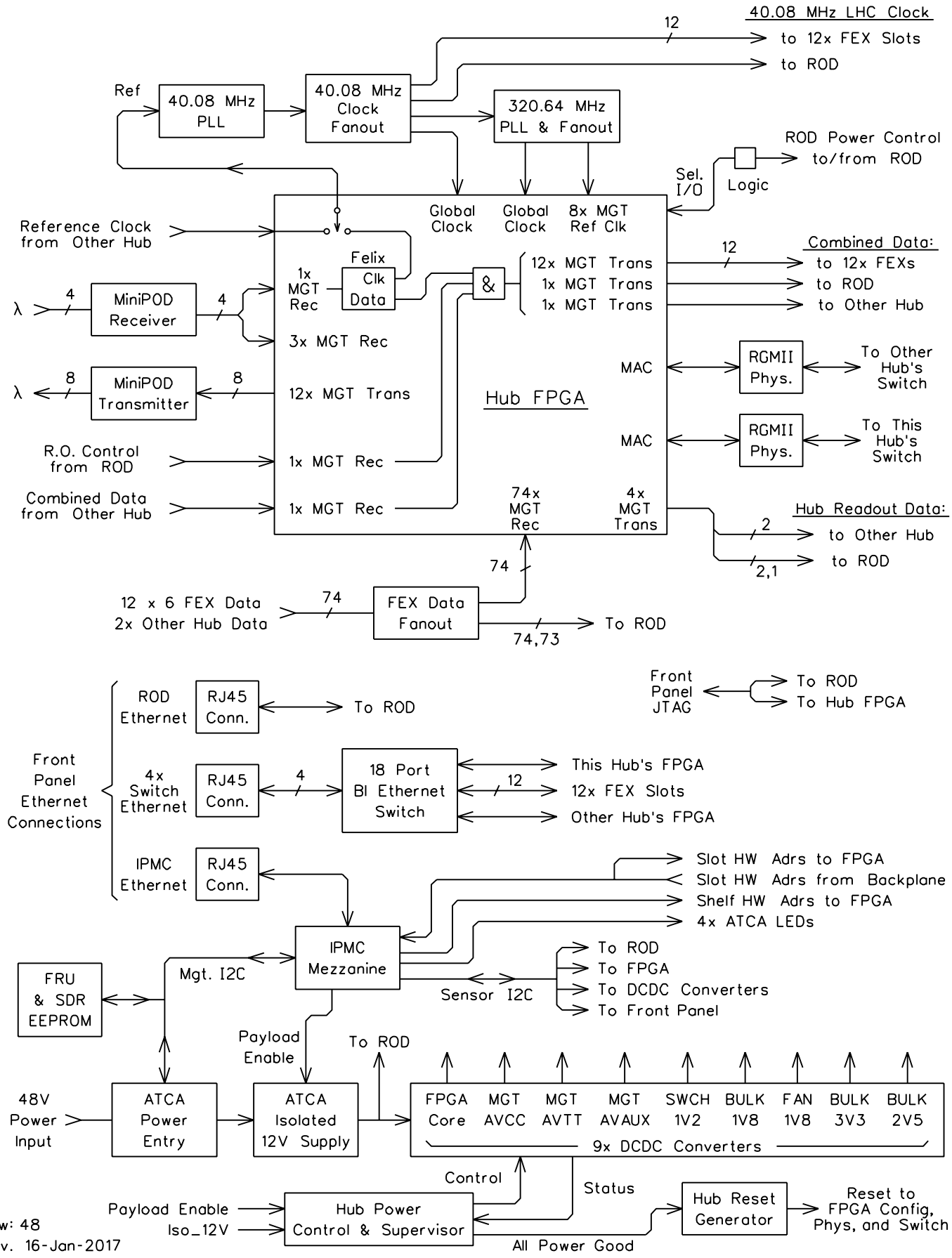
Sensor I2C Twisted-Pair Cable

Hub J2 Connector Pins					External I2C Master
SDA	12	→	10	SDA	
Gnd.	9	→	6	Gnd.	
SCL	11	→	9	SCL	
Gnd.	7	→	6	Gnd.	

JTAG Pod Twisted-Pair Cable

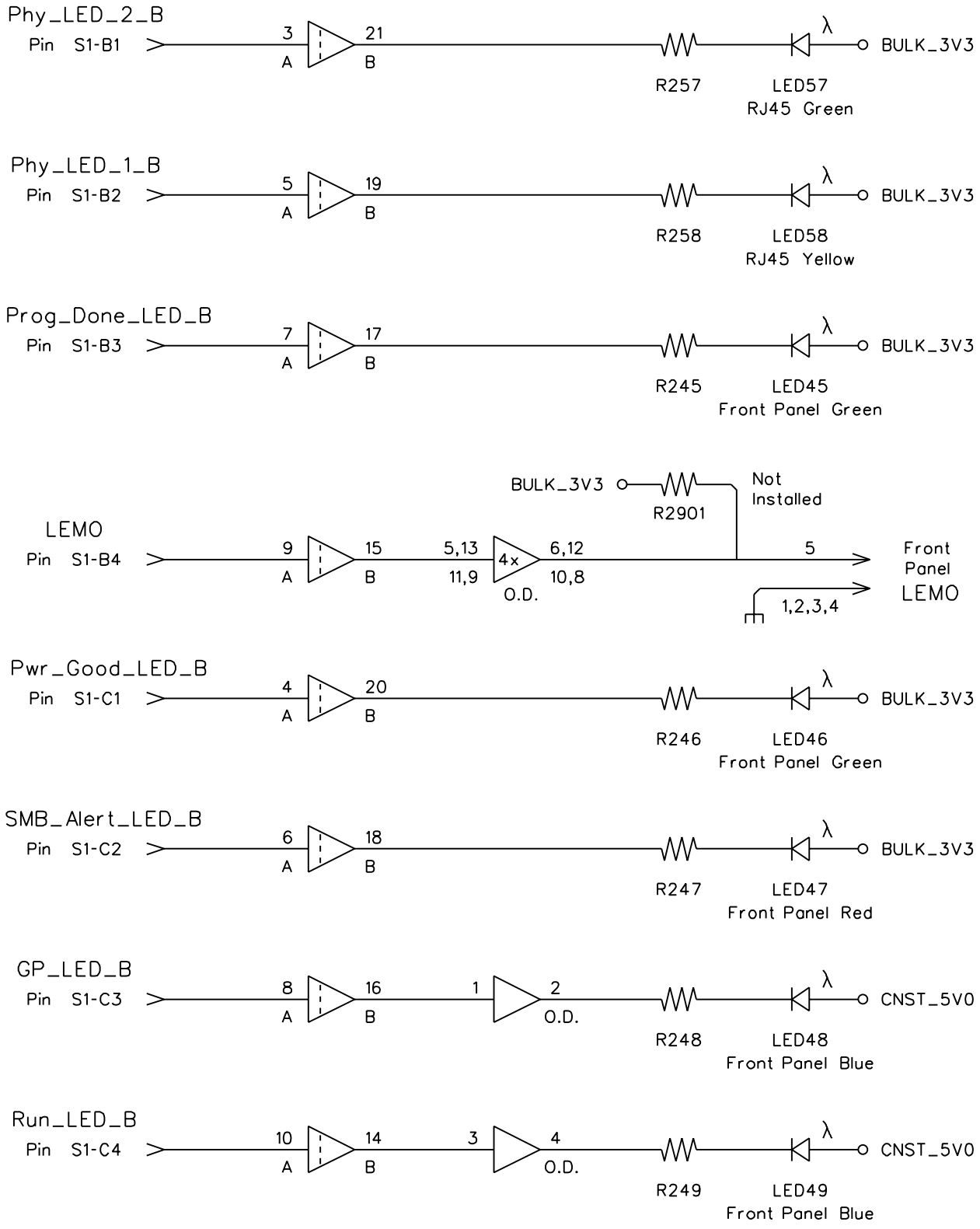
Hub J2 Connector Pins					JTAG Pod Connector
TDI	10	→	10	TDI	
Gnd.	9	→	9	Gnd.	
TDO	8	→	8	TDO	
Gnd.	7	→	7	Gnd.	
TCK	6	→	6	TCK	JTAG Pod Pins 11:14 are not used
Gnd.	5	→	5	Gnd.	
TMS	4	→	4	TMS	
Gnd.	3	→	3	Gnd.	
JTAG Pod Power	2	→	2	JTAG Pod Power	
Gnd.	1	→	1	Gnd.	

Hub-Module Overall Block Diagram



Drw: 48
Rev. 16-Jan-2017

Hub - Front Panel Resources for ROD



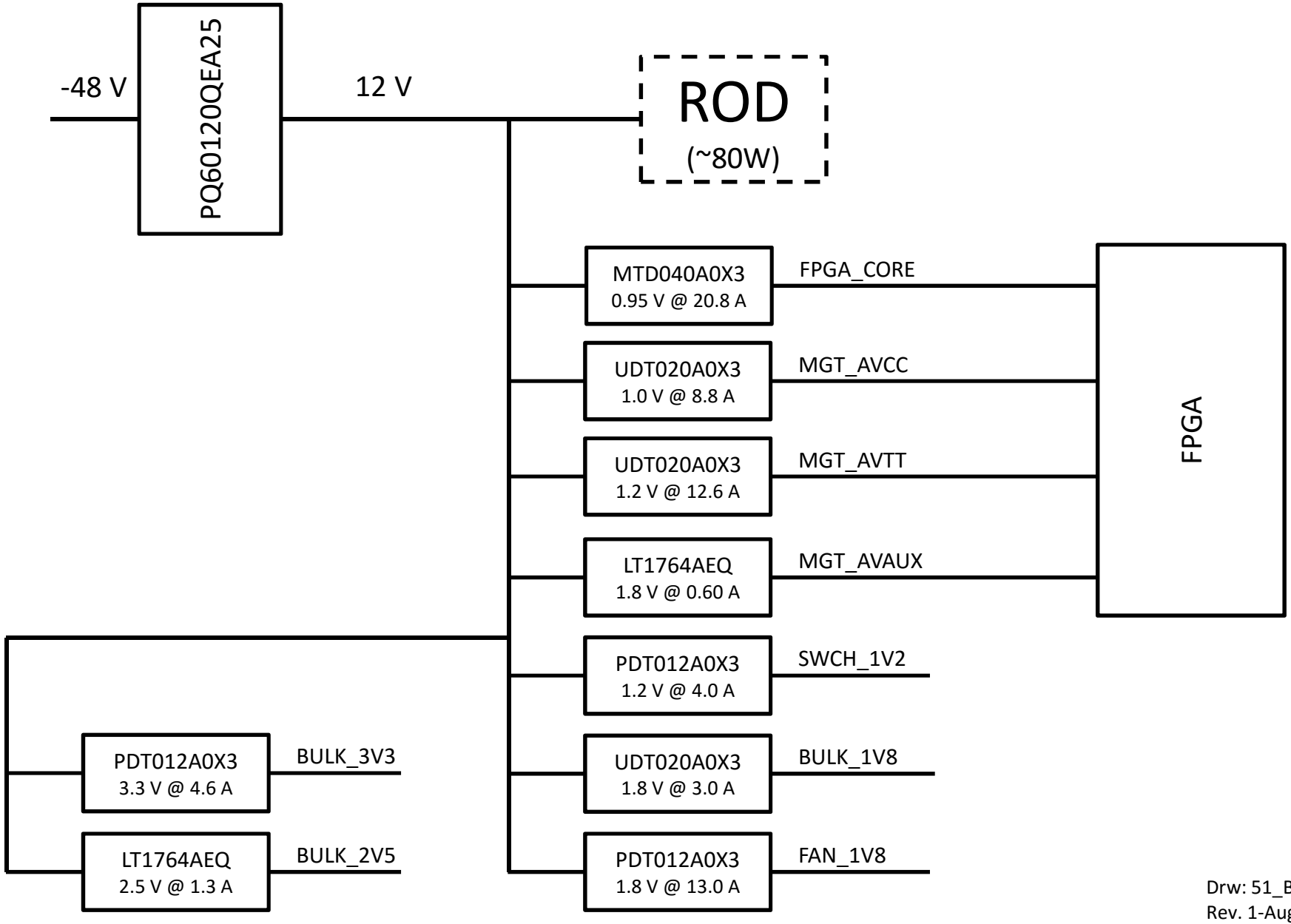
U551
74AVCH8T245
DIR HI A->B
A=1V8 B=3V3

U552
74LVC07A
Vcc=BULK_3V3
Open Drain

R245:R247 240 Ohm
R248,R249 330 Ohm
R257,R258 240 Ohm

Drw. 50
Rev. 2-July-2016

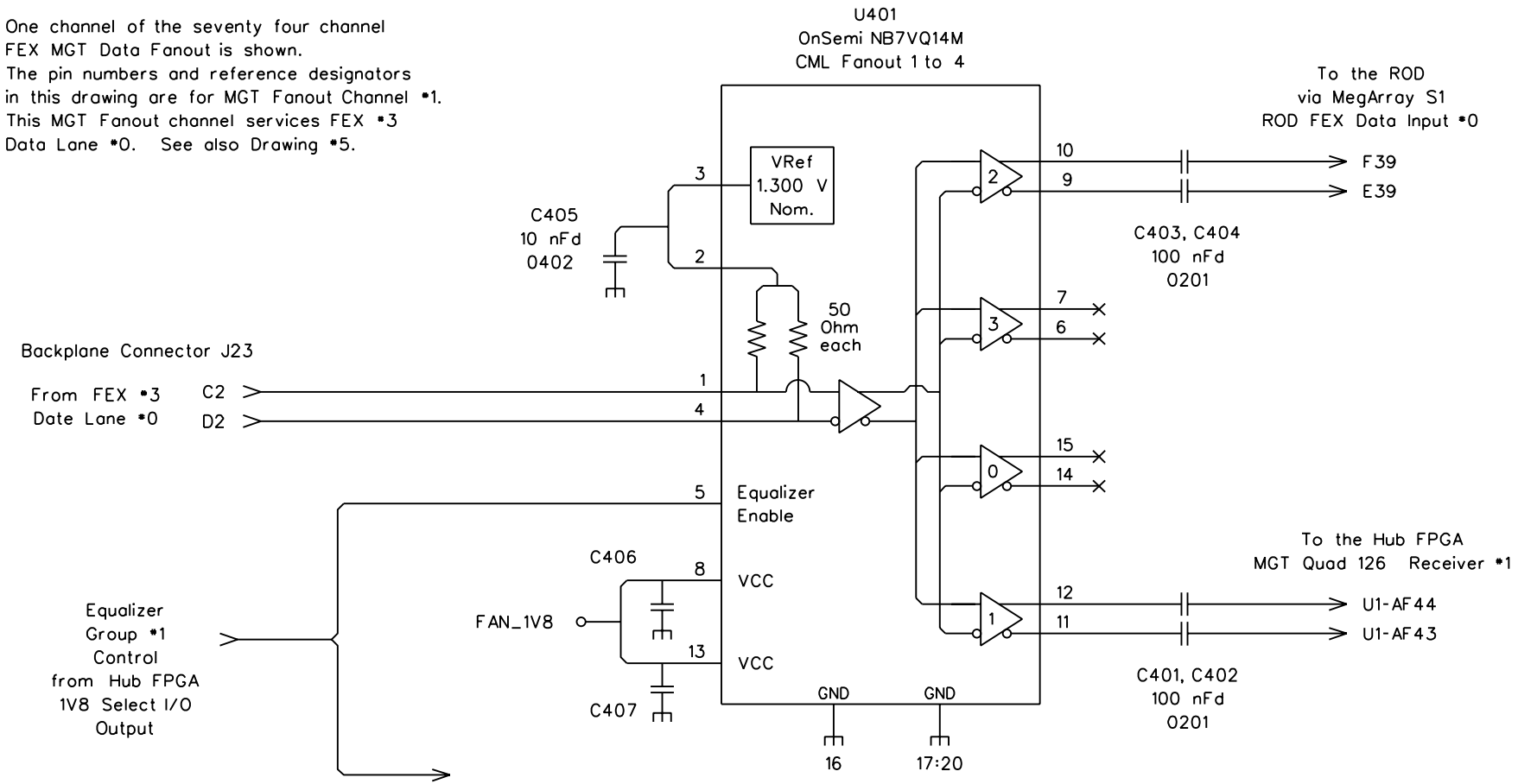
HUB Power System Block Diagram Drawing #51



Drw: 51_Blk
Rev. 1-Aug-2016

FEX MGT Data FanOut

One channel of the seventy four channel
FEX MGT Data Fanout is shown.
The pin numbers and reference designators
in this drawing are for MGT Fanout Channel *1.
This MGT Fanout channel services FEX *3
Data Lane *0. See also Drawing *5.



C406 47 nFd 0402
C407 100 nFd 0402

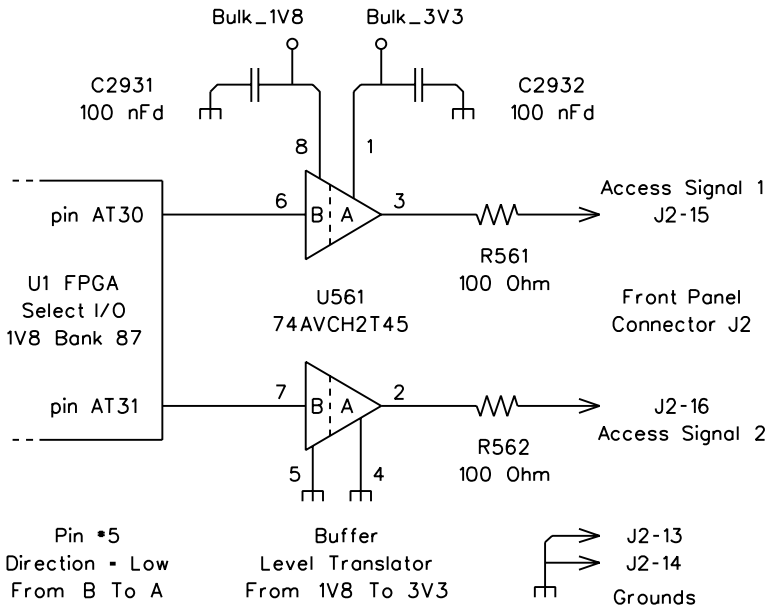
There is an independent Equalizer Group
Control signal for each FEX Data Source.

Expected Vcc current per chip:
170 mA typ. 210 mA max.
Expected total MGT Fanout current:
12.6 Amps typ. 15.5 Amps max.
With the FAN_1V8 supply set for 1.800 Volts,
Expected total MGT Fanout power:
22.6 Watts typ. 28.0 Watts max.

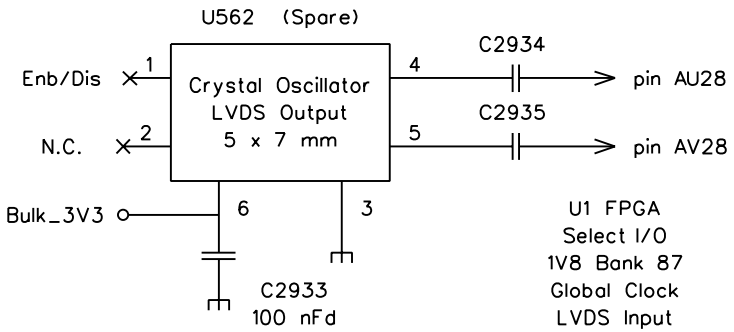
Drw: 52
Rev. 4-Sept-2016

Front Panel Access Signals and Spare Gates

Hub Module Access Output Signals



Hub Module Spare Clock Oscillator



Hub Module Spare Gates

U554 Translator	pin 19 In	pin 5 out
U554 Translator	pin 20 In	pin 4 out
U554 Translator	pin 21 In	pin 3 out

TI - 40400 Standard Control Loop Setup

TI Example Design

Vin = 12 Volts
Vout = 1.2 Volts
Max Output = 20 Amps

Inductor = 0.75 uH

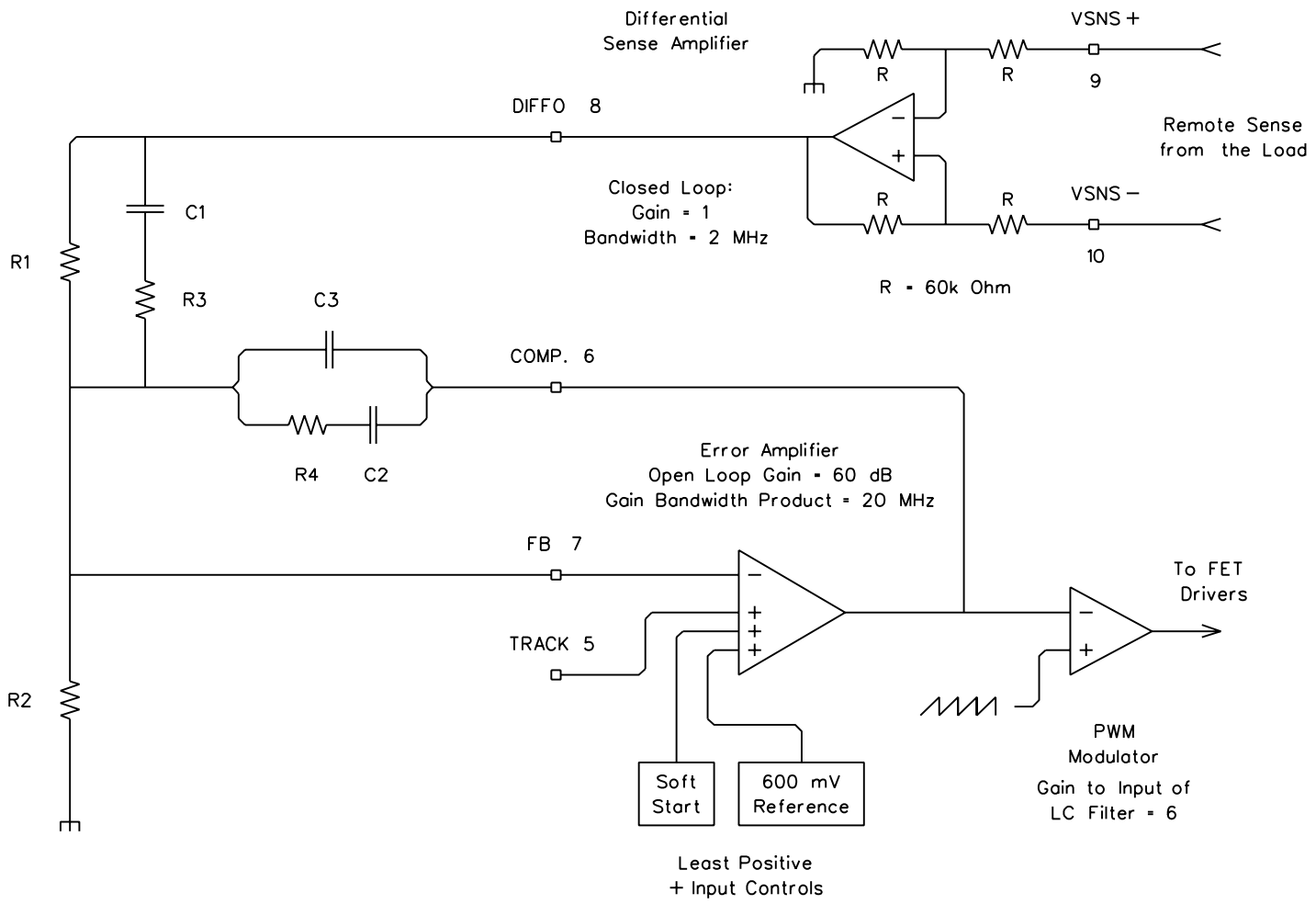
R1 = 10k Ohm
R2 = 10k Ohm
C1 = 820 pFd
R3 = 2.74k Ohm
C3 = 680 pFd
C2 = 2.2 nFd
R4 = 4.99k Ohm

$$Vout = Vref \times \frac{R1 + R2}{R2}$$

$$R2 = R1 \times \frac{Vref}{Vout - Vref}$$

TI Datasheet Pin Names
& Reference Designators

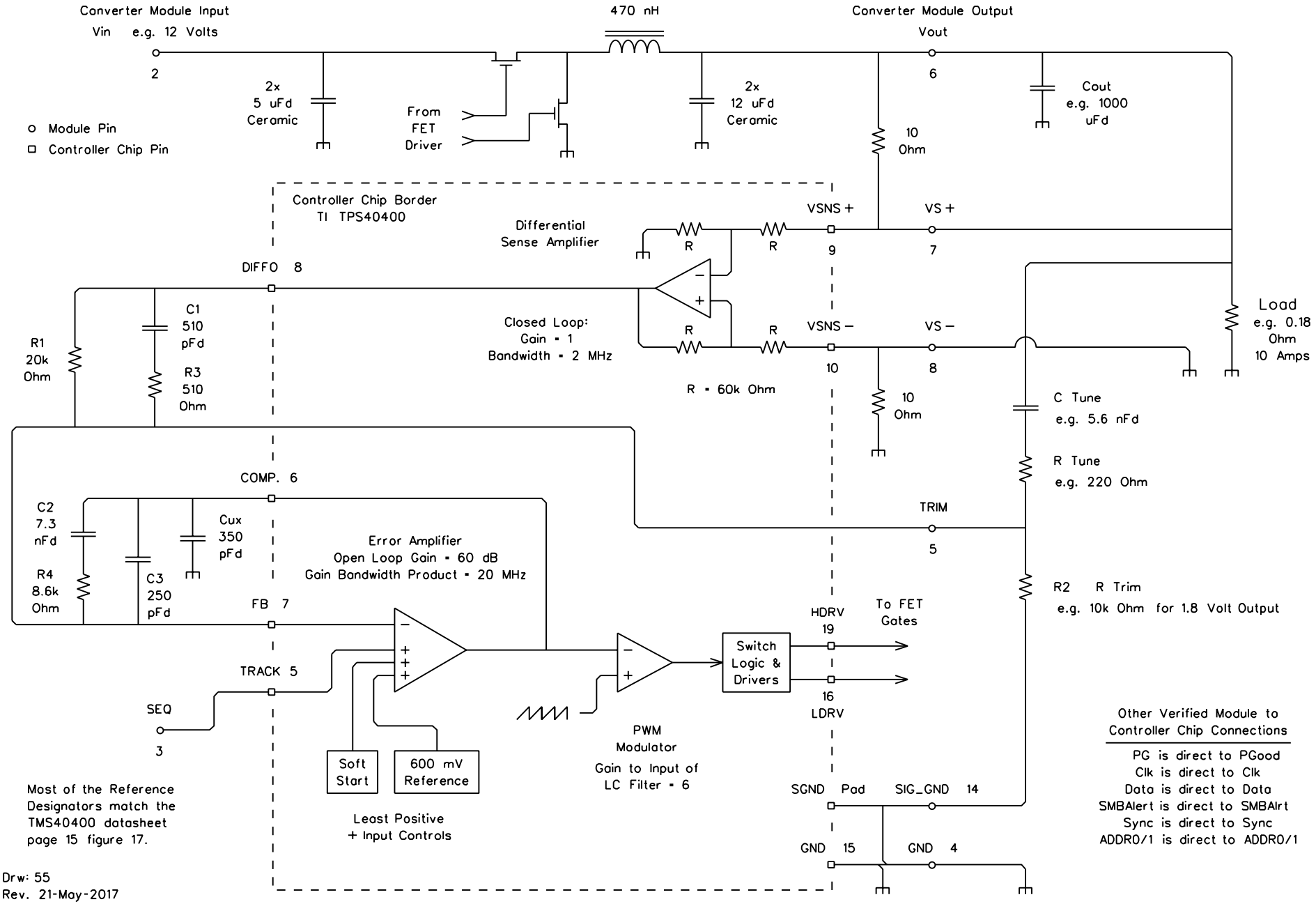
□ TPS40400 Chip Pin



Drw: 54

Rev. 21-May-2017

Lineage Power Assumed Standard 20 Amp Setup



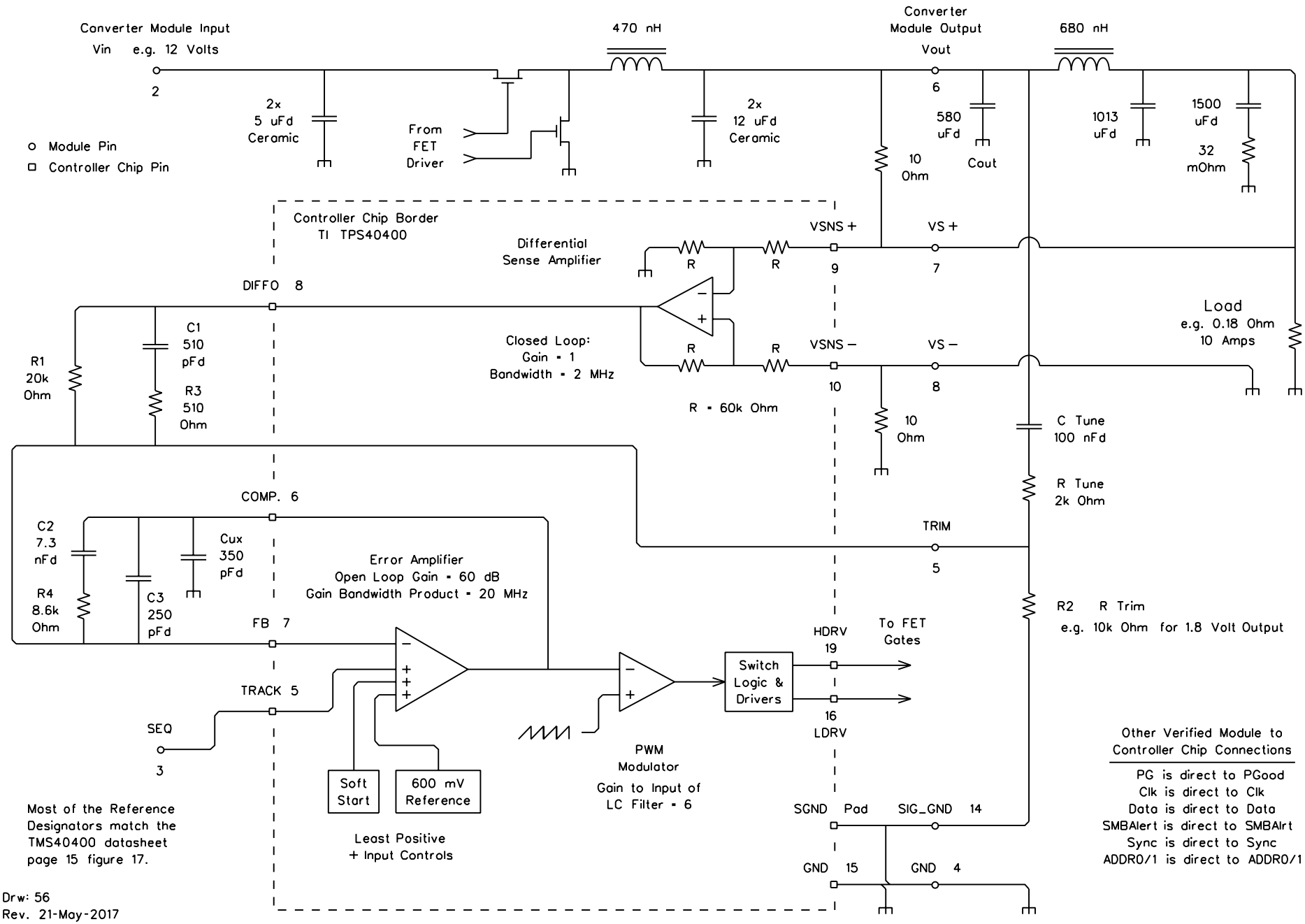
Most of the Reference Designators match the TMS40400 datasheet page 15 figure 17.

Other Verified Module to Controller Chip Connections

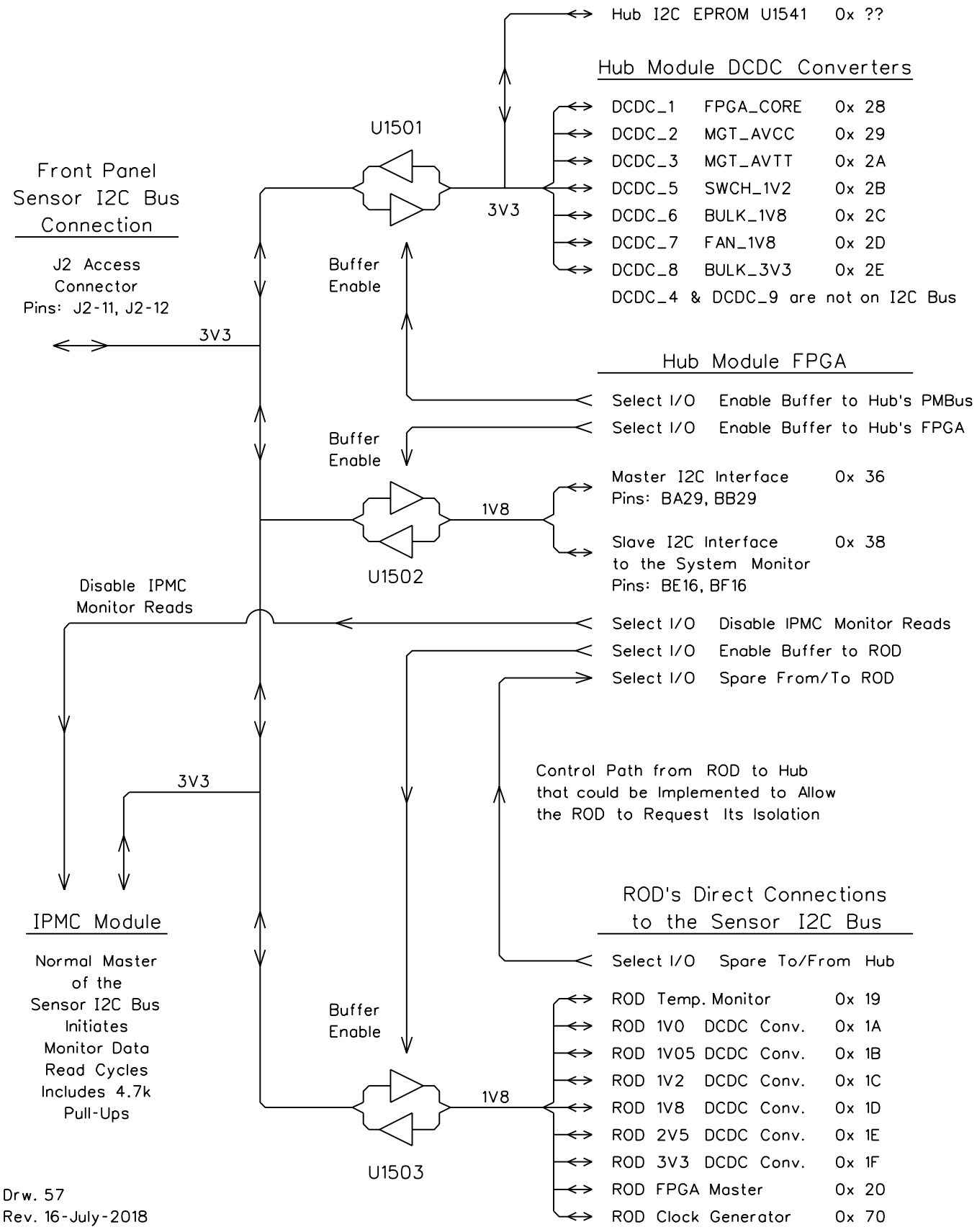
PG is direct to PGood
Clk is direct to Clk
Data is direct to Data
SMBAlert is direct to SMBAlrt
Sync is direct to Sync
ADDR0/1 is direct to ADDR0/1

Drw: 55
Rev. 21-May-2017

Lineage Power 20 Amp Setup with External LC Filter

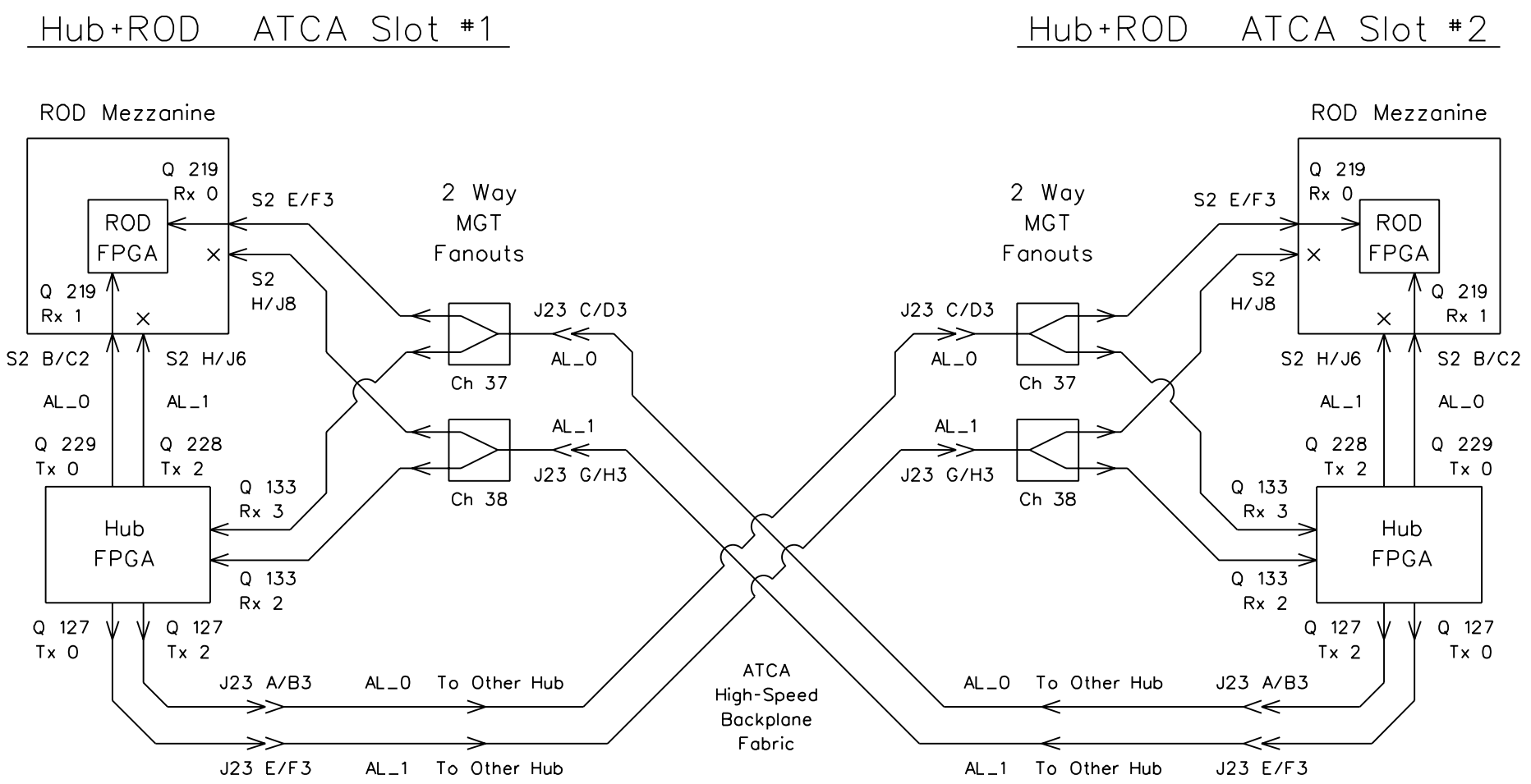


ROD plus Hub Overall Sensor I2C Bus



Drw. 57
Rev. 16-July-2018

Hub Readout Data Connections



The lines in this drawing show the flow of Hub Readout Data both within a Hub card and between the two Hub cards.

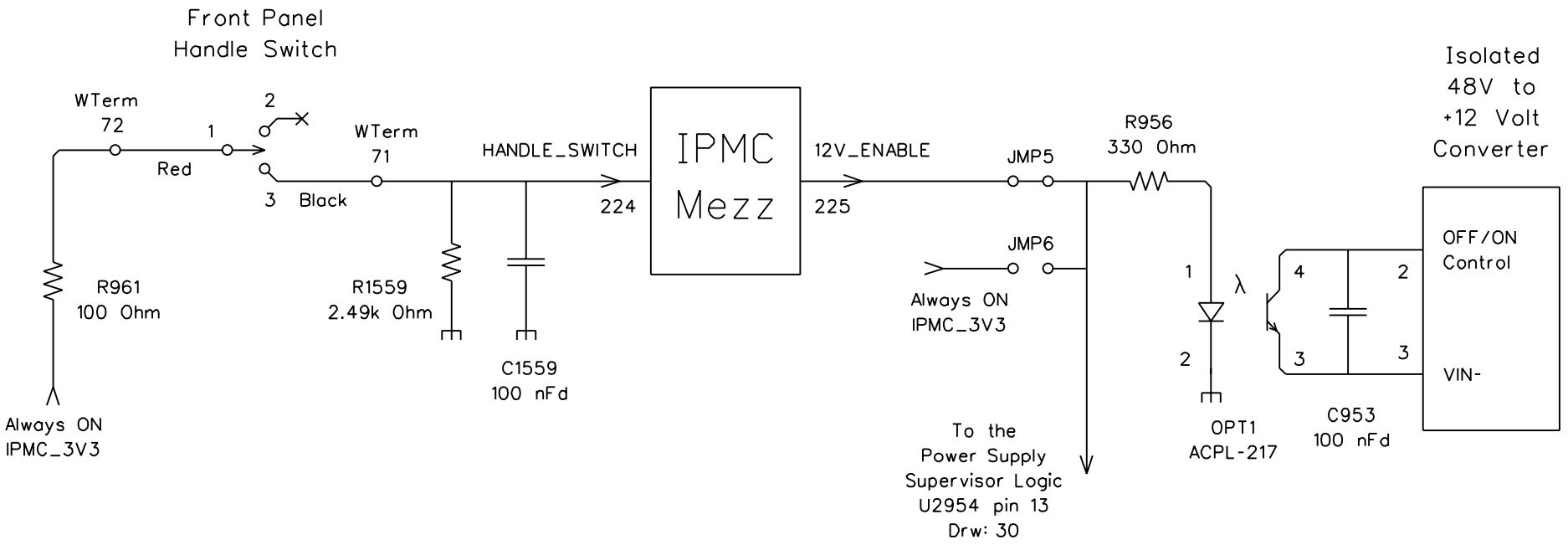
AL_0 ---> Aurora Lane 0
AL_1 ---> Aurora Lane 1

"Q" ---> MGT Quad Number
Rx/Tx ---> Channel In Quad

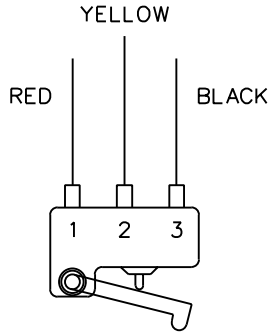
Drw: 58

Rev. 13-June-2018

ATCA Standard IPMC Power Control & Handle Switch



Handle Switch Contacts
1 - 3 Are Open &
1 - 2 Are Closed
Only When the Card is
Fully Inserted and the
Handle is Latched.



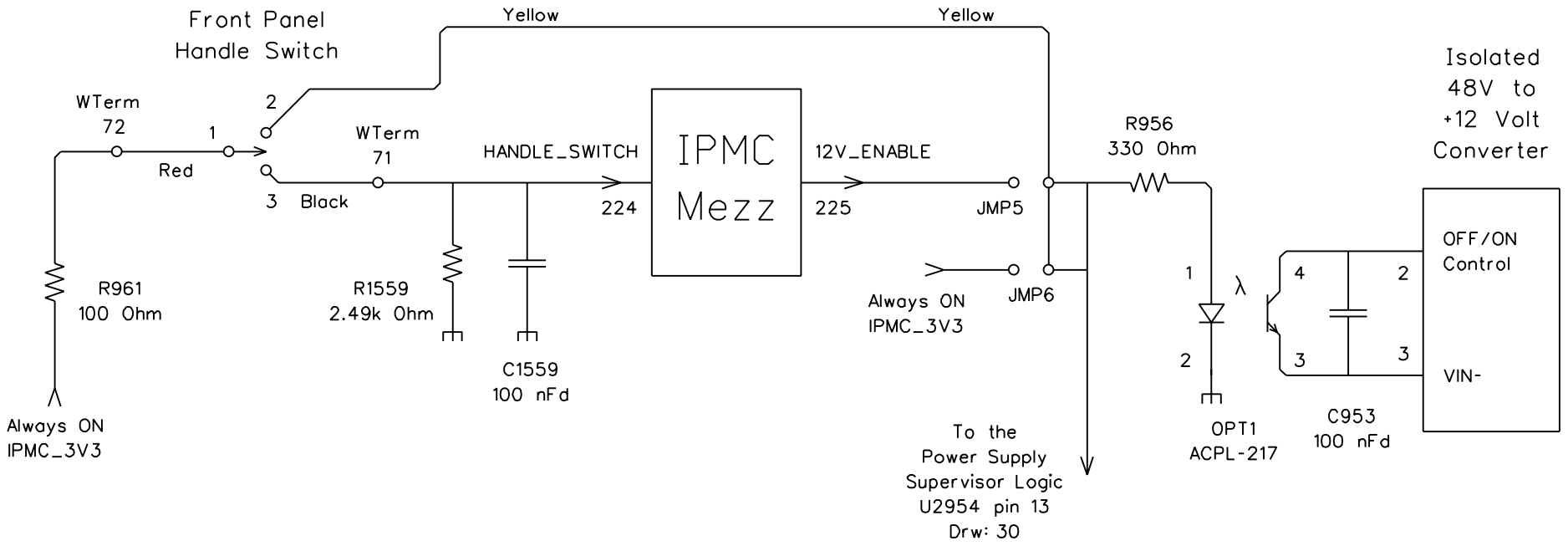
For Normal Standard ATCA Operation:

Switch Terminal #2 and the Yellow Wire Are Not Used
Jumper JMP5 Is Installed
Jumper JMP6 Is Not Installed

Drw: 59

Rev. 17-Feb-2020

IPMC Power Control Bypass



This Drawing Shows the IPMC Power Control Bypassed and the Handle Switch Used to Both Send the Card Extraction Signal to the IPMC and to Control the ON/OFF State of the Isolated 48V to 12V Converter:

Switch Terminal #2 and the Yellow Wire Are Used as Shown.

Both Jumpers JMP5 and JMP6 Must Be Removed.

The Yellow Wire Was Connected to the Common Pin of Both JMP5 and JMP6 for Added Mechanical Support.

Simpler Bypass of the IPMC Power Control:

Remove Either the IPMC or JMP5 or Both of them.

With Light-Weight Twisted-Pair Wires Connect a Miniature Toggle Switch Across Jumper JMP6.

Handle Switch Terminal #2 & Yellow Wire Are NOT Used.

Handle Switch Only Needs to Be Wired If You Need to Send the Extraction Signal to the IPMC.

Drw: 60

Rev. 17-Feb-2020