Hub Power Good and Board Startup Reset

All_Hub_Power_Good_to_FPGA

Board_Startup_Reset_B is asserted LOW from the time
that the Hub receives 48V power until 500 msec after
all Hub power supplies are up and stable.

Board_Startup_Reset_B

BULK_3V3

R27
4.99k Ohm

CNST_5V0

Vcc   6

Generate
BOARD_STARTUP_
_RESET_B
500 msec.

U9   TPS3808

1

5

3

MR_B

2

C2961
100
nFd

4

R29
2.7k Ohm

8

U6

R28
4.99k Ohm

13
12
10
9

6

U5

8

U5

1
2
4
5

9
10
12
13

CNST_5V0

R31:R37
10k
Ohm

DCDC 1 Power Good
DCDC 2 Power Good
DCDC 3 Power Good
DCDC 5 Power Good

DCDC 6 Power Good
DCDC 7 Power Good
DCDC 8 Power Good

Enable Iso_12V

R25 10k Ohm

CNST_5V0

Vcc   6

Detect
MGT_AVAUX

U7   TPS3808

1

4

5

3

2

MGT_AVAUX
1.800 Volts

R21 10k Ohm
R22 3.48k Ohm
1.569 Vthrshd 87%

R26 10k Ohm

CNST_5V0

Vcc   6

Detect
BULK_2V5

U8   TPS3808

1

4

5

3

2

BULK_2V5

R23 10k Ohm
R24 2.26k Ohm
2.197 Vthrshd 88%

5 Volt version of the Enable Isolated +12V signal
from drawing *30, Hub Power Supply Control.

Need to mix in Enable Iso_12V so that Board_Startup_Reset_B
is asserted LOW before the power supplies begin to fail.
This is to protect the Flash memory during normal power shut down.

4 input AND is   74HC21   U5, U6

All ICs and gates on this page are powered by the
"Constant 5V0" supply from the ATCA Power Entry.

The actual Power Good and Board Startup Reset
Reference Designators are higher by 2950.

The TPS3808 internal reference is 0.405 Volt.

ByPass capacitors C2962:C2966 go with this page.