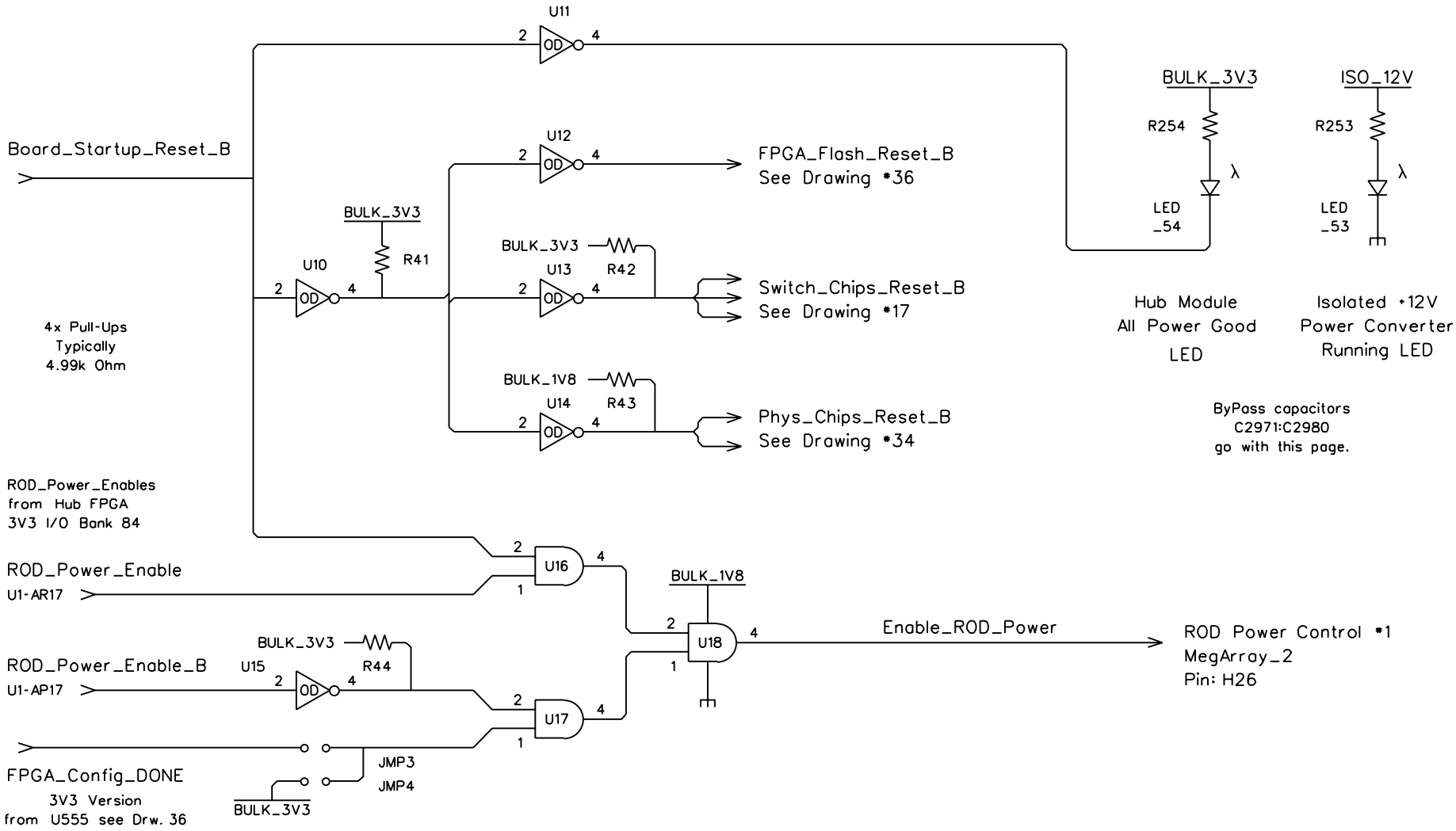
Board Reset Distribution - ROD Power Control



Consumers of the Board_Startup_Reset_B signal and Rules:

When all power is Good and Board_Startup_Reset_B has finished, then turn ON the front panel Power Good LED.

Allow FPGA to Configure, hold FPGA INIT Low with open-drian until ready to Configure, pull-up to 1V8.

Flash active Low Reset must be held Low for 300 usec min after all power good, 1V8 signal.

Switch chips active Low Reset, 80 msec min Low with 25 MHz clock running and power good, Max rise time 25 nsec, 3V3 signal.

Phys chip active Low Reset must be held Low for 10 msec min after all power good, 1V8 signal.

Enable_ROD_Power must drive 1V8 signal into a 1k Ohm load to Gnd on the ROD.

Open Drain Inverters are NC7SV05
2 input ANDs are NC7SV08

All ICs on this page are powered by BULK_3V3 except as indicated.

Except for the LED circuits, the actual Ref Desigs on this page are higher by 2950.

Drw: 32
Rev. 28-Nov-2016