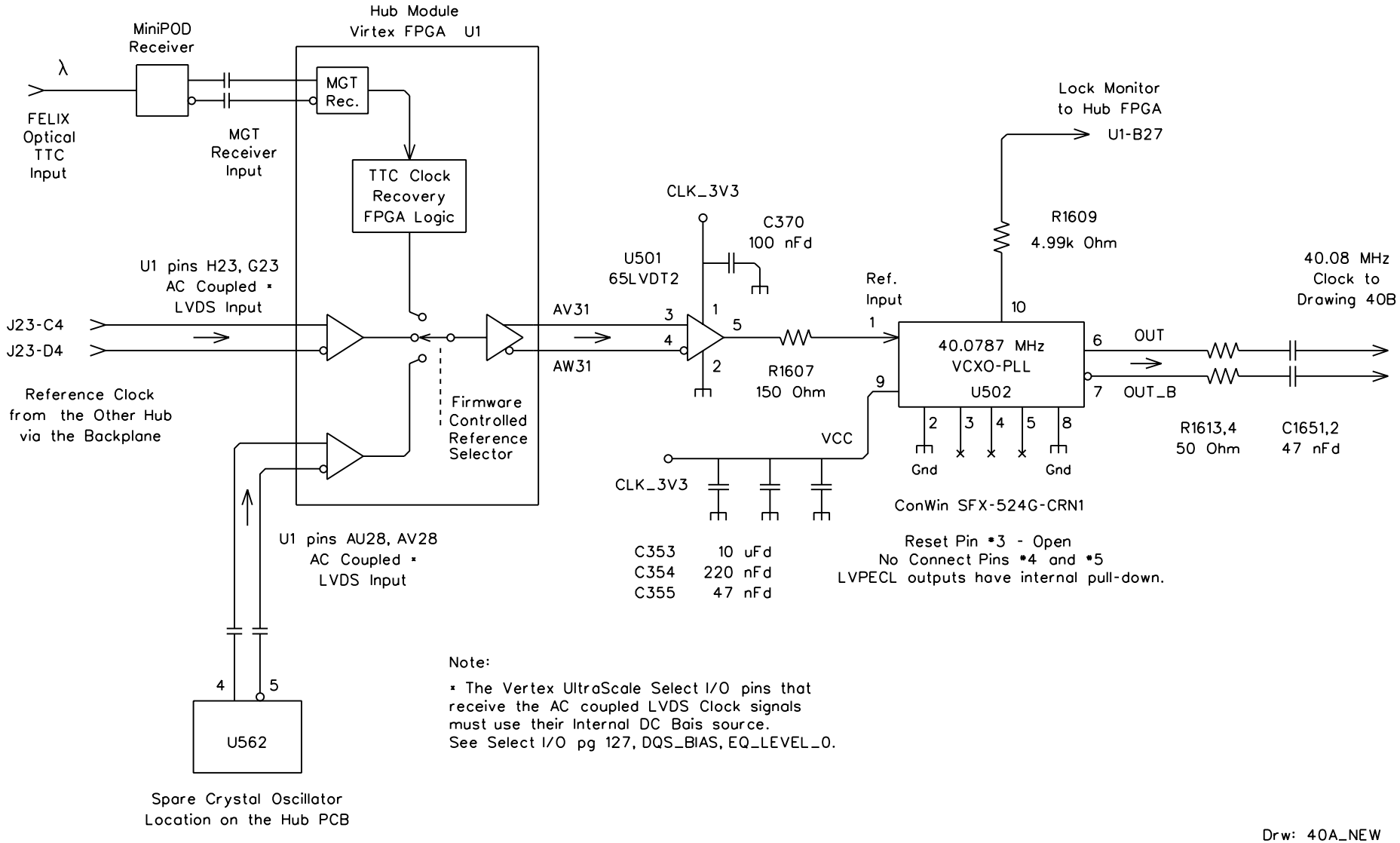
Hub 40.08 MHz LHC Clock Generation



Note:

* The Vertex UltraScale Select I/O pins that receive the AC coupled LVDS Clock signals must use their Internal DC Bais source. See Select I/O pg 127, DQS_BIAS, EQ_LEVEL_0.

Drw: 40A_NEW
Rev. 5-June-2017