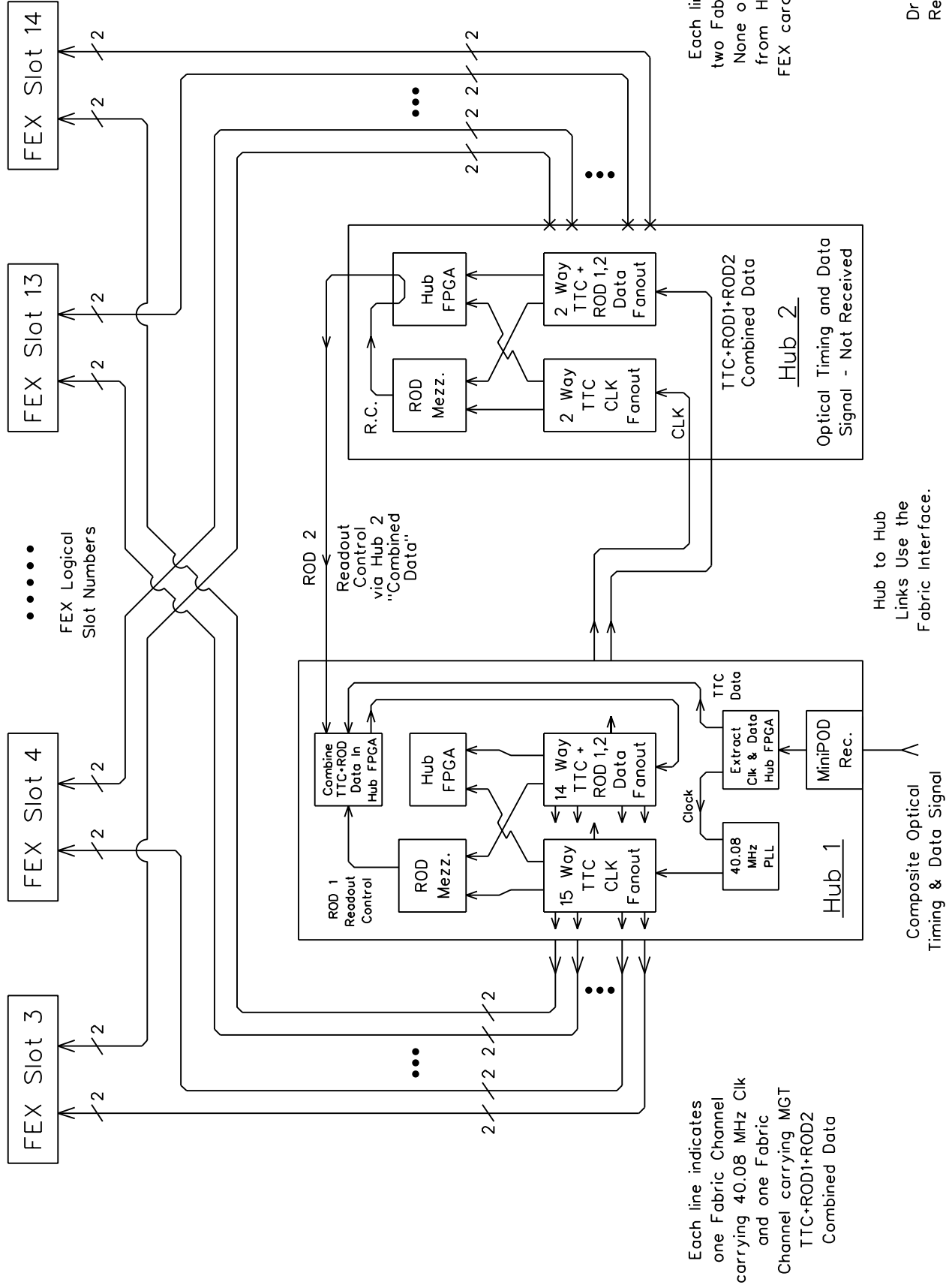
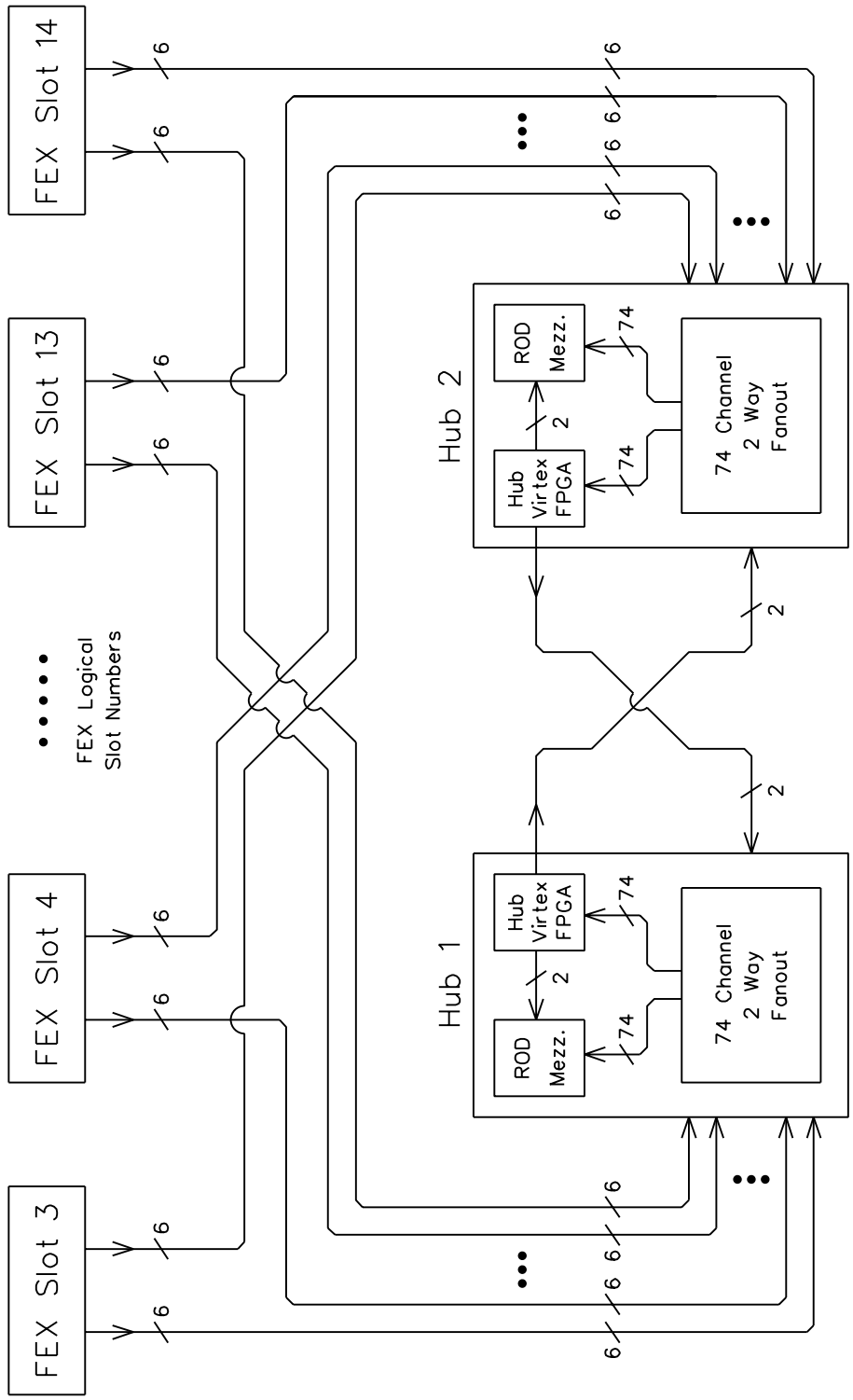


Hub Clock and Combined Data Distribution



Hub-Module Readout Data Distribution

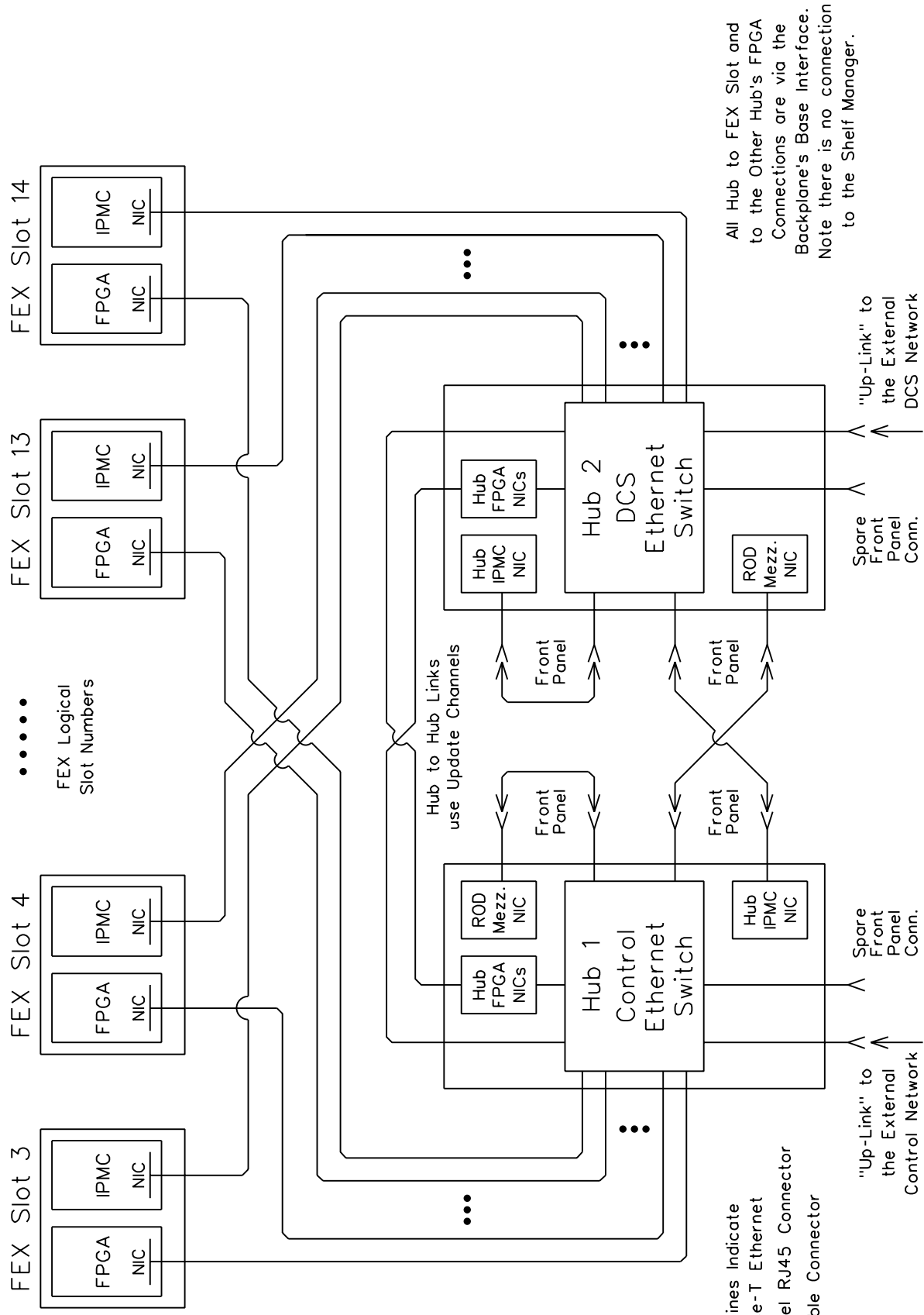


Each line indicates six Fabric Interface Channels carrying FEX Slot Readout Data to the ROD's and to the Hub-Module's Virtex FPGAs

The FEX Slot Readout Data on each Fabric Interface Channel is received by an MGT Transceiver on both the ROD's and the Hub-Module's Virtex FPGAs.

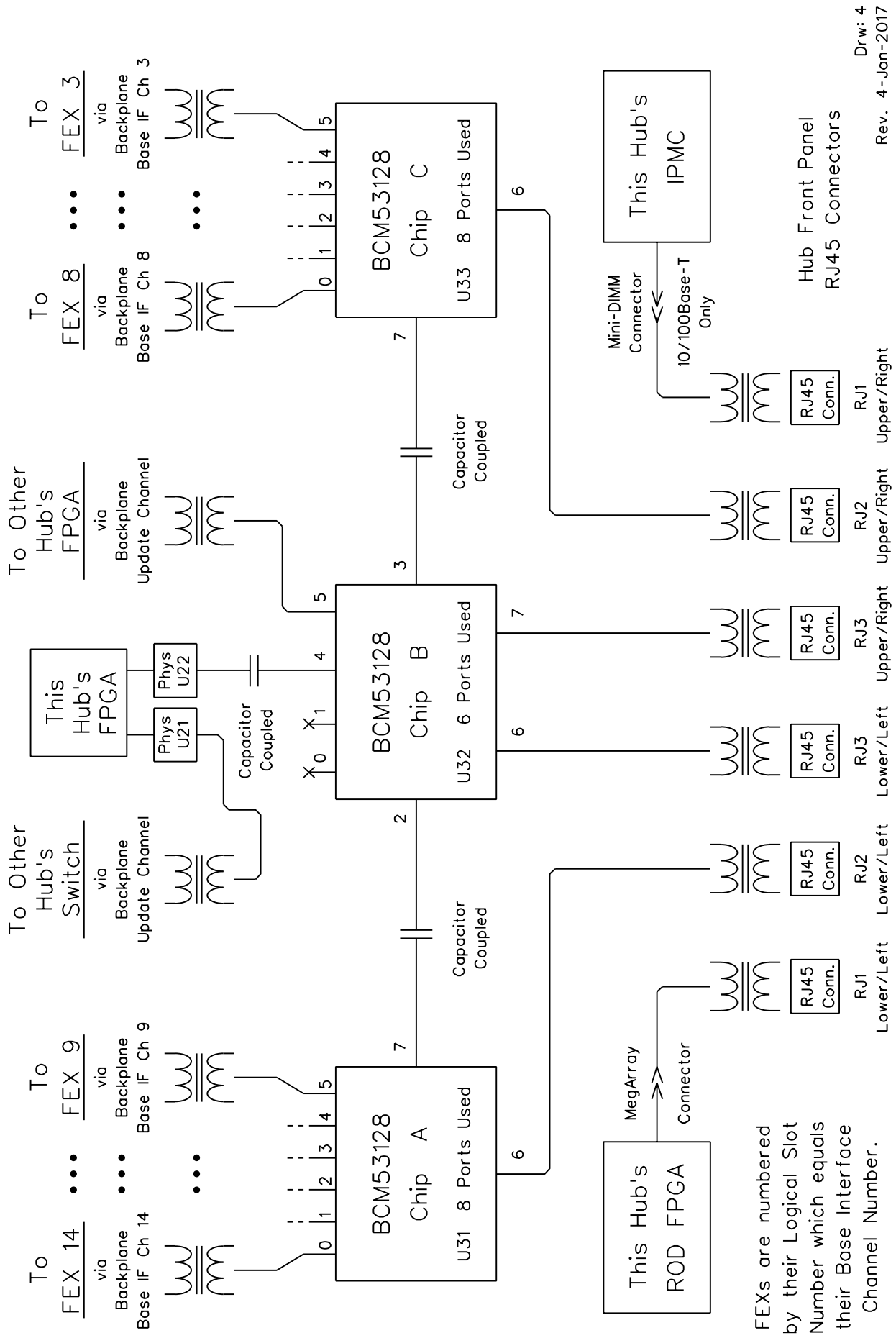
Hub to Hub Links use the Fabric Interface.

Hub-Module Ethernet Switch Connections



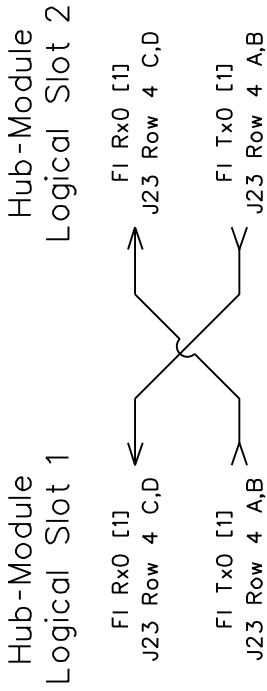
All Hub to FEX Slot and to the Other Hub's FPGA Connections are via the Backplane's Base Interface. Note there is no connection to the Shelf Manager.

Hub-Module All Ethernet Connections



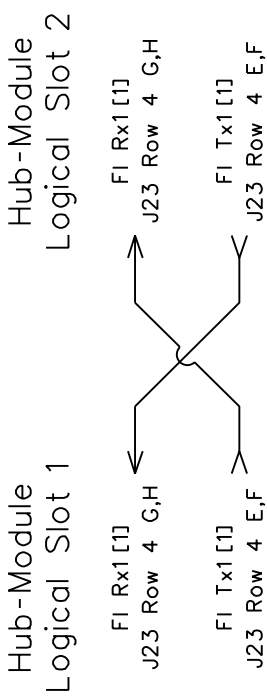
Hub-Module to Hub-Module Backplane Connections

40.08 MHz LHC Clock Links



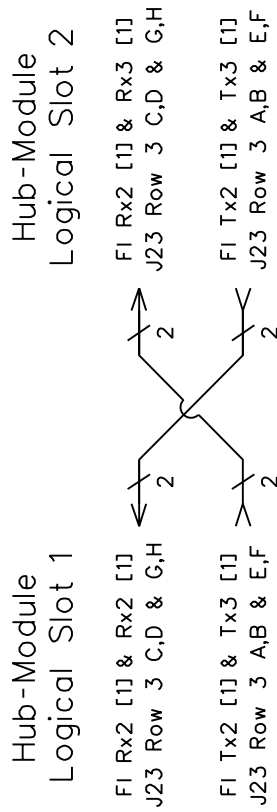
These links start in dedicated clock hardware.
These links end at an LVDS Select I/O input on FPGA.
The Hub-2 to Hub-1 link is typically not used.

Combined TTC + RO Control Links



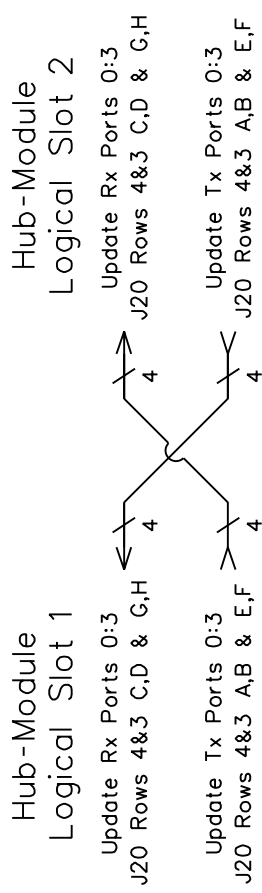
These links start and end in Virtex MGT Transceivers.
The Hub-2 to Hub-1 link typically carries only Hub-2 RO Control information back to Hub-1 for distribution.

Links that Carry the Hub's Readout Data



These links start from a Hub FPGA MGT Transmitter.
These links run to the Other Hub's FEX Data Fanout.

10/100/1000 Base-T Ethernet Links



All of these links start at the Hub's Ethernet Switch "B" Port 5
and end at the Hub's FPGA Phys Chip U21.
The normal Hub-to-Hub Base Interface Channel 2 is not used.